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Modeling and Control of Modular Multilevel Matrix Converter for Low-Frequency AC Transmission

Zheren Zhang, Yanqiu Jin and Zheng Xu *

Department of Electrical Engineering, Zhejiang University, Hangzhou 310027, China
* Correspondence: xuzheng007@zju.edu.cn

Abstract: The modular multilevel matrix converter (M3C) is the core component in low-frequency AC (LFAC) transmission, which is a competitive scheme for offshore wind power integration. In this paper, the M3C control strategy with the reduced switching frequency SM voltage balancing method is proposed. First, based on the conventional αβ0 and dq transformations, the M3C mathematical model is derived. Then, the dual-loop control structure with outer loop and inner loop controllers commonly used in voltage source converters is applied to the M3C. The inner loop controller consists of the current tracking controller in the dq reference frame and the circulating current suppressing controller in the αβ0 reference frame; the outer loop controller is proposed for the offshore wind farm LFAC integration scenario. Additionally, according to the operating characteristics of full-bridge submodules (FBSMs), three characteristic variables are defined and a reduced switching frequency SM voltage balancing method based on the nearest level control (NLC) is proposed. Finally, time-domain simulations in PSCAD/EMTDC demonstrate the feasibility of the proposed control strategy.

Keywords: M3C; low frequency AC transmission; mathematical model; dual-loop control; SM voltage balance

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1. Introduction

With the development of offshore wind farms far from the coast, the long-distance transmission of offshore wind power has drawn extensive attention from academia and industry [1,2]. At present, the commissioned distant offshore wind farms are generally connected to onshore AC grids by high-voltage direct current (HVDC) systems [3]. However, the offshore converter platform of the HVDC scheme is costly. In addition, since the HVDC circuit breaker is extremely expensive and the weight and dimension of the HVDC circuit breaker are extremely large, the high-voltage large-capacity DC circuit breaker limits the development of the HVDC grid for offshore wind power integration. To overcome these shortcomings, the low-frequency alternating current (LFAC) transmission is proposed as an alternative, dating back to the 1950s in conception [4,5]. With the development of power electronics, the LFAC scheme is found increasingly competitive for offshore wind farm integration with technical and economic advantages: the transmission distance and capacity can be increased under lower frequency; investment costs are reduced by eliminating the offshore converter platform [6].

The onshore frequency converter is the core equipment in the LFAC system. Early research has focused on the cycloconverter, which suffers from severe harmonics and unsatisfactory fault ride-through ability [7]. The modular multilevel matrix converter (M3C), first proposed in 2001 [8], is generally regarded as the next-generation frequency converter due to its low voltage harmonic level, high scalability, and decoupled active and reactive power control [9]. Currently, the 200 kV/300 MW M3C-based Hangzhou LFAC demonstration project is under construction, and the M3C-based LFAC shows good potential in high-voltage bulk power transmission.

To apply the M3C to the LFAC system, an intuitive mathematical model and a satisfactory control strategy are crucial. The existing literature on modeling and control of the M3C is mainly based on the double αβ0 transformation, which is first proposed in [10,11] to achieve the decoupled model and control. However, the physical meaning of variables is not clear with the double αβ0 transformation. In comparison, the conventional αβ0 and dq transformations can provide more definite physical meaning, and the derivation process is more straightforward and easier to understand. For readers familiar with conventional modular multilevel converter (MMC) technology, the αβ0 and dq transformations are preferable. If the M3C can be considered as an extension of the MMC, the M3C controller design can be simplified by adopting the design method of the MMC controller.

Balancing the sub-module (SM) voltages in each arm is essential in the M3C control strategy, which is generally achieved by the voltage sorting algorithm based on the modulation method. Current studies on the M3C control are mainly based on the electric drive application [12,13], where the pulse-width modulation (PWM) is selected as the SM number is small enough. As for the LFAC transmission system, the number of series-connected SMs in each arm is sufficiently large to withstand the high voltage. In this case, the nearest level control (NLC) widely used in the MMC-based HVDC is more suitable due to lower switching losses and less calculation burden [14]. However, current studies still apply the PWM to the M3C in the LFAC system [15–17] and few studies mention the application of the NLC to the M3C.

In [18,19], a conventional SM voltage balancing algorithm based on the NLC is proposed, which sorts all capacitors' voltages and triggers the SMs with the highest or lowest capacitor voltages. However, the conventional algorithm has to be executed in each control cycle. Thus, even if the total number of inserted SMs in one arm is unchanged, unnecessary switching operations are generated. To reduce the switching losses due to the unnecessary switching operations, reference [20] proposed a reduced switching frequency modulation, which considers the extra number of SMs that need to be switched on or off in the following control cycle. The conventional SM voltage balancing algorithm, a hybrid balancing algorithm, and a fundamental frequency balancing algorithm are investigated in [21]. Reference [22] proposed a reduced switching frequency algorithm with a balancing adjusting number to avoid large SM voltage fluctuation. In [23], a voltage balancing strategy juggling the low voltage deviation and the low switching frequency is proposed. However, these algorithms are suitable for the MMC with half-bridge sub-modules (HBSMs). Reference [24] introduced an optimized voltage sorting algorithm for the M3C to shorten the sorting time without affecting the switching frequency. No literature has considered the reduced switching frequency modulation in the M3C with full-bridge sub-modules (FBSMs). Considering that there are hundreds of SMs in the M3C, an SM voltage balancing method with reduced switching frequency can thus decrease the switching losses and promote the application of M3C in the LFAC system, which requires further study.

The contributions of this paper are as follows:

(1) The mathematical model of the M3C is derived based on the extended MMC topology and the multiple αβ0 and dq transformations. The dual-loop controllers are designed according to the derived mathematical model.
(2) A reduced switching frequency SM voltage balancing method based on the NLC is proposed. According to state sorting and incremental switching, this optimized SM voltage balancing method can avoid unnecessary switching.

The rest of this paper is organized as follows. In Section 2, the basic structure and decoupled mathematical model of the M3C are elaborated as a basis. Then, the inner loop controller is designed in Section 3. In Section 4, the reduced switching frequency SM voltage balancing method is proposed based on state sorting and incremental switching. Section 5 presents the outer loop controller. To verify the proposed control strategy, a case is presented in Section 6. Finally, conclusions are drawn in Section 7.

2. Basic Structure and Mathematical Model of M3C

An intuitive presentation of the main circuit structure is significant for understanding the M3C. Instead of the original presentation in [8], it is more straightforward to display the M3C main circuit structure as shown in Figure 1, which makes the M3C topology regarded as an extended MMC topology by adding three middle arms to the conventional MMC.

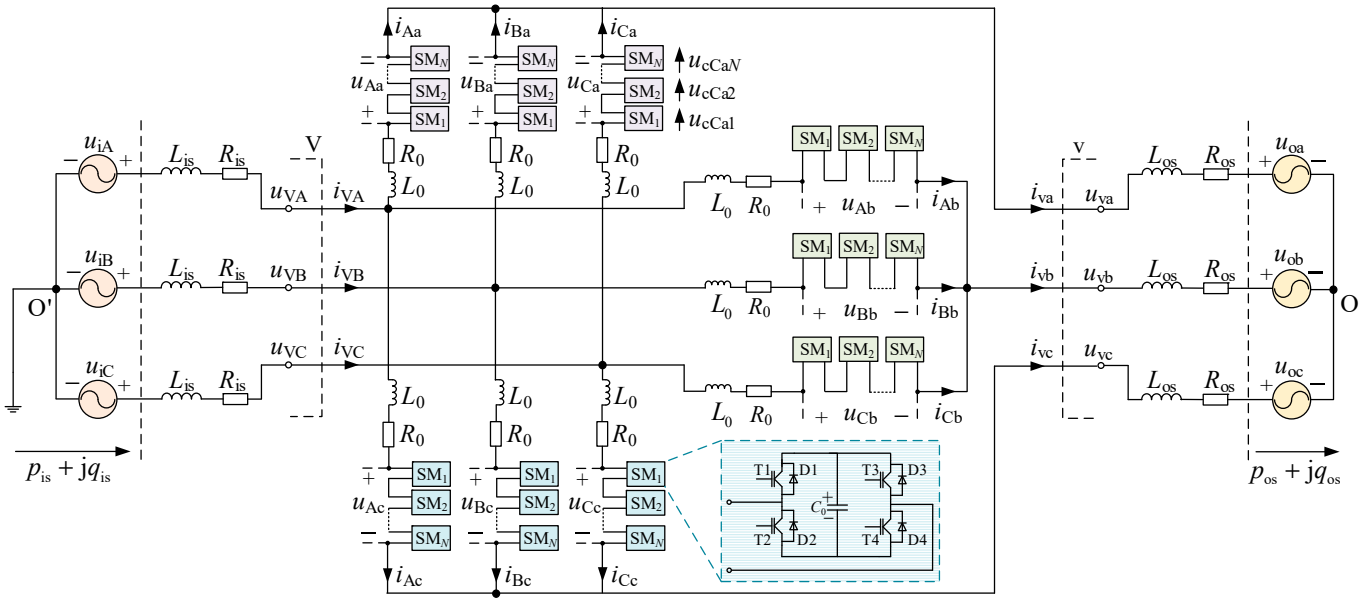

Figure 1. Main circuit structure of M3C.

The physical meanings and reference directions of the basic variables in the M3C are plotted in Figure 1. j (j = A, B, C) and k (k = a, b, c) in the subscript denote phase j on the input side and phase k on the output side, respectively. u_{ij} and u_{ok} represent the system voltage on the input side and the output side. p_{is} and q_{is} are the instantaneous active power and reactive power of the input system. The instantaneous active power and reactive power of the output system are expressed as p_{os} and q_{os}. The system resistance and inductance on the input side are denoted as R_{is} and L_{is}. R_{os} and L_{os} represent the system resistance and inductance on the output side. In addition, V and v are symbols of the M3C AC ports on the input side and the output side. u_{Vj} and i_{Vj} denote the M3C AC voltage and current on the input side. u_{vk} and i_{vk} are the M3C AC voltage and current on the output side. In addition, SMs in the M3C are FBSMs, each FBSM involves four insulated gate bipolar transistors (IGBTs) T_h (h = 1, 2, 3, 4) with four anti-parallel diodes D_h and a storage capacitor C_0. L_0 is the arm inductance and R_0 represents the equivalent arm resistance. u_{jk} and i_{jk} express the voltage and current of arm jk, and u_{cjkm} is the capacitor voltage of the mth SM in arm jk. O′ and O denote the neutral point of the input side and the output side.

According to the basic structure in Figure 1, the mathematical model of the M3C is derived. First, applying the Kirchhoff's voltage law (KVL) to Figure 1 yields:

$$\begin{aligned}
&(L_0\tfrac{\mathrm{d}}{\mathrm{d}t}+R_0)\begin{bmatrix} i_{\mathrm{Aa}} & i_{\mathrm{Ab}} & i_{\mathrm{Ac}} \\ i_{\mathrm{Ba}} & i_{\mathrm{Bb}} & i_{\mathrm{Bc}} \\ i_{\mathrm{Ca}} & i_{\mathrm{Cb}} & i_{\mathrm{Cc}} \end{bmatrix}+\begin{bmatrix} u_{\mathrm{Aa}} & u_{\mathrm{Ab}} & u_{\mathrm{Ac}} \\ u_{\mathrm{Ba}} & u_{\mathrm{Bb}} & u_{\mathrm{Bc}} \\ u_{\mathrm{Ca}} & u_{\mathrm{Cb}} & u_{\mathrm{Cc}} \end{bmatrix} \\
&=-(L_{\mathrm{is}}\tfrac{\mathrm{d}}{\mathrm{d}t}+R_{\mathrm{is}})\begin{bmatrix} i_{\mathrm{VA}} & i_{\mathrm{VA}} & i_{\mathrm{VA}} \\ i_{\mathrm{VB}} & i_{\mathrm{VB}} & i_{\mathrm{VB}} \\ i_{\mathrm{VC}} & i_{\mathrm{VC}} & i_{\mathrm{VC}} \end{bmatrix}-(L_{\mathrm{os}}\tfrac{\mathrm{d}}{\mathrm{d}t}+R_{\mathrm{os}})\begin{bmatrix} i_{\mathrm{va}} & i_{\mathrm{vb}} & i_{\mathrm{vc}} \\ i_{\mathrm{va}} & i_{\mathrm{vb}} & i_{\mathrm{vc}} \\ i_{\mathrm{va}} & i_{\mathrm{vb}} & i_{\mathrm{vc}} \end{bmatrix} \\
&+\begin{bmatrix} u_{\mathrm{iA}} & u_{\mathrm{iA}} & u_{\mathrm{iA}} \\ u_{\mathrm{iB}} & u_{\mathrm{iB}} & u_{\mathrm{iB}} \\ u_{\mathrm{iC}} & u_{\mathrm{iC}} & u_{\mathrm{iC}} \end{bmatrix}-\begin{bmatrix} u_{\mathrm{oa}} & u_{\mathrm{ob}} & u_{\mathrm{oc}} \\ u_{\mathrm{oa}} & u_{\mathrm{ob}} & u_{\mathrm{oc}} \\ u_{\mathrm{oa}} & u_{\mathrm{ob}} & u_{\mathrm{oc}} \end{bmatrix}+\begin{bmatrix} u_{\mathrm{O'O}} & u_{\mathrm{O'O}} & u_{\mathrm{O'O}} \\ u_{\mathrm{O'O}} & u_{\mathrm{O'O}} & u_{\mathrm{O'O}} \\ u_{\mathrm{O'O}} & u_{\mathrm{O'O}} & u_{\mathrm{O'O}} \end{bmatrix}
\end{aligned} \tag{1}$$

where $u_{O'O}$ is the voltage difference of two neutral points.

Based on the Kirchhoff's current law (KCL), the relationships between the arm currents and the AC currents on the input side and output side of the M3C can be expressed as:

$$\begin{bmatrix} i_{VA} \\ i_{VB} \\ i_{VC} \end{bmatrix} = \begin{bmatrix} i_{Aa} \\ i_{Ba} \\ i_{Ca} \end{bmatrix} + \begin{bmatrix} i_{Ab} \\ i_{Bb} \\ i_{Cb} \end{bmatrix} + \begin{bmatrix} i_{Ac} \\ i_{Bc} \\ i_{Cc} \end{bmatrix} \tag{2}$$

$$\begin{bmatrix} i_{va} \\ i_{vb} \\ i_{vc} \end{bmatrix} = \begin{bmatrix} i_{Aa} \\ i_{Ab} \\ i_{Ac} \end{bmatrix} + \begin{bmatrix} i_{Ba} \\ i_{Bb} \\ i_{Bc} \end{bmatrix} + \begin{bmatrix} i_{Ca} \\ i_{Cb} \\ i_{Cc} \end{bmatrix} \tag{3}$$

Define u_{sumj} (j = A, B, C) and u_{comk} (k = a, b, c) as the common-mode voltages on the input side and the output side:

$$\begin{bmatrix} u_{sumA} \\ u_{sumB} \\ u_{sumC} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} u_{Aa} + u_{Ab} + u_{Ac} \\ u_{Ba} + u_{Bb} + u_{Bc} \\ u_{Ca} + u_{Cb} + u_{Cc} \end{bmatrix} \tag{4}$$

$$\begin{bmatrix} u_{coma} \\ u_{comb} \\ u_{comc} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} u_{Aa} + u_{Ba} + u_{Ca} \\ u_{Ab} + u_{Bb} + u_{Cb} \\ u_{Ac} + u_{Bc} + u_{Cc} \end{bmatrix} \tag{5}$$

For the modeling analysis and controller design of the M3C, it is more convenient to implement in the orthogonal reference frame, where the physical quantities on each axis can be decoupled and the redundant equations can be naturally eliminated. The αβ0 reference frame is one of the most widely used orthogonal reference frames. The abc-αβ0 (ABC-αβ0) reference frame transformation matrix is defined as [25]:

$$\boldsymbol{T}_{abc-\alpha\beta0} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \tag{6}$$

Transform the common-mode voltages u_{sumj} (j = A, B, C) and u_{comk} (k = a, b, c) to the αβ0 reference frame through premultiplying (4) and (5) by $\boldsymbol{T}_{abc\text{-}\alpha\beta0}$:

$$\begin{bmatrix} u_{sum\alpha} \\ u_{sum\beta} \\ u_{sum0} \end{bmatrix} = \boldsymbol{T}_{abc-\alpha\beta0} \begin{bmatrix} u_{sumA} \\ u_{sumB} \\ u_{sumC} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} u_{\alpha a} + u_{\alpha b} + u_{\alpha c} \\ u_{\beta a} + u_{\beta b} + u_{\beta c} \\ u_{0a} + u_{0b} + u_{0c} \end{bmatrix} \tag{7}$$

$$\begin{bmatrix} u_{com\alpha} \\ u_{com\beta} \\ u_{com0} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} u_{coma} \\ u_{comb} \\ u_{comc} \end{bmatrix} \tag{8}$$

Transform the arm currents from the ABC reference frame to the αβ0 reference frame:

$$\begin{bmatrix} i_{\alpha a} & i_{\alpha b} & i_{\alpha c} \\ i_{\beta a} & i_{\beta b} & i_{\beta c} \\ i_{0a} & i_{0b} & i_{0c} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} i_{Aa} & i_{Ab} & i_{Ac} \\ i_{Ba} & i_{Bb} & i_{Bc} \\ i_{Ca} & i_{Cb} & i_{Cc} \end{bmatrix} \tag{9}$$

Transform the arm voltages from the ABC reference frame to the αβ0 reference frame:

$$\begin{bmatrix} u_{\alpha a} & u_{\alpha b} & u_{\alpha c} \\ u_{\beta a} & u_{\beta b} & u_{\beta c} \\ u_{0a} & u_{0b} & u_{0c} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} u_{Aa} & u_{Ab} & u_{Ac} \\ u_{Ba} & u_{Bb} & u_{Bc} \\ u_{Ca} & u_{Cb} & u_{Cc} \end{bmatrix} \tag{10}$$

Substituting (9) into (2) gives:

$$\begin{bmatrix} i_{V\alpha} \\ i_{V\beta} \\ i_{V0} \end{bmatrix} = \boldsymbol{T}_{abc-\alpha\beta0} \begin{bmatrix} i_{VA} \\ i_{VB} \\ i_{VC} \end{bmatrix} = \begin{bmatrix} i_{\alpha a} + i_{\alpha b} + i_{\alpha c} \\ i_{\beta a} + i_{\beta b} + i_{\beta c} \\ i_{0a} + i_{0b} + i_{0c} \end{bmatrix} \tag{11}$$

Inserting (3) into (9) yields:

$$\begin{bmatrix} i_{0a} \\ i_{0b} \\ i_{0c} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} i_{Aa} + i_{Ba} + i_{Ca} \\ i_{Ab} + i_{Bb} + i_{Cb} \\ i_{Ac} + i_{Bc} + i_{Cc} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} i_{va} \\ i_{vb} \\ i_{vc} \end{bmatrix} \tag{12}$$

Substituting (5) into (10) gives:

$$\begin{bmatrix} u_{0a} \\ u_{0b} \\ u_{0c} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} u_{Aa} + u_{Ba} + u_{Ca} \\ u_{Ab} + u_{Bb} + u_{Cb} \\ u_{Ac} + u_{Bc} + u_{Cc} \end{bmatrix} = \sqrt{3} \begin{bmatrix} u_{coma} \\ u_{comb} \\ u_{comc} \end{bmatrix} \tag{13}$$

Then, transform (1) from the ABC reference frame to the αβ0 reference frame through premultiplying (1) by $\boldsymbol{T}_{abc\text{-}\alpha\beta0}$:

$$\begin{aligned} &(L_0 \tfrac{d}{dt} + R_0) \begin{bmatrix} i_{\alpha a} & i_{\alpha b} & i_{\alpha c} \\ i_{\beta a} & i_{\beta b} & i_{\beta c} \\ i_{0a} & i_{0b} & i_{0c} \end{bmatrix} + \begin{bmatrix} u_{\alpha a} & u_{\alpha b} & u_{\alpha c} \\ u_{\beta a} & u_{\beta b} & u_{\beta c} \\ u_{0a} & u_{0b} & u_{0c} \end{bmatrix} \\ &= -(L_{is} \tfrac{d}{dt} + R_{is}) \begin{bmatrix} i_{V\alpha} & i_{V\alpha} & i_{V\alpha} \\ i_{V\beta} & i_{V\beta} & i_{V\beta} \\ i_{V0} & i_{V0} & i_{V0} \end{bmatrix} - \sqrt{3}(L_{os} \tfrac{d}{dt} + R_{os}) \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ i_{va} & i_{vb} & i_{vc} \end{bmatrix} \\ &+ \begin{bmatrix} u_{i\alpha} & u_{i\alpha} & u_{i\alpha} \\ u_{i\beta} & u_{i\beta} & u_{i\beta} \\ u_{i0} & u_{i0} & u_{i0} \end{bmatrix} - \sqrt{3} \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ u_{oa} & u_{ob} & u_{oc} \end{bmatrix} + \sqrt{3} \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ u_{O'O} & u_{O'O} & u_{O'O} \end{bmatrix} \end{aligned} \tag{14}$$

Equation (14) can be split into (15) and (16), which describe the characteristics of the input side and the output side of the M3C, respectively:

$$\begin{aligned} &(L_0 \tfrac{d}{dt} + R_0) \begin{bmatrix} i_{\alpha a} & i_{\alpha b} & i_{\alpha c} \\ i_{\beta a} & i_{\beta b} & i_{\beta c} \end{bmatrix} + \begin{bmatrix} u_{\alpha a} & u_{\alpha b} & u_{\alpha c} \\ u_{\beta a} & u_{\beta b} & u_{\beta c} \end{bmatrix} \\ &= -(L_{is} \tfrac{d}{dt} + R_{is}) \begin{bmatrix} i_{V\alpha} & i_{V\alpha} & i_{V\alpha} \\ i_{V\beta} & i_{V\beta} & i_{V\beta} \end{bmatrix} + \begin{bmatrix} u_{i\alpha} & u_{i\alpha} & u_{i\alpha} \\ u_{i\beta} & u_{i\beta} & u_{i\beta} \end{bmatrix} \end{aligned} \tag{15}$$

$$\begin{aligned} &(L_0 \tfrac{d}{dt} + R_0) \begin{bmatrix} i_{0a} \\ i_{0b} \\ i_{0c} \end{bmatrix} + \begin{bmatrix} u_{0a} \\ u_{0b} \\ u_{0c} \end{bmatrix} = -(L_{is} \tfrac{d}{dt} + R_{is}) \begin{bmatrix} i_{V0} \\ i_{V0} \\ i_{V0} \end{bmatrix} + \begin{bmatrix} u_{i0} \\ u_{i0} \\ u_{i0} \end{bmatrix} \\ &-\sqrt{3}(L_{os} \tfrac{d}{dt} + R_{os}) \begin{bmatrix} i_{va} \\ i_{vb} \\ i_{vc} \end{bmatrix} - \sqrt{3} \begin{bmatrix} u_{oa} \\ u_{ob} \\ u_{oc} \end{bmatrix} + \sqrt{3} \begin{bmatrix} u_{O'O} \\ u_{O'O} \\ u_{O'O} \end{bmatrix} \end{aligned} \tag{16}$$

Substituting (12) and (13) into (16) gives:

$$\begin{aligned} &[(L_0 + 3L_{os}) \tfrac{d}{dt} + (R_0 + 3R_{os})] \begin{bmatrix} i_{va} \\ i_{vb} \\ i_{vc} \end{bmatrix} + 3 \begin{bmatrix} u_{coma} \\ u_{comb} \\ u_{comc} \end{bmatrix} \\ &= -\sqrt{3}(L_{is} \tfrac{d}{dt} + R_{is}) \begin{bmatrix} i_{V0} \\ i_{V0} \\ i_{V0} \end{bmatrix} + \sqrt{3} \begin{bmatrix} u_{i0} \\ u_{i0} \\ u_{i0} \end{bmatrix} - 3 \begin{bmatrix} u_{oa} \\ u_{ob} \\ u_{oc} \end{bmatrix} + 3 \begin{bmatrix} u_{O'O} \\ u_{O'O} \\ u_{O'O} \end{bmatrix} \end{aligned} \tag{17}$$

Premultiplying (17) by $\boldsymbol{T}_{\text{abc-}\alpha\beta0}$, the variables on the M3C output side are transformed from the abc reference frame to the αβ0 reference frame:

$$\begin{aligned}&[(L_0+3L_{\text{os}})\tfrac{\text{d}}{\text{d}t}+(R_0+3R_{\text{os}})]\begin{bmatrix} i_{\text{v}\alpha} \\ i_{\text{v}\beta} \\ i_{\text{v}0} \end{bmatrix}+3\begin{bmatrix} u_{\text{com}\alpha} \\ u_{\text{com}\beta} \\ u_{\text{com}0} \end{bmatrix}\\ &=-3(L_{\text{is}}\tfrac{\text{d}}{\text{d}t}+R_{\text{is}})\begin{bmatrix} 0 \\ 0 \\ i_{\text{V}0} \end{bmatrix}+3\begin{bmatrix} 0 \\ 0 \\ u_{\text{i}0} \end{bmatrix}-3\begin{bmatrix} u_{\text{o}\alpha} \\ u_{\text{o}\beta} \\ u_{\text{o}0} \end{bmatrix}+3\sqrt{3}\begin{bmatrix} 0 \\ 0 \\ u_{\text{O'O}} \end{bmatrix}\end{aligned} \tag{18}$$

where $i_{\text{V}0} = i_{\text{v}0} = u_{\text{i}0} = u_{\text{o}0} = 0$ as the three-phase AC systems on both sides of the M3C are symmetrical. Then, (18) can be split into (19) and (20):

$$(L_{\text{o}\Sigma}\frac{\text{d}}{\text{d}t}+R_{\text{o}\Sigma})\begin{bmatrix} i_{\text{v}\alpha} \\ i_{\text{v}\beta} \end{bmatrix}=-\begin{bmatrix} u_{\text{com}\alpha} \\ u_{\text{com}\beta} \end{bmatrix}-\begin{bmatrix} u_{\text{o}\alpha} \\ u_{\text{o}\beta} \end{bmatrix} \tag{19}$$

$$u_{\text{com}0}=\sqrt{3}\cdot u_{\text{O'O}} \tag{20}$$

where $L_{\text{o}\Sigma} = L_{\text{os}} + L_0/3$, $R_{\text{o}\Sigma} = R_{\text{os}} + R_0/3$.

Combining (7), (8), (13), and (20) gives:

$$u_{\text{sum}0}=u_{\text{com}0}=\sqrt{3}\cdot u_{\text{O'O}} \tag{21}$$

Equation (15) can be split into (22)–(24):

$$(L_0\frac{\text{d}}{\text{d}t}+R_0)\begin{bmatrix} i_{\alpha\text{a}} \\ i_{\beta\text{a}} \end{bmatrix}+\begin{bmatrix} u_{\alpha\text{a}} \\ u_{\beta\text{a}} \end{bmatrix}=-(L_{\text{is}}\frac{\text{d}}{\text{d}t}+R_{\text{is}})\begin{bmatrix} i_{\text{V}\alpha} \\ i_{\text{V}\beta} \end{bmatrix}+\begin{bmatrix} u_{\text{i}\alpha} \\ u_{\text{i}\beta} \end{bmatrix} \tag{22}$$

$$(L_0\frac{\text{d}}{\text{d}t}+R_0)\begin{bmatrix} i_{\alpha\text{b}} \\ i_{\beta\text{b}} \end{bmatrix}+\begin{bmatrix} u_{\alpha\text{b}} \\ u_{\beta\text{b}} \end{bmatrix}=-(L_{\text{is}}\frac{\text{d}}{\text{d}t}+R_{\text{is}})\begin{bmatrix} i_{\text{V}\alpha} \\ i_{\text{V}\beta} \end{bmatrix}+\begin{bmatrix} u_{\text{i}\alpha} \\ u_{\text{i}\beta} \end{bmatrix} \tag{23}$$

$$(L_0\frac{\text{d}}{\text{d}t}+R_0)\begin{bmatrix} i_{\alpha\text{c}} \\ i_{\beta\text{c}} \end{bmatrix}+\begin{bmatrix} u_{\alpha\text{c}} \\ u_{\beta\text{c}} \end{bmatrix}=-(L_{\text{is}}\frac{\text{d}}{\text{d}t}+R_{\text{is}})\begin{bmatrix} i_{\text{V}\alpha} \\ i_{\text{V}\beta} \end{bmatrix}+\begin{bmatrix} u_{\text{i}\alpha} \\ u_{\text{i}\beta} \end{bmatrix} \tag{24}$$

Adding up (22), (23), and (24) yields:

$$\begin{aligned}&(L_0\tfrac{\text{d}}{\text{d}t}+R_0)\begin{bmatrix} i_{\alpha\text{a}}+i_{\alpha\text{b}}+i_{\alpha\text{c}} \\ i_{\beta\text{a}}+i_{\beta\text{b}}+i_{\beta\text{c}} \end{bmatrix}+\begin{bmatrix} u_{\alpha\text{a}}+u_{\alpha\text{b}}+u_{\alpha\text{c}} \\ u_{\beta\text{a}}+u_{\beta\text{b}}+u_{\beta\text{c}} \end{bmatrix}\\ &=-3(L_{\text{is}}\tfrac{\text{d}}{\text{d}t}+R_{\text{is}})\begin{bmatrix} i_{\text{V}\alpha} \\ i_{\text{V}\beta} \end{bmatrix}+3\begin{bmatrix} u_{\text{i}\alpha} \\ u_{\text{i}\beta} \end{bmatrix}\end{aligned} \tag{25}$$

According to (7) and (11), (25) can be rewritten as:

$$(L_{\text{i}\Sigma}\frac{\text{d}}{\text{d}t}+R_{\text{i}\Sigma})\begin{bmatrix} i_{\text{V}\alpha} \\ i_{\text{V}\beta} \end{bmatrix}=-\begin{bmatrix} u_{\text{sum}\alpha} \\ u_{\text{sum}\beta} \end{bmatrix}+\begin{bmatrix} u_{\text{i}\alpha} \\ u_{\text{i}\beta} \end{bmatrix} \tag{26}$$

where $L_{\text{i}\Sigma} = L_{\text{is}} + L_0/3$, $R_{\text{i}\Sigma} = R_{\text{is}} + R_0/3$.

Define $i_{l\text{cir}1}$ and $i_{l\text{cir}2}$ (l = α, β) as circulating currents in the αβ0 reference frame as in (27); define $u_{l\text{cir}1}$ and $u_{l\text{cir}2}$ (l = α, β) as circulating voltages in the αβ0 reference frame as in (28):

$$\begin{bmatrix} i_{\alpha\text{b}}-i_{\alpha\text{a}} \\ i_{\beta\text{b}}-i_{\beta\text{a}} \end{bmatrix}=\begin{bmatrix} i_{\alpha\text{cir}1} \\ i_{\beta\text{cir}1} \end{bmatrix},\begin{bmatrix} i_{\alpha\text{c}}-i_{\alpha\text{a}} \\ i_{\beta\text{c}}-i_{\beta\text{a}} \end{bmatrix}=\begin{bmatrix} i_{\alpha\text{cir}2} \\ i_{\beta\text{cir}2} \end{bmatrix} \tag{27}$$

$$\begin{bmatrix} u_{\alpha\text{b}}-u_{\alpha\text{a}} \\ u_{\beta\text{b}}-u_{\beta\text{a}} \end{bmatrix}=\begin{bmatrix} u_{\alpha\text{cir}1} \\ u_{\beta\text{cir}1} \end{bmatrix},\begin{bmatrix} u_{\alpha\text{c}}-u_{\alpha\text{a}} \\ u_{\beta\text{c}}-u_{\beta\text{a}} \end{bmatrix}=\begin{bmatrix} u_{\alpha\text{cir}2} \\ u_{\beta\text{cir}2} \end{bmatrix} \tag{28}$$

Subtracting (22) from (23) and (24), respectively, the relationship between the circulating currents and the circulating voltages can be described as:

$$(L_0\frac{\mathrm{d}}{\mathrm{d}t}+R_0)\begin{bmatrix}i_{\alpha\mathrm{cir1}}\\ i_{\beta\mathrm{cir1}}\end{bmatrix}+\begin{bmatrix}u_{\alpha\mathrm{cir1}}\\ u_{\beta\mathrm{cir1}}\end{bmatrix}=0 \tag{29}$$

$$(L_0\frac{\mathrm{d}}{\mathrm{d}t}+R_0)\begin{bmatrix}i_{\alpha\mathrm{cir2}}\\ i_{\beta\mathrm{cir2}}\end{bmatrix}+\begin{bmatrix}u_{\alpha\mathrm{cir2}}\\ u_{\beta\mathrm{cir2}}\end{bmatrix}=0 \tag{30}$$

It is noticed that the circulating currents are only determined by the arm reactance and the arm voltage inside the M3C and have no direct relationship with the input side and the output side of the M3C.

Hence, (19), (21), (26), (29), and (30) constitute the 9th order mathematical model of the M3C in the αβ0 reference frame.

To simplify the controller design, (19) and (26) corresponding to the external quantities of the M3C are transformed to the dq reference frame. The αβ0-dq reference frame transformation matrices on the input side and the output side of the M3C are defined as [25]:

$$\boldsymbol{T}^{\omega_\mathrm{i}}_{\alpha\beta0-\mathrm{dq}}=\begin{bmatrix}\cos\omega_\mathrm{i}t & \sin\omega_\mathrm{i}t\\ -\sin\omega_\mathrm{i}t & \cos\omega_\mathrm{i}t\end{bmatrix} \tag{31}$$

$$\boldsymbol{T}^{\omega_\mathrm{o}}_{\alpha\beta0-\mathrm{dq}}=\begin{bmatrix}\cos\omega_\mathrm{o}t & \sin\omega_\mathrm{o}t\\ -\sin\omega_\mathrm{o}t & \cos\omega_\mathrm{o}t\end{bmatrix} \tag{32}$$

where $\omega_\mathrm{i}t$ is the voltage phase angle of phase-A of the input system and $\omega_\mathrm{o}t$ is the voltage phase angle of phase-a of the output system, both of which are acquired by the phase-locked loop (PLL).

Premultiplying (26) and (19) by (31) and (32), respectively, the input and output side characteristics of the M3C in the dq reference frame can be expressed as:

$$L_{\mathrm{i}\Sigma}[\frac{\mathrm{d}}{\mathrm{d}t}-\begin{bmatrix}0 & \omega_\mathrm{i}\\ -\omega_\mathrm{i} & 0\end{bmatrix}]\begin{bmatrix}i_{\mathrm{Vd}}\\ i_{\mathrm{Vq}}\end{bmatrix}+R_{\mathrm{i}\Sigma}\begin{bmatrix}i_{\mathrm{Vd}}\\ i_{\mathrm{Vq}}\end{bmatrix}+\begin{bmatrix}u_{\mathrm{sumd}}\\ u_{\mathrm{sumq}}\end{bmatrix}=\begin{bmatrix}u_{\mathrm{id}}\\ u_{\mathrm{iq}}\end{bmatrix} \tag{33}$$

$$L_{\mathrm{o}\Sigma}[\frac{\mathrm{d}}{\mathrm{d}t}-\begin{bmatrix}0 & \omega_\mathrm{o}\\ -\omega_\mathrm{o} & 0\end{bmatrix}]\begin{bmatrix}i_{\mathrm{vd}}\\ i_{\mathrm{vq}}\end{bmatrix}+R_{\mathrm{o}\Sigma}\begin{bmatrix}i_{\mathrm{vd}}\\ i_{\mathrm{vq}}\end{bmatrix}+\begin{bmatrix}u_{\mathrm{comd}}\\ u_{\mathrm{comq}}\end{bmatrix}=-\begin{bmatrix}u_{\mathrm{od}}\\ u_{\mathrm{oq}}\end{bmatrix} \tag{34}$$

Until now, the mathematical model of the M3C has been derived based on the extended MMC topology in Figure 1 and the multiple αβ0 and dq transformations, as shown in (21), (29), (30), (33), and (34). The major benefits of the multiple αβ0 and dq transformations are in the following three aspects:

(1) By applying the multiple αβ0 and dq transformations, the derivation process can be more straight forward and easier to understand.

(2) Through the multiple αβ0 and dq transformations, the mathematical models of the input side and the output side of the M3C are basically consistent with the AC side mathematical model of the MMC. Thus, one M3C is equivalent to two decoupled MMCs on the input side and the output side. In other words, the M3C can be considered as an extension of the conventional MMC, which is beneficial for analyzing the M3C operating characteristics.

(3) The design of the M3C controller can be transformed into the design of controllers for two MMCs. In this way, the design method of the MMC controller can be adapted to the M3C controller design directly, which is beneficial for simplifying the M3C controller design.

3. Inner Loop Controller

Based on the previously derived mathematical model, the inner loop controller is divided into two parts to control the external characteristics and internal characteristics of

the M3C, respectively. The current tracking controller of the external characteristics on the input and output sides described by (10) and (11) is designed in the dq reference frame. The circulating current suppressing controller of the internal characteristics expressed by (5) and (6) is designed in the αβ0 reference frame. The outputs of the inner loop controller are integrated to obtain the voltage references of the 9 arms of the M3C.

3.1. Current Tracking Controller

By Laplace transform of (10), the dynamic characteristics of the input side in the s domain are represented as:

$$\begin{cases} (R_{i\Sigma} + L_{i\Sigma}s)i_{Vd}(s) = u_{id}(s) - u_{sumd}(s) + \omega_i L_{i\Sigma} i_{Vq}(s) \\ (R_{i\Sigma} + L_{i\Sigma}s)i_{Vq}(s) = u_{iq}(s) - u_{sumq}(s) - \omega_i L_{i\Sigma} i_{Vd}(s) \end{cases} \tag{35}$$

From (35), it is noticed that the currents on the input side (output variables) are determined by the system voltages (disturbance variables) and the common-mode voltages (control variables) on the input side. The current tracking controller on the input side is to obtain control variable references $u_{sumd}{}^*$ and $u_{sumq}{}^*$ by making output variables track their references $i_{Vd}{}^*$ and $i_{Vq}{}^*$.

To simplify the controller design, substituting variables in (35) with new control variables denoted by V_d and V_q yields:

$$\begin{cases} V_d(s) = u_{id}(s) - u_{sumd}(s) + \omega_i L_{i\Sigma} i_{Vq}(s) \\ V_q(s) = u_{iq}(s) - u_{sumq}(s) - \omega_i L_{i\Sigma} i_{Vd}(s) \end{cases} \tag{36}$$

According to (35) and (36), the transfer function between output variables and new control variables can be expressed as:

$$\begin{cases} \frac{i_{Vd}(s)}{V_d(s)} = \frac{1}{R_{i\Sigma} + L_{i\Sigma}s} = G(s) \\ \frac{i_{Vq}(s)}{V_q(s)} = \frac{1}{R_{i\Sigma} + L_{i\Sigma}s} = G(s) \end{cases} \tag{37}$$

Based on the classical negative feedback control theory, the control system with the simplest negative feedback shown in Figure 2 is adopted to make the output variables track their references.

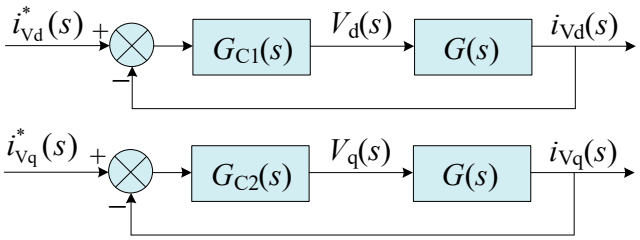

Figure 2. d-axis and q-axis closed-loop control system of output current.

In Figure 2, $G_{C1}(s)$ and $G_{C2}(s)$ are transfer functions of the d-axis controller and the q-axis controller, respectively:

$$\begin{cases} G_{C1}(s) = k_{p1} + \frac{k_{i1}}{s} \\ G_{C2}(s) = k_{p2} + \frac{k_{i2}}{s} \end{cases} \tag{38}$$

where k_{pg} and k_{ig} (g = 1, 2) are parameters of the current tracking proportional–integral (PI) controller on the input side.

According to (36), (37), (38), and Figure 2, the block diagram of the current controller and the system dynamic of the input side is illustrated in Figure 3.

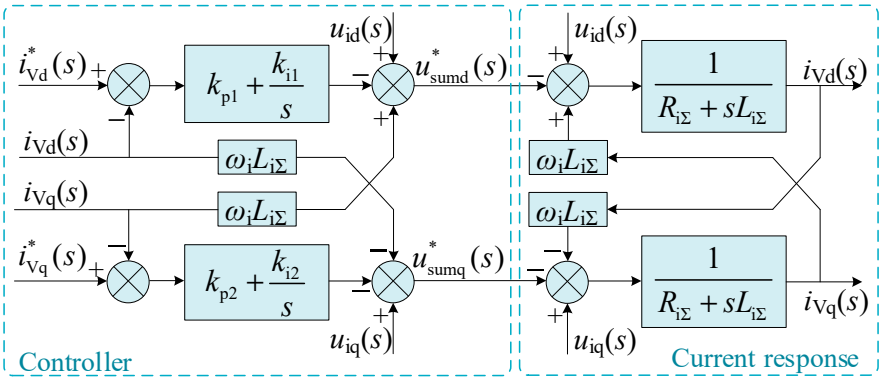

Figure 3. Block diagram of current tracking controller on input side of M3C.

Similar to the design of the current tracking controller on the input side, applying the Laplace transform on (34) yields:

$$\begin{cases} (R_{o\Sigma} + L_{o\Sigma}s) \cdot i_{vd}(s) = -u_{od}(s) - u_{comd}(s) + \omega_o L_{o\Sigma} i_{vq}(s) \\ (R_{o\Sigma} + L_{o\Sigma}s) \cdot i_{vq}(s) = -u_{oq}(s) - u_{comq}(s) - \omega_o L_{o\Sigma} i_{vd}(s) \end{cases} \tag{39}$$

It is obvious that the current on the output side (the output variables) depends on the system voltage and the common-mode voltage (the input variables) of the output side. The current tracking controller on the output side is to obtain the input variable references $u_{comd}{}^*$ and $u_{comq}{}^*$ by making output variables track their reference values $i_{vd}{}^*$ and $i_{vq}{}^*$.

The design steps of the current tracking controller on the output side are similar to those on the input side. The controller block diagram is illustrated in Figure 4, where $k_{pg}{}'$ and $k_{ig}{}'$ (g = 1, 2) are the parameters of the current tracking PI controller on the output side.

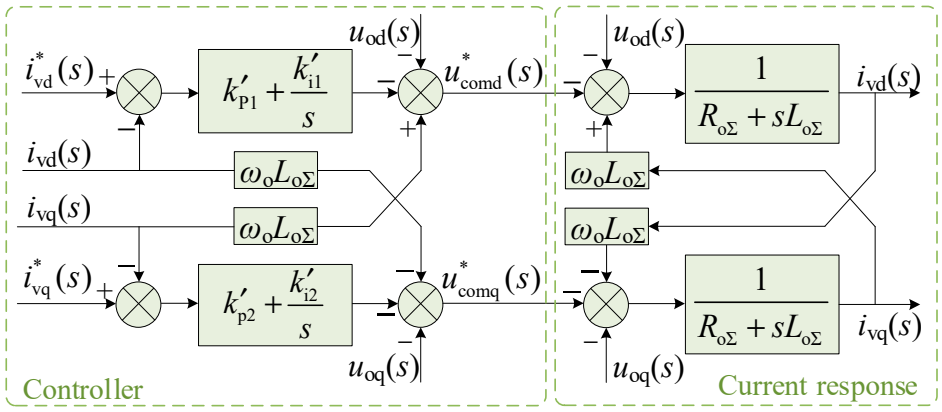

Figure 4. Block diagram of current tracking controller on the output side of M3C.

3.2. Circulating Current Suppressing Controller

Circulating currents only flow among the arms and produce no direct effects on either the input side or the output side of the M3C. The circulating currents will increase the power losses in the M3C and usually need to be suppressed. The circulating currents contain harmonic components of various frequencies, and it is unnecessary to design the controllers for each harmonic in the circulating currents. Therefore, the simple proportional controller as in (40) and (41) can be adopted for suppressing the circulating currents in the αβ0 reference frame. According to the relationship between the circulating voltages and the circulating currents in (29) and (30), the negative feedback theory can be adopted.

The circulating voltage references $u_{l\text{cir1}}{}^*$ and $u_{l\text{cir2}}{}^*$ (l = α, β) can be obtained by making circulating currents track their references $i_{l\text{cir1}}{}^*$ and $i_{l\text{cir2}}{}^*$:

$$\begin{bmatrix} u^*_{\alpha\text{cir1}} \\ u^*_{\beta\text{cir1}} \end{bmatrix} = k_{\text{cir1}} \begin{bmatrix} i^*_{\alpha\text{cir1}} - i_{\alpha\text{cir1}} \\ i^*_{\beta\text{cir1}} - i_{\beta\text{cir1}} \end{bmatrix} \tag{40}$$

$$\begin{bmatrix} u^*_{\alpha\text{cir2}} \\ u^*_{\beta\text{cir2}} \end{bmatrix} = k_{\text{cir2}} \begin{bmatrix} i^*_{\alpha\text{cir2}} - i_{\alpha\text{cir2}} \\ i^*_{\beta\text{cir2}} - i_{\beta\text{cir2}} \end{bmatrix} \tag{41}$$

where k_{cir1} and k_{cir2} are proportional coefficients of the circulating current suppressing controller, and circulating current references $i_{l\text{cir1}}{}^*$ and $i_{l\text{cir2}}{}^*$ are usually set as 0.

3.3. Calculation of Arm Voltage References

The key of the M3C controller design is to determine the voltage values that the 9 arms need to generate at any time, namely, the arm voltage references. The current tracking controller on the input side designed above generates references of the common-mode voltage on the input side, denoted as $u_{\text{sumd}}{}^*$ and $u_{\text{sumq}}{}^*$. Analogously, the references of the common-mode voltage on the output side $u_{\text{comd}}{}^*$ and $u_{\text{comq}}{}^*$ are acquired by the current tracking controller on the output side. The voltage references in the dq reference frame should be converted back to the αβ0 reference frame to obtain $u_{\text{sum}\alpha}{}^*$, $u_{\text{sum}\beta}{}^*$, $u_{\text{com}\alpha}{}^*$, and $u_{\text{com}\beta}{}^*$. Moreover, $u_{\text{O'O}}{}^*$ is set as 0. In addition, the circulating voltage references are attained in (40) and (41). Thus, the arm voltage references can be obtained as:

$$\boldsymbol{U}^*_{\text{arm}} = \begin{bmatrix} u^*_{\text{Aa}} & u^*_{\text{Ab}} & u^*_{\text{Ac}} \\ u^*_{\text{Ba}} & u^*_{\text{Bb}} & u^*_{\text{Bc}} \\ u^*_{\text{Ca}} & u^*_{\text{Cb}} & u^*_{\text{Cc}} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix}^{\text{T}} \begin{bmatrix} \boldsymbol{U}^*_{\alpha\beta} \\ \boldsymbol{U}^*_0 \end{bmatrix} \tag{42}$$

where $U_{\alpha\beta}{}^*$ and $U_0{}^*$ are calculated as:

$$\boldsymbol{U}^*_{\alpha\beta} = \begin{bmatrix} u^*_{\text{sum}\alpha} u^*_{\text{sum}\beta} \\ u^*_{\alpha\text{cir1}}\ u^*_{\beta\text{cir1}} \\ u^*_{\alpha\text{cir2}}\ u^*_{\beta\text{cir2}} \end{bmatrix}^{\text{T}} \begin{bmatrix} 1/3 & -1 & -1 \\ 1/3 & 1 & 0 \\ 1/3 & 0 & 1 \end{bmatrix}^{-1} \tag{43}$$

$$\boldsymbol{U}^*_0 = \sqrt{2} \begin{bmatrix} u^*_{\text{com}\alpha} \\ u^*_{\text{com}\beta} \\ u^*_{\text{com0}} \end{bmatrix}^{\text{T}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \tag{44}$$

4. SM Voltage Balancing Method

After obtaining the arm voltage references, the resulting issue is to determine how to switch the SMs to make each arm voltage track its reference and maintain voltage balance among all SMs in one arm. Meanwhile, unnecessary switching operations should be avoided to minimize the switching frequency. To achieve these objectives, a reduced switching frequency SM voltage balancing method is proposed in this section.

4.1. Operating Characteristics of FBSM

The SMs constituting the M3C are FBSMs, each of which involves four IGBTs T_h (h = 1, 2, 3, 4) with four anti-parallel diodes D_h and an SM capacitor C_0. The output voltage of the SM is represented as u_{sm}, and U_{c} denotes the rated SM capacitor voltage. The positive direction of the capacitor current is consistent with that of the arm current indicated in Figure 1, which is defined as the capacitor charging direction. The operating states of the FBSM are summarized in Table 1.

Table 1. Operating states of FBSM.

States	T1	T2	T3	T4	u_{sm}	Arm Current Direction	Capacitor Current Direction
Positively inserted	on	off	off	on	$+U_c$	Positive Negative	Positive Negative
Negatively inserted	off	on	on	off	$-U_c$	Positive Negative	Negative Positive
Bypassed	on off	off on	on off	off on	0	Positive Negative	—
Blocked	off	off	off	off	$+U_c$ $-U_c$	Positive Negative	Positive Positive

According to Table 1, it can be concluded that the operating states of the FBSM are only related to the conduction state of IGBTs. The first three normal operating states can be classified based on the polarity of the output voltage of the FBSM and the last state is abnormal, which is used during system startup or fault clearing. Moreover, the SM capacitor will not be charged in the bypassed state.

4.2. Switching Strategy of SM

Define the three characteristic variables S_{state}, D_{arm}, and C_{change} as:

$$S_{\text{state}} = \text{sign}(u_{jk}^*) = \begin{cases} 1 & \text{if } u_{jk}^* \geq 0 \\ -1 & \text{if } u_{jk}^* < 0 \end{cases} \tag{45}$$

$$D_{\text{arm}} = \text{sign}(i_{\text{arm}}) = \begin{cases} 1 & \text{if } i_{\text{arm}} \geq 0 \\ -1 & \text{if } i_{\text{arm}} < 0 \end{cases} \tag{46}$$

$$C_{\text{charge}} = S_{\text{state}} \cdot D_{\text{arm}} = \begin{cases} 1 \\ -1 \end{cases} \tag{47}$$

where $u_{jk}{}^*$ is the voltage reference of arm jk (j = A, B, C and k = a, b, c), and i_{arm} is the arm current. S_{state} represents the direction of the arm voltage, D_{arm} denotes the direction of the arm current, and C_{change} expresses the charging/discharging state of the SM capacitor. According to Table 1, the charging/discharging state of the capacitor is related to both the direction of the arm voltage and the direction of the arm current. If $C_{\text{change}} = 1$, it means that the capacitor is in the charging state; if $C_{\text{change}} = -1$, it means that the capacitor is in the discharging state.

The voltages of each arm are synthesized by the SM capacitor voltages. The number of the inserted SMs in arm jk is calculated as:

$$n_{jk} = \left| \text{round}\left(\frac{u_{jk}^*}{U_c}\right) \right| \geq 0 \tag{48}$$

where round() is the function to calculate the nearest integer; U_c denotes the rated SM voltage capacitor.

The variation of n_{jk} between two adjacent control moments is defined as:

$$\Delta n_{jk} = \begin{cases} n_{jk} - n_{jk,\text{old}} & \text{if } S_{\text{state}} = S_{\text{state,old}} \\ n_{jk} & \text{if } S_{\text{state}} \neq S_{\text{state,old}} \end{cases} \tag{49}$$

where the subscript 'old' expresses the value at the previous control moment.

The conventional SM voltage balancing algorithm based on sorting all capacitors' voltages proposed in [18] is as follows:

- When the arm current charges the capacitors ($C_{\text{change}} = 1$), n_{jk} SMs with the lowest capacitor voltages are inserted positively or negatively according to S_{state} and the other SMs are bypassed.
- When the arm current discharges the capacitors ($C_{\text{change}} = -1$), n_{jk} SMs with the highest capacitor voltages are inserted positively or negatively according to S_{state} and the other SMs are bypassed.

The conventional algorithm will result in a high switching frequency since the switchings of SMs are based on the SM capacitor voltages only at the present moment regardless of the previous state of SMs.

To decrease switching frequency by avoiding unnecessary switchings, a reduced switching frequency SM voltage balancing method is proposed as shown in Figure 5. This optimized balancing method considers the previous state of SMs and performs incremental switching as follows:

- If $\Delta n_{jk} = 0$, SMs in arm *jk* have no switching operation at the current control moment and directly wait for the next control moment.
- If $\Delta n_{jk} > 0$, the number of the inserted SMs should be increased. Then, if $C_{\text{change}} = 1$, Δn_{jk} SMs with the lowest voltage are inserted; if $C_{\text{change}} = -1$, Δn_{jk} SMs with the highest voltage are inserted. S_{state} determines whether the insertion is positive or negative.
- If $\Delta n_{jk} < 0$, the number of the inserted SMs should be decreased. Then, if $C_{\text{change}} = 1$, Δn_{jk} SMs with the highest voltage are bypassed, and if $C_{\text{change}} = -1$, Δn_{jk} SMs with the lowest voltage are bypassed.

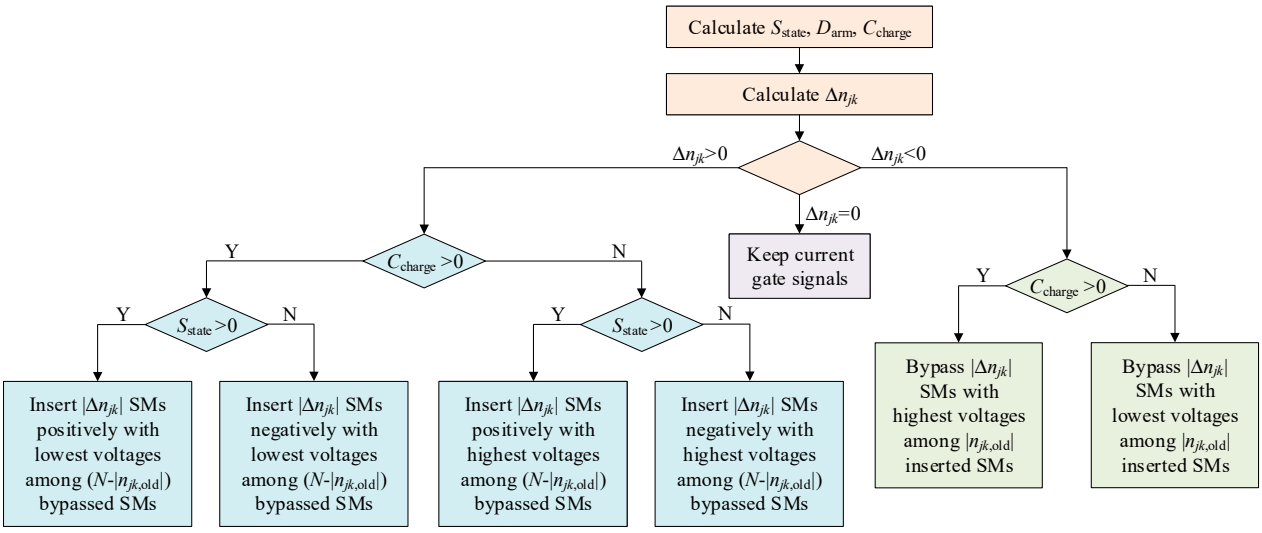

Figure 5. Reduced switching frequency SM voltage balancing method based on state sorting and incremental switching.

5. Outer Loop Controller

The outer loop controller is required for both the input side and the output side of the M3C. For the scenario of M3C-based offshore wind power LFAC integration, the input side of the M3C is connected to the offshore AC system with grid-following wind turbines, and the input side should operate in the V/f mode to provide stable AC voltage support; the output side of the M3C is connected to the onshore AC grid, and the control target is to maintain the SM capacitor voltage. The outer loop controller is designed according to the reference direction as shown in Figure 1.

5.1. Outer Loop Controller on Input Side

The input side of the M3C should operate in the V/f mode to provide stable AC voltage support for the offshore wind farm. There are two control objectives: one is to control the frequency of the offshore system to the rated frequency and the other is to control the voltage amplitude of the input side AC bus constant.

The outer loop control strategy on the input side of the M3C has two significant characteristics:

(1) PLL is no longer needed because the frequency of the offshore system is given, i.e., the electrical angle is completely determined and the rotating speed of the dq reference frame is fixed.

(2) Define the space vector of the AC bus voltage on the input side as $\boldsymbol{u}_{\mathrm{is}}$. The outer loop controller on the input side is used for keeping the amplitude of $\boldsymbol{u}_{\mathrm{is}}$ unchanged and keeping $\boldsymbol{u}_{\mathrm{is}}$ aligned with the d-axis. In other words, the constant amplitude of $\boldsymbol{u}_{\mathrm{is}}$ means that the voltage amplitude of the input side AC bus is constant; the alignment of $\boldsymbol{u}_{\mathrm{is}}$ with the d-axis means that the voltage frequency of the input side AC bus equals the rated frequency.

To achieve the above two points, the outer loop controller on the input side makes $u_{\mathrm{id}} = U_{\mathrm{im}}$ by controlling the d-axis current reference $i_{\mathrm{Vd}}{}^{*}$, and $u_{\mathrm{iq}} = 0$ by controlling the q-axis current references $i_{\mathrm{Vq}}{}^{*}$. $i_{\mathrm{Vd}}{}^{*}$ and $i_{\mathrm{Vq}}{}^{*}$ are the current references for the current tracking controller on the input side of the M3C. Moreover, limiters are added to ensure that the current references are within the upper limits. The upper limits vary with operating conditions and can be simplified as:

$$\begin{cases} i_{\mathrm{Vdmax}} = \sqrt{I_{\mathrm{Vmmax}}^2 - i_{\mathrm{Vq}}^2(t - T_{\mathrm{ctrl}})} \\ i_{\mathrm{Vqmax}} = \sqrt{I_{\mathrm{Vmmax}}^2 - i_{\mathrm{Vd}}^2(t - T_{\mathrm{ctrl}})} \end{cases} \tag{50}$$

where I_{Vmmax} denotes the maximum current on the input side, which can be derived from the rated capacity and the rated AC voltage; $i_{\mathrm{Vd}}(t - T_{\mathrm{ctrl}})$ (or $i_{\mathrm{Vq}}(t - T_{\mathrm{ctrl}})$) is the d-axis (or q-axis) current on the input side measured in the previous control period.

After considering the above factors, the structure of the outer loop controller on the input side of the M3C is shown in Figure 6.

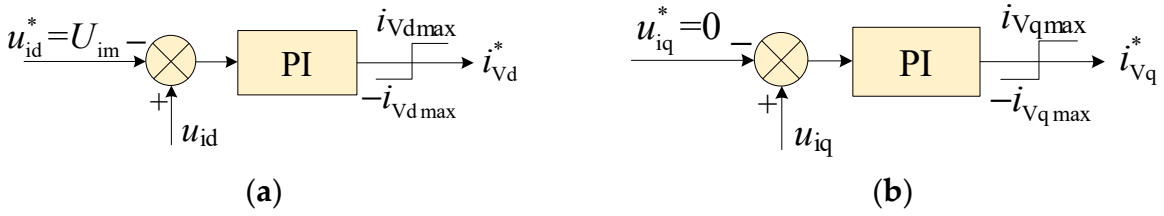

Figure 6. Outer loop controller on the input side of M3C: (**a**) d-axis controller; (**b**) q-axis controller.

5.2. Outer Loop Controller on the Output Side

The instantaneous active power p_{os} and the instantaneous reactive power q_{os} on the M3C output side can be expressed as:

$$\begin{bmatrix} p_{\mathrm{os}} \\ q_{\mathrm{os}} \end{bmatrix} = \begin{bmatrix} u_{\mathrm{od}} & u_{\mathrm{oq}} \\ u_{\mathrm{oq}} & -u_{\mathrm{od}} \end{bmatrix} \begin{bmatrix} i_{\mathrm{vd}} \\ i_{\mathrm{vq}} \end{bmatrix} \tag{51}$$

In the steady state, the q-axis component of the output side system voltage u_{oq} is 0, and the d-axis component of the output side system voltage u_{od} is equal to the system voltage amplitude U_{om}. Thus, (51) can be rewritten as:

$$p_{\mathrm{os}} = u_{\mathrm{od}} i_{\mathrm{vd}} = U_{\mathrm{om}} i_{\mathrm{vd}} \tag{52}$$

$$q_{os} = -u_{od} i_{vq} = -U_{om} i_{vq} \tag{53}$$

The control objectives of the outer loop controller on the output side are divided into two categories, including the active power control objective and the reactive power control objective:

(1) The reference of the active power control is the average capacitor voltage of all SMs $U_{c,ave}^*$; from the perspective of energy balance, this side behaves as a power balance station.
(2) Either the reactive power Q_{os}^* or the AC voltage amplitude U_{om}^* on the output side is the reference of the reactive power control.

The outputs of the outer loop controller on the output side are the d- and q-axis current references i_{vd}^* and i_{vq}^* for the current tracking controller on the output side. When the vector current control is adopted, the active power control loop and the reactive power control loop can be decoupled.

5.2.1. Active Power Control Loop

The active power control loop has to maintain the SM capacitor voltage as shown in Figure 7. Moreover, considering that the M3C cannot be overloaded, the output i_{vd}^* of the active power control loop shall be limited. The upper limit i_{vdmax} can be calculated as:

$$i_{vdmax} = \sqrt{I_{vmmax}^2 - i_{vq}^2(t - T_{ctrl})} \tag{54}$$

where I_{vmmax} denotes the maximum current on the output side; $i_{vq}(t - T_{ctrl})$ is the q-axis current on the output side measured in the previous control period.

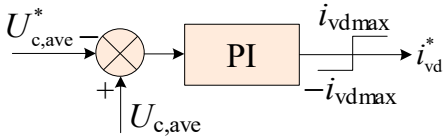

Figure 7. Active power control loop of outer loop controller on output side of M3C.

5.2.2. Reactive Power Control Loop

In accordance with (53), i_{vq}^* can be directly calculated when Q_{os}^* is given; yet to eliminate the steady-state error, the negative feedback of the reactive power by the PI controller is required. Therefore, the reactive power control loop with given Q_{os}^* is illustrated in Figure 8a. Figure 8b represents the reactive power control loop with prescribed U_{om}^*. In addition, the output i_{vq}^* of the reactive power control loop should be limited to avoid the overload of the M3C. Analogously, the upper limit i_{vqmax} is given by:

$$i_{vqmax} = \sqrt{I_{vmmax}^2 - i_{vd}^2(t - T_{ctrl})} \tag{55}$$

where $i_{vd}(t - T_{ctrl})$ is the d-axis current on the output side measured in the previous control period.

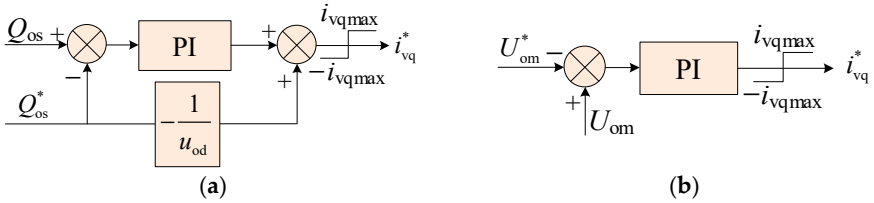

Figure 8. Reactive power control loop of outer loop controller on output side of M3C when (**a**) Q_{os}^* is given; (**b**) U_{om}^* is given.

6. Case Study

To verify the effectiveness of the proposed control strategy of the M3C, the electromagnetic transient simulation model of the M3C-based offshore wind power LFAC transmission system is established in PSCAD/EMTDC. The structure of the simulation model is shown in Figure 9 and the main circuit parameters are listed in Table 2. The detailed PSCAD/EMTDC models of the main circuit, the outer loop controller, and the inner loop controller of the M3C are shown in Figures A1–A3 in Appendix A.

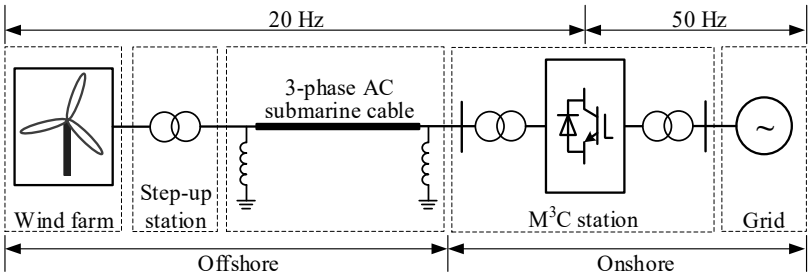

Figure 9. Schematic diagram of test system.

Table 2. Main circuit parameters of test system.

Items	Parameters	Values
M3C	Transformer rated capacity	330 MVA
	Transformer rated ratio	220 kV/97.5 kV
	Transformer leakage inductance	0.15 p.u.
	M3C rated power	300 MW
	Number of SMs per arm	111
	Rated SM capacitor voltage	1.66 kV
	SM capacitance	18000 μF
	Input-side rated frequency	20 Hz
	Output-side rated frequency	50 Hz
Submarine cable	Line resistance	26.8 mΩ/km
	Line inductance	0.395 mH/km
	Line capacitance	0.167 μF/km
	Length	100 km
	High-voltage reactor capacity	2 × 35 Mvar
Boosting transformer	Rated capacity	330 MVA
	Rated ratio	220 kV/35 kV
	Leakage inductance	0.105 p.u.
Aggregated wind turbine	Rated power	300 MW
	Rated AC voltage	35 kV

In the test system, the input side of the M3C is connected to the offshore AC system. Thus, the input side of the M3C is operating in the V/f mode to establish the offshore AC voltage so that the wind turbine can work in the grid-following mode. The output side of the M3C is connected to the onshore AC grid. The goal of maintaining the SM capacitor voltage is accomplished by the output side of the M3C. Moreover, the output side of the M3C controls the reactive power output to the onshore grid as 0.

6.1. Characteristics of Reduced Switching Frequency SM Voltage Balancing Method

To verify the reduced switching frequency SM voltage balancing method, the voltage of the SMs in arm Aa is compared under the optimized balancing method in Figure 10a and the conventional balancing method in Figure 10b. The instantaneous maximum value, the instantaneous average value, and the instantaneous minimum value of all SM capacitor voltages in arm Aa are denoted as u_{cAa_max}, u_{cAa_ave}, and u_{cAa_min}, respectively.

Figure 11a,b compare the gate signals of one SM in arm Aa under different balancing methods. The average switching frequency of a single SM can be calculated as:

$$f_{\text{sw\_ave}} = \frac{N_{\text{switch}}}{N_{\text{SM}}} \tag{56}$$

where N_{switch} denotes the sum of switching times per second of all SMs in one arm. Both switching-on and switching-off are counted in N_{switch}. N_{SM} is the number of SMs per arm.

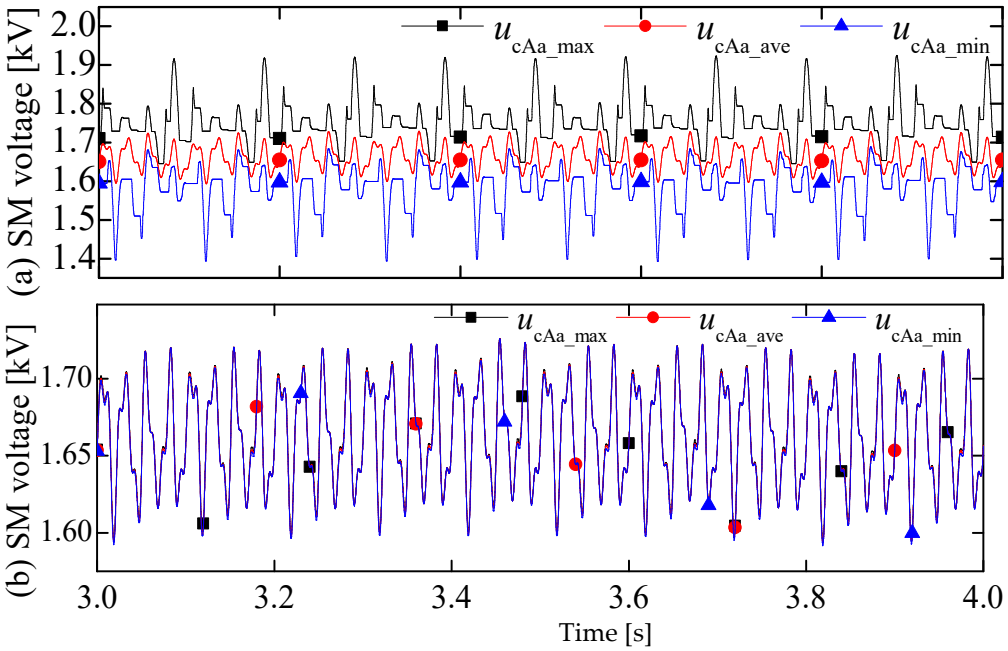

Figure 10. Instantaneous maximum, average, and minimum values of the SM capacitor voltage in arm Aa with different SM voltage balancing methods: (**a**) reduced switching frequency method; (**b**) conventional method.

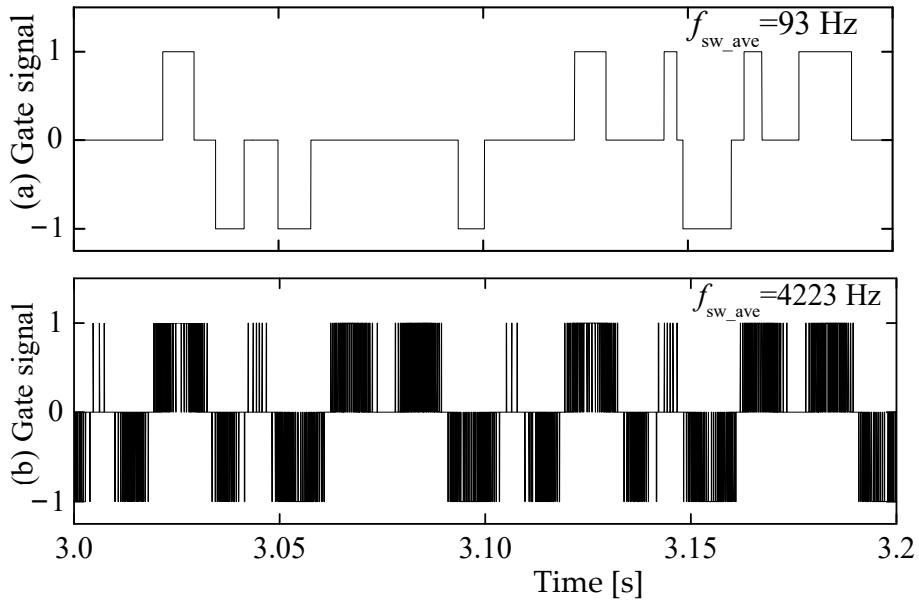

Figure 11. Gate signals of one SM in arm Aa with different SM voltage balancing methods: (**a**) reduced switching frequency method; (**b**) conventional method.

As shown in Figure 10a,b, the average SM voltages of both methods are stable. With the conventional method, the voltage of all SMs in one arm is highly consistent as in Figure 10b, but the average switching frequency f_{sw_ave} is very high (4223 Hz in Figure 11b). In comparison, the average switching frequency f_{sw_ave} with the proposed reduced switching frequency method is much lower (93 Hz in Figure 11a) and the SM voltages are also well balanced.

To reduce the switching frequency caused by the SM voltage balancing method, the SM voltage ripple will inevitably increase. It is true that the higher the switching frequency is, the more consistent the SM capacitor voltages are. However, the high switching frequency leads to high switching losses, which defects the economic benefit of the M3C project. In fact, excessive consistency of the SM voltages is not necessary, as long as the following two requirements of the SM capacitor voltage can be satisfied:

(1) The SM capacitor voltage should keep balanced, i.e., the average voltage of all SM capacitors does not deviate too much from the rated value.
(2) The maximum SM capacitor voltage should be within the upper limit voltage of the SM capacitor (usually 1.2 times the rated SM voltage).

It is observed from simulation results that these two requirements can be met with the proposed reduced switching frequency method, which means that the negative impact on the SM capacitor voltage ripple is acceptable.

In practical engineering, the aforementioned two requirements can be achieved by the selection of the SM capacitor and the rated SM voltage. Thus, higher fluctuation in the SM capacitor voltage within the allowable voltage range is not a severe problem.

The above comparisons are summarized in Table 3.

Table 3. Comparison of proposed method and conventional method.

Method Type	Algorithm Complexity	Maximum SM Voltage Ripple	Average Switching Frequency
SM voltage balancing method based on sorting all capacitors' voltages	Higher	1.04 p.u.	4223 Hz *
Reduced switching frequency SM voltage balancing method based on state sorting and incremental switching	Lower	1.17 p.u.	93 Hz *

* The average switching frequency of the reduced switching frequency method is much lower than the SM voltage balancing method based on sorting all capacitors' voltages.

6.2. Wind Speed Fluctuation

After the simulation model enters the steady-state operation, the active power generated by the wind farm drops from 1.0 p.u. to 0.8 p.u. at t = 4.0 s due to the wind speed fluctuation. The response characteristics of the M3C are shown in Figure 12.

It can be seen from Figure 12 that after the input power from the wind farm drops, the whole system can smoothly transition to a stable operating state, and the active power at the low-frequency side and the power frequency side of M3C will decrease steadily. The SM capacitor voltage can keep balanced, and the maximum SM capacitor voltage decreases a little when the transmitted active power drops. The output side of the M3C controls the output reactive power at its reference, which is set as 0. Thus, the reactive power output to the onshore grid Q_{os} is 0. Because the input side of the M3C operates in the V/f mode to establish the offshore AC voltage, the input side of the M3C functions as a power balancing bus for the low-frequency AC network, and the reactive power absorbed from the input side Q_{is} is about 11 Mvar in the steady state.

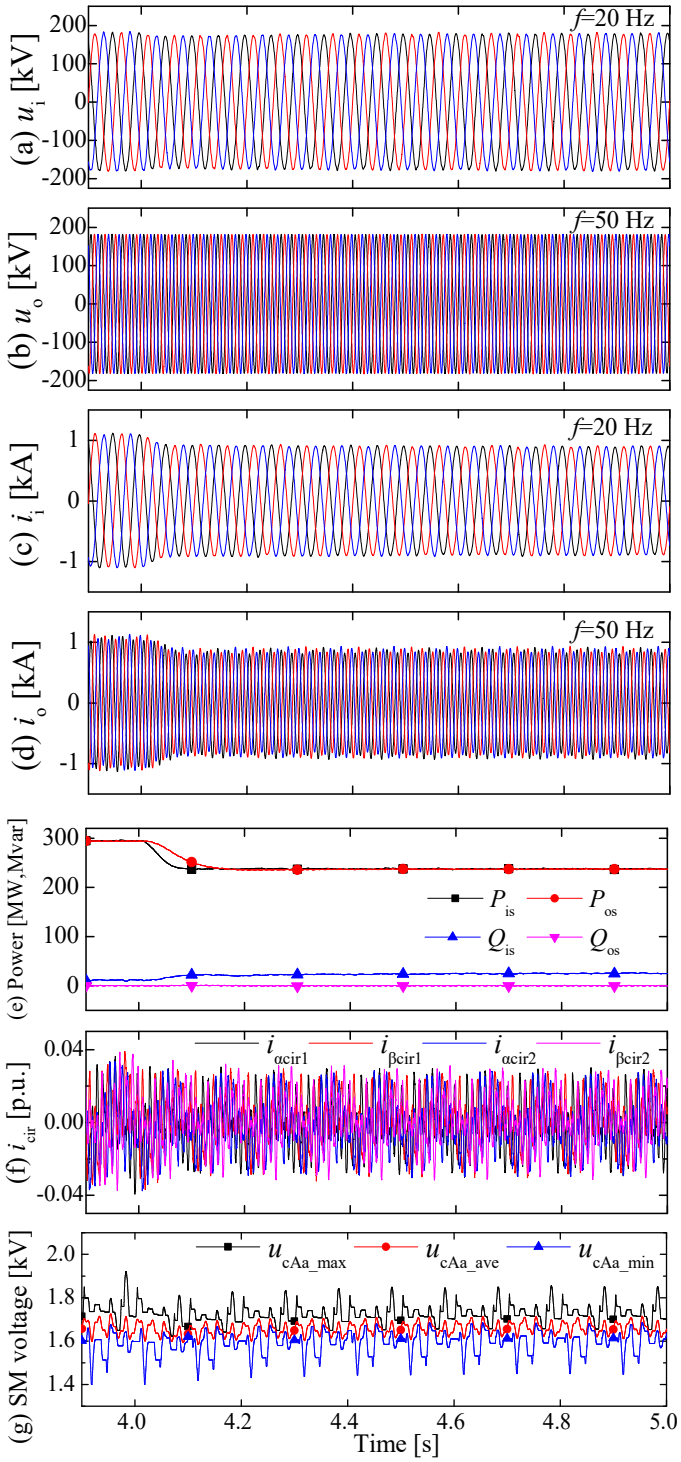

Figure 12. System responses to the wind speed step change: (**a**) voltage on input side; (**b**) voltage on output side; (**c**) current on input side; (**d**) current on output side; (**e**) input and output powers; (**f**) circulating current; and (**g**) instantaneous maximum, average, and minimum values of SM capacitor voltage in arm Aa.

6.3. Offshore Side Fault

The system entered the steady state before the fault. Assuming that a solid three-phase-to-ground fault at the M3C offshore side AC bus occurs at 4.0 s and lasts 100 ms, the system responses are plotted in Figure 13.

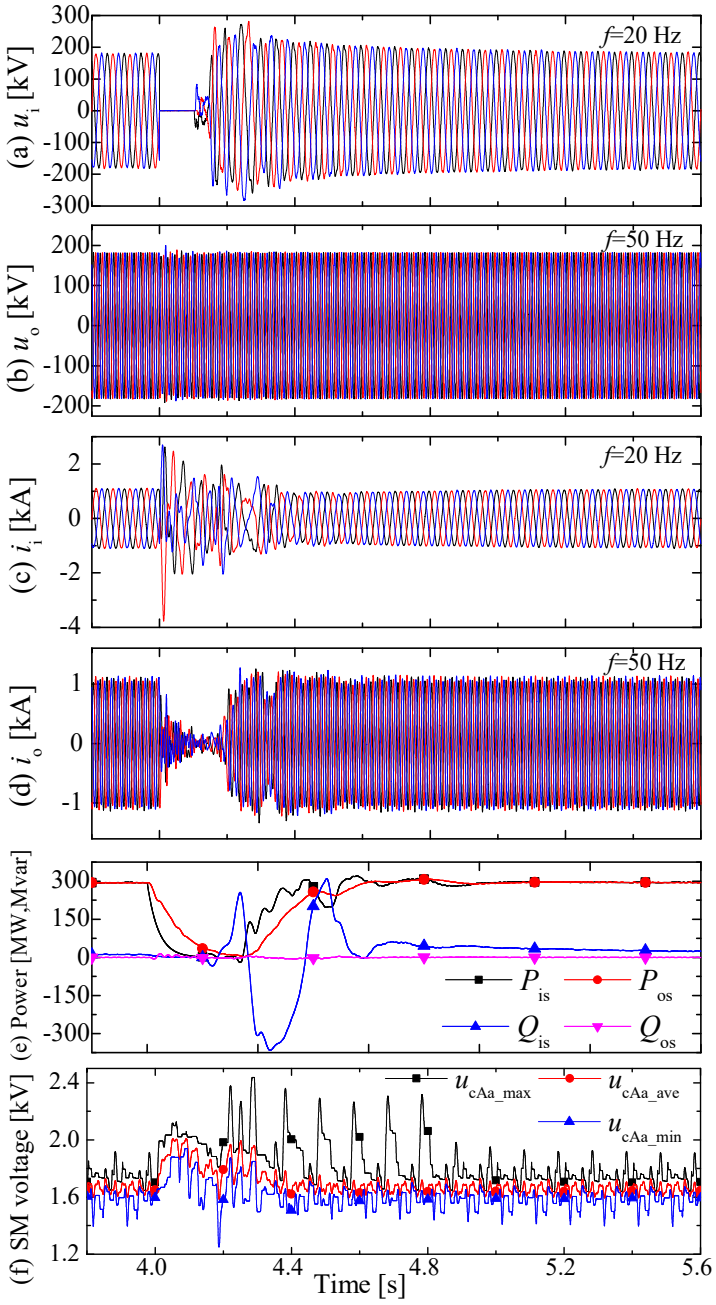

Figure 13. System responses to the offshore side fault: (**a**) voltage on input side; (**b**) voltage on output side; (**c**) current on input side; (**d**) current on output side; (**e**) input and output powers; and (**f**) instantaneous maximum, average, and minimum values of SM capacitor voltages in arm Aa.

When the fault occurs, the AC bus voltage on the M3C offshore side drops to 0 instantaneously, and the active power transmission from the offshore wind farm is blocked. Due to the SM capacitor voltage control, the active power transmitted to the onshore grid also drops to 0 during the fault to maintain the SM capacitor voltage. When the fault is cleared, the AC voltage recovers and the active power transmission resumes. The SM capacitor voltages do not deviate too much from the rated value during the fault and recover quickly when the fault is cleared.

7. Conclusions

A control strategy with a novel SM voltage balancing method of the M3C is proposed in the paper. The conclusions are summarized as follows:

(1) The ninth order mathematical model of the M3C is derived based on the extended MMC topology and the multiple αβ0 and dq transformations, making the M3C equivalent to two decoupled MMCs on the input side and the output side. The detailed equations of the current tracking controller are deduced in the dq reference frame and the circulating current suppressing controller is designed in the αβ0 reference frame. The outer loop controller is proposed for the scenario of offshore wind power LFAC integration based on M3C.

(2) A reduced switching frequency SM voltage balancing method of the M3C is proposed based on three characteristic variables and the NLC, which not only meet the requirements of SM capacitor voltage balance but also immensely reduce switching frequency. Simulation results in PSCAD/EMTDC verify the availability of the proposed control strategy.

Author Contributions: Conceptualization, Z.X.; methodology, Z.X.; software, Y.J.; validation, Z.Z. and Z.X.; formal analysis, Z.Z., Y.J. and Z.X.; investigation, Z.Z. and Y.J.; resources, Z.Z. and Z.X.; writing—original draft preparation, Y.J.; writing—review and editing, Z.Z.; visualization, Y.J. All authors have read and agreed to the published version of the manuscript.

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Appendix A

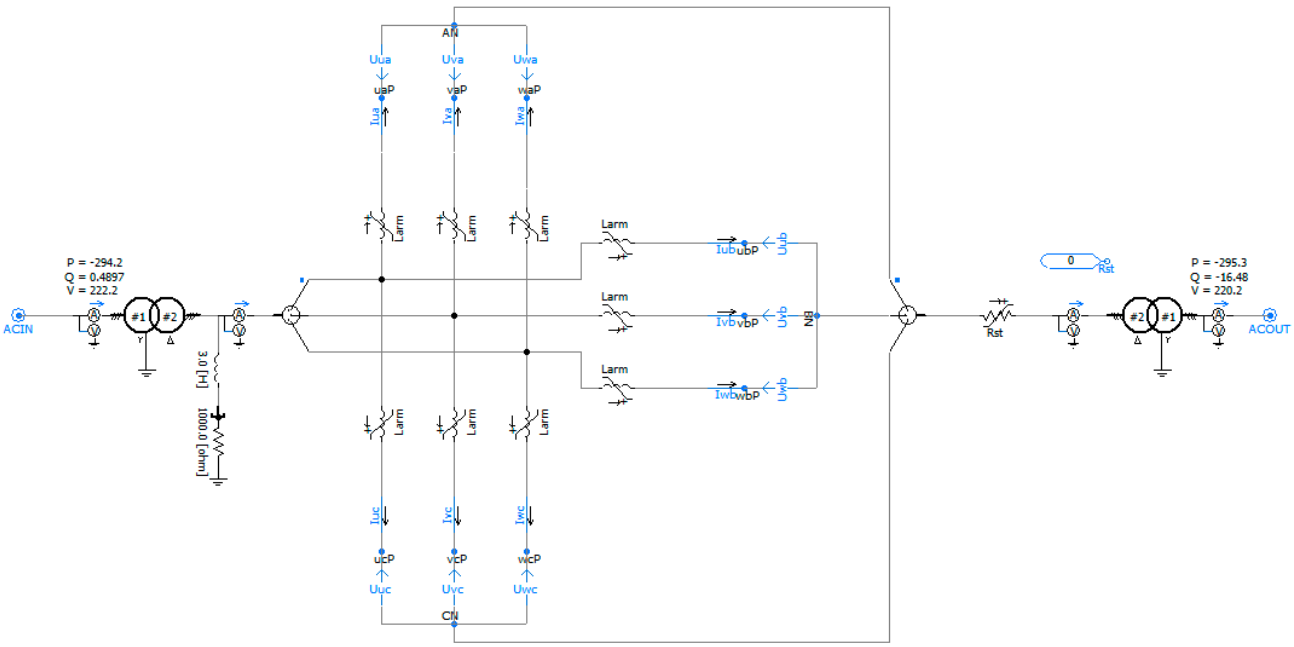

Figure A1. Simulation model of M3C main circuit.

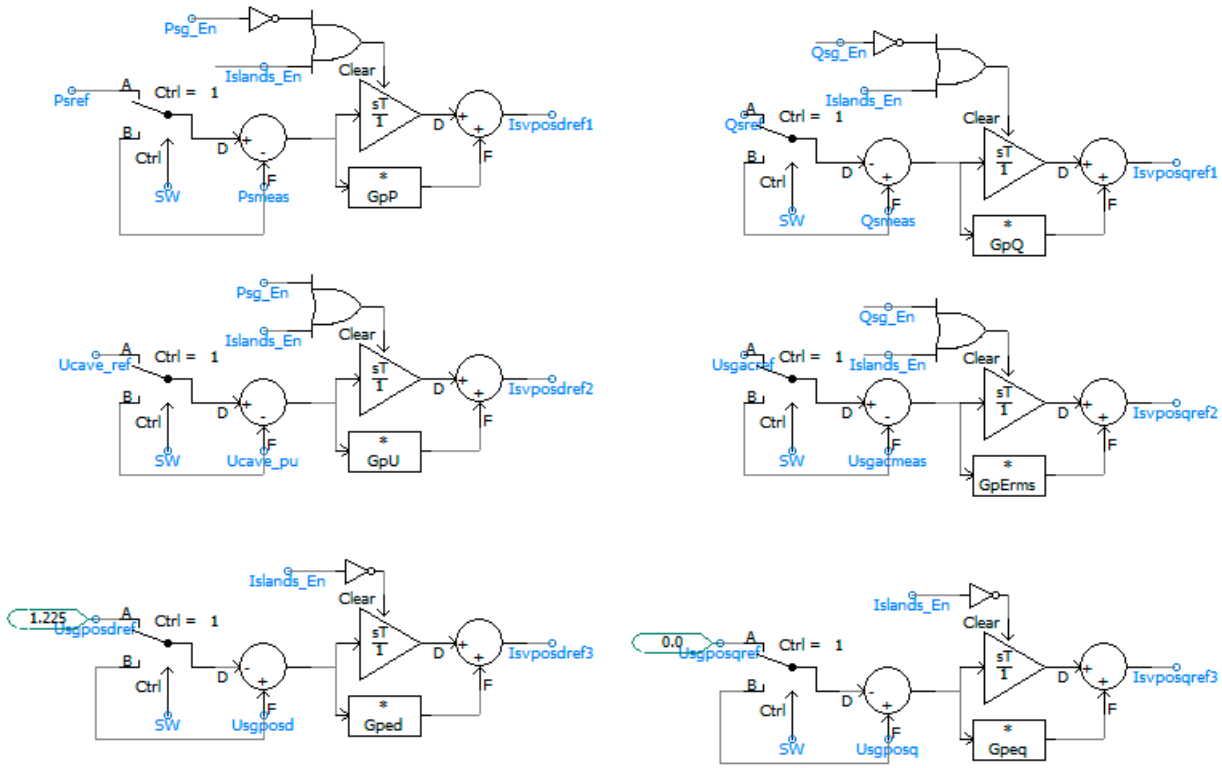

Figure A2. Simulation model of M3C outer loop controller.

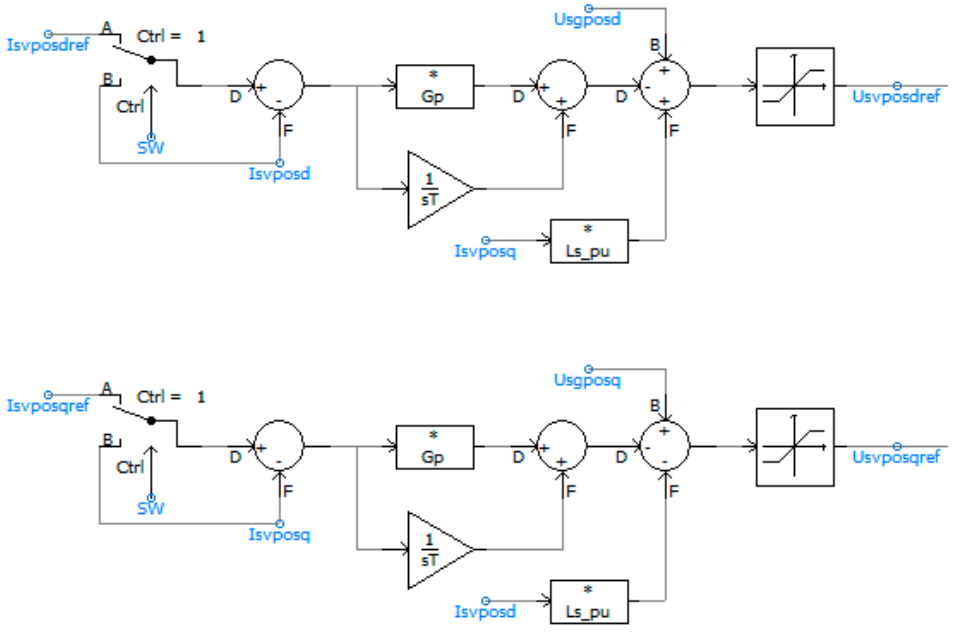

Figure A3. Simulation model of M3C inner loop controller.

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