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Reduction of Auto-Power Procedure Influence on the Photovoltaic Inverter On-Board Bus System Caused by Pulsed Loads

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Abstract: The article presents an on-board power system designed for ships, aviation, and space vehicles using energy from photovoltaic panels. The power structure includes both DC and high-frequency AC power buses. As a result of pulse loads, this system is exposed to disturbances that cause electronic systems to reboot. To reduce the effect of the appearance of secondary disturbances in the AC bus to which the photovoltaic converter is connected, a new control strategy has been proposed. This strategy improves the operation of the proportional resonant regulator that controls the AC bus current by making the reference values linearly dependent on the DC bus voltage. A prototype of such a system was designed in the laboratory. The FPGA control board was pulse-disturbed, leading to start the auto-power procedure, and additional disturbances were observed in the AC bus for the standard system. Reduction in the impact of these disturbances was achieved using the proposed control method by reaching a limitation of the bus current in dynamic states caused by the auto-power on process from 280% to less than 100% of the steady-state value. Experimental results verified the validity of the proposed method.

Keywords: on-board grid; power bus; disturbance; control; pv system; flying platform

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1. Introduction

Electricity management in power grids often requires the use of intelligent power systems [1] and optimal instantaneous prediction of voltage instability caused by transient power faults, taking into account the dynamic effect of generators [2]. The application of more electric technology in the area of mobile platforms, such as ships, aviation, and space technology, is currently a major technological trend that is being developed [3–5]. The number of loads traditionally powered by pneumatic systems is now increasingly electric [6]. This requires the use of DC and AC electrical grids in the on-board power system, which are used to supply basic infrastructure equipment. These power grids distribute the energy generated onboard the mobile platform. At first, only air-flow-powered generators of up to 1 kW were used, which were the main power generation components [4,6]. With the development of technology, facilities were constructed at higher and higher speeds, resulting in increased resistance caused by airflow-driven generators and additional problems [7]. These problems led to the replacement of flow generators by motor-driven generators. According to the authors of the publication [7], two motorized DC generators and one or two batteries as part of the backup power system began to be used as a standard. In such a situation, a power electronic converter was used to supply power to the AC equipment from the DC bus. AC generators operating in parallel were used in aviation as far back as the second half of the 20th century. Onboard systems containing 400 Hz generators, each with a capacity of about 40 kVA, are still used today, for example, in aircraft tankers [5].

On-board AC grids are most often higher frequency grids, which makes it possible for on-board instruments powered from them to achieve smaller dimensions relative to

instruments of the same power but with a lower nominal frequency. As a result, a reduction in the size of on-board instruments was made, thereby reducing the consumption of materials, such as iron and copper, necessary for their production.

On-board grids are isolated systems that must supply power to equipment in a reliable and resilient manner to disturbances generated outside, as well as inside the system. One of the main factors that disrupts the stable operation of on-board grids is the presence of electrical loads with impulsive power characteristics. These loads include electric drives in the start-up phase, radars, and all kinds of electromagnetic weapons. The presence in the on-board grid of disturbances with a very high peak factor and different frequencies of their occurrence significantly reduces the reliability of the power system and the quality of energy distributed in the on-board grid [8].

Changes in power consumption and changes in system structure always occur in each power system. One of the effects of these changes may be instability of the system voltage. When the voltage is unstable, the entire system can perform an unstable behavior [9]. Electrical loads are powered by the main power source, such as generators and batteries. These sources are connected to AC and DC power buses, respectively. Since the dynamics of the main power source is different from that of pulsed loads, the output voltage on the power buses can fall dramatically, increasing the possibility of equipment shutdown. To solve this problem, an energy storage unit, such as a supercapacitor or electrolytic capacitor with high dynamics, can be connected to DC power buses to build a ripple energy storage system. This requires controlling the voltage on the storage unit to remove the ripple component and allow the average load power to be reflected by the main power supply. Using such a decoupled power control, it is possible to make the output voltage on the DC power bus relatively stable during disturbances. The most commonly used power regulation decoupling techniques can be divided into passive decoupling [10,11] and active decoupling [12–14]. Although the first one is simple to implement, its applications in the aerospace field are not desirable due to the requirement for large capacitors. In contrast, active power decoupling control is more promising. When DC/DC converters are placed between the energy storage and the DC bus, the voltage fluctuation range of the decoupling capacitor can be increased. After all, the capacitor used for power decoupling can be very small, and the power on the DC bus can be greatly increased. There are two commonly used control strategies for active decoupling, namely, series decoupling [12,15] and parallel decoupling [16]. Although serial decoupling has higher conversion efficiency, it requires two DC/DC conversion stages, increasing cost and reducing reliability. Meanwhile, the parallel decoupling strategy is widely used in real applications because only a bidirectional DC/DC converter is needed, which makes the system economical and helps to increase the specific power of the system.

Many of the studies conducted focus on the control architecture, operating principle, and design details of the active capacitor. Since the main power sources in electric ships, electric vehicles, and aircrafts are usually generators mounted on the engine, active capacitors in these applications are controlled only to reduce ripple. Therefore, the size and weight of such devices are determined after the load profile is established. In some special applications, such as rockets and missiles, the main power supply only needs to provide load power for a few minutes. Thus, a small set of batteries is generally used as the main power source instead of a generator [17–19]. In addition to generators and storage power sources, renewable energy sources in the form of photovoltaic panels are increasingly being used in ships, aeronautics, and space vehicles. The use of this technology makes it possible not only to supply energy to the system, but also to reduce the power ripple and control reactive power in AC buses [20–23]. The operation on board of facilities under consideration of different energy sources with different characteristics requires the design of a power system containing power buses with different nominal values and voltage characteristics. The most common are buses of the main on-board grid AC with high frequency (400 Hz) and DC buses for connecting capacitors or batteries, as well as buses distributing power to electronic avionics equipment. The reliability of such a system depends mainly on the

control strategy implemented, but it is also very much dependent on the electronic system in which the required algorithms are implemented.

The problems of on-board grids under pulsed loads are well known and have been described many times in the literature [24,25]. The main challenge reported is when a load-specific energy storage element is charged over a specific interval of time and then rapidly discharged. The charging of the energy storage element constitutes an intermittent load that disrupts the operation of the power system [26]. The power requirements of such loads are very high, and charging times are in the order of seconds to minutes. When discharge occurs, it happens in a much shorter time, and is often essentially instantaneously compared to the charging period [27]. As a result of the occurrence of a large magnitude electric pulse on board a ship or flying platform, the impedance of the system causes a fault on the avionic power buses, which will cause the electronic system to stop operating [10]. The automatic return of power state of the electronic systems results in a return to stable operation after a period of time during which the control algorithms lose current information about the state of the system. This causes a cascade effect, since controlled photovoltaic panel converters disturb the AC bus current.

If the pulse load occurring in the on-board grid leads to the activation of auto power on procedures, it will thus transfer the disturbance to other components of the on-board system. In the case under consideration, this impact can be observed in the currents of the photovoltaic converter, so the main purpose of the work and the motivation for the research undertaken is to develop a new control strategy for the converter that reduces such an impact. The system proposed in this paper is based on the dependence of the reference values of the regulation process on the instantaneous value of the voltage of the power bus. As a result of the proposed strategy, the system brings the global variables to the output values, which always start from the initial values when the voltage returns. This mitigates the effect of disturbing the AC bus current by the photovoltaic inverter. However, this strategy can also be used to control motors powered by inverters connected to the DC bus. In this case, the proposed system is a fly-start system that allows a motor operating at an unknown speed to be connected to voltage sources. However, this aspect will not be considered in this paper.

The rest of this paper is organized as follows. Section 2 presents the system architecture under consideration. The characteristics of AC bus current regulation are also briefly presented, and locations particularly susceptible to the occurrence of disturbances to the control board power supply are pointed out. The proposed method is also discussed in detail, and formulas are presented that make the reference values of the regulation processes dependent on the DC supply voltage. Section 3 describes the test stand and presents selected experimental results that illustrate the operation of the proposed system. Section 4 presents the final conclusions.

2. System Description

The new method proposed in the paper to reduce the impact of the voltage drop in the DC bus below the value that allows the correct operation of electronic devices was used and studied in a photovoltaic converter system. This converter operates in an on-board system, which is characterized by an extended voltage frequency of 400 Hz. The power electronic system for converting energy from photovoltaic panels is controlled by a reconfigurable FPGA-type logic system. The essence of the implementation of the control algorithm requires that the supply voltage of the FPGA be maintained above a threshold value. This is a consequence of the fact that the FPGA of the Cyclone II family used do not have an internal memory that holds information about the configuration of logic resources used in the control process. Consequently, a drop in the supply voltage below a threshold value results in the loss of the internal configuration of logical resources and the reboot of the chip. During restart, the internal configuration that performs control tasks must be read from external serial memory and used to reconfigure the resources [28]. This is a relatively long process that results in resetting all the information about the variables used in the

control process. If a restart of the control system occurs during energy conversion by the converters, resetting the measurement values and information about the current load status will result in a disturbance of the energy flowing from the grid converter into the on-board grid and may cause an excessive increase in its instantaneous value.

The paper has considered a system with the block diagram shown in Figure 1.

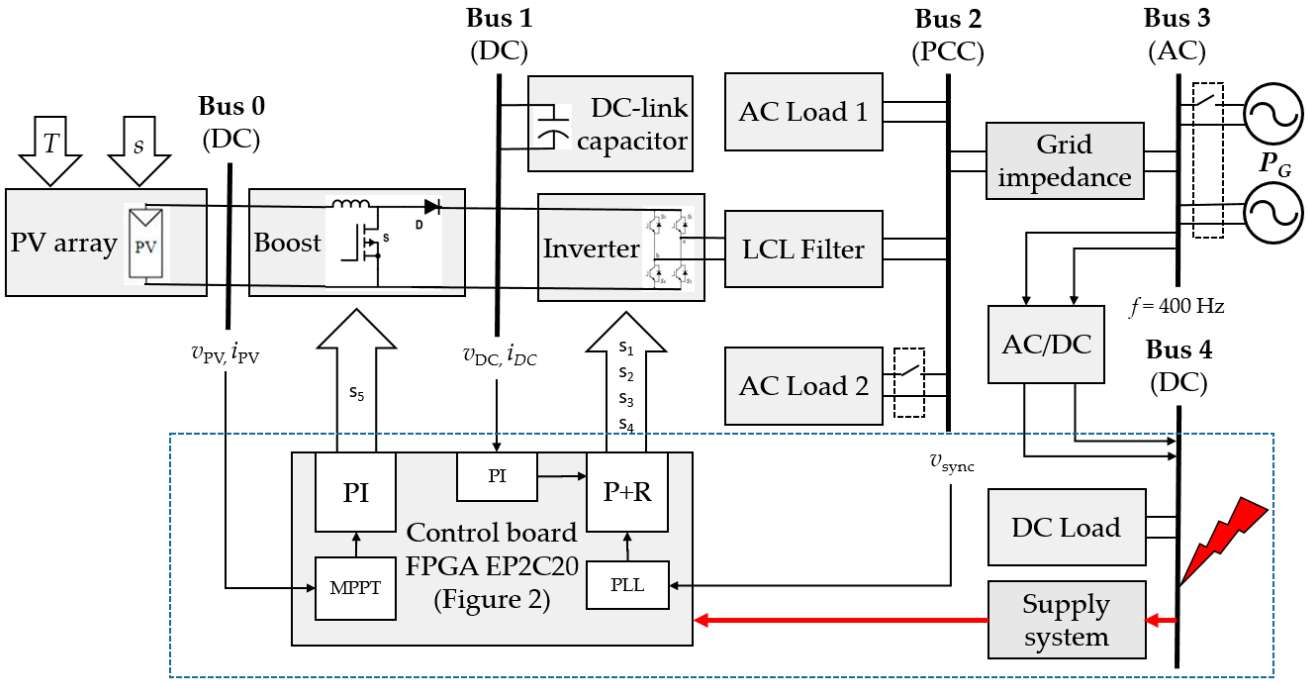

Figure 1. Block diagram of the system under study that includes the grid converter, photovoltaic panels, on-board grid, additional loads, control device, and power system for electronic systems.

Figure 1 shows an on-board power system characterized by the ability to obtain energy from photovoltaic panels (PV). The various components of the system are connected using three DC buses and two AC buses. Bus 0 is the connection of external photovoltaic panels to the on-board system. Depending on atmospheric conditions related to outdoor temperature (T) and sunlight (s), energy is produced. Measurement of voltage (u_{PV}) and current (i_{PV}) on this bus is used in the process of finding the maximum power point (MPP) of the photovoltaic system. The maximum power point tracker (MPPT) implemented in the control system uses these signals to maximize the value of current (i_{DC}) feed bus 1 (DC). Due to the higher nominal value of the voltage (u_{DC}) of bus 1, a DC-DC boost converter is used for voltage adjustment. The energy harvested from PV results in voltage fluctuations in the capacitor connected to bus 1, and a PI-type control system stabilizes it, setting the DC link voltage at a preset level by varying the amplitude of the current fed by the grid inverter into the on-board grid at 400 Hz. The system for controlling the current supplied to bus 2, which is the point of common connection of AC loads (PCC), operating on the principles of proportional resonant regulation with limited gain (P+R) [23]. Bus 2 voltage (v_{sync}) is used in the control system to keep the active and reactive components of the current and thus compensate for reactive power of the system. For this purpose, the phase-locked loop (PLL) generates a virtual orthogonal coordinate system, allowing independent proportional resonant control of the grid current components. As a result of the inverter's coupling of the DC bus with the single-phase AC bus, 800 Hz power ripples are generated. To ensure that they do not negatively affect the currents onboard the grid and the operation of photovoltaic panels, the control system was tuned so that these ripples appear as voltage ripples on the DC link capacitor.

The studies reported in this publication primarily address the impact of disturbances generated at bus 4. This is a DC bus to which the voltage is maintained at a preset level by

a rectifier connected to the generator (bus 3). This is a low voltage bus to which DC loads and the electronic control board power system are connected. The disturbances marked with a red lightning bolt in Figure 1 can arise mainly as a result of pulsed loads on the DC bus or disturbances on the rectifier and generator units. Based on observations and previous studies, it seems that there may be situations during system operation in which the supply voltage drops below the threshold value necessary to sustain the electronics operation. If a FPGA is used in the control system, this will cause the device to reboot, resulting in a disturbance in the on-board AC grid. The system section considered in the paper is marked in Figure 1 with a blue dashed line.

The control board was designed based on an Altera reconfigurable chip of type EPC20F484 that executed the following tasks simultaneously:

- measurement of currents and voltages of buses 0 and 1;
- synchronization with the fundamental component of the bus 2 voltage and extraction of orthogonal components of this voltage (method described in the paper [29]);
- execution of the algorithm for maximum photovoltaic power (the method proposed in [30]);
- PI-type control of the DC-link charging current, maximizing the value of energy extracted from PV;
- PI-type control of bus 1 voltage;
- proportional-resonant control with limited gain of DC-link current.

Figure 2 shows the control structure implemented in the FPGA. The control board containing the reconfigurable chip has an EPCS4-type serial EEPROM that stores configuration data for the Cyclone II FPGA. These configuration data are automatically loaded from the EEPROM into the FPGA whenever power is applied to the control board. Saving or changing the non-volatile data stored in the serial EEPROM is always performed offline by downloading the configuration bit stream using the JTAG interface. The EEPROM provides non-volatile storage of the bit stream, retaining the configuration even when the control board is powered off. When the board is powered on, the configuration data on the EPCS4 device automatically load into the Cyclone II FPGA. This auto-power-on procedure sequence results in disturbances in the on-board grid, causing unpredictable disconnections of energy sources and transients due to their reconnection to the common grid. In Figure 2, in the location labeled "Error", information about the current state of bus 4 is available. The proposed system uses it to modify the current state of the control system by applying formula (7) to prevent it from unexpected shutdown.

The basic tasks of the onboard grid power converter control system were implemented in the FPGA and are shown in Figure 2. A proportional–integral (PI)-type control system of the DC-DC boost converter was used, which operates with the MPPT system with the structure described in [30]. The same structure as that of the proportional-integral-type control system was used to control the DC link voltage. Based on the reference value of the grid current, which is a variable that depends on the value of the photovoltaic current and the current value of the voltage in bus 1, the current deviation (e_G) is calculated. The value of the current deviation e_G is calculated to determine the reference current waveform of the grid by using a proportional-resonant controller transmittance:

$$Y(s) = (K_P + G_R)E_G(s), \tag{1}$$

where K_P is the transmittance of the proportional component with a gain of k_P and E_G is the Laplace transform of the signal e_G. G_R is the transmittance of the resonant component:

$$G_R(s) = K_i \frac{2\xi\omega s}{s^2 + 2\xi\omega s + \omega^2}, \tag{2}$$

where

$$\omega = \frac{1}{\sqrt{T_1 T_2}} \quad \xi\omega = \frac{k}{2T_1} \quad K_i = \frac{1}{k}. \tag{3}$$

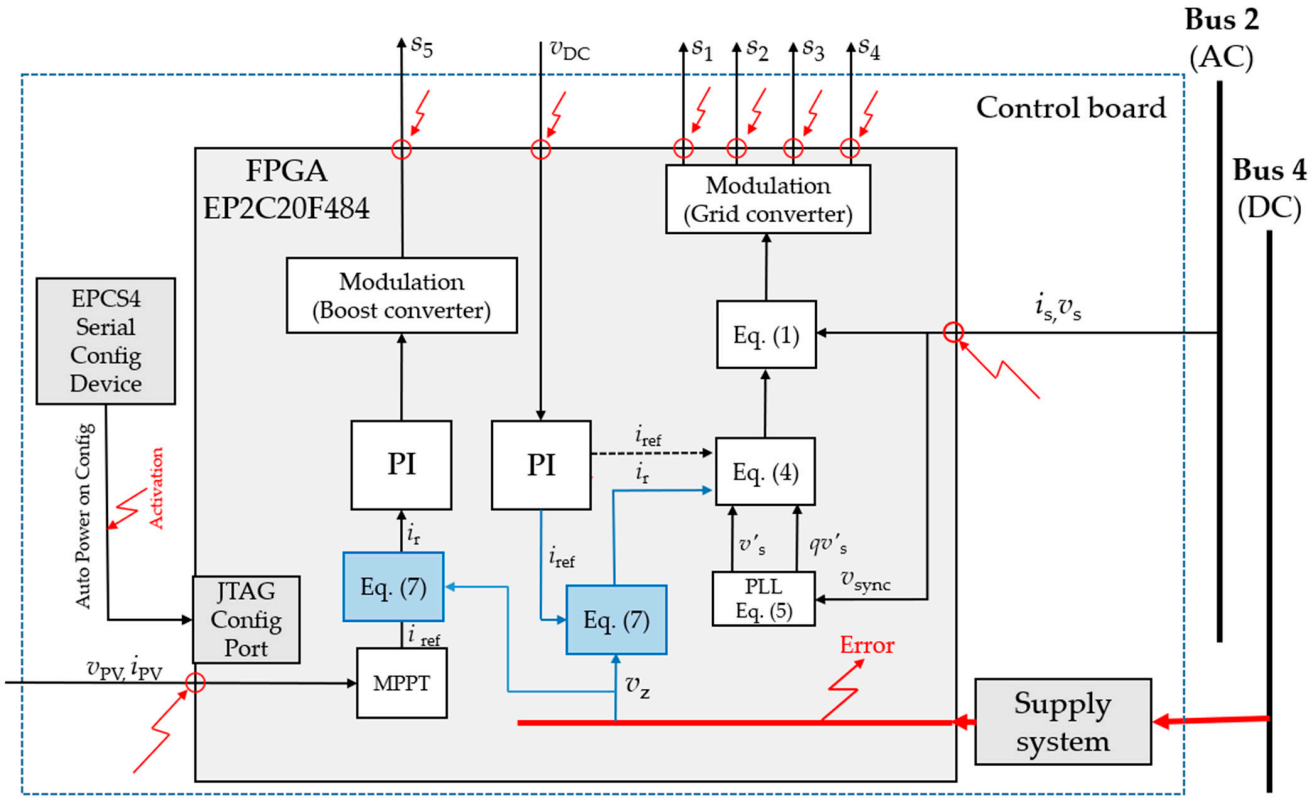

Figure 2. Topology of the control system components located on the control board.

The e_G signal is calculated from the measured current on bus 2 ($k_s i_s$) and the value of the reference current i_{ref} by applying the equation:

$$e_G = i_{ref}\, qv'_s + i_{qref}\, v'_s - k_s i_s, \tag{4}$$

where $qv'_s = \cos 800\pi t$ and $v'_s = \sin 800\pi t$ represent the orthogonal voltage components on bus 2 and i_{qref} is the reference reactive component of the current in the on-board grid. Due to the assumption of reactive power compensation on bus 2, the value of this component is equal to zero.

Implementation of the control procedure in the FPGA requires discretization of the measured single-phase voltage in bus 2 and the transformation of measurement results to a virtual orthogonal system. The discretization process was carried out on the basis of the commonly used trapezoidal method. As a result of the transformations, the discrete equation of the fundamental component was obtained:

$$v'_s[n] = b_0\,(v_s[n] - v_s[n-2]) + a_1\, v'_s[n-1] + a_2\, v'_s[n-2]. \tag{5}$$

The coefficients in equation (5) were calculated using formulas:

$$b_0 = \frac{2k\omega T_s}{2k\omega T_s + (\omega T_s)^2 + 4},\quad a_1 = \frac{8 - 2(\omega T_s)^2}{2k\omega T_s + (\omega T_s)^2 + 4} \text{ and } a_2 = \frac{2k\omega T_s - (\omega T_s)^2 - 4}{2k\omega T_s + (\omega T_s)^2 + 4} \tag{6}$$

where Ts is used as the sampling period, and k is the gain of the general structure of a single-phase PLL based on the second order generalized integrator.

The on-board control system shown in Figure 1 was designed and described in detail in [24] and has been experimentally verified. In order to increase the reliability of a device exposed to pulse loads, this structure had to be modified. The modification proposed in the paper mainly concerns the development of a strategy for managing power flow when the bus voltage can cause the device to restart automatically. In Figure 2, the source considered

for triggering the controller restart procedure is marked in red, and the signals that are disturbed are indicated with red arrows. When the automatic configuration procedure is activated, the information about the current and voltage values measured on buses 0, 1, and 2 is lost. At the same time, the reference value of the onboard converter current and the signals triggering the inverter transistors are reset to zero. This causes a disturbance in the photovoltaic energy conversion loop, the consequence of which is the formation of a restart of the maximum power tracking system and a step change in the force of the current control system. Such a condition causes the energy stored in the capacitors connected to bus 1 to generate a current disturbance in the onboard grid.

The new control system proposed in the paper eliminates the described disturbances in the current flow by modifying the value of the reference current. This modification was made by making the reference value of the current a linear function of the supply voltage. The proposed idea is shown in Figure 3 and marked in blue in Figure 2 in places of its implementation.

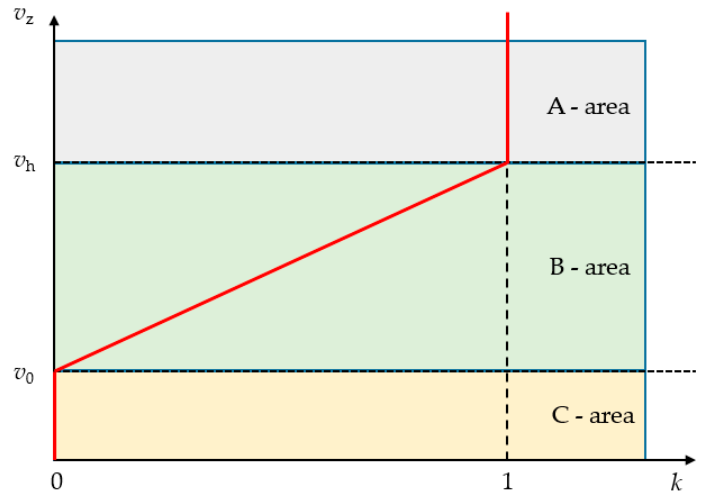

Figure 3. Relationship between the supply voltage v_z and the scale factor k.

Depending on the value v_z of the DC voltage on bus 4, three areas were separated:

- the A area in which there is no modification of the reference current;
- the B area in which the reference value is a linear function of the supply voltage;
- the C area of resetting the reference value.

If bus 4 voltage is in zone A, then its value is sufficiently high for the power system to satisfy the energy demand of the control board. This is the state of normal operation, which means that the control system is set to execute the assumed control tasks resulting from the current reference values. In the case when the proposed system detects the danger of activating the auto power on procedure, it will take priority action, resulting in a reduction of the controllers' reference values, thereby reducing the energy fed into the system. It corresponds to the voltage of bus 4 located in zone B. A reduction in the voltage value in zone B triggers a reduction in the photovoltaic energy fed into the on-board grid. Zone C denotes the state in which the voltage of the power bus is too low for the control board to operate properly. Then, regardless of the state of the control process, the reference values are reset to zero. This means that, for supply voltages falling within zone C, there is no possibility of feeding photovoltaic energy into the on-board system.

As a consequence of the split of the voltage range in the power bus, there are two characteristic voltage values that separate these areas of v_0 and v_h. The threshold value of the voltage v_0 is the minimum value of the supply voltage at which the FPGA chip operates correctly. A voltage drop below v_0 can already cause the loss of configuration data and trigger the device's auto-power procedure. The value of the supply voltage v_h is the safe operating voltage of the FPGA, which is called the safe supply margin. In Figure 3, the

reference variables of the scaling factor of the control process (k) are marked in red. This factor scales the reference currents, according to Equation (7), causing different responses depending on the area in which the current value of the supply voltage is located. For supply voltages greater than the safe supply margin, this factor takes a unit value, thus not limiting control processes. If the supply voltage is below the threshold value, the scale factor resets to zero, thus stopping the regulation process. When the supply voltage is in the B area, the reference values in the control system depend linearly on the supply voltage. This relationship is described by Equation (8). As a consequence of the decrease in supply voltage, the reference values are reduced, causing the power generation process to slow down.

$$i_r = k(v_z) i_{ref}, \tag{7}$$

$$k(v_z) = \begin{cases} 0 & \text{for } v_z \leq v_0 \\ \frac{v_z}{v_h - v_0} - \frac{v_0}{v_h - v_0} & \text{for } v_0 < v_z < v_h, \\ 1 & \text{for } v_z \geq v_h \end{cases} \tag{8}$$

If the monitored voltage on the DC power bus is greater than the threshold value by the safety margin value, then the grid current reference signal is passed directly from the DC link voltage regulator to the proportional resonant regulator. In a situation where the supply voltage starts to fall, the reference values of the grid current and the boost converter will decrease linearly after the v_h value is exceeded. The effect of such control will be to simultaneously limit the photovoltaic current and the value of the current that feeds into the onboard grid. In a situation where the voltage in the grid drops to or below the threshold voltage level, despite the availability of energy from photovoltaic sources, it will not be supplied to the system. As a result, the reference current will reset to zero, and the auto-power of the FPGA chip will result in a smooth linear startup of the PV system.

3. Results

The tests of the proposed strategy that resulted in the reduction of current disturbances observed in the on-board grid were carried out in the designed system with the parameters shown in Table 1. The components of the system under study were power electronic converters operating onboard the grid with a frequency of 400 Hz and a control device made on the basis of a reconfigurable FPGA-type logic circuit.

Table 1. Electrical parameters of the on-board system.

Power System	
Rated bus 0 voltage	600 V
Maximum bus 0 current	6 A
Rated power	1 kW
Rated bus 1 voltage	700 V
Maximum bus 1 current	5 A
Switching frequency	20 kHz
Input over current protection	10 A
Maximum bus 2 current	+/− 5 A
Bus 2 voltage	325 V, 400 Hz (min 202 V, 400 Hz)

An FPGA chip was installed on the control board along with the configuration memory, which had the following processes implemented:

- MPTT algorithm;
- boost converter controller and modulator;
- bus 1 voltage controller;
- second-order generalized integrator;
- proportional-integral regulator and grid current modulator;

- proposed system for scaling reference quantities as a function of supply voltage.

Experimental studies were performed, assuming static environmental conditions that affect the volume of energy fed into the onboard system. The characteristics of the photovoltaic simulator were configured to correspond to constant solar irradiation and constant external temperature, and the parameters of the controllers implemented in the FPGA were tuned heuristically. The values of the applied environmental parameters, the settings of the grid current P+R controller, and the PI boost converter controller are summarized in Table 2.

Table 2. Summary of the environmental and control parameters used in the test.

Environmental Parameters	
External temperature (T)	298 K
Solar irradiance (s)	1000 W/m^2
Bus 2 P+R controller	
Gain of the proportional part (K_P)	1
Gain of the integrating part (K_I)	100
Pulsation (ω)	800π
Damping factor (ζ)	0.05
Bus 1 controller	
Gain (k_1)	1
Constant of integration	0.01

In addition to the converters and control board, the hardware stand included a DC power supply of the ITECH IT6526C type, which was used as a photovoltaic panel simulator, a 4-module ITECH 7900 series regenerative grid simulator, and programmable loads. Measurements were made using a Yokogawa DLM2000 mixed signal oscilloscope and the Signal Tap II logic analyzer operating with the FPGA via the JTAG interface. A photo of the test stand is shown in Figure 4. The verification of the proposed system was based on the observation of currents that feed into the PCC of the grid converter for different variants of voltage changes in the DC power bus. The investigated cases were limited to linear voltage changes in bus 4, which varied with the depth of the voltage sag and the dynamics of the sag. To confirm the effectiveness of the proposed system, the results obtained were compared with those observed during the operation of the standard system, without implementation of the proposed control strategy, for the same supply voltage disturbances.

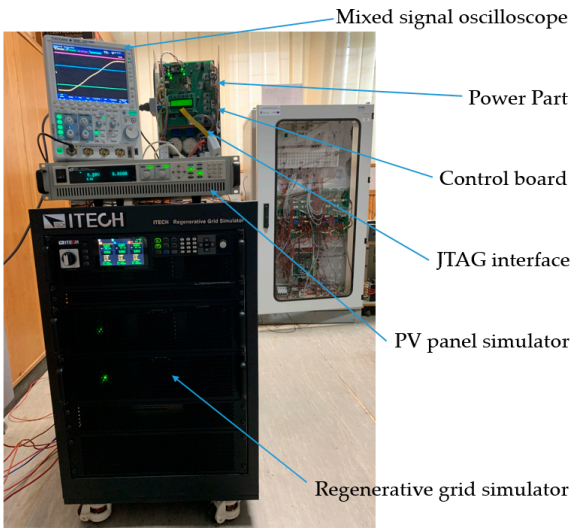

Figure 4. Photo of the test stand and the equipment used for the tests.

Verification of the proposed control strategy in the first phase of testing was carried out for a power bus voltage sag that caused the control board to shut down and trigger the power auto-restart procedure. The supply voltage was falling linearly to zero with a dynamic about 80 voltage per second, then, after about 60 ms, it began to rise linearly with a greater dynamic about 120 voltages per s. The voltage profile is shown in Figure 5a.

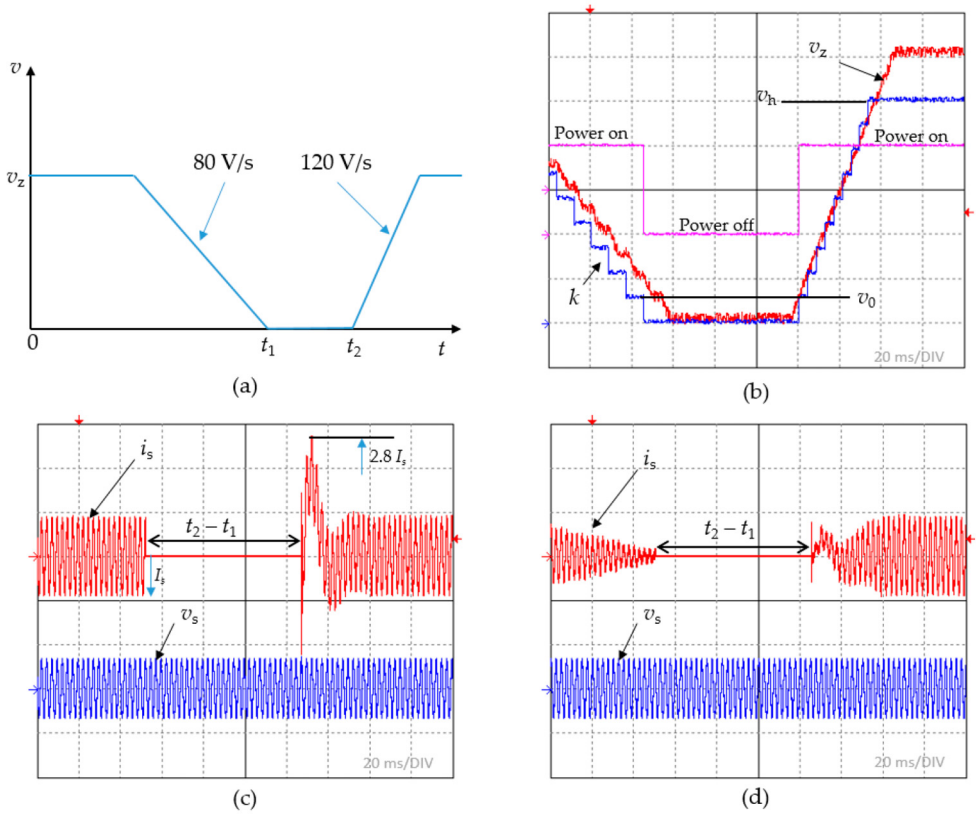

Figure 5. Dynamic response of the system to a voltage change on power bus 4: (**a**) assumed voltage profile on bus 4; (**b**) waveforms of the recorded voltage of bus 4 v_z, correction factor k, and supply voltage identifier (pink color); waveforms of current i_s and voltage vs. of bus 2 recorded in the classical system (**c**) and in the proposed system (**d**).

Figure 5b shows the voltage recorded on power bus 4 (v_z), which corresponds to the voltage profile assumed in the case under study. Additionally, shown is the correction factor for the reference values (k) in the system tested. The stepped form of this coefficient is due to the digital implementation of the controller and corresponds to the clocking of the correction calculation process with a frequency of 150 Hz. The pink color indicates the waveform of the supply voltage identifier, which displays the states when the control board is off or on. Figure 5b also displays the threshold voltage (v_0) and safe operating voltage (v_h) levels of the FPGA device. Analyzing Figure 5b, it is easy to see that supply voltages below the threshold voltage correspond to the state when the power is off, while voltages higher than the safe operating voltage cause saturation of the correction factor waveform (k). For a constant factor k, corresponding to voltages higher than v_h, the system is not corrected and performs as a conventional system. This proves that the system has achieved the assumed profile of response to voltage changes at bus 4. Figure 5c shows the current and voltage waveforms on bus 2, which were recorded for the assumed voltage profile on bus 4. This case is for a system in which the proposed method of correcting the regulators' reference sizes was not implemented. According to the preliminary assumptions, stable operation of the system was considered, excluding bus 4, so the voltage in the on-board grid vs. does not change. This is a stable condition in which photovoltaic energy is fed into the system in a stable manner. When the voltage supplying the electronic control board is disturbed, the

system is disturbed, as a consequence of which all registers of measurement systems are cleared. Returning the supply voltage to the expected level takes place when the reactance elements have stored energy. This situation causes a disturbance of the current, as observed in bus 2. Figure 5d shows an analogous situation to that in Figure 5c, with the proposed method implemented in the FPGA structure. The resulting perturbation of the voltage supplying the control board does not cause such a significant perturbation of the bus 2 current. By monitoring the voltage in bus 4 and conditioning the reference values in it, the current of bus 2 is limited. When the FPGA chip is turned off, the reference values are reset to zero. This allows the control board to restart and force a linear startup of the on-board system.

The next part of the experimental verification involved a case in which the voltage on bus 4 suddenly fell off and it began to rise after a certain time with a dynamic of 120 volts per s. The voltage profile for this case is shown in Figure 6a.

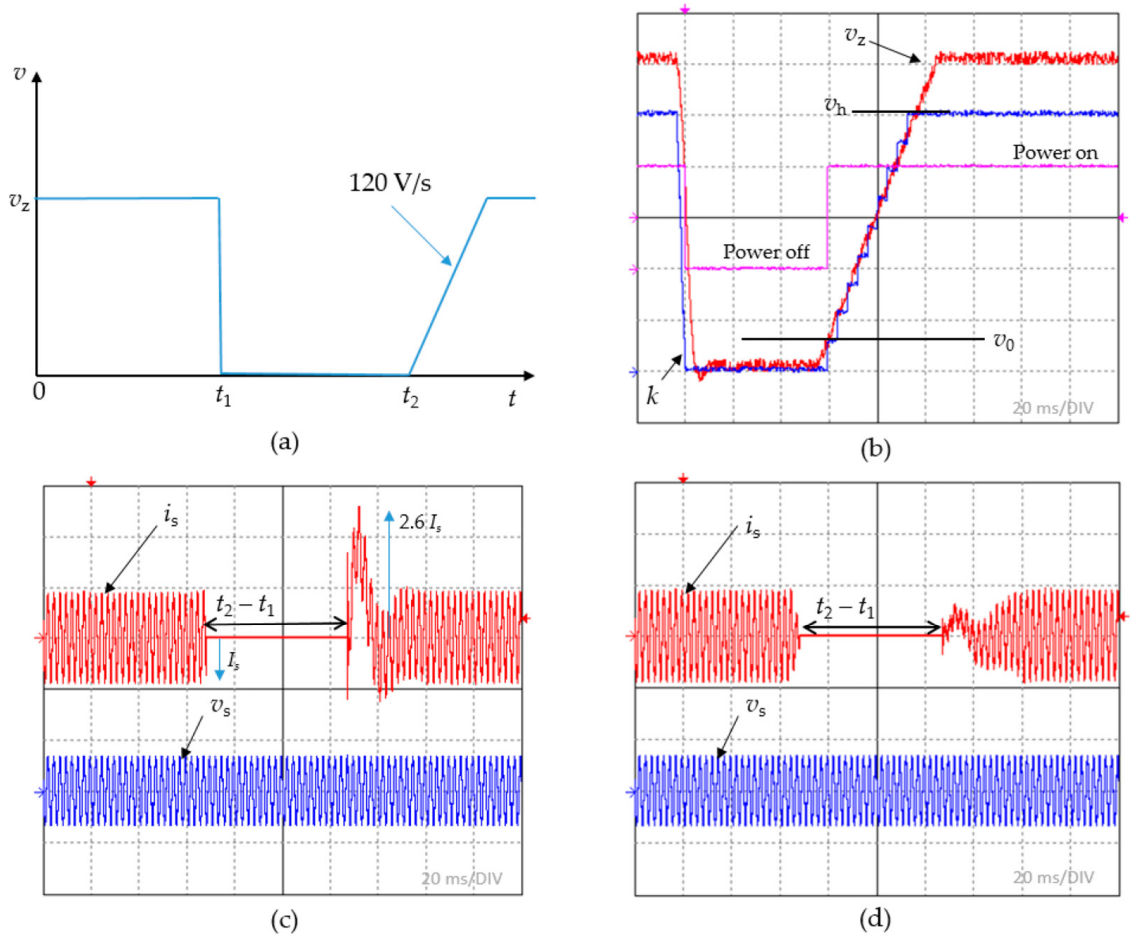

Figure 6. Dynamic response of the system to a voltage change on power bus 4: (**a**) assumed voltage profile on bus 4; (**b**) waveforms of the recorded voltage of bus 4 v_z, correction factor k, and supply voltage identifier (pink color); waveforms of current i_s and voltage vs. of bus 2 recorded in the classical system (**c**) and in the proposed system (**d**).

Figure 6b shows the waveform of the disturbed supply voltage and the correction factor k, which, according to the assumption, is reset at the same time as the voltage on bus 4. The supply voltage return process has the same dynamic as in the case presented in Figure 5. Therefore, no differences are visible in this case. Observation in Figure 6c of the AC bus current and voltage in the default case confirms the same nature of the dynamic response. This is related to the transient processes resulting from running the system in a non-zero energy state. Figure 6d shows the current and voltage of bus 2 for the proposed

system. As can be easily observed, the current is quickly reset to zero as a result of the response to the disturbance shown in Figure 6a. This is due to the rapid voltage drop and the shutdown of the control board. An increase in voltage with a dynamic rate of 120 volts per s causes the system to start up softly and return to stable operation.

The next variant of the tests performed involved the occurrence of a zero-tolerance error on bus 4 that feeds the control board circuit. The short-time pulse that shuts down the electronic system had the profile shown in Figure 7a and was recorded on bus 4 as the voltage v_z shown in Figure 7b. Due to the voltage step change, both the scaling factor and the control board power supply indicator repeated the shape of the disturbance. As a result of the instant return of the supply voltage, the proposed system returned to its original reference values within a single operation tact. The current injected into bus 2 showed essentially no instantaneous overregulation, as shown in Figure 7d. For the standard system, the current waveform is shown in Figure 7c. However, the observed disturbances are negligibly small without and for the proposed system. Observing the system's responses to a rapid transient voltage drop, one should conclude that the proposed system is not able to eliminate the effects of disturbance in the current in such cases. The effects of the disturbance are not repeatable, which is associated with the unpredictable energy state of the system.

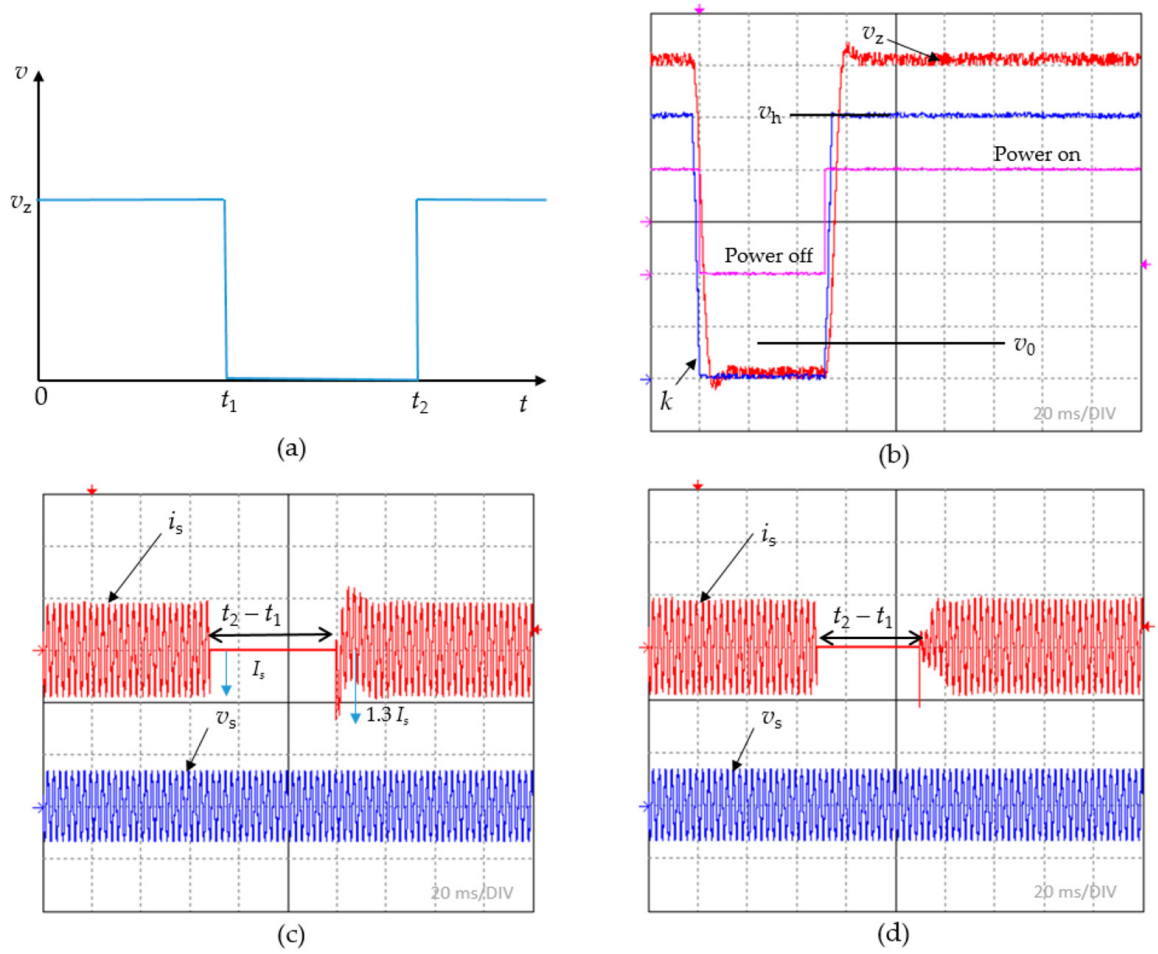

Figure 7. Dynamic response of the system to a voltage change on power bus 4: (**a**) assumed voltage profile on bus 4; (**b**) waveforms of the recorded voltage of bus 4 v_z, correction factor k, and supply voltage identifier (pink color); waveforms of current i_s and voltage vs. of bus 2 recorded in the standard system (**c**) and in the proposed system (**d**).

The case of a very short pulse disturbing bus 4 was also verified, which was characterized by a rising and falling edge dynamic of 120 volts per s. The profile of such a pulse is shown in Figure 8a. In the generated supply voltage v_z, shown in Figure 8b, it was possible to obtain a similar profile by decreasing the supply voltage with an assumed slope and, when reaching zero, increasing it with the same slope. This change in voltage on bus 4 resulted in a short-time shutdown of the power supply to the control board for voltages lower than the threshold voltage v_0. As can be seen in Figure 8b, the correction factor k followed the voltage changes, correcting the reference values of the controllers when the supply voltage was lower than the safe operating voltage to shut off the converter when the FPGA was in a restart mode. This is confirmed by the current waveform shown in Figure 8d. In the case where the system did not have the proposed system implemented, the bus 2 current showed an overshoot. However, this overshoot was small, comparable to that observed for the short pulse shown in Figure 7.

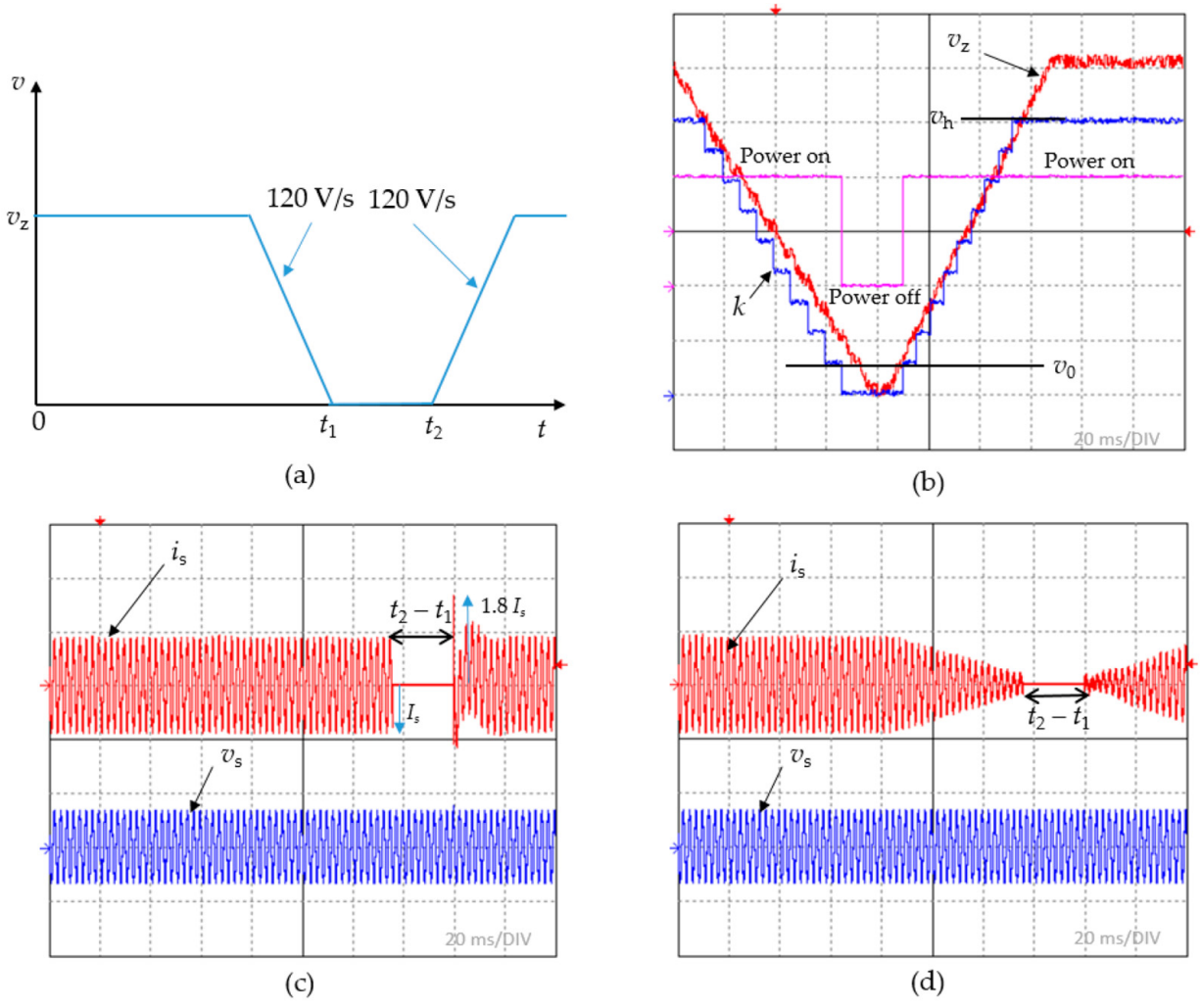

Figure 8. Dynamic response of the system to a voltage change on power bus 4: (**a**) assumed voltage profile on bus 4; (**b**) waveforms of the recorded voltage of bus 4 v_z, correction factor k, and supply voltage identifier (pink color); waveforms of current i_s and voltage vs. of bus 2 recorded in the classical system (**c**) and in the proposed system (**d**).

One of the cases studied concerned a short disturbance of bus 4 voltage, which did not fall below the threshold value v_0. The disturbance profile shown in Figure 9a was assumed. Figure 9b shows a linearly falling voltage, which began to rise before reaching the assumed threshold value. In other words, the proposed system identified a disturbance in the power

supply system, but it did not cause the photovoltaic converter to disconnect because the supply voltage was not in the C area. Consequently, the correction factor k did not reach zero, so the operation of the photovoltaic converter was not stopped. The power indicator on the control board monitored the correct power supply. If the proposed control strategy was not implemented in the tested system, the current of the photovoltaic system did not show any disturbance. This can be observed in Figure 9c. This is an obvious observation, as the disturbance could not cause the FPGA to shut down. Figure 9c shows the current flowing into the onboard grid for the system proposed in the paper. Although the voltage on bus 4 was sufficient to support the FPGA chip's configuration memory, the system prepared for a possible reboot by limiting the current flowing from the photovoltaic system. When the danger of shutting down the FPGA chip was eliminated, the bus current returned to its previous value. The effect of such a system response is to reduce the photovoltaic energy produced, thus constituting a disadvantage. However, this disadvantage is of negligible importance, since the duration of the disturbance is so short that the loss of photovoltaic energy is negligible.

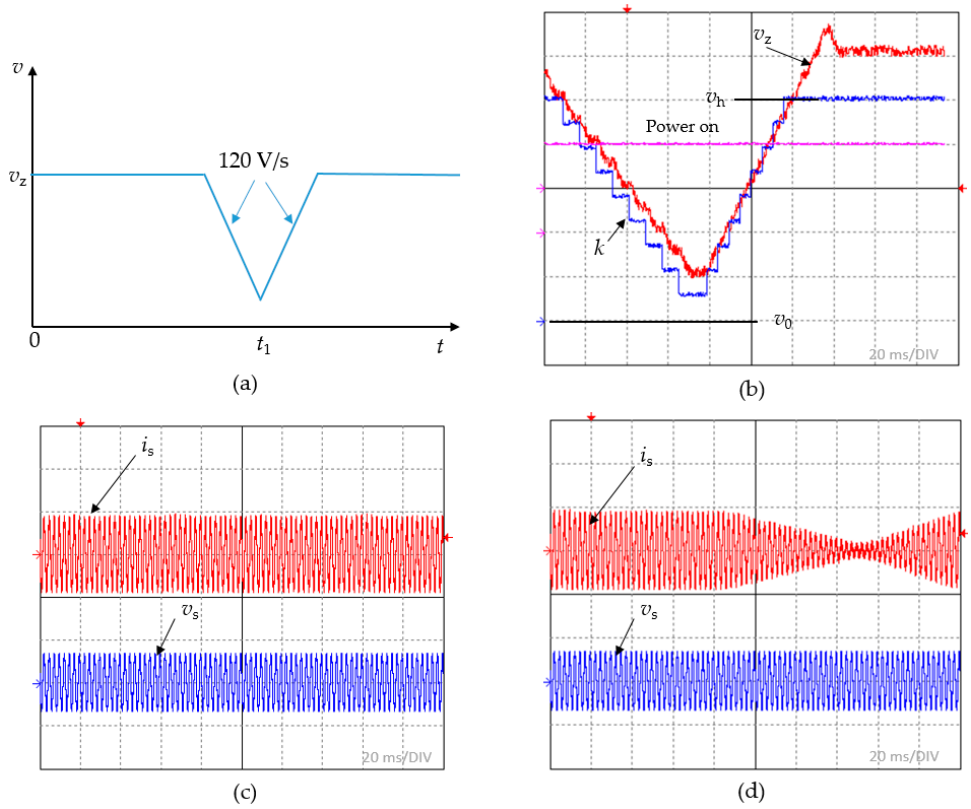

Figure 9. Dynamic response of the system to a voltage change on power bus 4: (**a**) assumed voltage profile on bus 4; (**b**) waveforms of the recorded voltage of bus 4 v_z, correction factor k, and supply voltage identifier (pink color); waveforms of current i_s and voltage vs. of bus 2 recorded in the classical system (**c**) and in the proposed system (**d**).

The last of the cases investigated involves a situation in which the voltage occurring on bus 4 is disturbed, but in such a way that it does not fall below the safe operating value of the FPGA v_h. The generated disturbance is shown in Figure 10b. Since the defined reference value correction rules should not affect the control process, no disturbance should be visible in the currents of onboard bus 2. This is confirmed by the recorded k-factor waveform and the active control board power indicator. Figure 10a confirms the applied strategy. The current of bus 2 is not disturbed, which is associated with the saturation of the scaling factor k.

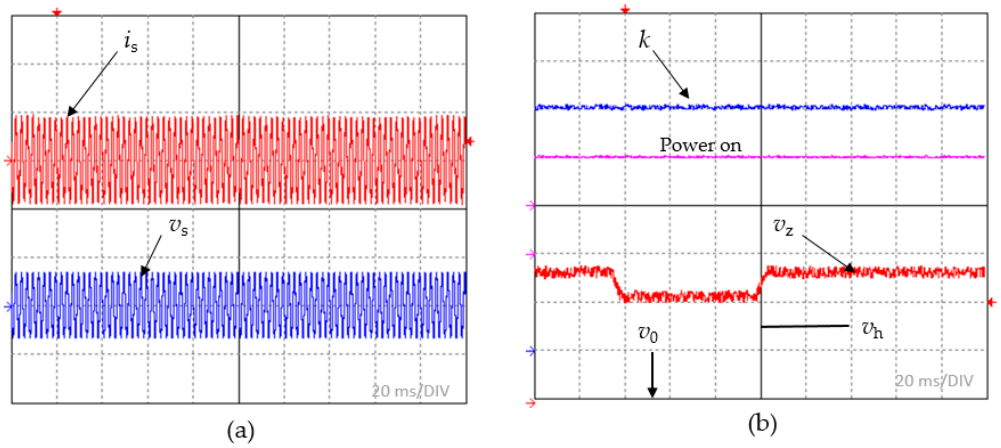

Figure 10. Dynamic response of the system to a voltage change on power bus 4: (**a**) waveforms of current i_s and voltage vs. on bus 2 recorded in the proposed system; (**b**) waveforms of the recorded voltage of bus 4 v_z, correction factor k, and supply voltage identifier (pink color).

Analyzing the experimental results, it can be concluded that the developed system sufficiently strengthens the reliability of the on-board power system. In the standard version, the system, in the case of strong impulse disturbances produced in the DC power bus, propagated them to other elements of the power grid. The effect of propagation was the result of temporary voltage drops in the electronic infrastructure that caused the control equipment to restart. As a result of the auto-power on procedure, currents flowing from photovoltaic sources were characterized by transients in which the instantaneous value of the current exceeded more than twice the value of the steady-state current, depending on the nature and duration of the disturbance. The system proposed in the paper reduced the impact of this type of disturbance, and thus its effect on the on-board grid, eliminating the abnormal rise of grid current during transients or significantly reducing it. Increased system reliability was achieved by reducing the value of grid current in transients caused by the auto power process from 280% to less than 100% of the steady-state value. The value of transient current reduction depends primarily on the duration of the disturbance and the steepness of the voltage drop and rise.

The results obtained during the tests for the proposed system were compared with the results for a system without the proposed method of limiting disturbance transmission. The maximum value of the transient current caused by the transmission of the disturbance coming from the bus supplying the control board (the first element in Table 3) was compared with each other and the effect of the disturbance on the photovoltaic current (the second element in Table 3) was identified using the logical variable Yes/No. The results are summarized in Table 3, assuming the following:

- Case 1—profile of the disturbance defined in Figure 5a;
- Case 2—profile of the disturbance defined in Figure 6a;
- Case 3—profile of the disturbance defined in Figure 7a;
- Case 4—profile of the disturbance defined in Figure 8a;
- Case 5—profile of the disturbance defined in Figure 9a
- Case 6—the disorder in Figure 10b.

Table 3. Comparison of the standard on-board system with the proposed system.

	Case 1	**Case 2**	**Case 3**	**Case 4**	**Case 5**	**Case 6**
Standard on-board system	2.8 I_s; Yes	2.6 I_s; Yes	1.3 I_s; Yes	1.8 I_s; Yes	1.0 I_s; No	1.0 I_s; No
Proposed system	<I_s; Yes	<I_s; Yes	<I_s; Yes	<I_s; Yes	<I_s; Yes	1.0 I_s; No

4. Conclusions

The paper presents a proposed on-board electrical system designed for ships, aviation, and space vehicles with improved reliability. The system connects standard electrical power sources, such as generators, batteries, and photovoltaic panels. As a result of pulse loads, a disturbance can occur on the power buses of the control board, causing electronic systems to reboot. To limit the propagation of the disturbance, a method was developed to reduce them by making the control process depend on the voltage value of the power bus. This novel approach limits the problem, which has not been reported before. The proposed system has special significance in critical infrastructure components due to its ability to increase the reliability of the power system and reduce the propagation of disturbances to other components of the power distribution system. Using the method described in this work, a lower impact of pulse disturbances and smooth power return can be observed during the auto power procedure. This is the strongest point of the system presented in this paper, which can be developed in the future by implementing an analogous method for other power facilities in the onboard grids.

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