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A Novel Solid-State Transformer with Improved Flyback Converter Equipped with Quasi Z-Source Converter for Medium-Voltage Utility Grid

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Abstract: This paper introduces an enhanced solid-state transformer topology for a medium-voltage (MV) utility grid. The main objective of the current study is to develop an improved flyback converter equipped with a quasi z-source converter (qZ_iFC) having a high-voltage conversion capability for the integration of low-input voltage to the DC link of an MV modular multilevel converter (MMC). The system integrates the quasi z-source and flyback converters by operating their existing switches complementary. Furthermore, the high-gain qZ_iFC allows for a reduction in the rated voltage of the input, as well as the use of a high-frequency transformer (HFT) with a unity turns ratio that provides galvanic isolation between the input and the output ports. Thus, using an HFT just for isolation purposes without voltage gain improves the system efficiency. In addition, a controller for (i) qZ_iFC which is regulating complementary switches to prevent the shoot-through current from reaching the HFT resulting in saturation; and (ii) a controller for MMC to produce MV-level AC voltage for loads are suggested. The performance of the proposed system was evaluated for several operating conditions. Results show that the proposed SST smoothly performs the power flow between the ports during steady-state and transient conditions. The power flow capabilities and efficiency values validate the viability and effectiveness of the proposed system.

Keywords: solid-state transformer; flyback converter; quasi z-source; high gain; medium-voltage utility

Citation: Cuma, M.U.; Anvari, A.D.; Savrun, M.M. A Novel Solid-State Transformer with Improved Flyback Converter Equipped with Quasi Z-Source Converter for Medium-Voltage Utility Grid. *Energies* **2023**, *16*, 2687. https://doi.org/10.3390/en16062687

Academic Editors: K. T. Chau and Pawel Rozga

Received: 20 January 2023
Revised: 23 February 2023
Accepted: 7 March 2023
Published: 13 March 2023

1. Introduction

Transformers are one of the essential components in electricity transmission and distribution systems, enabling transmission of power with the features of being relatively inexpensive, highly reliable, and highly efficient. While power transformers step up the voltage of the generator for transmission, they also step down the transmission voltages for industrial and residential uses [1]. However, while they are frequently used in transmission/distribution systems, they possess such drawbacks as: (i) bulky structure, because of the in-line operation frequency, (ii) sensitivity to harmonics, and (iii) voltage drops [2]. The emerging concepts for the conventional power transformers offer new magnetic/insulation materials [3,4], optimization in the core [5], and manufacturing processes [6].

Nowadays, the tendency to integrate technological advancements in power electronics in mid/high-voltage and high-power levels to empower future grids has grown dramatically. The capabilities and features of power electronics technology have led to improved power quality, increased stability, increased reliability, and more flexibility of power systems. In this regard, solid-state transformers (SST) [7] which are also known as power electronic transformers (PET) [8] and power electronic traction transformers (PETT) [9] are one of the emerging and promising power electronics technologies. SSTs have replaced the traditional bulky line transformers by performing many features, such as reactive

power compensation, galvanic isolation, power factor correction, size reduction, voltage regulation, and DC integration.

Recently, several SST topologies which are formed as (i) a single-stage including matrix or cycle converters [10], (ii) two-stage including AC–DC front end rectifier and inverter [11], and (iii) three-stage including AC–DC/DC–DC/DC–AC converters [12] have been proposed in the literature. Among them, although single-stage topology provides superior efficiency and power density, the three-stage SST is the most widely studied and used because of the smart features it can perform. The most outstanding feature of the three-stage SST is to provide low-voltage (LV) DC links for the integration of distributed generation (photovoltaic panels, fuel cells) and battery storage systems [13]. The integration of the aforementioned energy units and medium-voltage distribution grid can be realized with a DC–DC converter which is able to perform galvanic isolation and voltage gain, and an inverter which makes it possible to reach medium-voltage levels in AC from stages of SSTs. Numerous DC–DC converter topologies have been studied in the literature.

Dual active bridge (DAB) DC–DC converter topology is frequently used in SST applications because of the features of bidirectional power transfer, isolation, zero-voltage switching, flexible voltage range, and lower number of passive components [14,15]. In [16], a DAB-based SST study was conducted in order to interface photovoltaic arrays with 400 V and a utility grid with 10 kV. In addition to DAB topology, variations of it, such as LLC resonant and half-bridge topologies, are employed in SSTs adopted for medium-voltage applications. The front bridge arm of the DAB was replaced with half-bridge submodules in order to reduce the converter volume and the cost in [17]. Authors in [18] proposed an SST with a unidirectional LLC resonant converter. Some authors have addressed a topology that is integrated with a series-half-bridge LLC resonant DC–DC converter and a neutral-point clamped full-bridge inverter to reduce the series cell number in comparison with traditional two-level SSTs [19]. The aforementioned SST topologies adopted for medium-voltage applications are employed with cascaded/modular multilevel schemes. The related concepts consist of an extendable structure with converter cells including bidirectional DC–DC converters and inverters connected in series on the high-voltage AC side and in parallel on the low-voltage DC side, considering the voltage levels of the systems [7]. A current-fed series resonant converter-based SST topology presented in [20] reaches MV level using high turns-ratio HFT. The available typical SST concepts which are endowed with half-bridges, full-bridges, DABs, and 3-phase full bridges were categorized in [21]. The common aspect of the DAB-based SST topologies, and of the derivations of it, is the (requirement of modular structure) use of cascaded/modular multilevel structure in order to reach medium-voltage level. Also, the common drawback of the aforementioned DC–DC converter topologies is that they are operated at low-voltage gain for high efficiency. Therefore, a large number of series-connected converter cells and switching elements are required to reach the medium-voltage level. According to the existing topologies in the literature, a comparative investigation of the proposed topology is shown in Table 1. The proposed converter is compared with some DC–DC converter topologies used in SSTs in terms of five parameters: SST voltage, DC–DC converter voltage range, frequency, number of switches/diodes, and efficiency. As illustrated in Table 1, the proposed topology uses less switches. Furthermore, the efficiency of the proposed topology is higher than the compared existing topologies.

Along with the widespread applications of renewable energy sources (RESs) with low-output voltage, high-gain DC–DC converter topologies have also gained importance. Several high-gain DC–DC converter topologies have been improved, such as (i) z-source [22], (ii) quasi z-source [23], (iii) switched capacitor boost [24], (iv) stacked boost [25], (v) quadratic boost [26], (vi) three-level boost [27], and (vii) cascaded boost [28] converters in the literature. Although RES-powered systems are equipped with high-gain DC–DC converter topologies, they are not widely used in SST applications that allow the integration of RESs and energy storage units. As it is understood from the literature review, SST topologies are frequently formed with modular/cascaded multilevel converter cells that require

large number of active switching components with high costs to reach medium-voltage levels. In addition, the conventional DC–DC converter topologies are able to provide limited voltage gain because of the efficiency concern.

Table 1. A comparison of DC–DC converter topologies used in the proposed system and existing MV SST applications.

Refs.	SST Voltage	DC–DC Converter Voltage Range	Frequency	# of Switches and Diodes	Efficiency
[16]	10 kV	400–800 V	400 Hz	8 switches/8 diodes per module	97.5%
[18]	-	700 V–1 kV	30–60 kHz	4 switches/ 4 diodes/resonant components	97.18%
[19]	10 kV	800 V (400-400)–1050 V	200 kHz	4 switches/4 diodes/resonant components per module	98%
[20]	7.2 kV	240 V–7.2 kV	37 kHz	4 switches/4 diodes/resonant components per module	97.8%
Proposed	3.3 kV	100 V–1.1 kV	20 kHz	2 switches/4 diodes per module	98.5%

This paper proposes a novel SST structure with an improved flyback converter equipped with a quasi z-source converter for a medium-voltage utility grid. Also, the mathematical model of the proposed qZ_iFC and the corresponding control schemes are presented in the study. The proposed converter is composed of three cascaded converter cells and each converter cell consists of a quasi z-source converter, a flyback converter, a full-wave rectifier, and an inverter. The qZ_iFC is able to provide high-voltage gain with low-input voltage. Compared with the DC–DC converters employed in (conventional) SSTs presented in the literature, the proposed converter uses less switches to reach medium-voltage level. The performance of the proposed system is verified through different case studies.

The rest of the paper is organized as follows: Section 2 introduces the proposed improved SST topology and describes its mathematical model operation limits. Section 3 presents the control scheme of the overall system. Furthermore, the operations stages of the proposed novel qZ_iFC were analyzed. The performance results of the system are presented in Section 4. Section 5 presents the conclusions.

2. Power Circuit of the Proposed qZ_iFC-Based SST

In this section, a new, highly energy-efficient DC–DC/DC–AC stage of SST configuration, which is proposed to manage power flow from a low-voltage DC link to medium-voltage AC grid, is explained. The main motivation of the proposed converter is to provide high-voltage gain in order to makes it possible to reduce the number of series converter cells. The AC–DC stage of the SST is not investigated as it will be low-voltage rectifier topologies. The proposed system is capable of feeding from conventional and new generation low-voltage rectifiers, as well as directly feeding from renewable energy sources or DC microgrids. As illustrated in Figure 1, the proposed converter is composed of three quasi z-source converters, three flyback converters, and a full-bridge modular multilevel converter (FB-MMC) in order to interface 100 V input side and 3.3 kV (peak) medium-voltage grid. The quasi z-source converter is employed to reach high-voltage gain with reduced switch number in comparison with traditional SST topologies. The switches of the quasi z-source converter is triggered considering the gain requirement of the overall system. From a topological perspective, the improved converter integrating the flyback converter switch (S_f) and the S_{qz} switch form a complementary operation to generate a high-frequency AC voltage on the HFT. The flyback converter is equipped with an IGBT without body diode to prevent the shoot-through current which prevents saturation from reaching the HFT. The proposed qZ_iFC is endowed with an HFT with 1:1:1 turns ratio. Although increasing the turns ratio reduces the core losses due to the low magnetic flux density, it has a drawback in the overall efficiency of the system because it increases the winding losses [29,30]. For this reason, the high-gain capability is provided with the quasi-z-source converter. Thus, the proposed converter is able to achieve high gain while providing galvanic isolation.

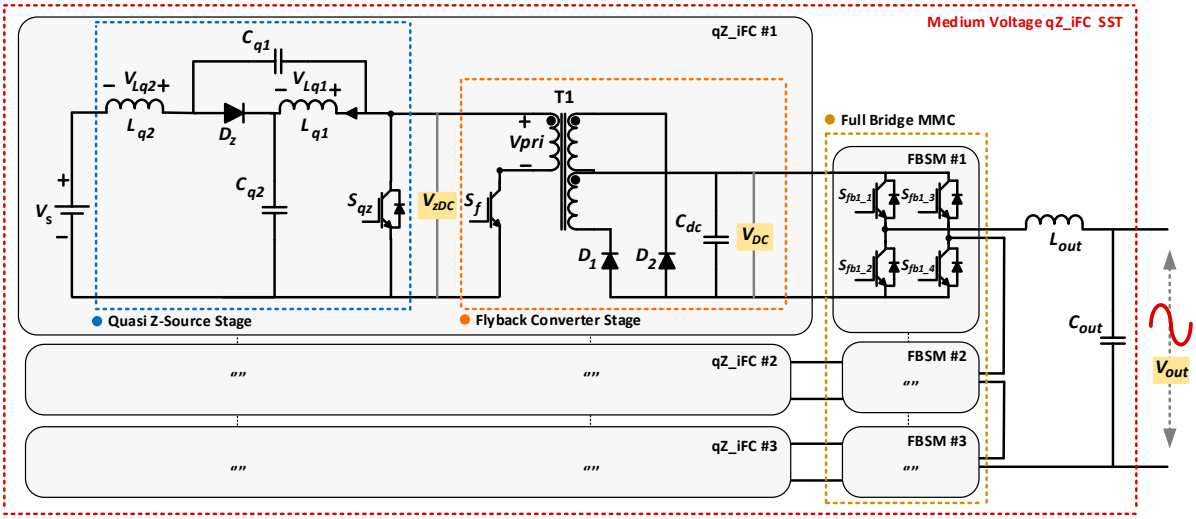

Figure 1. Circuit diagram of novel qZ_iFC-based SST.

The system can be assumed to be composed of a two-stage circuit and can be analyzed by dividing it into two parts. The first analysis is performed for quasi z-source converter and the second analysis is performed for the flyback converter. The quasi z-source converter has two types of operational state: the non-shoot-through state and the shoot-through state. Assuming that during one switching cycle T_s, the interval of the shoot-through state is DTs, and the interval of the non-shoot-through state is $(1 - D)T_s$. Since the closing of the switch S_{qz} represents the shoot-through state, D_{qz} represents the duty cycle of the S_{qz} switch. While the S_{qz} is triggered during the shoot-through state, the diode of the quasi z-source converter is forward biased during the non-shoot-through state.

During the time interval of non-shoot-through and shoot-through states, the voltages of the quasi z-source converter can be obtained as

$$V_{Lq2} = V_s - V_{Cq2}, V_{Lq1} = -V_{Cq1}, V_{zDC} = V_{Cq2} - V_{Lq1} = V_{Cq1} + V_{Cq2}, V_{Dz} = 0 \quad (1)$$

$$V_{Lq2} = V_s + V_{Cq1}, V_{Lq1} = V_{Cq2}, V_{zDC} = 0, V_{Dz} = V_{Cq1} + V_{Cq2} \quad (2)$$

where V_s and V_{pn} represent the supply voltage and output voltage of the quasi z-source converter, respectively.

The voltages of the quasi z-source converter stage capacitors can be derived as follows:

$$V_{Cq1} = V_s(D_{qz}/(1 - 2D_{\_qz})) \quad (3)$$

$$V_{Cq2} = V_s((1 - D_{qz})/(1 - 2D_{qz})) \quad (4)$$

The V_{zDC} voltage can be derived by summing Equations (3) and (4). Thus, the V_{zDC} and V_s voltage relations can be derived as follows:

$$V_{zDC} = V_s\,(1/(1 - 2D_{qz})) \quad (5)$$

The second analysis is performed for the flyback stage. The secondary side of the relevant converter is equipped with a center-tapped HFT. The switches of S_{qz} and S_f operate in a complementary fashion. The steady-state relationship between input and output sides of the improved flyback converter is derived as

$$V_{dc} = V_{zDCmean}((2D_f)/(1 - D_f)) \quad (6)$$

where D_f represents the duty cycle of the flyback converter switch.

For the designed qz_iFC, the voltage gain can be increased by regulating the duty cycle in order to reach the desired output voltage levels. The characteristics of qZ_iFC

topology is examined and the voltage gain/efficiency curve according to the duty cycle is illustrated in Figure 2. The proposed topology provides high-voltage gain values up to 20 and high-efficiency values up to 99.2%. The optimum duty cycle can be maintained between the range of 0.4 and 0.8 considering the most convenient area of efficiency and voltage gain for practical implementations.

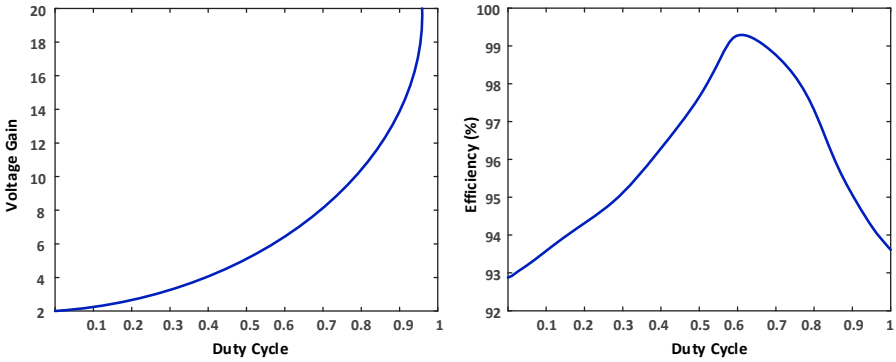

Figure 2. Voltage gain and efficiency curve of the proposed qZ_iFC.

The qZ_iFC makes it possible to eliminate the bulky line transformer from the inverter side using HFT. Thus, the MV power conversion system is only characterized by using H-bridge converters and an inductor (L)/capacitor (C) filter. The simplified circuit topology of the FB-MMC is shown in Figure 1. The FB-MMC consists of one phase and three series-connected full-bridge sub-modules (FBSMs) and each FBSM is fed by the individual DC links that are provided by the proposed qZ_iFC. While the switch pairs of S_{fb1_1}-S_{fb4_1} and S_{fb2_1}-S_{fb3_1} are triggered in turn, FBSMs are triggered synchronously. Moreover, the diodes of the switches are used to provide the paths for the load current driven by the stored energy in the inductor.

3. Control Scheme and Operation Stages of Proposed System

The control scheme of the proposed SST is composed of two different parts including qZ_iFC and inverter controllers as illustrated in Figure 3. The qZ_iFC controller is adopted to adjust the output voltage of the developed qZ_iFC stage by regulating the shoot-through duty cycle of S_{qz} and the duty cycle of Sf operating in reverse. The controller triggers the switches by complementary duty cycles considering the required output voltage rating. The related controller monitors the DC-link voltage (V_{dc}) continuously. It compares the difference between the actual and reference values of the DC link. Following the determination of the error value, the computed value is applied to a PI controller. The PI controller produces the duty cycle value for the Sf switch and its complement for the S_{qz} switch.

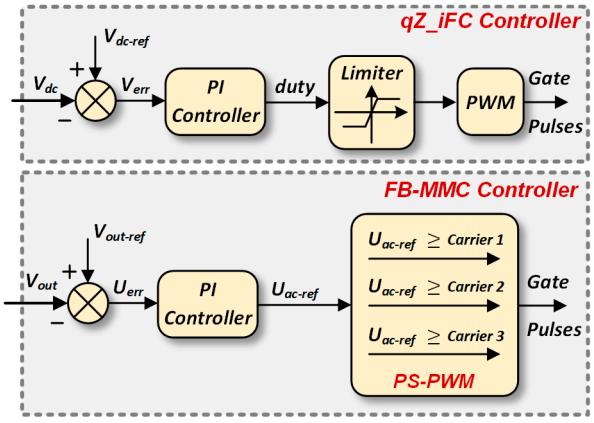

Figure 3. Control scheme of the proposed system.

The steady-state operation waveforms of qZ_iFC in terms of switching states (S_{qz}, S_f), input current (I_i), voltages of the quasi z-source converter's capacitors (C_{qz1}, C_{qz2}), and primary voltage of the HFT (V_{pri}) are presented in detail in Figure 4. As shown in Figure 4, the proposed converter has two operation stages during one switching cycle of T_s. Since the switches of S_{qz} and S_f operate in a complementary fashion, $1 - D_{qz}$ represents the D_f.

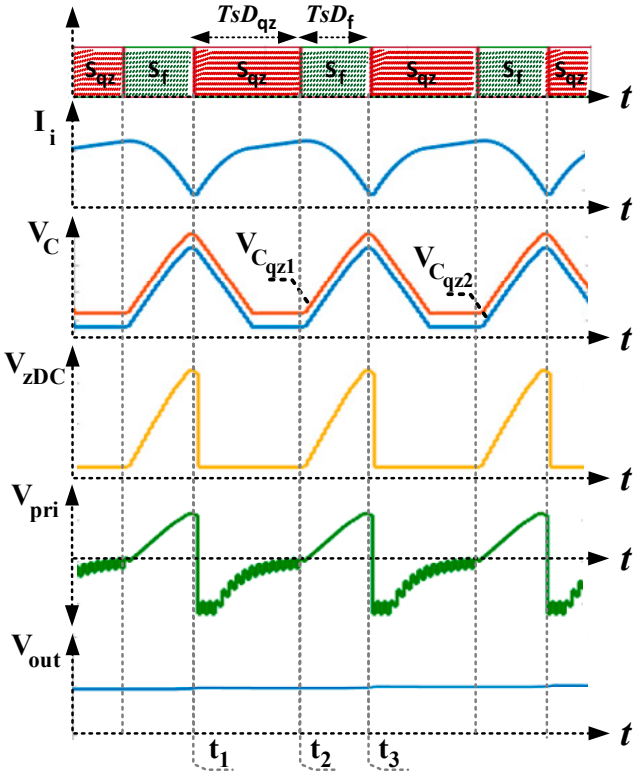

Figure 4. Key waveforms of the qZ_iFC.

Stage 1 [$t_1 - t_2$]: At t_1, S_{qz} switch is in ON state while S_f switch is in OFF state. Thus, quasi z-source converter operates in shoot-through state. Whenever it is in the related switching state, the current of the input inductor increases gradually. While the input inductor charges, the capacitors C_{qz1} and C_{qz2} discharge until the time point t_2. During this state, the shoot-through current path is blocked on the flyback converter side for high currents that can adversely affect the transformer, since there is no body diode in the S_f switch.

Stage 2 [$t_2 - t_3$]: At t_2, S_{qz} switch is in OFF state while S_f switch is in ON state. Thus, the quasi z-source converter operates in non-shoot-through state. During this operation, the capacitors C_{qz1} and C_{qz2} charge synchronously due to the energy stored in the inductors of the quasi z-source converter. The converter operates in continuous conduction mode. In parallel with the charging of the relevant capacitors, V_{zDC} voltage is also increased to high levels in proportion to their sum. The flyback converter switch provides the accumulation of energy in the HFT's primary winding, and the energy is transferred to the secondary windings. Following these operation sequences, the proposed qZ_iFC provides the desired DC-link voltage level with low ripple.

The inverter is equipped with phase-shift pulse width modulation (PS-PWM) to control the output voltage by rapidly switching the DC rail voltages. While the H-bridge converters share the same modulating sinusoidal signal of $V_{out\text{-}ref}$, three phase-shifted high-frequency carrier signals are used for individual H-bridge converters. The carriers are phase-shifted by an angle of 60 degrees obtained by dividing 180 degrees by the number of bridges.

4. Performance Analysis

This section presents the performance evaluation of the proposed qZ_iFC SST. In order to test and evaluate the performance of the improved SST topology and controller, a proof-of-concept model was developed in MATLAB/Simulink environment. The qZ_iFC SST model was designed for 3.3 kV (peak) application with 25 kVA cascaded qZ_iFCs (each rating is 8.3 kVA) and 25 kVA MMC. The operating frequencies are determined as 10 kHz and 20 kHz for MMC and qZ_iFC stages, respectively. The switching components of the power circuit are IGBT because of the power rating and switching frequency of the system. The parameters of the developed system are shown in Table 2. The presented system was tested with different case studies, including steady-state and transient conditions.

Table 2. Parameters of the developed system.

System	Parameter (per qZ_iFC SST)	Value
Quasi Z-Source Converter	Input voltage	100 V
	Gain	2–20
	Quasi z-source inductors	2 mH
	Quasi z-source capacitors	1 µF
	Switching frequency	20 kHz
Flyback Converter	High-frequency transformer turns ratio	1:1:1
	Switching frequency	20 kHz
	Magnetizing inductance	18 mH
Inverter	Filter inductor	50 mH
	Switching frequency	10 kHz
	Output voltage (AC)	3.3 kV (peak)
General	Power rating	25 kW
	DC link capacitor	470 µF
	Nominal DC link voltage (V_{DC})	1.1 kV

In this section, it is emphasized in some performance results of the proposed system for the 3.3 kV (peak) 25 kVA application. In the proposed system, a 100 V DC source is used as an input of the overall system. The presented system is tested under some case studies including transient and steady-state conditions of different loadings on the consumer-side. The dynamic load profile was created as 15, 25, and 19 kW. A 15 kW loading performance test was performed between t = 0 s and t = 3 s. Then, the load-side was increased to 25 kW at t = 3 s. Subsequently, the load was decreased to 19 kW at t = 6 s.

The main aim of the study is to increase the low-input voltage using high-gain qZ_iFC for the full-bridge MMC. Figure 5 shows the waveforms of the DC side of the proposed system. Voltage/current of input and V_{zDC}/V_{DC} voltages are illustrated for a variety of case studies. It is obvious that the low-input voltage level is increased to a high-voltage level using the shoot-through specification of the proposed converter. While the load variations directly affect the input current, the output voltage of the qZ_iFC (V_{DC}) remains constant at the desired level (1100 V). In other words, the proposed qZ_iFC supplies uninterrupted power transfer by providing a robust input DC link to the MMC.

The voltage, current, and power waveforms of load (AC) side are introduced in Figure 6. During the transient and steady-state operations, the output voltage of the proposed SST is kept constant at 3.3 kV peak value. In addition, the current waveform of the load varies in direct proportion to the load change. However, the state detection and reference extraction times cause instantaneous voltage fluctuations at point-of-load variations, the controller smoothly compensates the transient states. During these states, the switches of S_{qz} and S_f are triggered by the complementary duty cycle values computed by the controller in order to provide constant DC-link voltage for the inverter. As illustrated in Figure 6, the adapted duty cycle values of S_{qz} switch are 0.698, 0.799, and 0.759 for states, respectively. As understood from the zoom-in view of Figure 6, the total harmonic

distortion (THD) of load voltage is about 2.8% and is always kept below voltage harmonic limits of the IEEE 519-1992 standard [30].

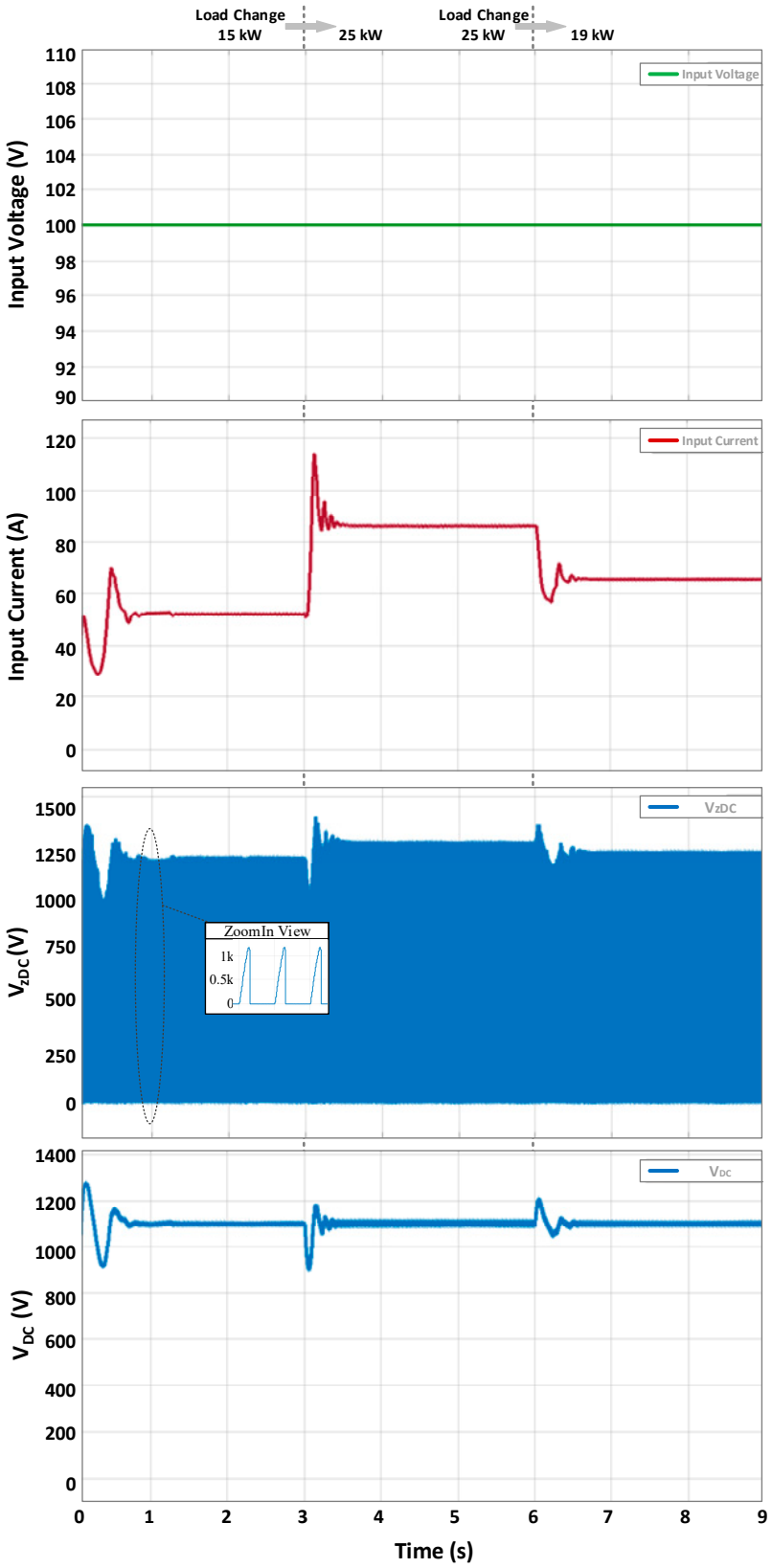

Figure 5. Performance results of DC side.

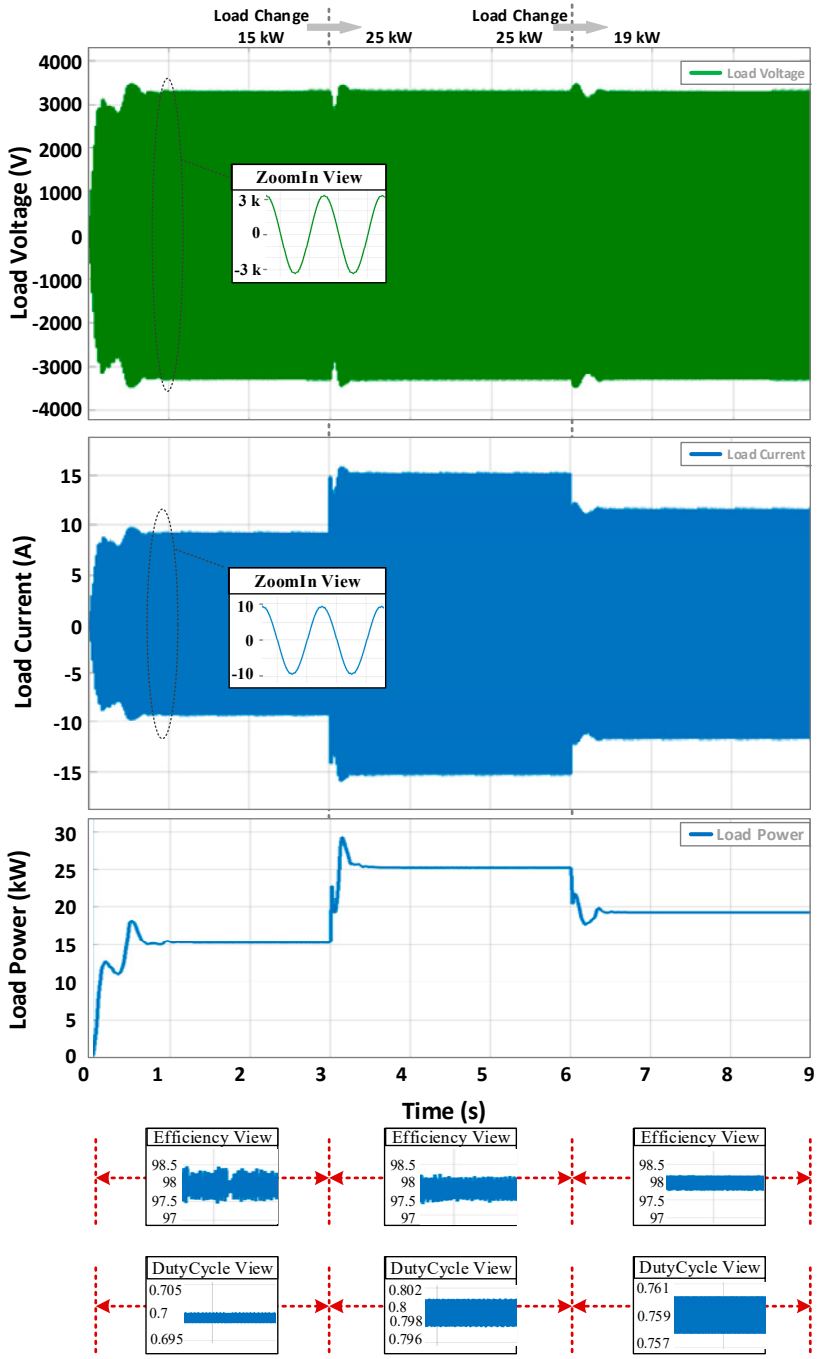

Figure 6. Performance results of AC side.

In addition, the presented system was also tested with the case studies of input voltage variations and disturbances under constant load conditions. During the related case, the input voltage variation is designed as follows: V_s = 75 V between 0 and 3 s, V_s = 125 V between 3 and 6 s, and V_s = 100 V between 6 and 9 s. In order to demonstrate the operation performance of the proposed converter, the input/output voltage, current and power waveforms are presented in Figure 7. The S_{qz} and S_f switches are triggered by the complementary duty cycle values computed by the controller in order to provide constant DC-link voltage for the inverter. As illustrated in Figure 7, the adapted duty cycle values of the S_{qz} switch are 0.78, 0.64, and 0.70 for states, respectively. The resulting DC-link voltage highlights that the proposed converter is able to keep the DC-link voltage constant during the input voltage variations.

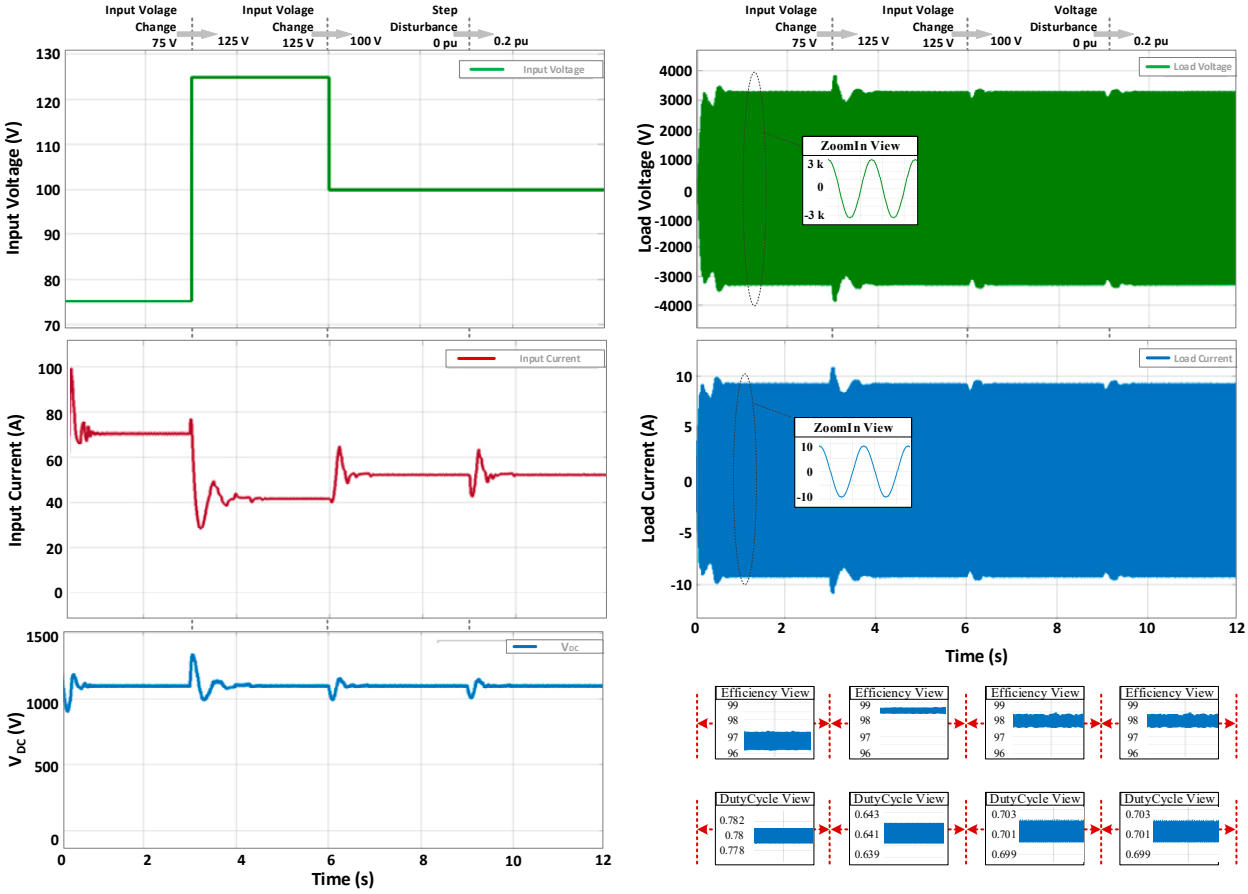

Figure 7. Performance results under varying input voltages and input disturbances.

Also, the disturbance rejection capability analysis was performed. As the load increases or decreases, the DC link often experiences undesired sags or swells to accommodate the varying load current. Therefore, the rejection capability of DC-link control against load disturbance becomes critical. The disturbance rejection capability of the converter can be described by applying disturbance to the input of the converter. A 20% (i.e., 0.2 p.u.) step disturbance that represents a sudden load disturbance was applied at t = 9 s to the output of three controllers of the qZ_iFC simultaneously. The responses of the synchronous controllers to the given disturbance, the DC-link voltage and the duty cycles are shown in Figure 7. As illustrated in Figure 7, the proposed control scheme achieves a high disturbance rejection capability with a smooth control signal. The DC-link voltage is not affected by the input disturbances. The disturbance rejection capability of the controller also verifies the robustness of the controller.

The efficiency of the system was investigated under dynamic loading, varying input voltages, and input disturbances states, and illustrated in performance results figures. In Figure 6, the system efficiency values are 97.9%, 97.7%, and 98% for the 15, 25, and 19 kW loading conditions, respectively. In Figure 7, the system efficiency values were obtained as a minimum of 96.5% and a maximum of 98.5% for varying input voltages and input disturbance conditions, respectively.

5. Conclusions

The utilization of SSTs in MV applications is still being studied and advanced gradually. With the widespread use of RESs, RES-buffered SSTs are anticipated to be used as popular energy generation units for daily applications of on-grid/off-grid integration in the next decades. In this study, a systemic analysis of a novel topology for SST application with a high-gain, high-efficiency conversion interface and control algorithm were presented. The

proposed system was designed for a medium-voltage utility grid. In the proposed system, an improved flyback converter equipped with a quasi z-source converter is positioned to convert a low-input voltage into a higher voltage at the DC link of the inverter. The main superior aspect of the proposed SST is the qZ_iFC including high-voltage gain and isolation specifications. While a mathematical model of the proposed novel qZ_iFC was presented, the performance validation of the proposed SST was examined for various case studies. In order to demonstrate the performance of the system, a 3.3 kV (peak) and 25 kVA proof-of-concept model was developed using the MATLAB/Simulink environment. The results highlight that the proposed qZ_iFC smoothly regulates the DC link of the inverter within a wide range of gain during load variations. Thus, uninterrupted power was provided for loads. In addition, it is observed that the efficiency of the overall system is approximately 96.5–98.5% in all cases. Compared with the existing topologies, the proposed system excels with the advantages of reduced switch count/control complexity and high efficiency. The results and efficiency values for different cases validate the applicability of the proposed system.

Author Contributions: Conceptualization, M.U.C. and M.M.S.; methodology, A.D.A. and M.M.S.; software, A.D.A. and M.M.S.; validation, M.U.C. and M.M.S.; formal analysis, A.D.A.; investigation, M.U.C. and A.D.A.; resources, A.D.A.; data curation, M.M.S.; writing—original draft preparation, M.U.C. and M.M.S.; writing—review and editing, M.U.C., A.D.A., and M.M.S.; visualization, M.U.C.; supervision, M.U.C. and M.M.S.; project administration, M.M.S.; funding acquisition, M.U.C. and M.M.S. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by Transformatör Elektromekanik Inc. R&D Center. Also, this research was funded by the Scientific Project Unit of Adana Alparslan Turkes Science and Technology University, grant number 21103002.

Acknowledgments: The authors would like to acknowledge Transformatör Elektromekanik Inc. R&D Center for full financial support. The authors also would like to acknowledge the Scientific Project Unit of Adana Alparslan Turkes Science and Technology University (Project Number: 21103002) for full financial support.

Conflicts of Interest: The authors declare no conflict of interest.

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