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Discrete-Time Sliding Mode Current Control for a Seven-Level Cascade H-Bridge Converter

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Abstract: This paper deals with the implementation and performance analysis of discrete-time sliding mode (DTSM) current control applied to a seven-level cascade H-bridge converter to track three-phase reference currents for a reactive load. The converter output voltages are synthesized using a modulation scheme based on phase-shifted carrier modulation. Simulation and experimental tests have been added to demonstrate the performance of the proposed controller. At the same time, the effectiveness of the DTSM is verified under transient and steady-state conditions, respectively, by measuring the total harmonic distortion and the mean square error.

Keywords: cascade H-bridge; current control; multilevel converter; nonlinear control; sliding mode control

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1. Introduction

Power electronics is a discipline that is increasingly involved in all stages of electrical energy processing, such as generation, conversion, transmission, distribution, and conditioning in its different stages and forms (CA → CC, CC → CA, etc.). Nevertheless, power electronic converters are restricted in their operational capabilities by switching devices, the limitations of which are imposed by the physical characteristics of semiconductor materials. In this regard, much research is being carried out around developing new semiconductor switching devices with higher voltage withstand capabilities. However, the goal of increasing the operating voltage of converters with existing circuit breakers also finds its way with the introduction of multilevel converters.

Multilevel converters are very attractive for high-power motor drives and uninterruptible power system applications [1,2]. The main reason is that they offer low harmonic content [3], higher efficiency [4], and increased device utilization at low modulation indices [5], among other features. Well-established topologies in the industrial and research area are Neutral-Point-Clamped (NPC) [6,7], Flying Capacitor (FC) [8,9], and cascade H-bridge (CHB) [10]. The NPC converter has a simple design. However, as the number of voltage levels increases, the number of clamping diodes increases, as well as the complexity of voltage balance control [11–13]. The FC and NPC converters are quite similar, as long as the clamping diodes in NPC are replaced with floating capacitors. As the number of voltage levels increases, it requires many capacitors and a complicated voltage balance control [12–14]. The CHB converter, in particular, has the attractive feature of modularity and power scalability [15,16], voltage-level redundancies (or extra degrees of freedom) [17,18], and is more reliable compared to FC and NPC converters [19].

From the point of view of applied current controllers to CHB converters, some are already presented in the literature. Decoupled control based on PI is widely used in power quality improvement applications, e.g., for a five-level CHB STATCOM [20,21]. In [20], the gains of the PI controllers depend on the parameters of the filters. In [21], the response

time reaches almost 40 ms and for a delta-connected seven-level CHB STATCOM, in [22] almost 10 ms. Furthermore, no robustness tests have been performed in any of these papers. The authors of [23,24] also used a PI as a current controller for a seven-level CHB STATCOM, and, in [25], for a 25-level version, and in [26], for a 45-level version. Although they obtained very good experimental results, the inner current controller is not their main contribution.

Lately, a fast dynamic response has been obtained with one of the most popular controllers, i.e., Model Predictive Control (MPC) variants. For a five-level CHB, the authors of [18] achieved a response time of 1 ms and reduced computational cost, and the authors of [27] proposed a long prediction horizon MPC, in which reference current tracking and common-mode voltage (CMV) minimization are achieved in a single optimization problem. In [28], an MPC is proposed as a current controller (inner loop) and a Sliding Mode Control (SMC) as a DC-link voltage regulator (outer loop). Despite all advantages of MPC, when this control is implemented in power converters, the free modulation becomes a disadvantage due to the unfixed switching frequency [29]. An interesting solution is shown in [30], for a seven-level CHB converter.

On the other hand, SMC is a nonlinear controller currently being applied to different systems and is mainly being studied in power electronics due to its simple implementation [31]. Most published articles refer to the application of this control technique (and some variants of it) to DC-DC converters [32,33], such as boost converters [34–39], buck converters [40–42], buck-boost converters [43], and, recently, to multiphase machines fed by DC-AC converters, such as two two-level voltage source converters [44,45] and matrix converters [46]. However, only a few publications are related to SMC applied to multilevel converters: NPC inverter [47] and modular multilevel converters (MMC) [48,49]. Then, there are no research studies about SMC applied to CHB as current controller, especially the seven-level version.

The paper's primary focus is the implementation of the Discrete-Time Sliding Mode (DTSM) control applied to a seven-level CHB converter, which could present many advantages in comparison to already published current controllers (mainly, its robustness since it offers a tracking error close to zero and a fast dynamic response comparable to that of the MPC). Therefore, simulation and experimental tests have been added to demonstrate the performance of this particular controller. At the same time, the effectiveness of the DTSM is verified under steady-state and transient conditions, respectively, by measuring the mean square error (MSE) and total harmonic distortion (THD).

The manuscript is organized as follows: the topology description and mathematical model of the seven-level CHB are presented in Section 2. In Section 3, the DTSM controller is described. Section 4 shows the simulation and experimental results in steady-state and transient conditions for performance analysis of the DTSM. Section 5 exposes the comparative performance of DTSM with the popular MPC technique. Finally, Section 6 summarizes the conclusion.

2. Topology Description and Mathematical Model

The three-phase seven-level CHB converter is shown in Figure 1. Each leg is composed of 3 identical H-bridge cells, which means that all DC-link voltages have the same values V_{dc}. The output voltage $v_{i\phi}$ of each cell depends on the states $s_{\phi ij}$ (0 → open and 1 → closed) of the four switching devices, as described by:

$$v_{i\phi} = \left(s_{\phi i1}\bar{s}_{\phi i2} - s_{\phi i3}\bar{s}_{\phi i4}\right)V_{dc} \quad (1)$$

where i is the corresponding cell 1, 2 or 3, j the corresponding switching device 1, 2, 3 or 4, and ϕ the corresponding phase a, b or c. However, only switches 1 and 3 are used to control one cell since they are always complementary with switches 2 and 4, respectively, to prevent short-circuit on DC-links. In this way, $v_{i\phi}$ has only three possible values, as shown in Table 1.

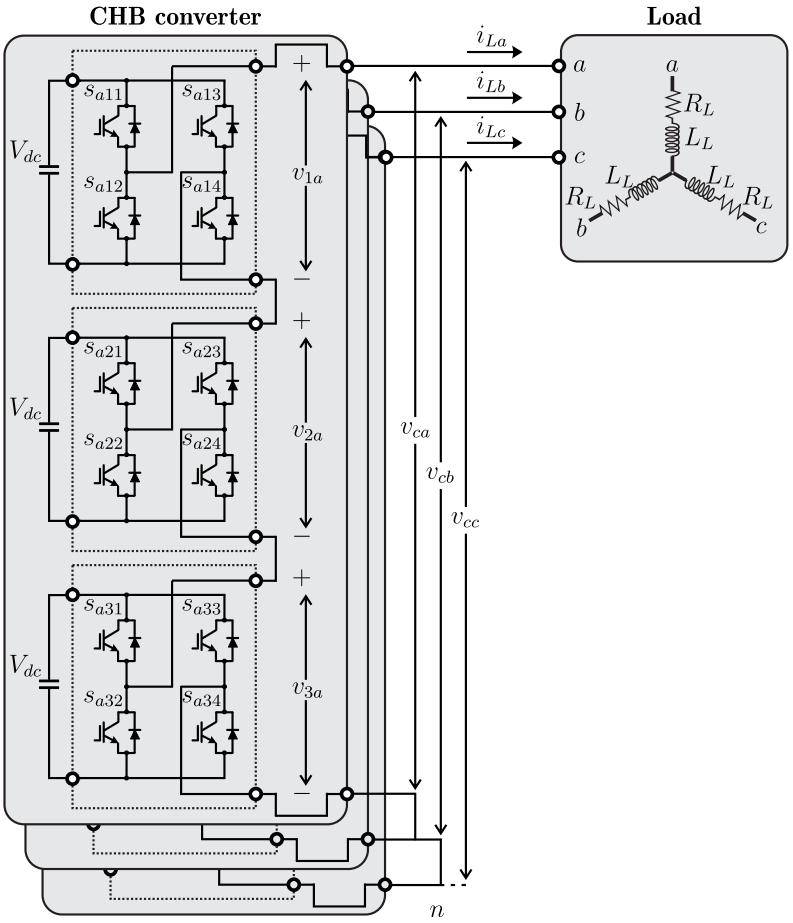


Figure 1. Three-phase reactive load (R_L-L_L) fed by a three-phase seven-level CHB.

Table 1. Possible voltages values for $v_{i\phi}$.

$s_{\phi i1}$	$s_{\phi i3}$	$s_{\phi i2}$ $(=\bar{s}_{\phi i1})$	$s_{\phi i4}$ $(=\bar{s}_{\phi i3})$	$v_{i\phi}$
0	0	1	1	0
0	1	1	0	$-V_{dc}$
1	0	0	1	$+V_{dc}$
1	1	0	0	0

The output voltage of the converter $v_{c\phi}$ can be obtained as the sum of the $v_{i\phi}$ voltages as follows:

$$v_{c\phi} = \sum_{i=1}^{3} v_{i\phi} \tag{2}$$

and referring to Table 1, the seven possible values for $v_{c\phi}$ are: $-3V_{dc}$, $-2V_{dc}$, $-V_{dc}$, 0, V_{dc}, $2V_{dc}$, and $3V_{dc}$

Considering the R_L-L_L load fed by the CHB converter as shown in Figure 1, the continuous model (for each phase) of the system is:

$$v_{c\phi} = R_L i_{L\phi} + L_L \frac{\mathrm{d}i_{L\phi}}{\mathrm{d}t} \tag{3}$$

where the load currents are defined by $i_{L\phi}$ considering that ϕ includes the corresponding phase a, b or c.

From Equation (3), using forward Euler discretization, we obtain:

$$i_{L\phi[k+1]} = \left(1 - \frac{R_L T_s}{L_L}\right) i_{L\phi[k]} + \frac{T_s}{L_L} v_{c\phi[k]} \tag{4}$$

where T_s is the sampling time and k identifies the actual discrete-time sample.

If state variables are defined by:

$$\begin{pmatrix} x_{1[k]} & x_{2[k]} & x_{3[k]} \end{pmatrix}^T = \begin{pmatrix} i_{La[k]} & i_{Lb[k]} & i_{Lc[k]} \end{pmatrix}^T \tag{5}$$

and the input and output variables by

$$\begin{pmatrix} u_{1[k]} & u_{2[k]} & u_{3[k]} \end{pmatrix}^T = \begin{pmatrix} v_{ca[k]} & v_{cb[k]} & v_{cc[k]} \end{pmatrix}^T \tag{6}$$

$$\begin{pmatrix} y_{1[k]} & y_{2[k]} & y_{3[k]} \end{pmatrix}^T = \begin{pmatrix} x_{1[k]} & x_{2[k]} & x_{3[k]} \end{pmatrix}^T \tag{7}$$

the state-space representation is obtained:

$$\begin{pmatrix} x_{1[k+1]} \\ x_{2[k+1]} \\ x_{3[k+1]} \end{pmatrix} = \begin{pmatrix} a_1 & 0 & 0 \\ 0 & a_1 & 0 \\ 0 & 0 & a_1 \end{pmatrix} \begin{pmatrix} x_{1[k]} \\ x_{2[k]} \\ x_{3[k]} \end{pmatrix} + \begin{pmatrix} b_1 & 0 & 0 \\ 0 & b_1 & 0 \\ 0 & 0 & b_1 \end{pmatrix} \begin{pmatrix} u_{1[k]} \\ u_{2[k]} \\ u_{3[k]} \end{pmatrix} \tag{8}$$

$$\begin{pmatrix} y_{1[k]} \\ y_{2[k]} \\ y_{3[k]} \end{pmatrix} = \begin{pmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} x_{1[k]} \\ x_{2[k]} \\ x_{3[k]} \end{pmatrix} \tag{9}$$

where the coefficients a_1 and b_1 of Equation (8) are defined according to the following equations:

$$a_1 = \left(1 - \frac{R_L T_s}{L_L}\right) \tag{10}$$

$$b_1 = \frac{T_s}{L_L} \tag{11}$$

3. Discrete-Time Sliding Mode Current Control

In this section, the proposed controller, named DTSM, is presented. First, the design procedure is described, and then, a stability analysis is proposed. Last, the convergence time for the system is estimated.

3.1. Design Procedure

The synthesis control procedure consists of the following steps:

- Define the sliding surface.
- Satisfy the sliding condition by selecting the reaching law.

For the current tracking problem, the conventional discrete-time sliding surfaces are defined for $i = 1, 2, 3$ as follows:

$$S_{i[k]} = e_{i[k]} = x^*_{i[k]} - x_{i[k]} \tag{12}$$

where $e_{i[k]}$ are the current tracking errors with $x^*_{i[k]}$ as the desired load currents (reference variables are represented through the superscript *).

To satisfy the sliding conditions

$$S_{i[k]} = S_{i[k+1]} = 0 \tag{13}$$

the reaching law is chosen as:

$$S_{i[k+1]} = \Lambda S_{i[k]} - LT_s \text{sign}\left(S_{i[k]}\right) \tag{14}$$

where Λ is chosen between 0 and 1, while $L > 0$ and the sign is defined by:

$$\text{sign}\left(S_{i[k]}\right) = \begin{cases} 1, & \text{if } S_{i[k]} > 0 \\ 0, & \text{if } S_{i[k]} = 0 \\ -1, & \text{if } S_{i[k]} < 0 \end{cases} \tag{15}$$

Then, from Equations (12) and (14), we have:

$$e_{i[k+1]} = x^*_{i[k+1]} - x_{i[k+1]} = \Lambda e_{i[k]} - LT_s \text{sign}\left(e_{i[k]}\right) \tag{16}$$

Considering Equations (8) and (16) results in:

$$x^*_{i[k+1]} - a_1 x_{i[k]} - b_1 u_{i[k]} = \Lambda e_{i[k]} - LT_s \text{sign}\left(e_{i[k]}\right) \tag{17}$$

Then, resolving Equation (17) gives the control law for the load currents as follows:

$$u_{i[k]} = \frac{x^*_{i[k+1]} - a_1 x_{i[k]} - \Lambda e_{i[k]} + LT_s \text{sign}\left(e_{i[k]}\right)}{b_1} \tag{18}$$

Figure 2 shows the DTSM control scheme for the CHB converter, where the control actions represented by Equation (18) are normalized between -1 and 1 and sent to a modulator to synthesize the output voltage of the CHB converter. The modulation stage consists of the phase-shift carrier pulse width modulation (PSC-PWM) technique, considering the carrier signal amplitude equal to 1 and the carrier frequency (f_{cr}) equal to the sampling frequency.

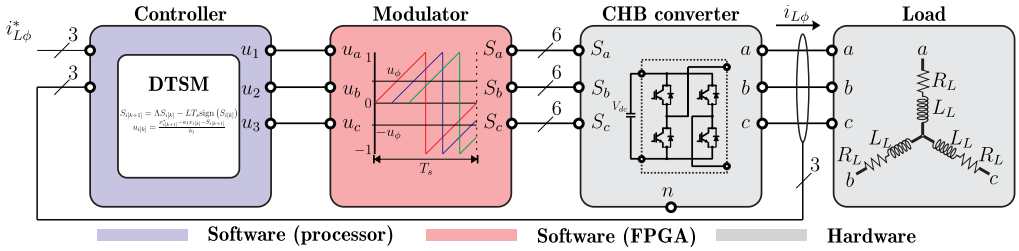


Figure 2. Block diagram of the DTSM current control method.

3.2. Stability Analysis

The existence of a quasi-sliding mode should be discussed to prove the stability of the closed-loop system. In other words, the system is stable if the following conditions hold for $i = 1, 2, 3$:

$$\begin{aligned} &e_{i[k]} > \varepsilon \Rightarrow -\varepsilon \leq e_{i[k+1]} < e_{i[k]} \\ &e_{i[k]} < -\varepsilon \Rightarrow e_{i[k]} < e_i(k+1) \leq \varepsilon \\ &|e_{i[k]}| \leq \varepsilon \Rightarrow |e_{i[k+1]}| \leq \varepsilon \end{aligned} \tag{19}$$

where $\varepsilon > 0$ depicts the bandwidth of the quasi-sliding mode. In this paper, we choose $\varepsilon = LT_s$. A simplified version of Equation (16) gives for $i = 1, 2, 3$:

$$e_{i[k+1]} = \Lambda\, e_{i[k]} - LT_s\, \text{sign}(e_{i[k]}) \tag{20}$$

1. Assuming that $e_{i[k]} > LT_s$ means that $e_{i[k]} > 0$, $\text{sign}(e_{i[k]}) = 1$ and:

$$\begin{aligned} e_{i[k+1]} &= \Lambda\, e_{i[k]} - LT_s \\ e_{i[k+1]}) - e_{i[k]} &= (\Lambda - 1)\, e_{i[k]} - LT_s \end{aligned} \tag{21}$$

since $(\Lambda - 1) < 0$, then $e_{i[k+1]} - e_{i[k]} < 0 \Rightarrow e_{i[k+1]} < e_{i[k]}$.
Furthermore, $-LT_s \leq e_{i[k+1]}$ can be written as:

$$\Lambda\, e_{i[k]} - LT_s \geq -LT_s \tag{22}$$

Hence,

$$e_{i[k]} \geq 0 \tag{23}$$

which is true with the assumption made.

2. Now, assuming $e_{i[k]} < -LT_s$ means that $e_{i[k]} < 0$ and $\text{sign}(e_{i[k]}) = -1$. Then, $e_{i[k]} < e_{i[k+1]}$ is similar to:

$$\begin{aligned} e_{i[k]} &< \Lambda\, e_{i[k]} + LT_s \\ (1-\Lambda)\, e_{i[k]} &< LT_s \end{aligned} \tag{24}$$

which is always true for any positive value of L. In addition, we can rewrite $e_{i[k+1]} < LT_s$ as:

$$\Lambda\, e_{i[k]} + LT_s < LT_s \tag{25}$$

which is true since $e_{i[k]} < 0$. Finally, the second condition of Equation (19) holds.

3. Now, let us assume that $|e_{i[k]}| \leq LT_s$, then:

   a. If $e_{i[k]} > 0$, then $|e_i(k)| \leq LT_s$ becomes:

$$0 < e_{i[k]} < LT_s \tag{26}$$

   Multiplying Equation (26) by Λ and adding $-LT_s$ to all the parts leads to:

$$\begin{aligned} -LT_s < e_{i[k+1]} < (\Lambda - 1)LT_s < LT_s \\ |e_{i[k+1]}| \leq LT_s \end{aligned} \tag{27}$$

   b. If $e_{i[k]} < 0$, then $|e_{i[k]}| \leq LT_s$ becomes:

$$-LT_s < e_{i[k]} < 0 \tag{28}$$

   Again, by multiplying Equation (28) with Λ and adding LT_s to all the parts gives:

$$\begin{aligned} -LT_s < (1-\Lambda)LT_s < e_{i[k+1]} < LT_s \\ |e_{i[k+1]}| < \varepsilon \end{aligned} \tag{29}$$

   Hence,

$$|e_{i[k+1]}| < \varepsilon = LT_s \tag{30}$$

   This implies that the third condition of Equation (19) is always true.

As a result, the conditions in Equation (19) are met, which proves the occurrence of a convergent quasi-sliding mode. Thus, the proposed DTSM is stable.

3.3. Convergence Time

Let us suppose that $e_{i[0]} \neq 0$ and $\text{sign}(e_{i[0]}) = \text{sign}(e_{i[1]}) = \cdots = \text{sign}(e_{i[k_i'+1]})$.

1. Firstly, assuming that $e_{i[0]} > 0$ and $e_{i[m]} > 0$ for all $m \leq (k_i' + 1)$ leads to:

$$\begin{aligned} e_{i[1]} &= \Lambda\, e_{i[0]} - LT_s \leq e_{i[0]} - LT_s \\ e_{i[2]} &\leq e_{i[1]} - LT_s \leq e_{i[0]} - 2LT_s \\ &\vdots \\ e_{i[m]} &\leq e_{i[m-1]} - LT_s \leq e_{i[0]} - mLT_s \\ &\leq |e_{i[0]}| - mLT_s \end{aligned} \tag{31}$$

   Hence, it is obvious that there exists a step $k_i' = \dfrac{|e_{i[0]}|}{LT_s}$ that ensures

$$|e_{i[0]}| - k_i^{'} LT_s = 0 \tag{32}$$

It follows that

$$\begin{aligned} e_{i[k_i^{'}+1]} &\leq |e_{i[0]}| - (k_i^{'}+1)LT_s \\ &< |e_{i[0]}| - k_i^{'} LT_s = 0 \end{aligned} \tag{33}$$

which is contradictory to the fact that $e_{i[m]} > 0$, $\forall\, m \leq (k_i^{'}+1)$.

2. Firstly, assuming that $e_{i[0]} < 0$ and $e_{i[m]} < 0$ for all $m \leq (k_i^{'}+1)$ leads to:

$$\begin{aligned} e_{i[1]} &= \Lambda\, e_{i[0]} + LT_s \geq e_{i[0]} + LT_s \\ e_{i[2]} &\geq e_{i[1]} + LT_s \geq e_{i[0]} + 2LT_s \\ &\vdots \\ e_{i[m]} &\geq e_{i[m-1]} + LT_s \geq e_{i[0]} + mLT_s \\ &\geq -|e_{i[0]}| + mLT_s \end{aligned} \tag{34}$$

Thus, it is obvious that $k_i^{'} = \dfrac{|e_{i[0]}|}{LT_s}$ verifies

$$-|e_{i[0]}| + k_i^{'} LT_s = 0 \tag{35}$$

It follows that

$$\begin{aligned} e_{i[k_i^{'}+1]} &\geq -|e_{i[0]}| + (k_i^{'}+1)LT_s \\ &> -|e_{i[0]}| + k_i^{'} LT_s = 0 \end{aligned} \tag{36}$$

which is contradictory to the fact that $e_{i[m]} < 0$, $\forall\, m \leq (k_i^{'}+1)$.

This concludes that each current will reach its desired reference within at most $k_i^{'}+1$ steps, where for $i = 1, 2, 3$:

$$k_i^{'} = \frac{|e_{i[0]}|}{LT_s} \tag{37}$$

4. Simulation and Experimental Results

The performance of the DTSM controller is analyzed in steady-state and transient conditions. For steady-state conditions, the DTSM technique behavior is studied using a reference amplitude $\left|i_{L\phi}^{*}\right| = 1$ A and a reference frequency $f^{*} = 50$ Hz. For transient conditions, the analysis is performed as follows. On the one hand, after a change in the reference amplitude from 0.5 A to 1 A (with a constant reference frequency equal to 50 Hz). In addition, on the other hand, after a change in the reference frequency, from 50 Hz to 100 Hz (with constant reference amplitude and equal to 1 A). Simulation and experimental results are analyzed in terms of MSE obtained between reference and measured load currents and THD of the CHB output voltages and load currents. MSE is measured in amperes (A) and obtained as follows:

$$\mathrm{MSE}\left(i_{L\phi}\right) = \sqrt{\frac{1}{N}\sum_{j=1}^{N}\left(i_{L\phi}^{*} - i_{L\phi}\right)^2} \tag{38}$$

where N is the number of samples. While THD is obtained as follows:

$$\mathrm{THD}(\Psi_\phi) = \sqrt{\frac{1}{\Psi_{\phi 1}^2}\sum_{i=2}^{N}\Psi_{\phi i}^2} \tag{39}$$

where $\Psi_{\phi 1}$ corresponds to the fundamental variable (voltage or current) whereas $\Psi_{\phi i}$ is the harmonic variable (multiple of the fundamental variable).

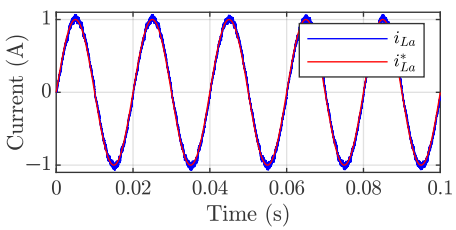
4.1. Simulation Results

Numerical integration based on first-order Euler's algorithm has been computed to the progress of the proposed controller. MATLAB/Simulink R2018b simulations have been performed in order to verify the feasibility of the DTSM control law given by Equation (18), considering the simulation parameters listed in Table 2.

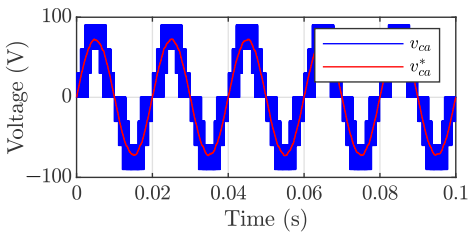
Table 2. Simulation parameter description.

Parameter	Symbol	Value	Unit
DC-link voltage	V_{dc}	30	V
Load resistance	R_L	72.2	Ω
Load inductance	L_L	10	mH
Sampling frequency	f_s	9.76	kHz
Simulation step	–	10.24	µs
Gain	λ	0.001	–
Gain	L	10	–

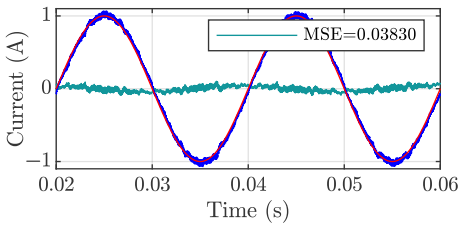
Figure 3 shows simulation results for phase a in steady-state condition. Figure 3a shows the time-evolution of the load current i_{La} and current reference i_{La}^*. Figure 3b presents the control action $u_1 = v_{ca}^*$ and CHB output voltage v_{ca}. Figure 3c,d denotes a portion of samples (two cycles) used for the computation of the MSE and THD parameters. Hence, $N = 5860$ in Equations (38) and (39). Figure 3c also illustrates the dynamic behavior of the current tracking error with an MSE value of 0.03829 A. Figure 3e presents the fast Fourier transform analysis of the load current i_{La} with a THD value of 3.52%. At the same time, Figure 3f presents the fast Fourier transform analysis of the CHB output voltage v_{ca} with a THD value of 35.80%. Similar simulation results in steady-state condition were obtained for phases b and c, and Table 3 summarizes the values obtained for THD and MSE parameters.



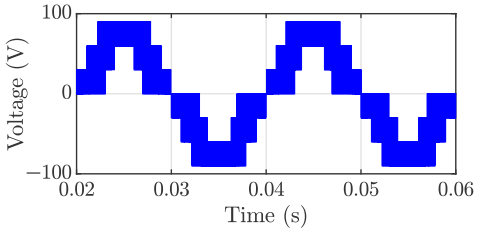
(**a**) Current tracking.



(**b**) CHB output voltage.

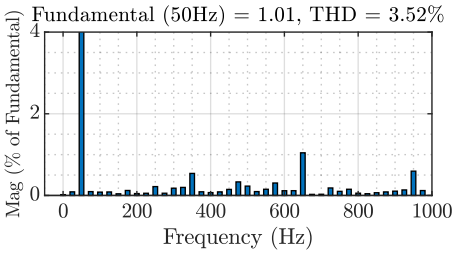


(**c**) Portion of interest for MSE.

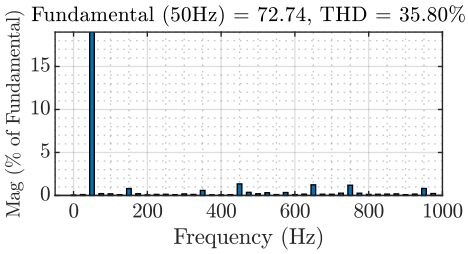


(**d**) Portion of interest for THD.

Figure 3. *Cont.*



(**e**) FFT analysis of i_{La}.



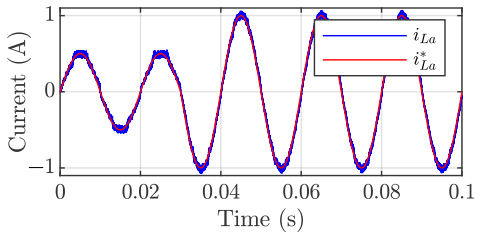
(**f**) FFT analysis of v_{ca}.

Figure 3. Simulation results for phase *a* in steady-state condition.

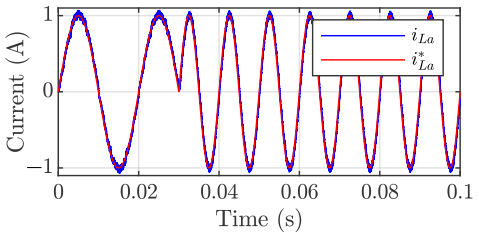
Table 3. Simulation results in steady-state condition.

Parameter	Phase *a*	Phase *b*	Phase *c*
MSE ($i_{L\phi}$)	0.03829 A	0.03864 A	0.03819 A
THD ($i_{L\phi}$)	3.52%	3.52%	3.57%
THD ($v_{c\phi}$)	35.80%	35.77%	36.02%

Figure 4 shows simulation results for phase *a* in transient conditions. Figure 4a shows the transient response of the load current i_{La} when a sudden change in the amplitude reference from 0.5 A to 1 A at t = 0.03 s is applied. Figure 4c demonstrates the control action $u_1 = v_{ca}^*$ value and CHB output voltage v_{ca} variation when the reference amplitude current changes. Figure 4b also presents the transient response of the load current i_{La}, for the case of a sudden change in the reference frequency from 50 Hz to 100 Hz at t = 0.03 s. Figure 4d demonstrates the control action $u_1 = v_{ca}^*$ value and the CHB output voltage v_{ca} variation when the reference frequency changes. Figure 4e,f denotes a portion of samples (two cycles) used for the computation of the MSE parameter. Hence, $N = 5860$ in Equation (38). The current tracking error behavior for both cases is illustrated in Figure 4e (MSE value of 0.03713 A) and Figure 4f (MSE value of 0.06109 A). Similar simulation results in transient conditions were obtained for phases *b* and *c*. To quantify the dynamic response, the results in *abc* frame are converted into the *dq*0 frame using Park's transformation (invariant amplitude). Figure 4g illustrates the case for current i_{Ld} when $|i_{Ld}^*| = |i_{La}^*|$ changes and Figure 4h when f^* changes; they present a rise time of 0.3 and 0.4 ms, respectively. In both cases, an overshoot of less than 1% is observed.

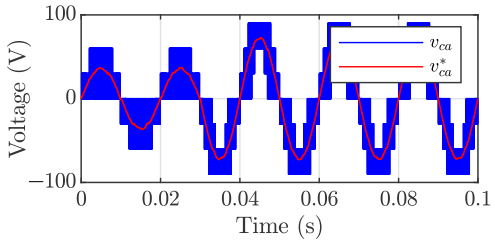


(**a**) Current tracking when $|i_{La}^*|$ changes.

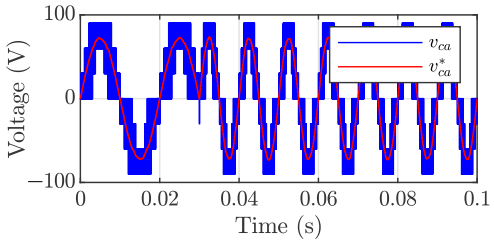


(**b**) Current tracking when f^* changes.

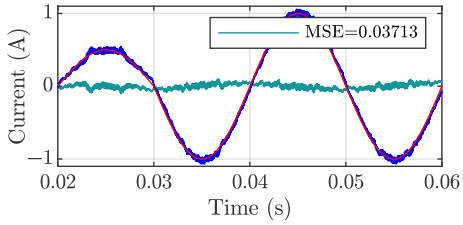
Figure 4. *Cont.*



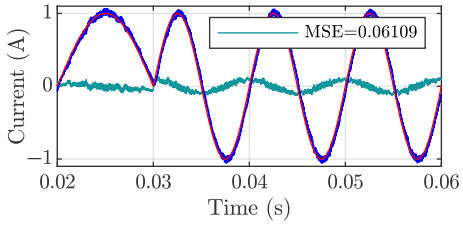
(**c**) CHB output voltage when $|i^*_{La}|$ changes.



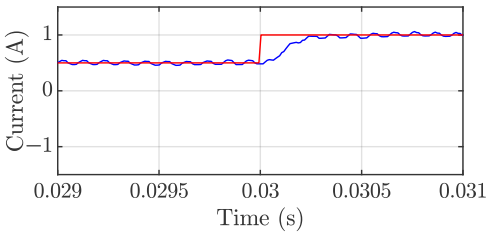
(**d**) CHB output voltage when f^* changes.



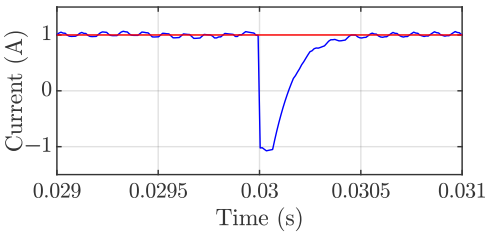
(**e**) Portion of interest for MSE when $|i^*_{La}|$ changes.



(**f**) Portion of interest for MSE when f^* changes.



(**g**) Step response when $|i^*_{La}|$ changes.



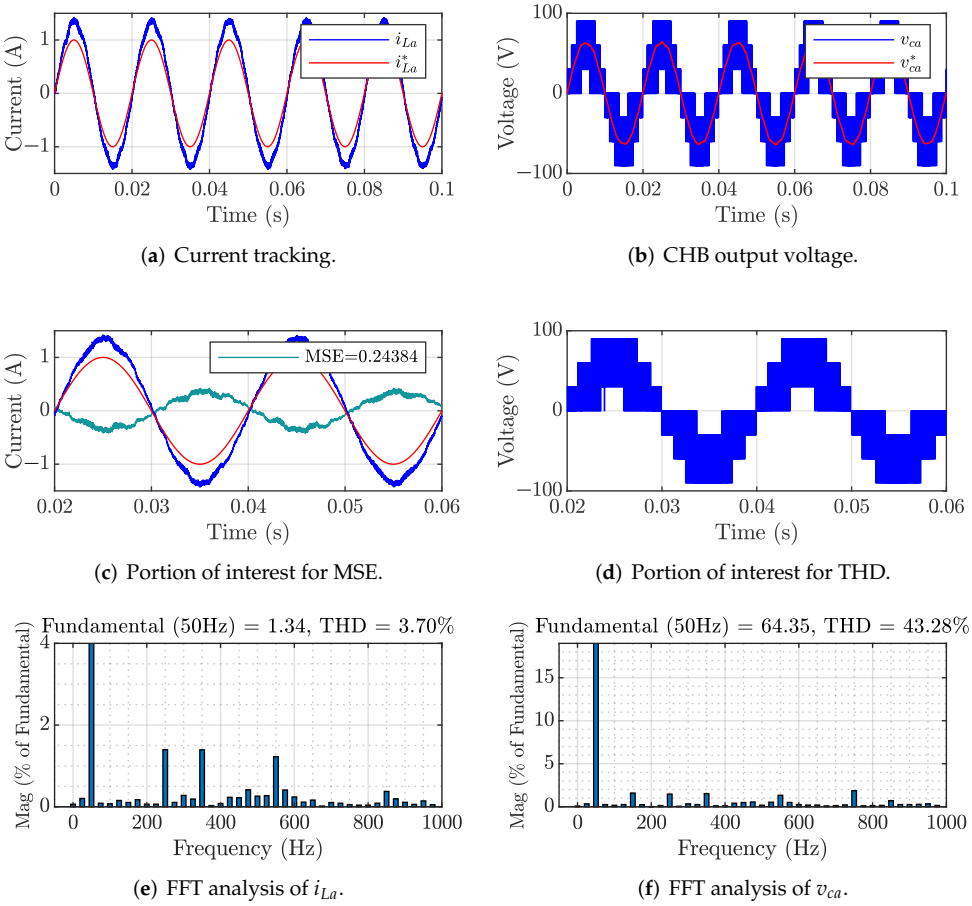
(**h**) Step response when f^* changes.

Figure 4. Simulation results for phase a (**a**–**f**) and i_{Ld} (**g**,**h**), in transient conditions.

Figure 5 shows the simulation results for phase a in the presence of parametric uncertainties, varying the value of the load (R_L equal to 48.13 Ω) and keeping the reference amplitude at 1 A and the reference frequency at 50 Hz. The value of R_L has also been maintained equal to 72.2 Ω in Equation (18). Figure 5a shows the time-evolution of the load current i_{La} and current reference i^*_{La}. Figure 5b presents the control action $u_1 = v^*_{ca}$ and CHB output voltage v_{ca}. Figure 5c,d denotes a portion of samples (two cycles) used for the computation of the MSE and THD parameters. Hence, $N = 5860$ in Equations (38) and (39). Figure 3c also illustrates the dynamic behavior of the current tracking error with an MSE value of 0.24383 A. Figure 5e presents the fast Fourier transform analysis of the load current i_{La} with a THD value of 3.70%. At the same time, Figure 5f presents the fast Fourier transform analysis of the CHB output voltage v_{ca} with a THD value of 43.28%. Similar simulation results in steady-state condition were obtained for phases b and c, and Table 4 summarizes the values obtained for THD and MSE parameters.

Table 4. Simulation results in the presence of parametric uncertainties.

Parameter	Phase a	Phase b	Phase c
MSE ($i_{L\phi}$)	0.24383 A	0.24364 A	0.24438 A
THD ($i_{L\phi}$)	3.70%	3.66%	3.77%
THD ($v_{c\phi}$)	43.28%	43.32%	43.28%



(**a**) Current tracking.

(**b**) CHB output voltage.

(**c**) Portion of interest for MSE.

(**d**) Portion of interest for THD.

(**e**) FFT analysis of i_{La}.

(**f**) FFT analysis of v_{ca}.

Figure 5. Simulation results for phase *a* in the presence of parametric uncertainties.

4.2. Experimental Results

For the experimental tests of the DTSM control described in Section 3, the test equipment, shown in Figure 6, is examined to validate its effectiveness, employing an AC variable load bank as R_L (it can vary from 1 kW to 20 kW). The other electrical and control parameters are the same as described in Table 2. The seven-level CHB converter is based on CAS120M12BM2 series SiC-MOSFET half-bridge modules, and nine independent voltage DC sources. A dSPACE MicroLabBox DS1201 control unit and Simulink version 9.5 have been used to implement the DTSM control technique. RTI FPGA programming block-set version 3.9.3 and Vivado 2019.2 have been used to implement the digital modulator on the dSPACE FPGA platform. Normalization is done between −128 and +127, because the carrier signals (sawtooth) are formed from signed 8-bit digital counters. On the other hand, the SiC-MOSFET half-bridge modules have a turn-on delay time of $t_{on} = 38$ ns and a turn-off delay time of $t_{off} = 70$ ns; therefore, as established in [50], a dead time period of 1 µs is taken. Furthermore, considering a maximum switching frequency of semiconductor devices of 100 kHz, the changes in the states of $s_{\phi ij}$ (from 0 to 1, or from 1 to 0) must occur in at least 11 µs.

The choice of an n-bits counter and a sampling period of T_s µs establishes a step of $T_s/2^n$ µs for each counter, i.e., the carrier signal must fit exactly in one sampling period of the controller. Another requirement is that $T_s/2^n$ µs must be a multiple of the FPGA clock (10 ns). With the choice of T_s =102.4 µs, a step of 0.4 µs results for each counter. Current sensors of the CS60-100L series have been used for the experimental measurements. Finally, the acquired results through the Tektronix TDS3034C series digital oscilloscope are analyzed through MATLAB/Simulink R2018b code.

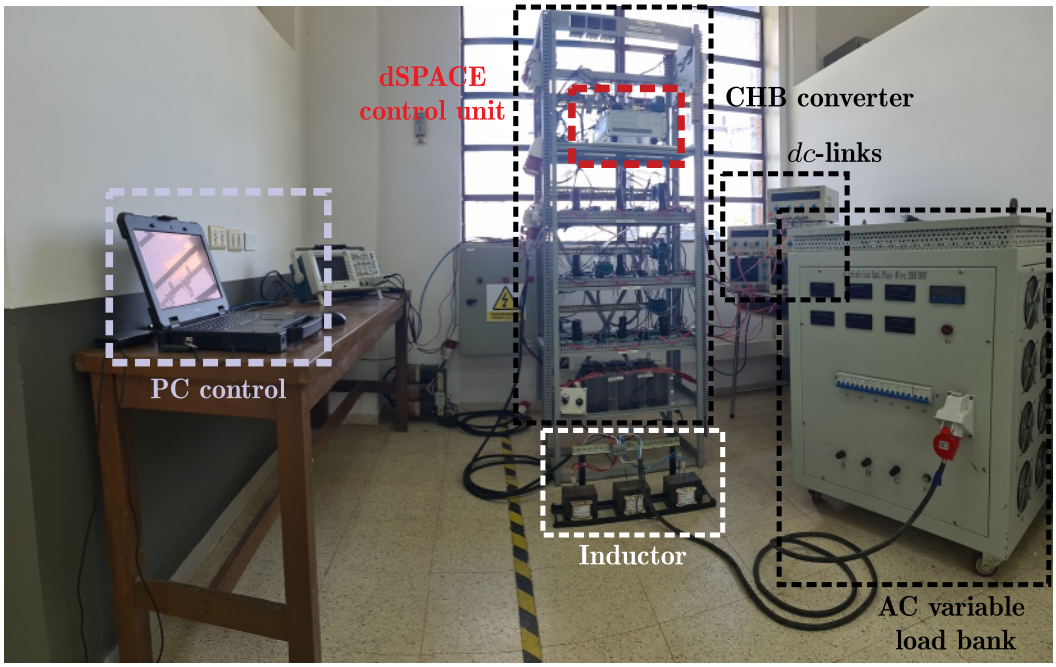
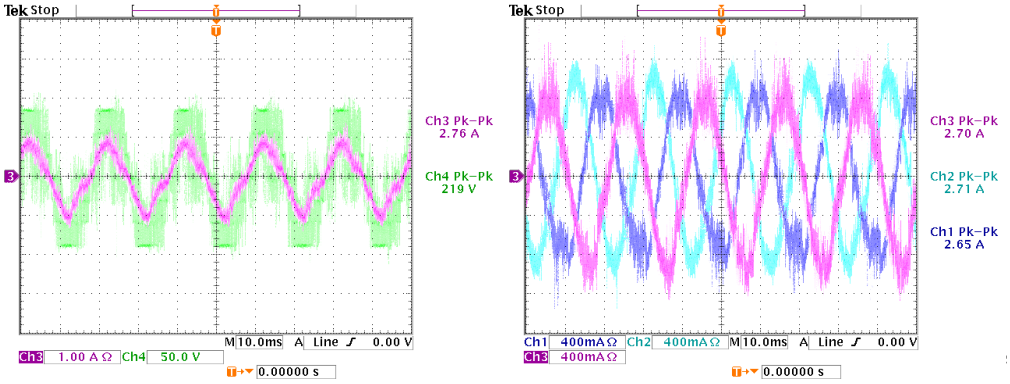


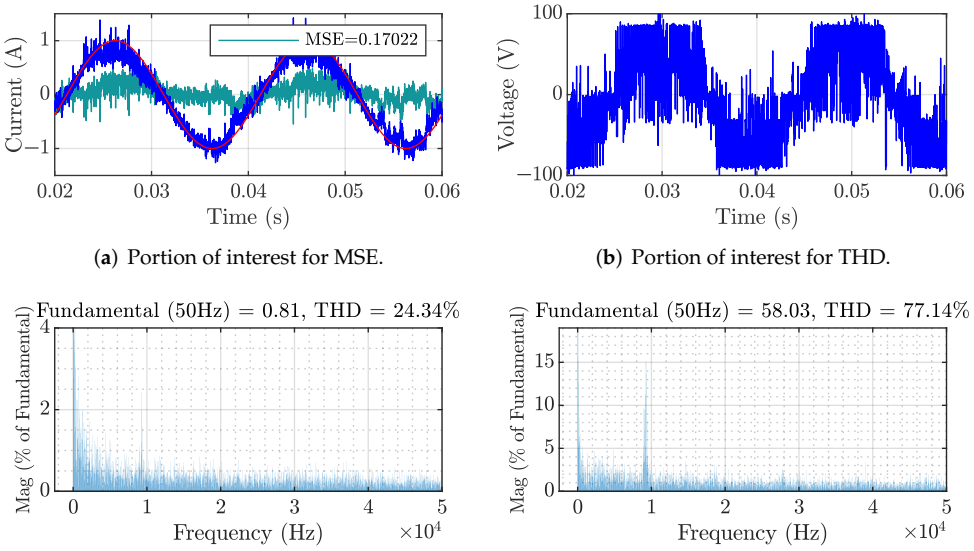
Figure 6. Experimental test equipment.

Figures 7 and 8 show the experimental results for phase a in steady-state condition and a load of 2 kW as R_L. Figure 7a shows the screenshot of the oscilloscope with the voltage and current in phase a and Figure 7b the three-phase currents. Figure 8a,b denotes a portion of samples (two cycles) used for the computation of the MSE and THD parameters. Hence, $N = 6000$ in Equations (38) and (39). Figure 8a also illustrates the dynamic behavior of the current tracking error with an MSE value of 0.17022 A. Figure 8c presents the fast Fourier transform analysis of the load current i_{La} with a THD value of 24.34%. At the same time, Figure 8d presents the fast Fourier transform analysis of the CHB output voltage v_{ca} with a THD value of 77.14%. Similar simulation results in steady-state conditions were obtained for phases b and c, and Table 5 summarizes the values obtained for THD and MSE parameters.



(**a**) Load current and CHB output voltage. (**b**) Three-phase load currents.

Figure 7. Load currents and CHB output voltage in steady-state conditions.



(**a**) Portion of interest for MSE.

(**b**) Portion of interest for THD.

(**c**) FFT analysis of i_{La}.

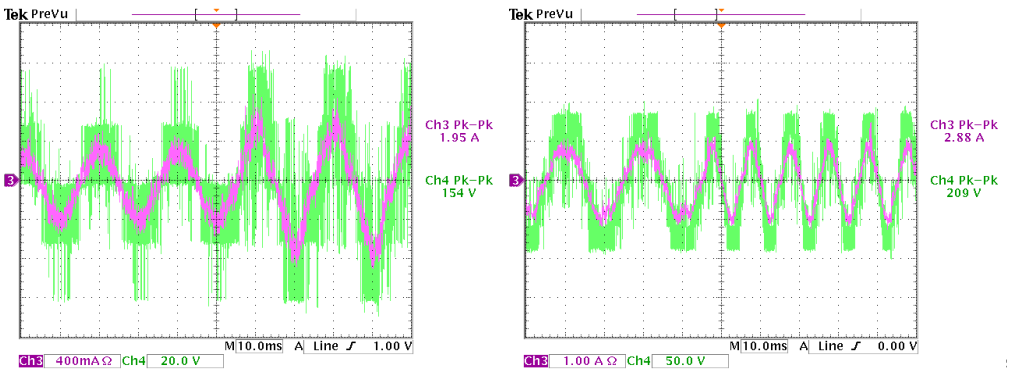
(**d**) FFT analysis of v_{ca}.

Figure 8. Experimental results for phase *a* in steady-state conditions.

Table 5. Experimental results in steady-state conditions.

Parameter	Phase *a*	Phase *b*	Phase *c*
MSE ($i_{L\phi}$)	0.17022 A	0.17697 A	0.17940 A
THD ($i_{L\phi}$)	24.34%	24.77%	25.94%
THD ($v_{c\phi}$)	77.14%	76.43%	75.27%

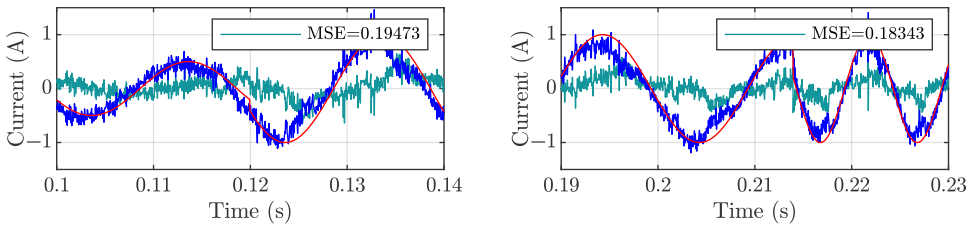
Figures 9 and 10 show the experimental results for phase *a* in transient state conditions. Figure 9a shows the transient response of the load current i_{La} and the CHB output voltage v_{ca} when a sudden change in the amplitude reference from 0.5 A to 1 A is applied. Figure 9b also presents the transient response of the load current i_{La} and the CHB output voltage v_{ca}, for the case of a sudden change in the reference frequency, from 50 Hz to 100 Hz. Figure 10a,b denotes a portion of samples (two cycles) used for the computation of the MSE parameter. Hence, $N = 6000$ in Equation (38). The current tracking error behavior for both cases is illustrated in Figure 10a (MSE value of 0.19473 A) and Figure 10b (MSE value of 0.18343 A). Similar experimental results in transient conditions were obtained for phases *b* and *c*, showing a fast dynamic response during the transient.



(**a**) when $|i^*_{La}|$ changes.

(**b**) when f^* changes.

Figure 9. Load current and CHB output voltage in transient conditions.



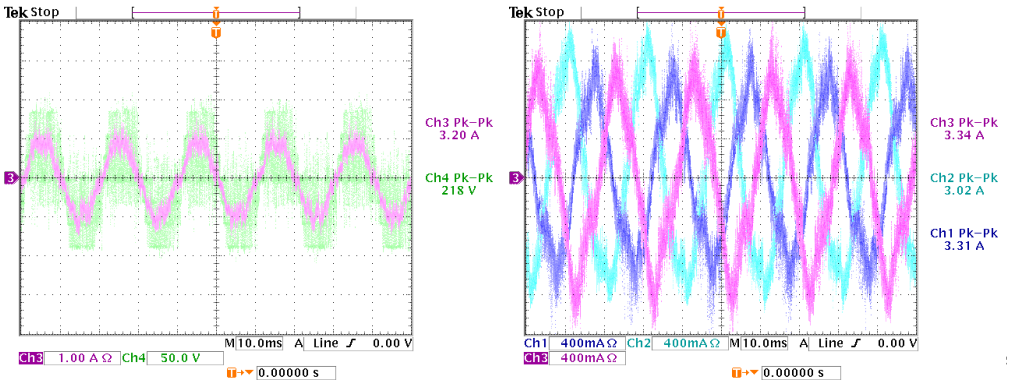
(**a**) Portion of interest for MSE when $|i^*_{La}|$ changes. (**b**) Portion of interest for MSE when f^* changes.

Figure 10. Experimental results for phase a in transient conditions.

Figures 11 and 12 show the experimental results for phase a in the presence of parametric uncertainties. Experimental tests were carried out by varying the load value (3 kW as R_L) and keeping the reference amplitude at 1 A and the reference frequency at 50 Hz. Figure 11a shows the screenshot of the oscilloscope with the voltage and current in phase a and Figure 11b the three-phase currents. Figure 12a,b denotes a portion of samples (two cycles) used for the computation of the MSE and THD parameters. Hence, $N = 6000$ in Equations (38) and (39). Figure 12a also illustrates the dynamic behavior of the current tracking error with an MSE value of 0.19080 A. Figure 12c presents the fast Fourier transform analysis of the load current i_{La} with a THD value of 29.44%. At the same time, Figure 12d presents the fast Fourier transform analysis of the CHB output voltage v_{ca} with a THD value of 103.63%. Similar simulation results in steady-state conditions were obtained for phases b and c, and Table 6 summarizes the values obtained for THD and MSE parameters.

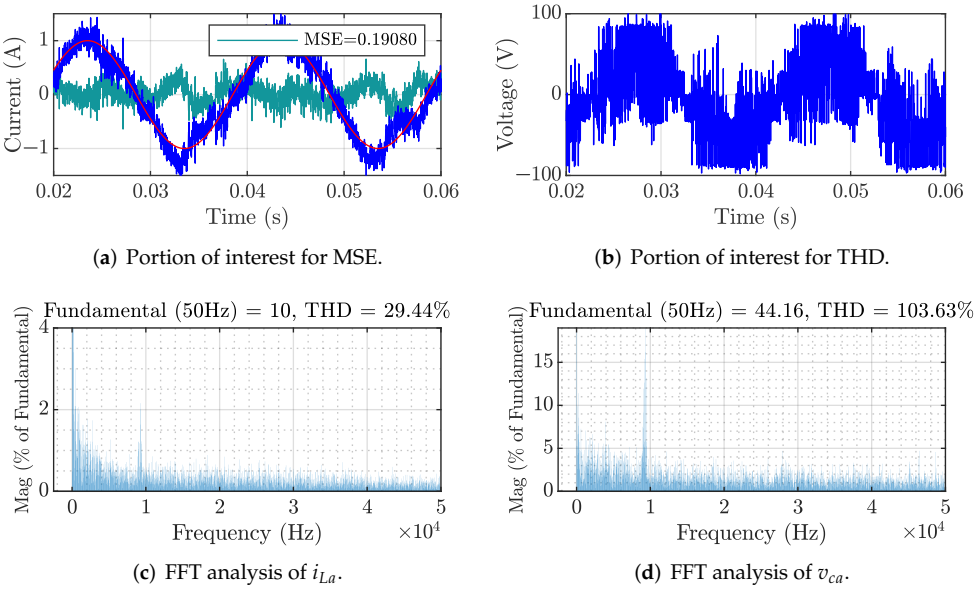
Table 6. Experimental results in the presence of parametric uncertainties.

Parameter	Phase a	Phase b	Phase c
MSE ($i_{L\phi}$)	0.14629 A	0.14954 A	0.14383 A
THD ($i_{L\phi}$)	20.37%	20.77%	21.12%
THD ($v_{c\phi}$)	103.63%	104.94%	105.47%



(**a**) Load current and CHB output voltage. (**b**) Three-phase load currents.

Figure 11. Load currents and CHB output voltage in the presence of parametric uncertainties.



(a) Portion of interest for MSE.

(b) Portion of interest for THD.

(c) FFT analysis of i_{La}.

(d) FFT analysis of v_{ca}.

Figure 12. Experimental results for phase *a* in the presence of parametric uncertainties.

5. Comparison between DTSM and FCS-MPC

For comparative purposes, simulation and experimental tests have also been added for the finite-control-set model predictive control (FCS-MPC) in combination with a modulation scheme based on PSC-PWM. This paper does not describe the design procedure for this technique, because the authors have a plan to make a detailed comparative analysis in another paper, meanwhile, interested readers may refer to [51]. First, simulation tests have been added for proportional-integral (PI) control and FCS-MPC, both with PSC-PWM. The PI control law for the load currents are:

$$u_{i[k]} = K_p e_{i[k]} + T_s K_i \sum_{j=0}^{k} e_{i[k]} \tag{40}$$

with $K_p = 21$ and $K_i = 100{,}000$, which have been obtained heuristically based on the trial and error method. The tests are carried out using the same scheme of Figure 2, replacing the DTSM controller with PI or FCS-MPC and considering the simulation parameters listed in Table 2. Tables 7 and 8 summarize the values obtained from the simulations for the THD and MSE parameters for PI control, and Tables 9 and 10 summarize the values obtained from the simulations for the THD and MSE parameters for FCS-MPC. These results show a better performance in the current tracking of the FCS-MPC compared with PI, from the point of view of the MSE parameter. Tables 11 and 12 summarize the values obtained from the experimental tests for FCS-MPC.

Table 7. Simulation results for PI in steady-state conditions.

Parameter	Phase *a*	Phase *b*	Phase *c*
MSE ($i_{L\phi}$)	0.16210 A	0.16285 A	0.16291 A
THD ($i_{L\phi}$)	4.40%	4.38%	4.40%
THD ($v_{c\phi}$)	44.42%	44.35%	44.45%

Table 8. Simulation results for PI in the presence of parametric uncertainties.

Parameter	Phase *a*	Phase *b*	Phase *c*
MSE ($i_{L\phi}$)	0.17449 A	0.17542 A	0.17515 A
THD ($i_{L\phi}$)	5.12%	5.03%	5.06%
THD ($v_{c\phi}$)	66.97%	67.07%	67.30%

Table 9. Simulation results for FCS-MPC in steady-state conditions.

Parameter	Phase *a*	Phase *b*	Phase *c*
MSE ($i_{L\phi}$)	0.06324 A	0.06241 A	0.06316 A
THD ($i_{L\phi}$)	7.43%	7.33%	7.28%
THD ($v_{c\phi}$)	40.05%	40.11%	40.19%

Table 10. Simulation results for FCS-MPC in the presence of parametric uncertainties.

Parameter	Phase *a*	Phase *b*	Phase *c*
MSE ($i_{L\phi}$)	0.25156 A	0.25151 A	0.25238 A
THD ($i_{L\phi}$)	9.33%	9.24%	9.18%
THD ($v_{c\phi}$)	42.51%	42.53%	42.47%

Table 11. Experimental for FCS-MPC results in steady-state conditions.

Parameter	Phase *a*	Phase *b*	Phase *c*
MSE ($i_{L\phi}$)	0.21820 A	0.21908 A	0.22471 A
THD ($i_{L\phi}$)	24.90%	24.77%	24.94%
THD ($v_{c\phi}$)	74.43%	74.51%	74.36%

Table 12. Experimental results for FCS-MPC in the presence of parametric uncertainties.

Parameter	Phase *a*	Phase *b*	Phase *c*
MSE ($i_{L\phi}$)	0.17106 A	0.16418 A	0.17281 A
THD ($i_{L\phi}$)	27.02%	26.96%	27.24%
THD ($v_{c\phi}$)	96.92%	95.99%	97.14%

6. Conclusions

A real-time implementation of a discrete-time sliding mode control in combination with a modulation scheme based on phase-shifted carrier modulation was applied to a seven-level CHB converter based on SiC-MOSFET half-bridge modules.

Steady-state simulation results show that DTSM control has a 39% reduction in MSE of current tracking (0.03837 A vs. 0.06293 A on average) and a 51% reduction in THD of the load current (3.54% vs. 7.34% on average), compared to FCS-MPC. Transient-state simulation results show that DTSM control has a 9% reduction in MSE of current tracking (0.09702 A vs. 0.10645 A on average) and a similar rise-time (between 0.3 and 0.4 ms), compared to FCS-MPC.

Steady-state experimental results show that DTSM control has a 22% reduction in MSE of current tracking (0.17053 A vs. 0.22066 A on average) and a slight 1% reduction in THD of the load current (24.62% vs. 24.87% on average), compared to FCS-MPC. Transient-state experimental results show that DTSM control has a 12% reduction in MSE of current tracking (0.19761 A vs. 0.22461 A on average) and a similar rise-time (between 0.4 and 0.5 ms), compared to FCS-MPC.

From the point of view of robustness, simulation and experimental results show that DTSM control is insensitive to load parameter variations in terms of THD of the load current, compared to steady-state results (simulation: 3.71% vs. 3.54%, experimental: 24.62%

vs. 20.49% on average). In addition, in terms of MSE of current tracking, experimental results confirm that the proposed controller is robust against load parameter variations (experimental: 0.14655 A vs. 0.17053 A on average). In the robustness test, a slight increase in the THD of the output voltage is observed due to the need to synthesize a low voltage to maintain the same reference current amplitude.

The differences between simulations and experimental results are mainly due to the non-modeling of the circuits that involve the signal conditioners (digital and analog), snubbers, the switching devices, as well as the electrical noises (internal and external), and the delays associated with the digital implementation.

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Abbreviations

The abbreviations used in this document are listed below:

CHB	Cascade H-bridge
DTSM	Discrete-time sliding mode
FC	Flying capacitor
FCS-MPC	Finite-control-set MPC
MPC	Model predictive control
MSE	Mean square error
NPC	Neutral-point clamped
PSC-PWM	Phase-shift carrier pulse width modulation
SMC	Sliding mode control
THD	Total harmonic distortion

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