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Advanced Control Algorithm for Three-Phase Shunt Active Power Filter Using Sliding DFT

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Abstract: This paper describes n digital control algorithm for a three-phase shunt active power filter (APF) using switching–sliding discrete Fourier transform (SSDFT). Traditionally, APF control algorithms use first harmonic detector circuits, which can be implemented using the SDFT algorithm. The classical SDFT algorithm is characterized by long-term stability issues, resulting from numerical errors. Many complex modifications to improve the stability of the SDFT algorithm have been proposed in the scientific literature. This article proposes a solution to the SDFT stability problem using the basic structure of the algorithm. The authors propose the use of the switching SDFT algorithm, where two original SDFT algorithms are implemented in parallel. Both algorithms are turned on alternately after a set period of time and reset to zero in order to reset numerical errors causing their unstable operation. Compared to the classical three-phase SDFT algorithm, the three-phase SSDFT requires only about 25% more arithmetic operations. The proposed approach has been validated using experimental tests and dramatically reduces the numerical errors. The control algorithm has been implemented using the TMS320F28379D microcontroller. The sampling method using only the internal A/D converter of a microcontroller is also presented. The article includes the experimental test results of the complete APF.

Keywords: active power filter (APF); switching reactive power compensator; sliding discrete Fourier transformation (DFT); simultaneous sampling

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1. Introduction

In the initial period of power engineering development, at the end of the nineteenth century, DC power was developed, which, however, was relatively quickly replaced by AC power. This led to the idea of three-phase circuits, which were pioneered by a Polish engineer, Michał Doliwo-Dobrowolski [1–3], among others. During the International Electrotechnical Exhibition in Frankfurt am Main, Germany, in 1891, AEG presented the first remote three-phase high voltage (15 kV) transmission line for electrical energy with a length of about 175 km, based on the concept of the AEG main constructor Michał Doliwo-Dobrowolski. In the same year, he also created a three-phase transformer and short-circuited (squirrel-cage) three-phase induction motor.

It is also worth noting that one of the world's first three-phase high voltage (10 kV) transmission lines for electrical energy was launched in 1896 in the area of the current Lubuskie Voivodeship, Poland. This line, 25 km long, connected the hydroelectric plant on the Bóbr River in Nowogród Bobrzański with the city of Zielona Góra [1,4].

To this day, electrical energy is transmitted chiefly using three-phase lines. In power stations, three-phase sinusoidal voltage is mainly produced by synchronous generators. It is vital to ensure that the output voltage closely follows the shape of an ideal sinusoidal waveform and that it is symmetrical in all phases. In the initial phases of development, the typical loads, such as light bulbs and electrical heaters, were linear loads, ensuring that the voltage and current in transmission lines remained sinusoidal. The increasing

use of such devices as arc furnaces, saturated transformers, and semiconductor switches draws non-sinusoidal currents from the power line. With further development of power electronics, the share of nonlinear receivers began to grow rapidly, and now more than 80% of electricity is converted by power electronics circuits.

As a result of this, non-sinusoidal currents and voltages appear within transmission lines and transformers. As a direct result of this phenomenon, there are increased power losses during generation and transmission of electrical energy. Additionally, non-sinusoidal currents also reduce the durability of isolation. Furthermore, it can lead to noises that affect the functioning of the power grid and its electricity consumers. As a result of non-linear loads, it is currently practically impossible to observe a sinusoidal waveform of the supply line on an oscilloscope; nowadays the waveform typically exhibits significant distortion, for example with clipped peaks of the sinusoid.

In order to eliminate these undesirable phenomena, passive filters were initially used. These filters have many undoubted advantages, such as low price, simplicity, reliability, etc. However, filters have one basic drawback: they are only well suited for stationary parameter loads. A solution that is better suited for variable workloads is an active power harmonic switching compensator, which is also called a shunt active power filter (APF) [5–20]. The APFs allow suppressing line current harmonics and reactive power.

Publications [5–21] present the historical development of the APF concept, their control algorithms, and issues related to the compensation of current and voltage harmonics. The latest literature features several papers with an overview of current harmonic compensations, compensators, and control methods. Paper [22] presents an extensive review on power electronics technologies applied to power quality improvement, as well as the main power electronics topologies for each technological solution. A large part of this article deals with the description of the APF topology. The elimination of harmonic currents by using APF is related to their dispersed distribution in the part of the network where such problems occur. However, the cost of these devices is relatively high. Therefore, research is being carried out to develop techniques for most optimal placement of APF devices to minimize their capital costs. An overview of such techniques is described in [23]. The publications [20,24–26] review several APF compensation strategies, including reference signal generation. One way to determine reference signals is to calculate the signal spectrum or individual harmonics using the discrete Fourier transform (DFT). Several low-complexity mathematical algorithms, so-called sliding transformations, have also been developed for discrete-time signal processing. The most common algorithm is sliding discrete Fourier transform SDFT [27–41]. This algorithm has operational instability due to numerical errors, which are significant when using low-precision fixed-point arithmetic. Several solutions have been proposed to improve the stability of the SDFT algorithm [28,34–40]. These solutions are associated with much greater algorithm complexity. In addition, several proposals for other solutions of sliding DFT algorithms have been proposed in the scientific literature [30,41–48]. The proposed algorithmic solutions are also highly complex.

This paper demonstrates the use of the switching sliding discrete Fourier transform (SSDFT) technique to control a shunt APF. This technique uses the classic structure of the SDFT algorithm, and the proposed innovation relates to the switching of two parallel working SDFT algorithms. Both algorithms working in parallel are turned on alternately after a set time. Then one of them is reset to clear any numerical errors causing them to run in an unstable manner. An appropriate structure for switching parallel working algorithms for three-phase APF control has been proposed. Compared to the classical three-phase SDFT algorithm, the proposed three-phase SSDFT algorithm requires only about 25% more arithmetic operations. The complexity of the algorithm is not high, and it is easy to implement using commonly available microcontrollers. The proposed algorithm has been verified by experimental tests in a three-phase APF, and the results indicate stable operation of the system.

The rest of the paper is structured as follows. Section 2 provides some general information about the APF circuit and operation. The control circuit of the APF is presented

in Section 3. Section 4 shows the experimental results for the three-phase shunt APF with proposed sliding discrete Fourier transform algorithm. Finally, Section 5 summarizes and concludes the article.

2. Circuit and Operation Description

The APF can be connected in series or in parallel with the power line. The second type, shunt APF (sometimes called: parallel APF or current-fed APF) permits compensation of the harmonics, reactive power, and asymmetries of the line currents caused by nonlinear loads.

A simplified diagram of a compensation circuit with shunt APF without feedback is shown in Figure 1. The APF has unity gain and was chosen because of its assured stability in use.

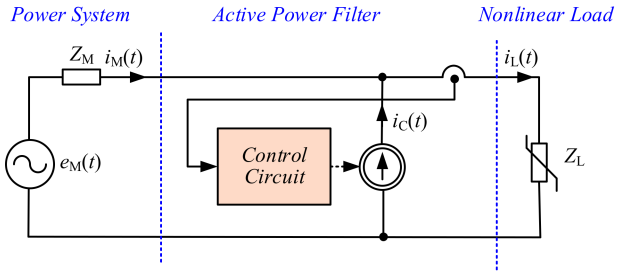

Figure 1. Block diagram of APF.

The shunt APF injects compensation current $i_C(t)$ to cancel out the power line current harmonics content and reactive power. The resulting line current $i_M(t)$ is the sum of the load current $i_L(t)$ and the compensation current $i_C(t)$:

$$i_M(t) = i_L(t) - i_C(t) \tag{1}$$

In the case of full compensation of reactive power and harmonics, the compensation current can be determined by

$$i_C(t) = i_L(t) - I_{H1} \sin(2\pi f_M t) \tag{2}$$

where: I_{H1}—amplitude of first harmonic of load current, f_M—power line frequency.

Substituting the Equation (2) into the Equation (1), the following can be obtained:

$$i_M(t) = i_L(t) - i_L(t) + I_{H1} \sin(2\pi f_M t) = I_{H1} \sin(2\pi f_M t) \tag{3}$$

As a result, full compensation of reactive power and harmonics is achieved.

The purpose of this paper is to present the project, its implementation, and the results of the APF research. In the design process, the following assumptions were made:

- Compensation of line current harmonics;
- Compensation of reactive power;
- Application of the sliding DFT in control algorithm;
- Implementation of the control system using the TMS320F28379D DSP microcontroller;
- Maximum amplitude of compensation current $i_C(t)$ is limited to 50 A;

A simplified diagram of the proposed three-phase APF compensation system is shown in Figure 2. In the APF power circuit, in order to obtain better dynamic parameters, a high transistor switching frequency f_c = 25.6 kHz was adopted, therefore fast IGBT should be used. In the APF IGBT FF100R12RT4, transistors from Infineon are used. The APF control circuit is based on the TMS320F28379D DSP microcontroller [49]. To simplify the design process, a module using the C2000 Delfino MCU F28379D LaunchPad is used [50]. In the design process, the assumption was made to maximize the use of the resources of this microcontroller with the smallest possible number of additional integrated circuits.

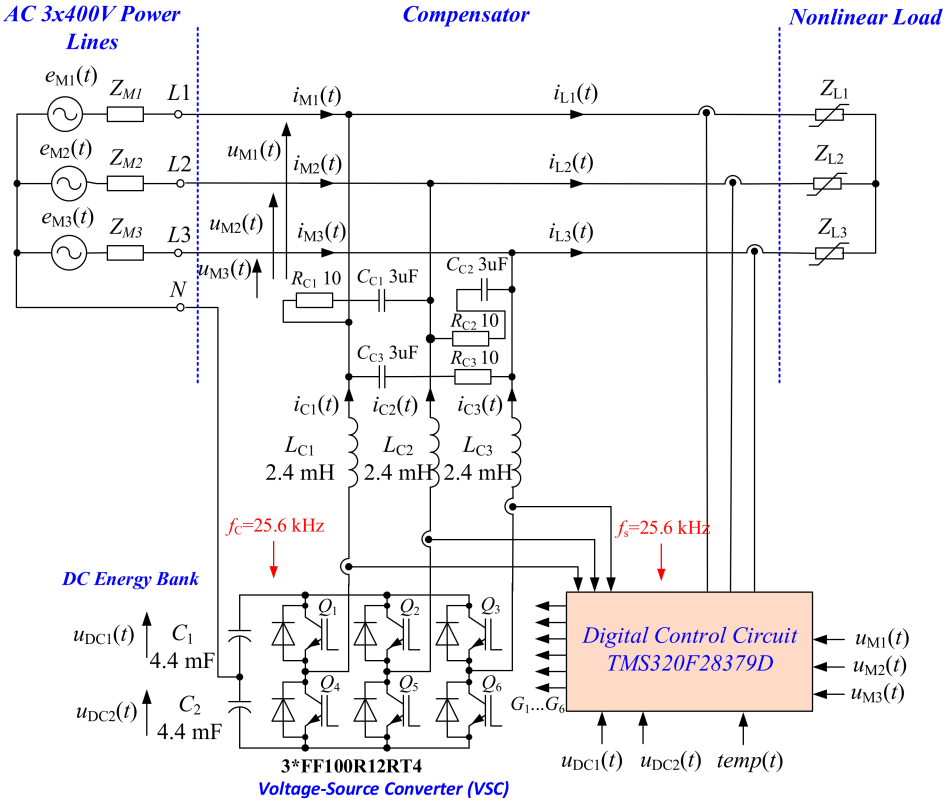

Figure 2. Three-phase active power filter compensation circuit.

The APF inverter circuit is powered from a DC bank. The DC bank contains two sets of capacitors, C_1 and C_2 (Figure 2). It was assumed that the rated operating voltages of these capacitors is equal to 400V.

The shunt APF output circuit acts as a digitally controllable current source. The output circuit is constructed using a three-phase transistor inverter as depicted in Figure 2. The output circuit acts as a voltage source inverter, and therefore it must be converted into a digitally controlled current source. In this solution the digital current controller and the output inductors L_{C1}, L_{C2}, and L_{C3} should be used. Additional filters $R_{C1}C_{C1}$, $R_{C2}C_{C2}$ and $R_{C3}C_{C3}$ are used to improve the EMC properties of the device. The main parameters of the designed APF are presented in Table 1.

Table 1. Main parameters of the APF system.

Symbol	Value
C_1, C_2	4.4 mF/450 V
L_{C1}, L_{C2}, L_{C3}	2.4 mH/50 A
C_{C1}, C_{C2}, C_{C3}	3 µF/1200 V
R_{C1}, R_{C2}, R_{C3}	10 Ω/10 W
f_c	25,600 Hz
f_s	25,600 Hz
i_{C1max}, i_{C2max}, i_{C3max},	50 A
u_{DC1}, u_{DC2}	400 V
$Q_1 \ldots Q_6$	IGBT FF100R12RT4
MCU	TMS320F28379D, 100 MHz

3. Control Circuit of APF

The simplified block diagram of a control circuit is depicted in Figure 3. It has twelve analog inputs: signals from currents $i_{C1}(t)$, $i_{C2}(t)$, $i_{C3}(t)$, $i_{L1}(t)$, $i_{L2}(t)$, and $i_{L3}(t)$, signals from voltages $u_{DC1}(t)$, $u_{DC2}(t)$, $u_{M1}(t)$, $u_{M2}(t)$, and $u_{M3}(t)$, and signal from radiator temperature sensor $temp(t)$. The current signals are generated by galvanically isolated high precision linear current sensors, the IC ACS770LCB-050B from Allegro [51]. The device consists of a precision, low-offset linear Hall circuit with a copper conduction path located near the die. The sensors are supplied by +5 V source. Signals from current sensors are connected to microcontroller input by resistor divider to reduce voltage range to 0 . . . 3.3 V.

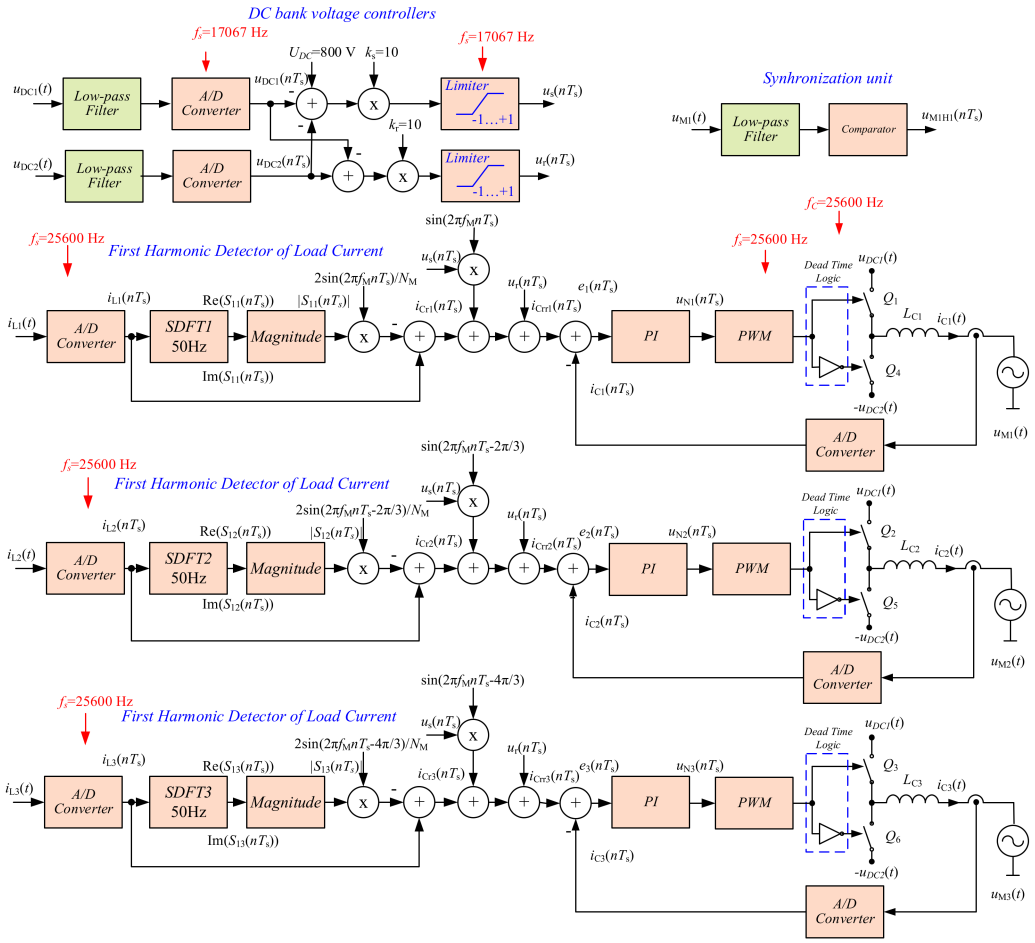

Figure 3. Simplified block diagram of APF control algorithm.

For galvanic isolation of voltage input signals the AMC1311 integrated circuits [52] are used. The AMC1311 is a precision, isolated amplifier with an output separated from the input circuitry by a capacitive isolation barrier. Its advantage is that it is highly resistant to magnetic interference. It is also important that this barrier is certified to provide reinforced galvanic isolation of up to 5 kV_{RMS} AC-cording to standards DIN EN IEC 60747-17 (VDE 0884-17) and UL1577 and supports a working isolation voltage of up to 1500 V_{RMS}. It has common mode transient immunity (CMTI) better than 100 kV/µs. So, according to its high EMC immunity, it is highly recommended for power electronics applications.

The control circuit generates signals that control the gates of the inverter transistors. It uses drivers with galvanic isolation type 2ED020I12FA from Infineon. For driver supply, DC/DC MGJD121509SC converters are used, which convert the 12 V voltage into galvanically isolated voltages of +15 V and −8 V.

A view of the APF control circuit, during the development process (during desktop testing), is shown in Figure 4.

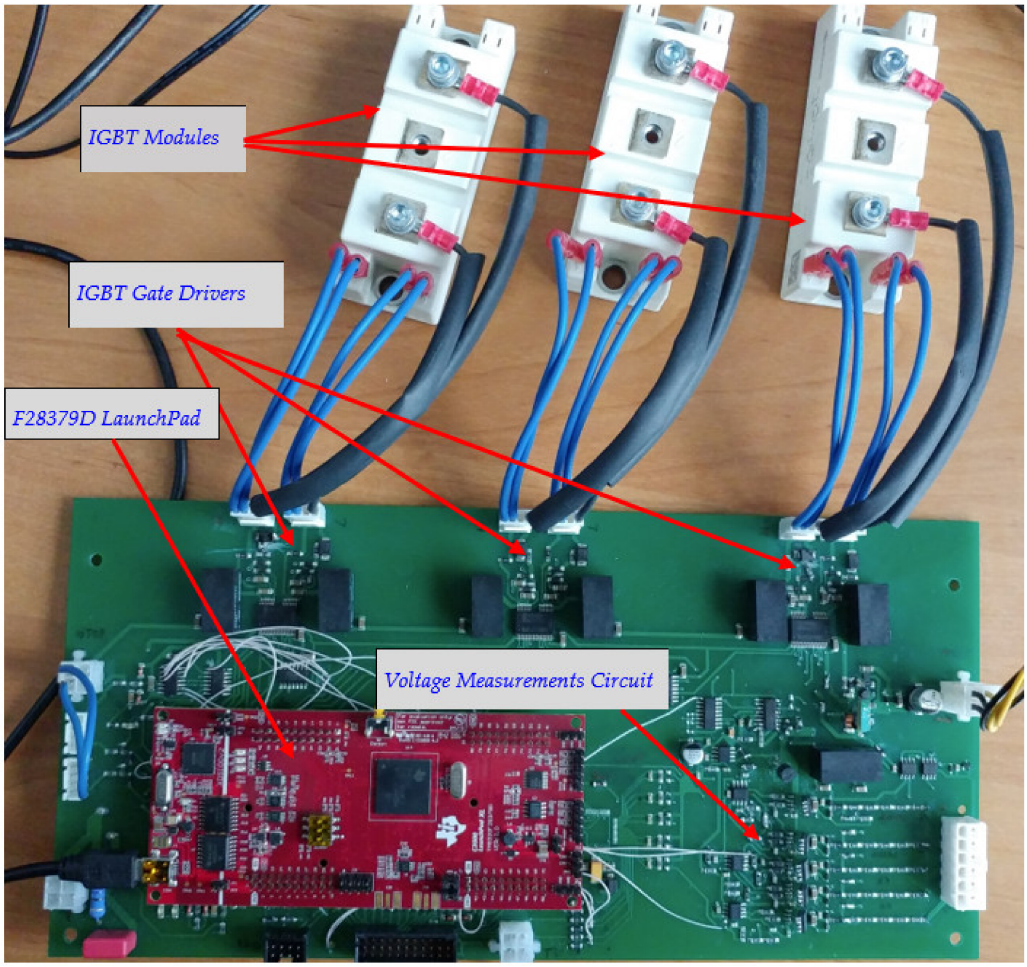

Figure 4. View of the APF control circuit during the development process (during desktop testing).

3.1. Control Algorithm

The APF system should ensure compensation of reactive power and harmonics. A simplified block diagram of the control algorithm that meets these requirements is shown in Figure 3. The control circuit consists of a few control loops.

Two digital proportional controllers are used to stabilize and symmetrize DC bank voltages and three digital output current PI controllers (Figure 3).

An algorithm based on sliding DFT is used to determine the first harmonic of the load current [26,37,38].

Due to the high stability of the power line frequency, the deviation is typically less than +/− 50 mHz [53], and the use of the phase lock loop (PLL) circuit has been abandoned. Thanks to this, low frequency oscillations associated with the reaction of the PLL system to disturbances in the supply network are avoided. Instead, a low-pass filter was applied to the $u_{M1}(t)$ voltage signal and zero-crossing detection to achieve synchronization of the control algorithm. The phase shift of the synchronization signal, which is introduced by the low-pass filter, is compensated digitally.

3.2. Digital Current Controller

The block diagram of the digital current PI controller is depicted in Figure 5. Below is the transfer function of the PI controller

$$H(z) = k_C + k_C \frac{T_s}{2T_i} \frac{1 + z^{-1}}{1 - z^{-1}} \tag{4}$$

where: k_C—controller gain, T_i—integrator time constant, T_s—sampling period.

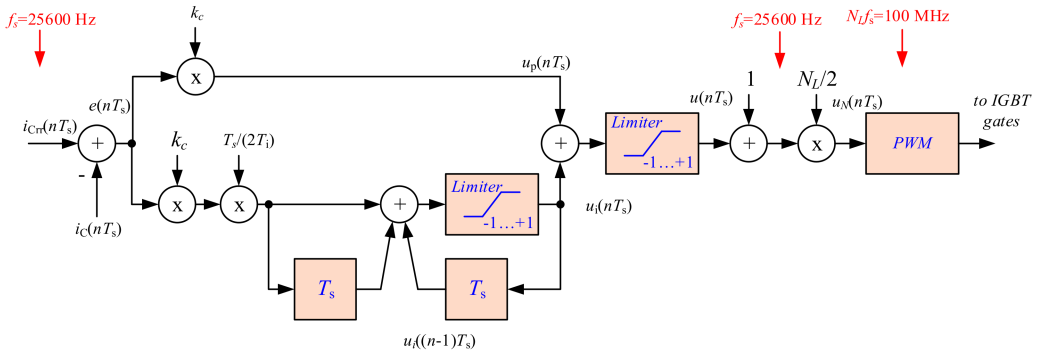

Figure 5. Simplified block diagram of digital PI current controller.

Using the controller transfer function (4), it is possible to obtain the difference equation of the control signal:

$$u(n) = k_C e(n) + \overbrace{k_C \frac{T_s}{2T_i}(e(n) + e(n-1)) + sum(n-1)}^{sum(n)} \tag{5}$$

where: $e(n) = i_{Crr}(n) - i_C(n)$ —error.

In the next step, the input signal of the PWM modulator is calculated:

$$u_N(n) = 1 + 0.5 N_L u(n) \tag{6}$$

where: N_L—number of PWM modulator states.

In Equations (5) and (6), the influence of the amplitude limiter has been neglected.

3.3. Analog Signal Sampling

As described above, the conversion of 12 analog signals is necessary to control the power circuit. Only nine signals were selected for A/D conversion, and the conversion of three supply line voltages are omitted. The signals representing currents are fast-varying, and the signals representing, e.g., DC bank voltages and temperatures are slow-varying. Hence, the best solution would be to use A/D converters with simultaneous sampling of current signals. The control circuit requires a minimum of six A/D converters with simultaneous sampling. Unfortunately, the TMS320F28379D has only four 12-bit A/D converters with simultaneous sampling [49]. Due to this, a hybrid solution was implemented in the control system that combines simultaneous and sequential sampling techniques. The sampling frequency of current signals was assumed to be equal to the switching frequency of the inverter transistors, f_s = 25.6 kHz. On the other hand, the frequency of the A/D converter operation was assumed to be twice as high. The process of sampling all signals consists in three cycles; these are described in Table 2. In summary, current signals are sampled at the f_s frequency, while voltage and temperature signals are sampled at the frequency of $2/3 f_s$ = 17,066 Hz.

Table 2. Sampling cycles.

Sampling Cycle	ADC Channel A	ADC Channel B	ADC Channel C	ADC Channel D
1	$i_{L1}(t)$	$i_{L2}(t)$	$i_{L3}(t)$	$u_{DC1}(t)$
2	$i_{C1}(t)$	$i_{C2}(t)$	$i_{C3}(t)$	$u_{DC2}(t)$
3	$i_{L1}(t)$	$i_{L2}(t)$	$i_{L3}(t)$	$temp(t)$

It is very important that the sampling process is triggered by an internal counter in the microcontroller with a constant and stable sampling rate of $2f_s$ = 51.2 kHz. This solution minimizes jitter, which deteriorates the signal-to-noise ratio [26].

The entire control algorithm is executed during the interrupt generated by the A/D converter. The four A/D converters can operate in simultaneous sampling mode with a sampling rate of $2f_s$ = 51.2 kHz. The timing diagram of data flow in the *APF* control circuit is depicted in Figure 6. The sampling period is equal to $T_s/2$ = 19.53125 µs, thus, the execution time of the interrupt program must be shorter. This time is too short to implement the whole control algorithm, so it has been divided into two parts, *Calc* 1 and *Calc* 2. The tasks for *Calc* 1 and *Calc* 2 have been divided so as to obtain almost equal use of the interrupt duration and is about 15 µs. This solution allowed for good use of the microcontroller's capabilities.

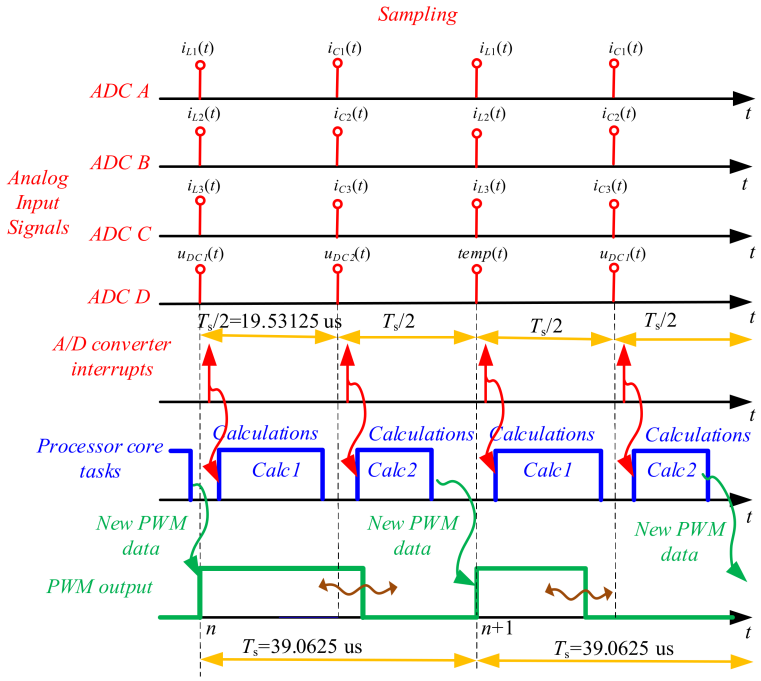

Figure 6. Timing diagram of data flow in the APF controls circuit.

3.4. Sliding DFT Algorithm

The sliding DFT (SDFT) algorithm is featured in publications [26–53]. The SDFT algorithm is useful for using in APF control circuits [26,37,38]. The principle of the algorithm is considered in publications [26–29]. For detecting the first harmonic of load current, only one signal-bin SDFT filter structure is used. The first harmonic spectral component signal of load current is calculated

$$S_1(n) = e^{j2\pi k/N_M}(S_1(n-1) - i_L(n-N_M) + i_L(n)) \quad (7)$$

where: $S_1(n)$—discrete signal representing first harmonic complex spectral component of load current, N_M—number samples per line period.

The discrete signal representing the load current first harmonic with zero phase angle between line voltage $u_M(t)$ and line current $i_{H1}(n)$:

$$i_{H1}(n) = 2/N_M|S_1(n)|\sin(2\pi 50nT_s) \quad (8)$$

Finally, compensation current signal is the result of a difference between the load current signal and the first harmonic sinusoidal signal of load current:

$$i_{Cr}(n) = i_L(n) - 2/N_M|S_1(n)|\sin(2\pi 50nT_s) \quad (9)$$

The block diagram of the circuit for calculating compensation current is depicted in Figure 7. The algorithm based on SDFT gave very good results during simulation tests and during preliminary laboratory tests. However, during long-term laboratory tests, it turned out that this approach produced a serious numerical error that causes a continuous decrease in the amplitude of the fundamental component. A significant error of the SDFT algorithm occurred after several dozen minutes of APF operation during laboratory tests. This was confirmed during additional simulation studies in Matlab.

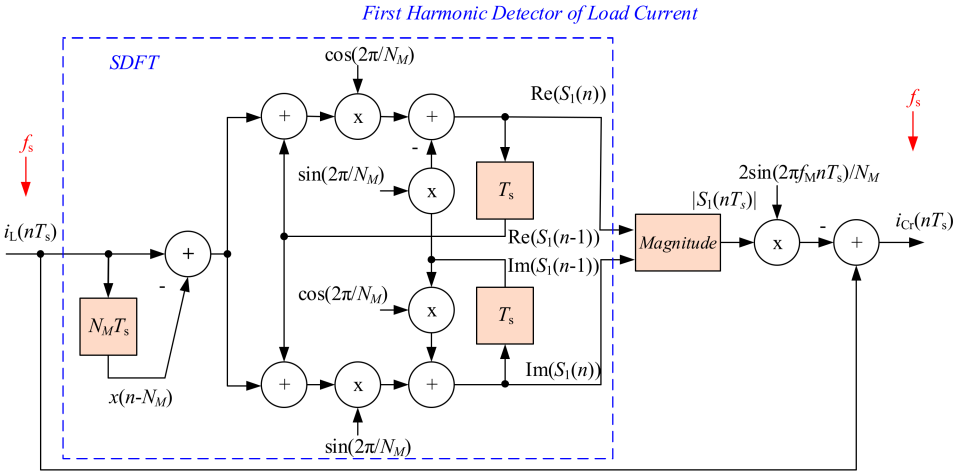

Figure 7. Block diagram of circuit for calculating compensation current.

It is possible to find many publications devoted to the stabilization method of the SDFT algorithm. For example, the works of Lyons, Duda, and many others [33–38]. However, these methods fail for the single precision floating point used in the microcontroller. The authors used their original solution to the problem. The SDFT algorithm has a response settling time equal to $N_M \cdot T_s$, i.e., one power line period. This solution consists of two SDFT circuits switched alternately. A block diagram of this switching SDFT (SSDFT) is shown in Figure 8. The working principle of SSDFT is described in Table 3.

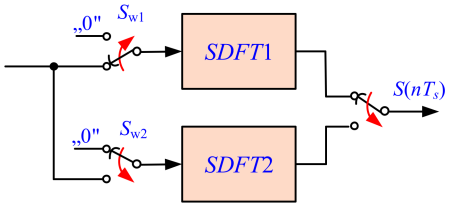

Figure 8. Block diagram of stable "switching" SSDFT.

Table 3. Working principle of SSDFT.

State Number	Line Period	SDFT1	SDFT2
1	1	I_L -> S	0
2	1	I_L -> S	I_L
3	1	0	I_L -> S
4	1	I_L	I_L -> S

The complete SSDFT concept has been thoroughly tested using simulation testing in Matlab and Psim. The simulation work confirmed that SSDFT works as intended, without a continuous increase in numerical errors. Figure 9 shows a waveform of magnitude error $|S_1(nT_s)|$ (see Figure 7) for unity input signal. Waveforms of the classical approach are shown in blue, whereas the SSDFT approach is marked in red. As can be seen in

Figure 9, the error continues to increase throughout the operation of the classical SDFT circuit, whereas the error is constrained for the SSDFT. The difference is that the SSDFT circuit is periodically reset, thanks to which the error does not grow.

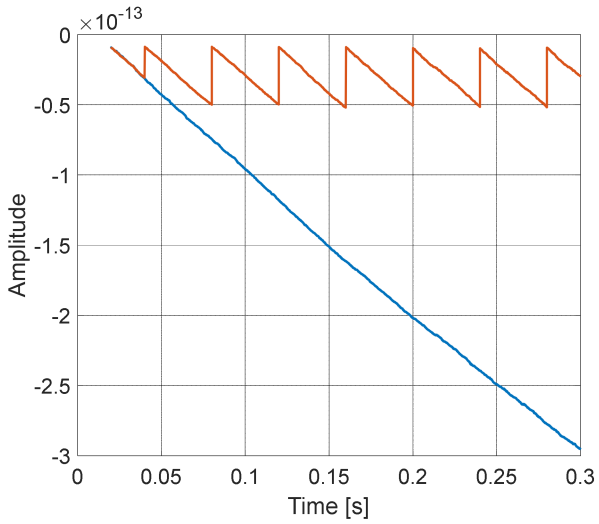

Figure 9. Error amplitudes on the output of first harmonic detector. Classical (blue curve), switching (red curve).

In subsequent tests, SSDFT implementation was tested experimentally using the TMS320F28379D microcontroller. To date, extensive experimental tests have confirmed the stability of this implementation.

The SSDFT concept was utilized in the design of three-phase first harmonic detectors. A block diagram of these detectors using a stable SSDFT is depicted in Figure 10. The principle of operation is shown in Table 4. Compared to the classical three-phase SDFT algorithm, the three-phase SSDFT requires only about 25% more arithmetic operations.

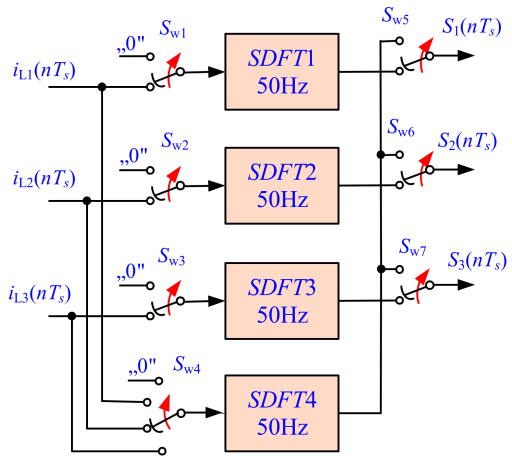

Figure 10. Block diagram of three-phase first harmonic detectors using stable SSDFT.

Table 4. The principle of three-phase SSDFT operation.

State Number	The Number of Line Period	SDFT1	SDFT2	SDFT3	SDFT4
1	8	I_{L1} -> S_1	I_{L2} -> S_2	I_{L3} -> S_3	0
2	1	I_{L1} -> S_1	I_{L2} -> S_2	I_{L3} -> S_3	I_{L1}
3	8	0	I_{L2} -> S_2	I_{L3} -> S_3	I_{L1} -> S_1

Table 4. *Cont.*

State Number	The Number of Line Period	SDFT1	SDFT2	SDFT3	SDFT4
4	1	I_{L1}	I_{L2} -> S_2	I_{L3} -> S_3	I_{L1} -> S_1
5	8	I_{L1} -> S_1	I_{L2} -> S_2	I_{L3} -> S_3	0
6	1	I_{L1} -> S_1	I_{L2} -> S_2	I_{L3} -> S_3	I_{L2}
7	8	I_{L1} -> S_1	0	I_{L3} -> S_3	I_{L2} -> S_2
8	1	I_{L1} -> S_1	I_{L2}	I_{L3} -> S_3	I_{L2} -> S_2
9	8	I_{L1} -> S_1	I_{L2} -> S_2	I_{L3} -> S_3	0
10	1	I_{L1} -> S_1	I_{L2} -> S_2	I_{L3} -> S_3	I_{L3}
11	8	I_{L1} -> S_1	I_{L2} -> S_2	0	I_{L3} -> S_3
12	1	I_{L1} -> S_1	I_{L2} -> S_2	I_{L3}	I_{L3} -> S_3

4. Laboratory Test of the APF

The described APF was built and tested experimentally. The view of the laboratory setup is shown in Figure 11. The operation of the APF has been intensively tested in the laboratory for two non-linear loads. The diagram of the loads used in laboratory test are depicted in Figure 12. The three-phase power controller with *R* and *RL* load shown in Figure 12a, and the three-phase thyristor-controlled rectifier with *R* and *RL* load is shown in Figure 12b. In both cases, positive results of the APF work were obtained.

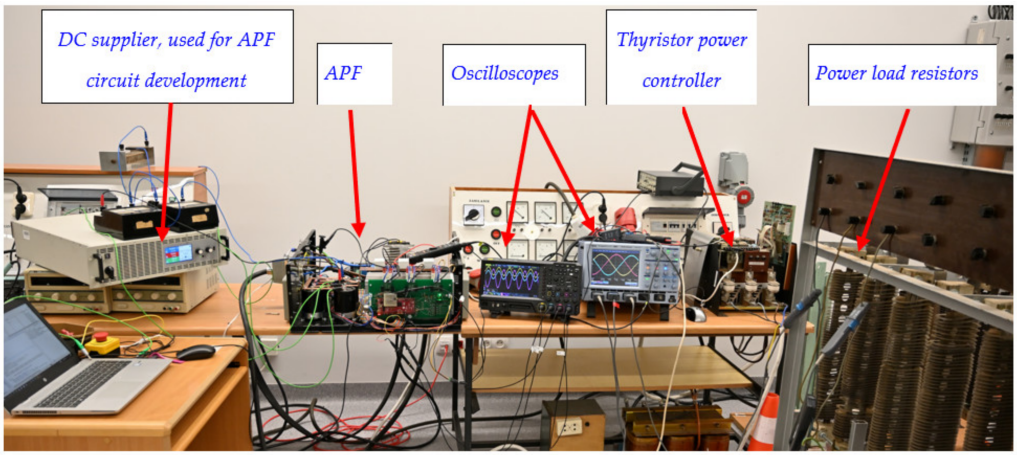

Figure 11. A view of the APF laboratory setup.

The APF control current dynamics is mainly dependent on the power inverter output circuit time constant, resulting from APF output inductance and resultant impedance of load and mains. Exemplary experimental waveforms of APF in steady state for nonlinear load with a three-phase thyristor power controller with *RL* loads are shown in Figure 13—line current $i_{M1}(t)$, compensation current $i_{C1}(t)$, load current $i_{L1}(t)$, and line voltage $u_{M1}(t)$. As can be seen in Figure 13, line voltage and current have zero-degree phase shift, signifying that the reactive power was fully compensated. When the value of load current changes rapidly, as in current $i_{L1}(t)$ in Figure 13, the APF transient response is too slow [26,54], and the line current $i_{M1}(t)$ suffers from dynamic distortion. This distortion causes an increase in harmonic content in the line current. The presence of these distortions increases the value of the total harmonics distortion ratio (*THD*) of the line current by about 10% [26,54]. The solution to this problem using a predictive control algorithm is presented separately by the author in [54]; this approach can also be combined with SSDFT.

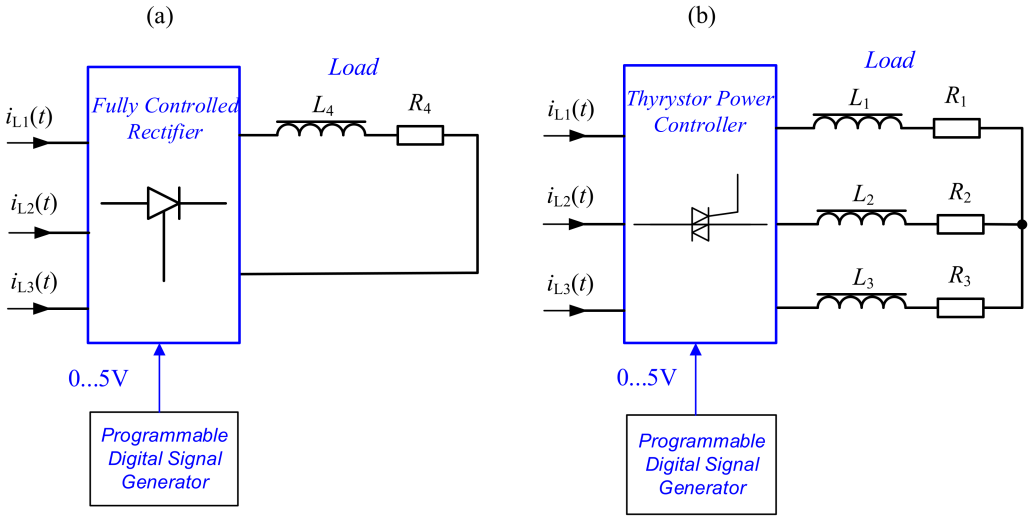

Figure 12. Three-phase nonlinear loads: (**a**) with fully controlled rectifier, (**b**) with thyristor power controller.

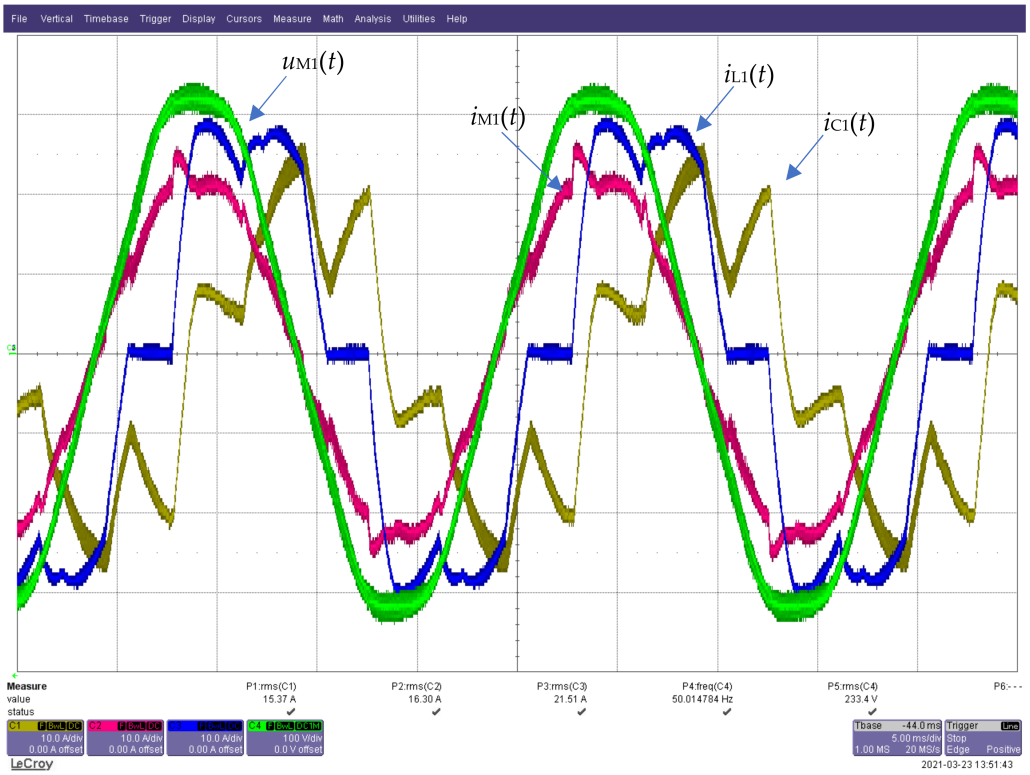

Figure 13. Exemplary experimental waveforms of the APF in steady state: line current $i_{M1}(t)$, compensation current $i_{C1}(t)$, load current $i_{L1}(t)$, and line voltage $u_{M1}(t)$.

Shown in Figures 14 and 15 are experimental three-phase waveforms of the APF in steady state for load with fully controlled rectifier. Figure 15 also shows the dynamic distortion of the line current resulting from the delay introduced by the inductors. It should be noted that, in the tested load, the rate of current changes is much higher than in typical industrial loads.

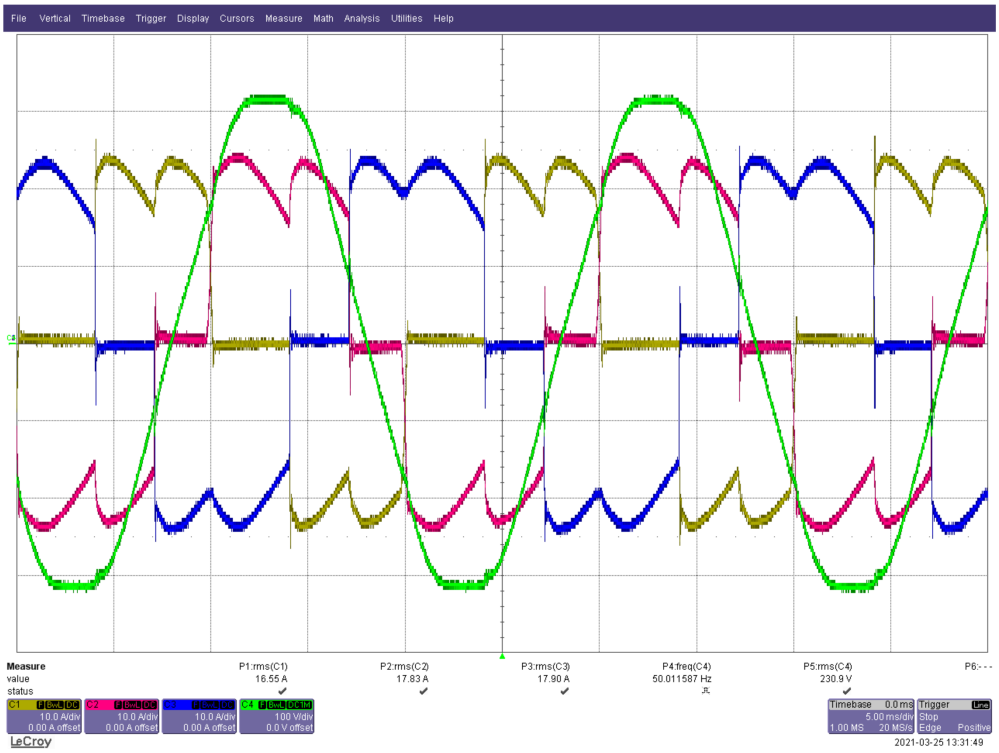

Figure 14. Exemplary experimental waveforms for fully controlled rectifier, load currents $i_{L1}(t)$ (red), $i_{L2}(t)$ (blue), $i_{L3}(t)$ (yellow), and line voltage $u_{M1}(t)$ (green).

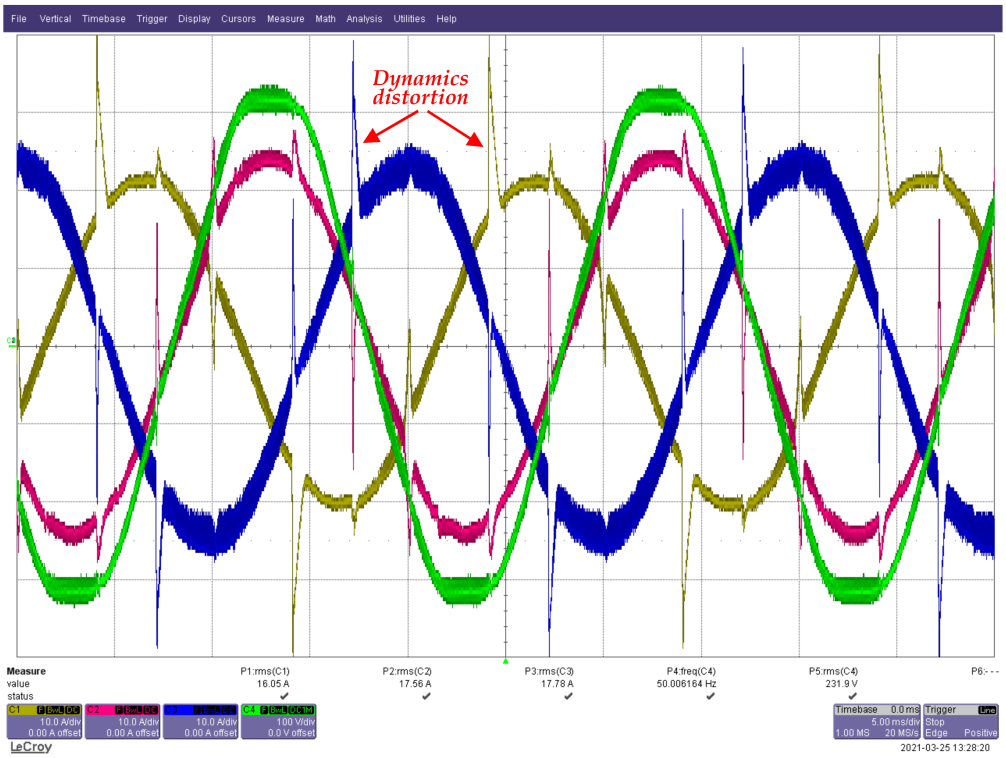

Figure 15. Exemplary experimental waveforms for fully controlled rectifier, APF is switch on, line currents: $i_{M1}(t)$ (red), $i_{M2}(t)$ (blue), $i_{M3}(t)$ (yellow), and line voltage $u_{M1}(t)$ (green).

Figure 16 illustrates the transient behavior of the APF. As you can see, from the moment the compensation algorithm is switched on to obtaining a full compensation, one period of the power supply network is needed.

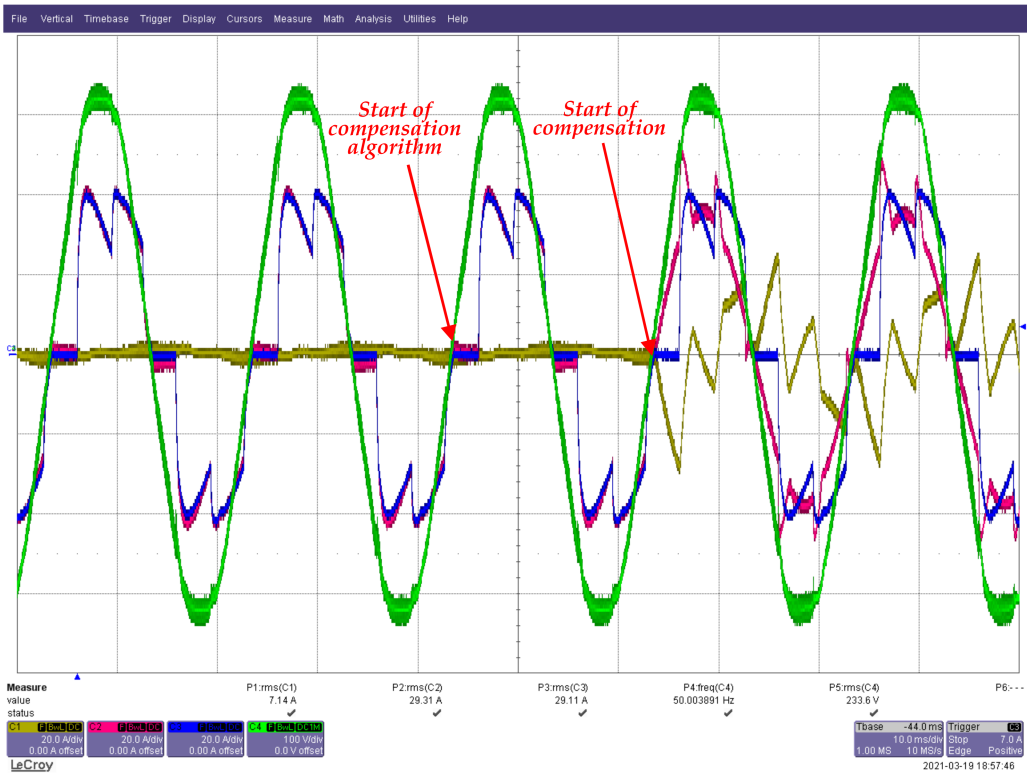

Figure 16. Experimental waveforms of the APF in transition state, line current $i_{M1}(t)$ (red), load current $i_{L1}(t)$ (blue), compensation current $i_{C1}(t)$ (yellow), and line voltage $u_{M1}(t)$ (green).

The operation of the APF for time-varying load current values is shown in a short video posted on the author's website [55]. The following waveforms are shown there: load current $i_{L1}(t)$ (magenta), compensation current $i_{C1}(t)$ (green), and line current $i_{M1}(t)$ (yellow). As you can see there, the APF performs well for changing load current.

5. Discussion and Conclusions

The presented method of the implementation of a limited number of A/D converters with simultaneous sampling was practically tested using both simulation and experimental work. This strategy allowed for a full use of the microcontroller's capabilities, without using any external A/D converters. Using the Delfino MCU F28379D LaunchPad module significantly simplified and accelerated the process of printed board design.

Use of the SSDFT algorithm allowed for agile and reliable SDFT implementation employing a microcontroller with only a single precision floating point arithmetic. The effectiveness of the whole APF was rigorously tested during extensive laboratory testing.

The design and development process of APF is one of the most difficult issues due to the fact that the power supply of the system is from the DC bank. In order for the DC bank to work, the current controllers and DC voltage controllers must work properly. In a DC system, the bank very easily obtains a voltage higher than the permissible voltage of capacitors, which can lead to their destruction, especially if the operating voltage of the capacitors is close to their maximum voltage. Overvoltage can be achieved very easily when creating and debugging a program for a microcontroller. Therefore, it is worth introducing hardware overvoltage protection.

Summing up, the most important contributions of the paper are:

- Development of a method for stabilizing the SDFT algorithm for implementation using single precision floating point;
- The three-phase SSDFT requires only about 25% more arithmetic operations than classic SDFT;

- Development of a method for sampling signals using a limited number of sample and hold systems;
- The sample and hold circuits are triggered by a hardware counter, which minimizes the jitter phenomenon.
- Design and implementation of a complex and difficult device, such as APF.

Currently, the APF is used intensively to research new control algorithms.

Future work in the area could include output *LCL* filter implementation. The *LCL* filter would permit reduction in the level of current ripples and would improve dynamic properties of the APF.

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List of Abbreviations and Symbols:

A/D	Analog-to-digital converter
APF	Active power filter
DFT	Discrete Fourier transformation
DSP	Digital signal processor
EMC	Electromagnetic compatibility
IC	Integrated circuit
PI	Proportional–integral controller
PLL	Phase lock loop
IGBT	Insulated gate bipolar transistor
MCU	Microcontroller unit
PWM	Pulse width modulation
SDFT	Sliding discrete Fourier transformation
SSDFT	Switching sliding discrete Fourier transformation
THD	Total harmonics distortion ratio
f_c	Transistor switching frequency
f_s	Sampling frequency
i_L	Load current
i_C	Compensation current
i_M	Line current
N_M	Number samples per line period
$S_1(n)$	Discrete signal representing first harmonic complex spectral component of load current
T_s	Sampling period
u_{DC1}, u_{DC1}	DC bank voltages
u_M	Line voltage
u	Current controller output signal
u_s	DC bank voltage controller output signal
u_r	DC bank difference voltage controller output signal

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