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Review

Active Damping Stabilization Techniques for Cascaded Systems in DC Microgrids: A Comprehensive Review

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Abstract: Microgrids have arisen as an alternate solution to the problem of power generation in distributed energy. Compared to ac microgrids, dc microgrids (DC MGs) are superior in terms of system efficiency, power quality, affordability, and ease of control. For the integration of renewable energy generation into microgrids, power electronic converters are required. When power electronics converters are tightly regulated, they behave as a constant power load (CPL) which exhibits a negative incremental impedance characteristic. As a result, oscillations occur in voltage response at a DC bus. To suppress the voltage oscillations in DC MGs, various damping stabilization techniques are proposed by researchers. This paper provides a comprehensive review on active damping stabilization techniques. To improve the system's stability, active damping can be implemented in three distinct zones: source-side, load side or CPL side, and intermediate level. After analyzing each zone, their merits and drawbacks have been presented. Moreover, CPL modelling, performance of cascaded DC–DC systems, the effect of the load on the source subsystem, the effect of the source on the load converter, and stability analysis are discussed. Finally, concluding remarks and future research directions are highlighted.

Keywords: DC microgrid; constant power load (CPL); CPL compensation techniques; negative impedance stability

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1. Introduction

Globally: Energy scarcity and related environmental issues are becoming major concerns. On the other hand, the ever-increasing need for electricity is putting a great strain on the present electrical supply system [1–4]. Renewable and sustainable energy development is a feasible solution to these problems. For the integration of renewable energy generation (REG) into microgrids (MGs), power converters are required [5,6]. The Microgrid Exchange Group (MEG) of the US Department of Energy (DOE) defines the microgrid as follows: "A microgrid is a group of interconnected loads and distributed energy resources within defined electrical borderlines that acts as a single controllable unit with respect to the grid. A microgrid can be connected/disconnected from the grid so that it can operate in grid-connected or island-mode" [7]. Figure 1 shows the typical DC Microgrid (DC MG) architecture, which consists of various micro sources, energy storage systems, energy conversion converters, resistive load and constant power load (CPL). A DC–DC conversion cascaded system is the most popular system in DC MGs and has been extensively employed, such as in more electric aircraft (MEA), satellites, hybrid vehicles, shipboards, electrical vehicles (EV), data centres and renewable applications in the last few decades [8–12]. The DC MG offers several benefits, including simple control, no reactive power and no frequency synchronisation issues. Furthermore, it allows natural connectivity with DC-based renewable energy sources (such as PV), electric loads (such as EVs) and energy storage systems (such as batteries) as compared to the AC Microgrid [13,14].

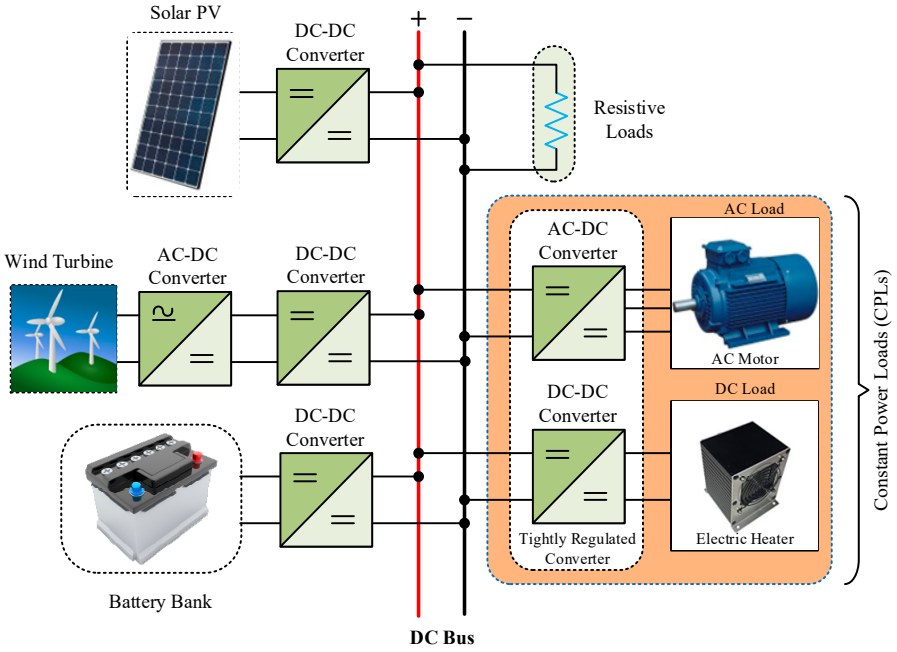


Figure 1. Architecture of DC Microgrid.

Therefore, DC MGs have been gaining attention recently. However, voltage stability is one of the issues with DC MGs [15,16].

Stable functioning of the DC MGs should be guaranteed under all situations in addition to voltage and current regulation. Points of load (POL) converters and their associated loads are often considered to be CPL (Figure 2); in particular, the power converter is tightly controlled. However, because of the negative incremental impedance (NII) characteristics of CPL, DC MGs are more prone to be unstable [17–19]. As a result, CPL causes limited cycle oscillation, reduced system damping, reduced stability margins, voltage collapse on the DC bus, and in the worst-case scenario, the entire system shutting down [16,20–22]. Source-side converters and CPLs are close to each other in some power electronic converter systems, like small power systems in EVs. In these kinds of systems, there is no need for an LC input filter because the output filter of the source-side converter can provide the same function, which reduces the noises caused by switching [18]. Figure 3 shows the typical cascaded DC system that comprises a source converter or input filter in series with a load converter. There is a significant effect on the stability of DC MGs due to the exponential rise in CPLs caused by the growing use of power electronics devices [23]. Electric motors driven by a DC/AC converter (e.g., BLDC motors), DC–DC converters feeding resistive loads and fast DC chargers for EVs that are tightly regulated are examples of CPLs [24,25]. As shown in Figure 3, individually, both the source and load converters can work properly, but the entire system may become unstable due to their impedance interaction reason, as explained in Section 3.3.

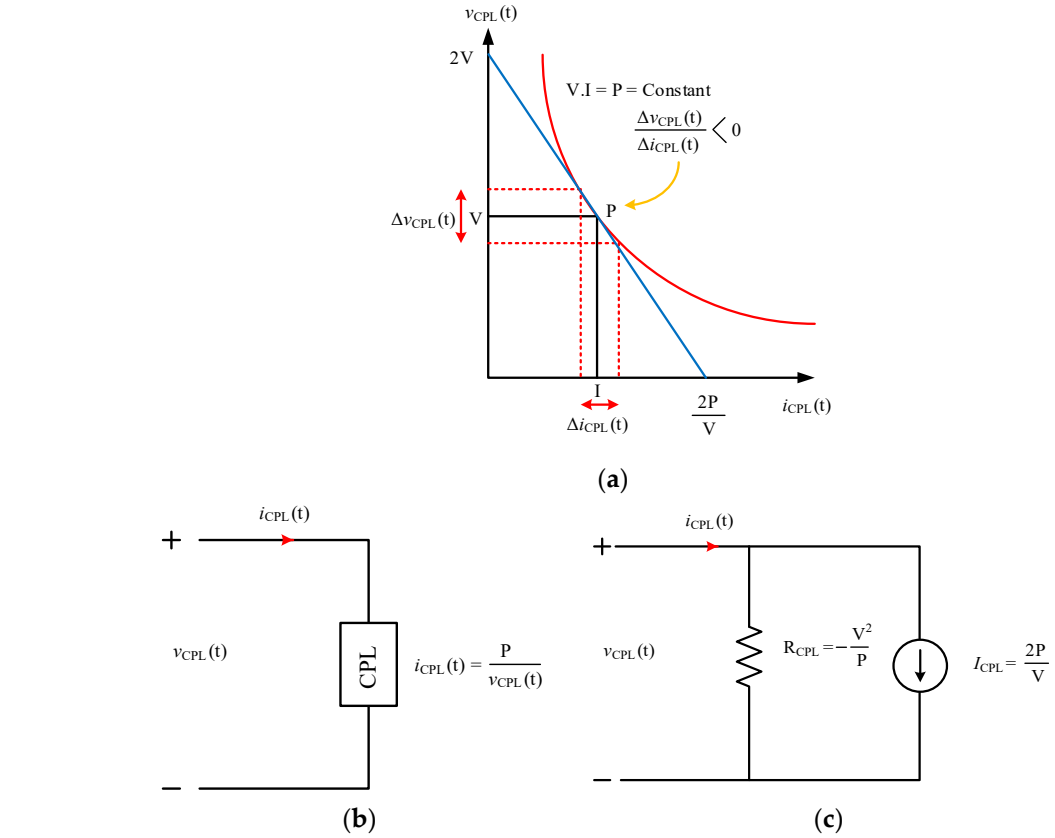


Figure 2. (**a**) Constant power load V-I Characteristics. (**b**) Large signal CPL model. (**c**) Small signal CPL model.

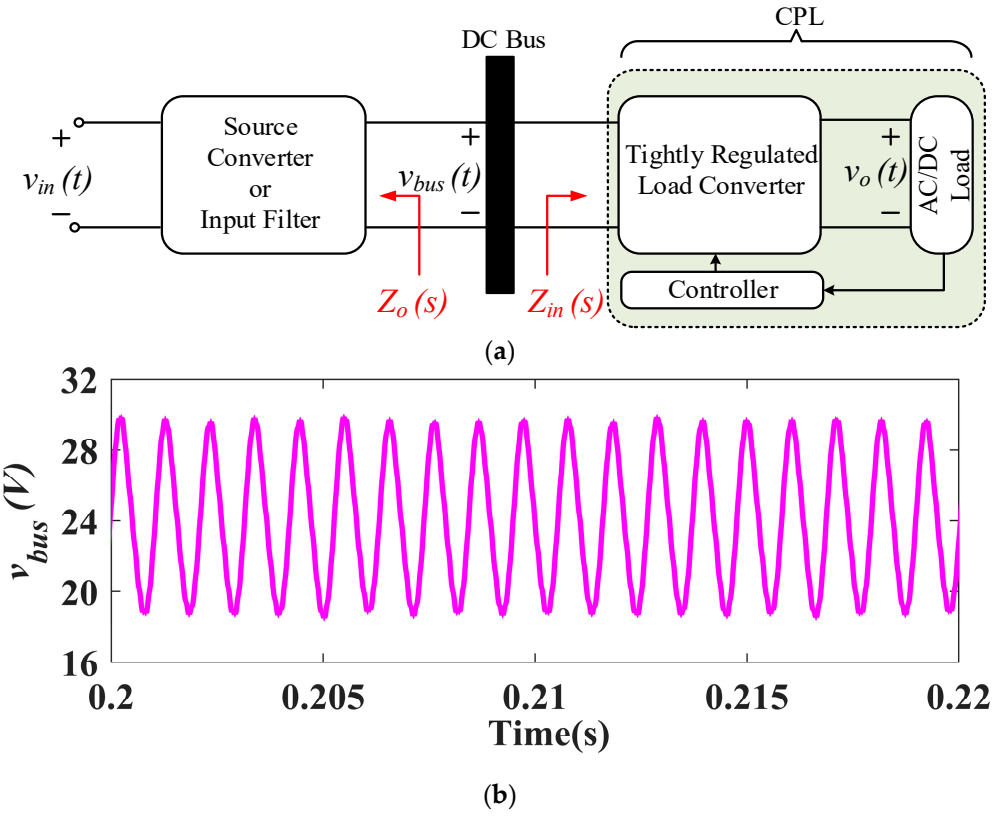


Figure 3. (**a**)A generic cascaded system feeding CPL. (**b**) Observed oscillation in DC bus voltage caused by CPL.

To improve the voltage stability of DC MGs, various schemes are proposed in the literature. These schemes are mainly categorized into passive and active damping techniques. Active compensation techniques have numerous advantages over passive damping (discussed in Section 4). Therefore, in this work, an extensive literature review is presented about various active damping methods.

The main contribution of this article can be summarized as follows:

1. This paper reviews the active damping compensation techniques for a cascaded system to stabilize the CPL effects in DC MGs. The merits and drawbacks of each scheme are elaborated.
2. Stability analysis and stability challenges of cascaded system in DC MGs have been presented.
3. The delays in digitally controlled systems and their effect on active damping control have been covered and discussed.
4. This review paves the road for further investigation on active damping control strategies and their application in DC MGs.

The structure of this paper is organized as follows. In Section 2, constant power load (CPL) modelling is presented. In Section 3, performance and stability analysis of cascaded DC–DC systems are discussed. The classification of CPL compensation techniques is reviewed in Section 4. The delays in digitally controlled systems and their effect on active damping control are discussed in Section 5. Finally, the challenges and future research directions of the DC MG, and our conclusions, are presented in Sections 6 and 7, respectively.

2. Constant Power Load (CPL) Modelling

Tightly regulated POL converters behave as CPLs, exhibiting NII and posing significant instability challenges for DC MGs [26–31]. This can be explained as follow: if a disturbance causes the load voltage to fall below the voltage value of the stable point, the load current will be greater than the load current at constant power of the load, resulting in the discharge of the filter capacitor. As a result, the load current will rise to maintain the power constant but the voltage will fall.

In the absence of a proper control mechanism, the voltage will drop to zero and the current will increase to infinity during a transient or any small disturbance [18,32–35]. Similarly, if the voltage of the source converter varies (i.e., decreases), the duty cycle of the load converter increases to control the voltage, which implies that the current increases to maintain constant power [36–42]. As a result, in the absence of a properly designed feedback control, the DC bus voltage tends to oscillate, resulting in limit cycle behaviour with an unstable equilibrium point. Limit cycles are undesirable because they create stress on the switches of the source power converters. This stress causes temperature to rise, limiting the lifespan of the switching components, or it may completely damage it [43,44]. Furthermore, the CPL model introduces nonlinearity to the system [45]. Figure 2a depicts the CPL V-I characteristic. As shown in Figure 2b, the current $i_{CPL}(t)$ through the CPL terminal can be expressed as (1)

$$i_{CPL}(t) = \frac{P}{v_{CPL}(t)} \tag{1}$$

For a given operating point $(I = P/V)$, the CPL small signal model can be approximated by a straight line tangent to the curve as seen in Figure 2a, which is computed as (2)

$$i_{CPL}(t) = -\frac{P}{V^2} v_{CPL}(t) + \frac{2P}{V} \tag{2}$$

Equation (2) can be represented as negative resistance $(R_{CPL} = -V^2/P)$ with a parallel constant current source $(I_{CPL} = 2P/V)$ as shown in Figure 2c.

3. Performance and Stability Analysis of Cascaded DC–DC Systems

Several research works have been conducted to solve cascaded system stability issues by establishing the source and the load subsystems at the DC bus interface of the POL converter. Figure 3a depicts the equivalent system divided into two subsystems, the source subsystem and the load subsystem, both of which are considered to be independently stable. $G_{vg,S}$ and $G_{vg,L}$ are the source and load converter input-to-output voltage stable transfer functions, respectively. Since switched-mode regulators are connected in cascade to form DC-distributed power systems (DPSs), the load converter modifies the dynamics of the source converter and vice versa (explained in Sections 3.1 and 3.2) [21,46]. As a result, both subsystems suffer from reduced relative stability margins [21]. Therefore, this section explains how cascading two DC–DC converters affect each one's dynamic performance. A generic cascaded system feeding CPL is depicted in Figure 3a, where, $Z_i(s)$, $Z_O(s)$, v_{in} v_o and v_{bus} are the input impedance of the load converter, the output impedance of the source converter, the input voltage of the source converter, the output voltage of the load converter and the DC bus voltage, respectively. The conventional model of a single-load-single-source that may be used to study the effect of negative input impedance on cascaded systems is depicted in Figure 3 [21]. The input-to-output voltage relationship for such a system may be defined as

$$\frac{\hat{v}_o}{\hat{v}_{in}} = \frac{G_{vg,S}\, G_{vg,L}}{(1+T_S)(1+T_L)(1+T_m)} \tag{3}$$

T_S and T_L are the voltage loop gains of the source and load converters, respectively. $T_m = Z_o/Z_{in}$ is called minor loop gain and plays an important role in the stability analysis of the overall system. Connecting the converters adds more poles to the system and affects its dynamic response [47] due to the added component $(1+T_m)$ in (3). Each converter in the cascaded system will work individually if $T_m \ll 1$. T_m is critical for guaranteeing both the stability and dynamic performance in order to assure the cascaded system's stability.

3.1. The Effect of the Load on the Source Subsystem

Because of the loading influence, the loop gain of the source converter is modified when the load converter is involved. This can be seen in [21,48].

$$T_S^L = \frac{T_S}{1+T_m(1+T_S)} \tag{4}$$

where T_S is the control loop gain of the source converter and T_S^L is the load-affected control loop gain. The source converter's dynamic performance will be maintained even if $Z_o \ll 1$ $(\text{i.e.}, T_S^L \approx T_S)$

3.2. The Effect of the Source on the Load Converter

According to [47,49], the source converter has an impact on the load converter's dynamics.

$$T_L^S = T_L \frac{1+T_m}{1+\frac{Z_o}{Z_{in\_ol}}} \tag{5}$$

where Z_{in_ol} represents the open-loop input impedance of the load converter, T_L represents the control loop gain of the load converter, and T_L^S represents the source-influenced control loop gain of the load. Similarly, the load dynamic performance will be maintained even if $Z_o \ll 1$ $(\text{i.e.}, T_L^S \approx T_L)$.

3.3. Impedance Interaction and Stability Analysis

Power electronics converters are often designed and tested separately using just resistive loads [49-51]. When an individually designed power converter is cascaded to other circuits, the stability properties of closed-loop converters designed as stand-alone devices

are no longer preserved, and the system may exhibit unanticipated dynamic responses [52-58]. Oscillation in DC bus voltage caused by CPL is depicted in Figure 3b. Because of impedance interactions between the source-side and load-side converters, voltage response oscillations occur.

This impedance interaction occurs when the POL converter's control loop gain and bandwidth are sufficiently greater than those of the source-side converter [58-60]. As a result, regardless of its terminal voltage, the CPL draws constant power from its feeder. The bode diagram of $Z_{in}(s)$ and $Z_o(s)$ shown in Figure 4 is plotted by using the parameter given in [61]. Figure 4 can be used to analyse if the amplitude curve of $Z_o(s)$ and $Z_{in}(s)$ intersects at a frequency where the phase angle difference is greater than 180°, the system is unstable. In order to ensure the stability of the cascaded system, at least one of the inequalities in (6) should be satisfied.

$$\begin{cases} \left|\frac{Z_o}{Z_{in}}\right| \le 1 \\ \varphi(Z_o) - \varphi(Z_{in}) \le 180° \end{cases} \quad (6)$$

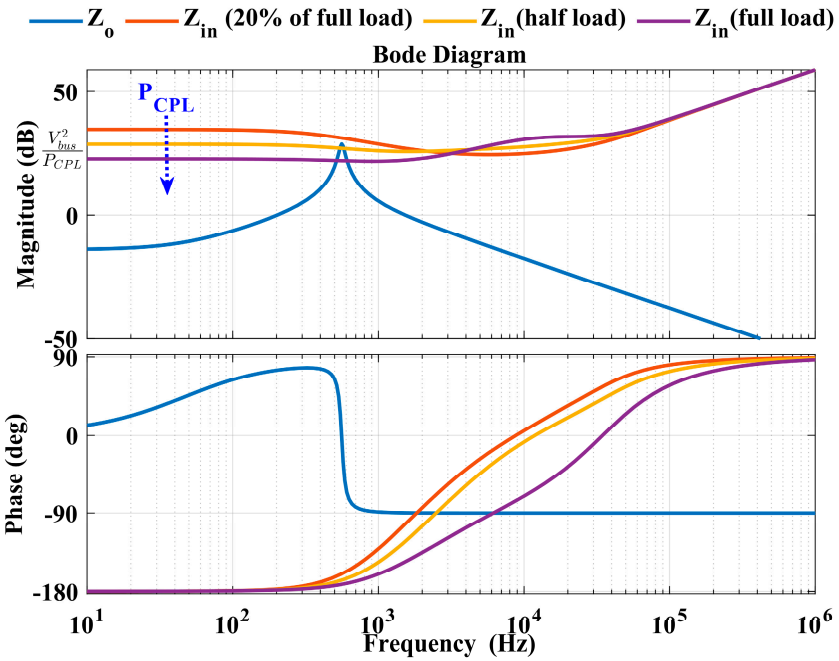


Figure 4. Bode diagram of $Z_{in}(s)$ and $Z_o(s)$ with different loading [61].

Various methods have been developed for small-signal stability analysis of the power electronics cascaded system. These methods are based on eigenvalue methods or impedance-based methods [40,62–64] For detailed systematic analysis, the eigenvalue technique is preferred because it has advantages in finding oscillation modes and instability roots of system variables. However, to carry out a stability analysis, it is necessary to have access to all system data, which varies between suppliers and may be kept private [62,63]. In an impedance-based method, a system is separated into a source equivalent and a load equivalent, and system stability is assessed using the Nyquist criteria by comparing the impedance ratios of the source and load. As a result, it is appropriate for examining how different subsystems interact as well as for converter design. The impedance-based method also includes a black box capability, which makes it a powerful tool for online stability study or when system information is unavailable [62]. However, some impedance stability criteria may result in a conservative design due to their conservatism, which makes it difficult to determine the oscillation modes and participation components [40,61–63]. As can be seen in Figure 5, numerous stability criteria for DC systems based on forbidden regions

for the minor loop gain have been presented in the literature to assess overall system stability. These include the Middlebrook Criterion [46] and its different extensions, such as the gain and phase margin (GMPM) criterion [65], the opposing argument criterion [65–68], the energy source analysis consortium (ESAC) criterion [69,70] and the maximum peak criterion (MPC) [71,72]. The system stability can be predicted with the help of impedances, by observing the nature of $Z_o(s)/Z_{in}(s)$ using the minor loop gain criterion [73–76]. The cascaded system is stable according to the minor-loop gain criterion, if and only if the Nyquist contour of $Z_o(s)/Z_{in}(s)$ does not encircle the critical point (−1, j0) in the complex plain. Figure 6 is plotted by using the parameter given in [61]. From Figure 6, it can be observed that a Nyquist plot of $Z_o(s)/Z_{in}(s)$ does not encircle the critical point (−1, j0) at 20% of full load, but it does encircle at half of the full load and at full load.

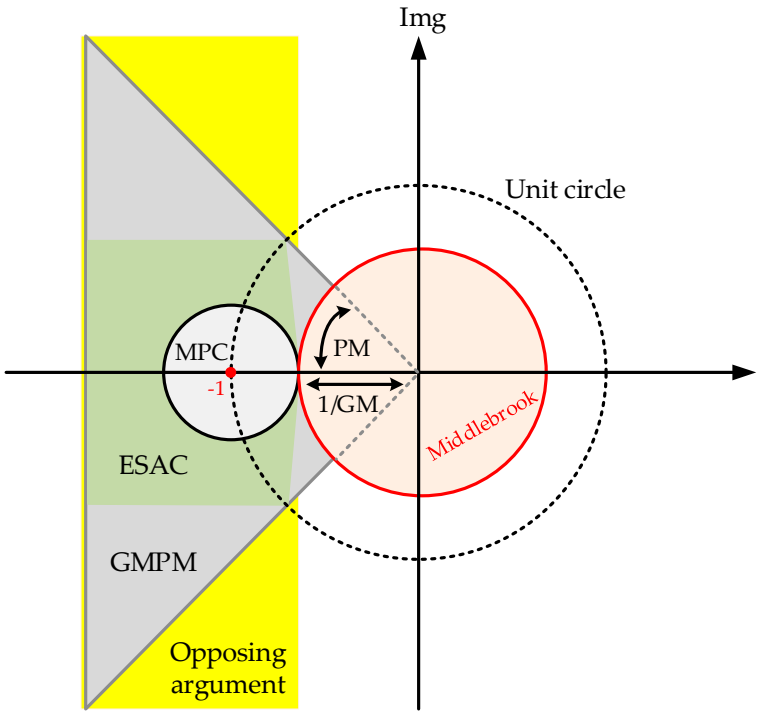


Figure 5. Stability Criteria boundaries [65].

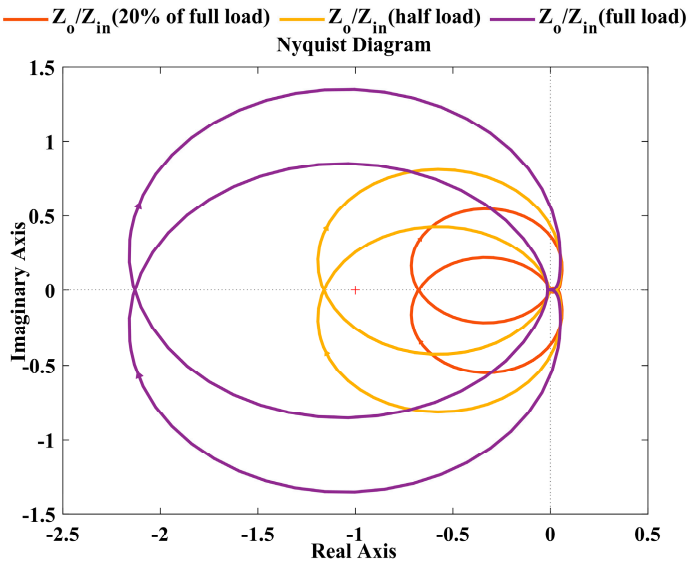


Figure 6. Nyquist diagram of $Z_{in}(s)$ and $Z_o(s)$ with different loading [61].

This stability can be ensured by reshaping either $Z_o(s)$ or $Z_{in}(s)$ using the proper stabilization techniques (i.e., passive damping or active damping).

4. Classification of CPL Compensation Techniques

To compensate for the instability caused by CPL connected in cascaded systems, numerous methods have been proposed. These methods essentially rely on two basic concepts: passive damping and active damping as shown in Figure 7.

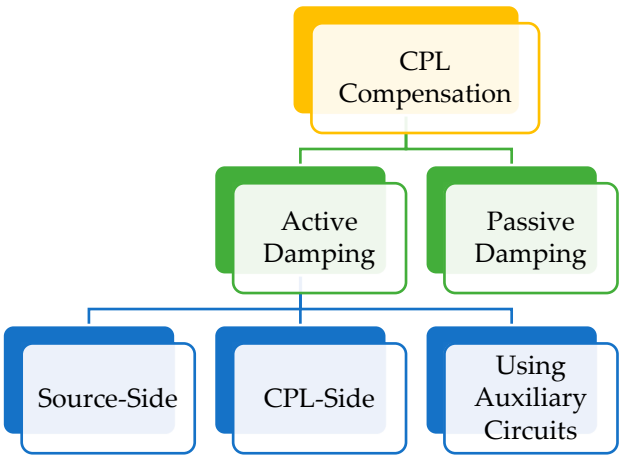


Figure 7. Broad classification of CPL compensation techniques.

4.1. Passive Damping

The damping of a system can be improved by adding passive elements such as a resistor (R), an inductor (L) and a capacitor (C), or any combination of these [77,78]. Different types of passive damping stabilization techniques have shown in Figure 8. Adding passive damping to a system is a simple way to increase its damping. The improvement is due to changes in either the cascaded system's source converter's output impedance or the load converter's input impedance. To stabilise the system, the authors of [29] proposed an RC parallel damper to overcome the NII of the CPL and the input LC filter. Moreover, the rise in rated voltage increases the chance of capacitor failure in passive damping [79].

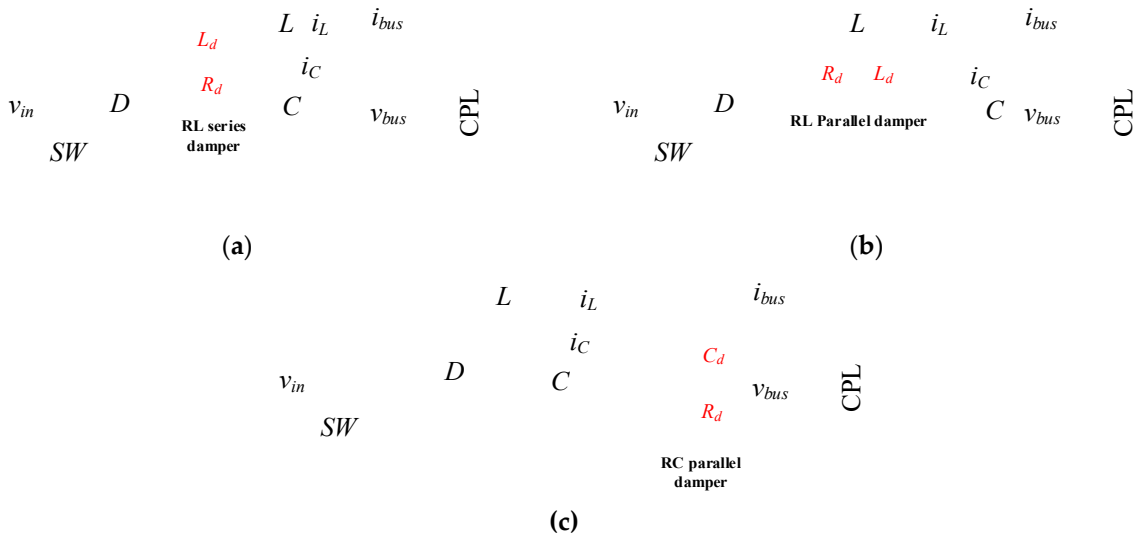


Figure 8. Passive damping stabilization techniques: (**a**) RL series damper; (**b**) RL parallel damper; (**c**) RC parallel damper [77].

The addition of the damping resistor is a very reliable and effective way to achieve stabilization, but it increases losses in the system and so reduces its energy efficiency [80]. The loss-free resistance (LFR) [81] method may be utilised to decrease power dissipation. The disadvantage of LFR is that it increases the system's size, complexity and expense.

4.2. Active Damping

Active damping approaches have been developed to address the shortcomings of passive damping. To meet the stability criterion, active damping modifies the control loop of the source side or load side converters [82–84]. To increase system stability, active damping can be applied at three distinct zones: source side, CPL side and intermediate level.

4.2.1. Source Side Active Damping

This section summarises source-side active damping implementation via modification in the control loops of the source converter. Active damping at the source side modifies the output impedance of the source converter so that the impedance stability criterion is fulfilled. The major advantage of this method is that the system can be stabilized without affecting the load performance. A virtual RC damper across the converter capacitor is adopted to mitigate the oscillations [24]. Furthermore, an adaptive parallel virtual resistance based on a proportional-derivative load current feedback strategy has been proposed in [53] to mitigate the oscillations. In the controller, the inductor current is used to damp oscillations by creating a virtual resistance in series with the converter inductor [85]. In [86], active damping on the source side has been used to dampen out the oscillation caused by CPLs and the transfer function is given in (7), which is derived from Figure 9. R_{eq} is the equivalent resistance of R and $R_{CPL.}$(i. e. , $R_{eq} = R||R_{CPL}$)

$$\frac{V_o(s)}{d(s)} = \frac{V_{in}}{LCs^2 + \left(\frac{L}{R_{eq}} + R_L.C\right)s + \left(1 + \frac{R_L}{R_{eq}}\right)} \tag{7}$$

By computing the locations of the pole of (7), we can easily investigate the DC–DC buck converter's stability.

$$P_1, P_2 = \frac{-\left(\frac{L}{R_{eq}} + R_L.C\right) \pm \sqrt{\left(\frac{L}{R_{eq}} + R_L.C\right)^2 - 4LC\left(1 + \frac{R_L}{R_{eq}}\right)}}{2LC} \tag{8}$$

From (8), it can be said that if $R_{eq} < 0$ and $|R_{eq}| > R_L$, the system will become unstable because the pole will lie in a right-half plane (RHP). Therefore, one of the LC filter parameters, i.e., R_L, L, or C, should be correctly modified to fulfil (9).

$$\frac{L}{|R_{eq}|} < R_L.C \tag{9}$$

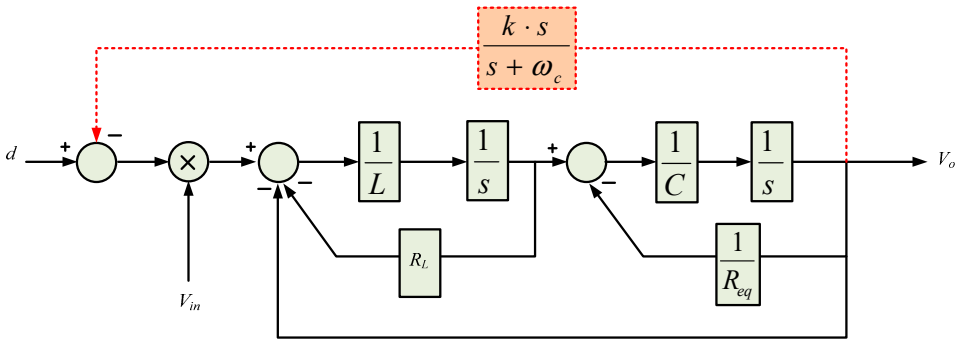


Figure 9. Block diagram representation of the buck converter with CPL [86].

The transfer function given in (10) is derived by implementing the proposed method in [86] as

$$\frac{V_o(s)}{d(s)} = \frac{V_{in}}{LCs^3 + \left(LC \cdot \omega_c + \frac{L}{R_{eq}} + R_L.C\right)s^2 + B \cdot s + \left(\frac{R_L}{R_{eq}} \cdot \omega_c + \omega_c\right)} \quad (10)$$

where

$$B = \left(\frac{L}{R_{eq}} \cdot \omega_c + R_L.C \cdot \omega_c + \frac{R_L}{R_{eq}} + 1 + k\right) \quad (11)$$

We can observe in Figure 10 that by varying damping parameters ω_c, poles of the $V_o(s)/d(s)$ move towards the negative real axis of the s-plane and ensure the stability of the cascaded system [86].

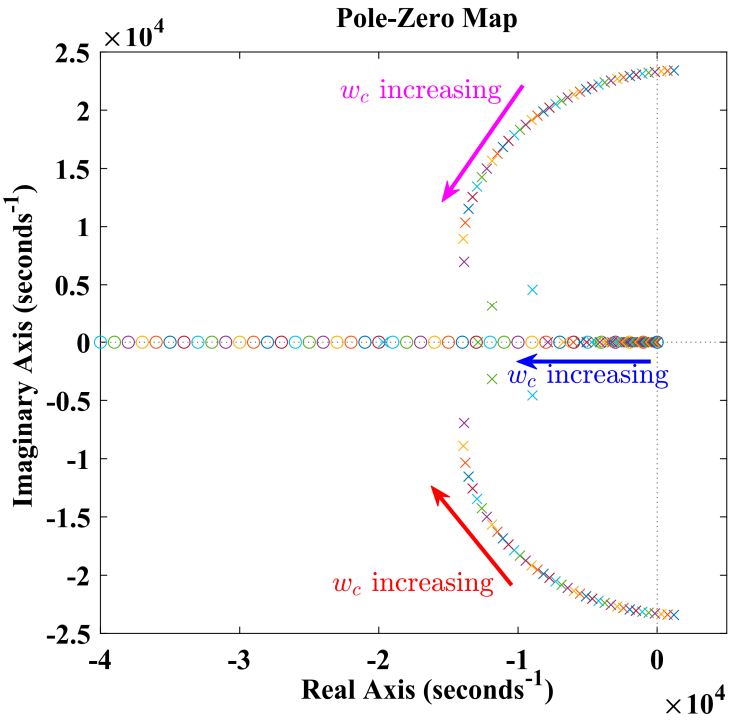


Figure 10. Pole-zero maps of $V_o(s)/d(s)$ given in (10) [86].

Case study on Source Side Active Damping

In [87], as shown in Figure 11, applying the AD stabiliser loop (red colour) behaves like a dependent voltage source V_{AD}, as shown in Figure 12a. Convert the Thevenin circuit, which includes the voltage source V_{AD} in series with the impedance $R_L - L$, to the appropriate Norton equivalent circuit, as illustrated in Figure 12b. As indicated in Figure 12b, dependent current source I_{AD} is moved between nodes x and y, first from node x to node z, then to node y, as illustrated in Figure 12c. The parallel dependent current source to the voltage source can be ignored [24]. Convert the dependent current source to an impedance Z_{AVRC} (Figure 12c) as illustrated in Figure 12d. Referring to Figure 12c, the expression for virtual impedance can be expressed as follows:

$$Z_{AVRC} = \frac{\hat{v}_o}{I_{AD}} = \frac{R_{eq}V_{Tr}R_L}{K_{AD}V_{in}sC} + \frac{LR_{eq}V_{Tr}}{K_{AD}V_{in}C} = \frac{1}{sC_{AVC}} + R_{AVR} \quad (12)$$

$$K_{AD(min)} = \frac{V_{Tr}}{V_{in}} \cdot \frac{C_{AVC(min)} \cdot R_{eq} \cdot R_L}{C} \quad (13)$$

where $C_{AVC(min)} = C_{min} - C$ in that C_{min} is calculated by using (9).

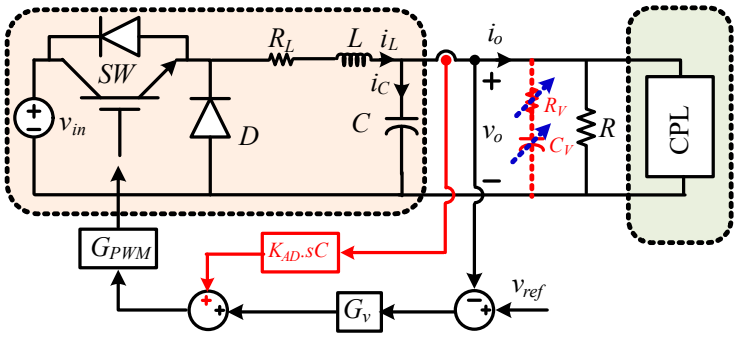


Figure 11. AVRC methods given in [87].

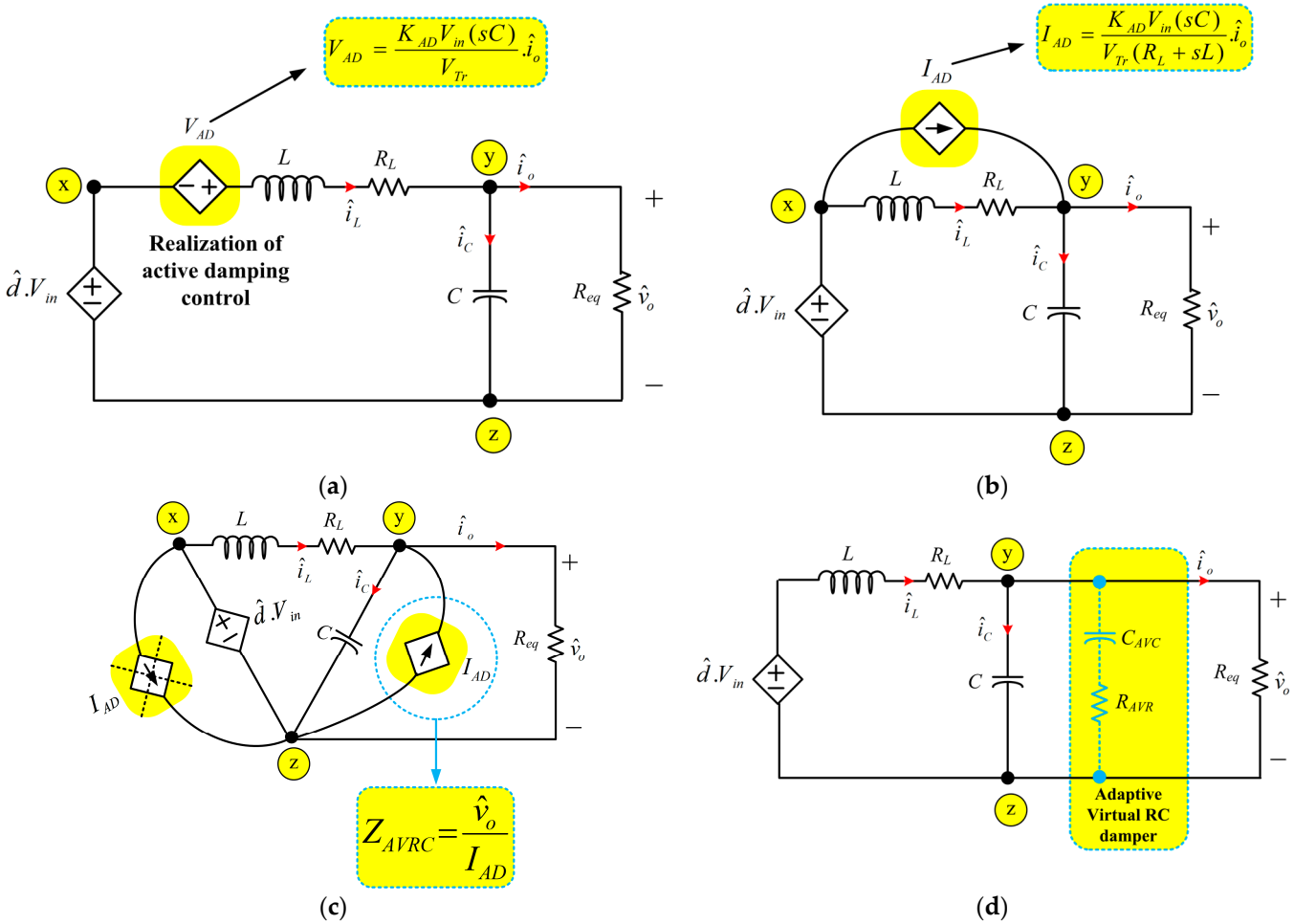


Figure 12. (**a**) Small-signal averaged model; (**b**) analytical interpretation of (a); (**c**) analytical represented in Figure 12b; (**d**) physical idea of AVRC damping [87].

The method reported in [87] is easy to tune, adaptive, has less settling time, includes digital delay and provides robust stabilization. However, effectiveness is affected by frequency switching. By using the parameter given in [87], the simulation result has been shown in Figure 13. Up to $t = 0.5s$, there is no AD control, so oscillation occurs in the output voltage. At $= 0.5s$, AD is enabled and oscillation dampened out, during the change in input voltage and constant power load at $= 1s$ and at $= 1.5s$, respectively. It is observed that in Figure 13, the given method in [87] provides robust stabilization.

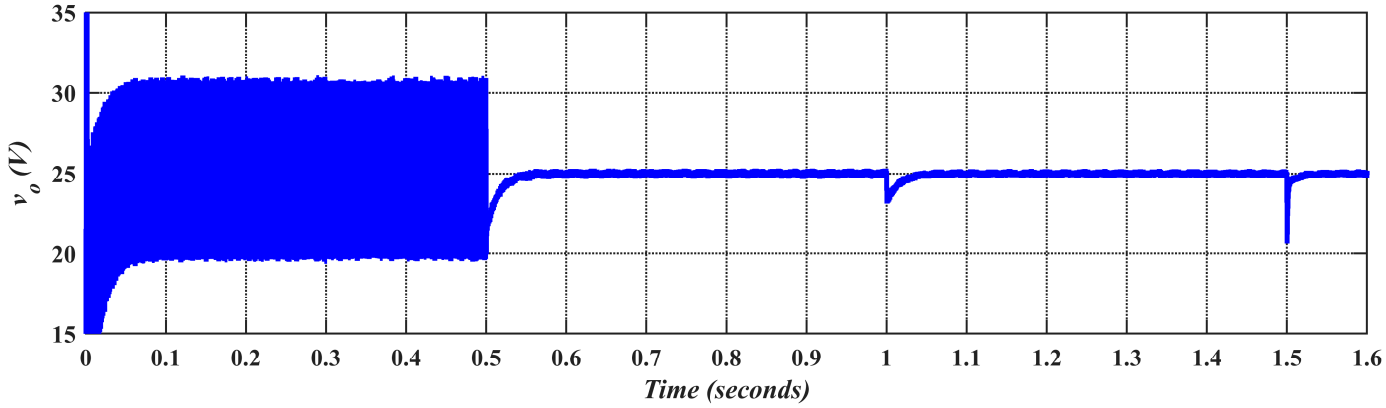
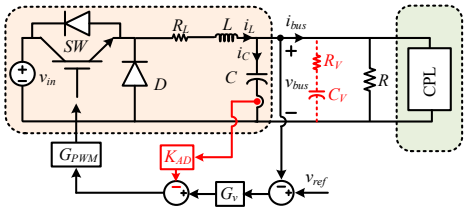
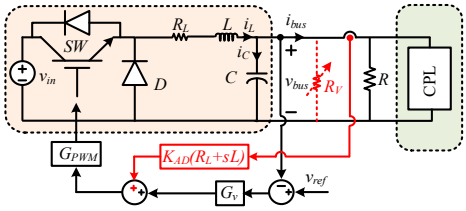
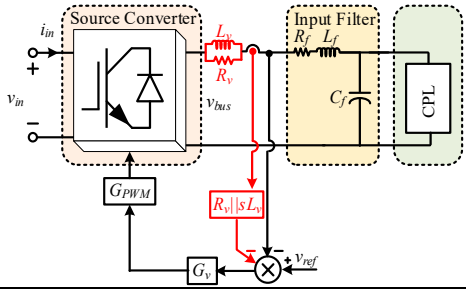
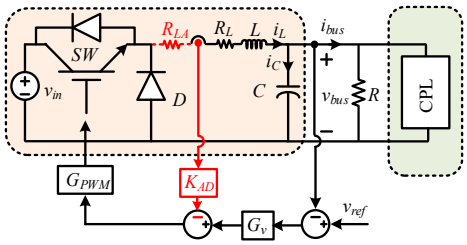
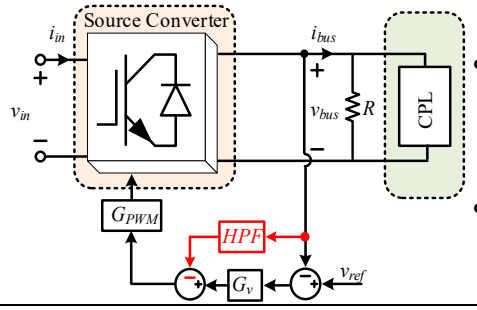
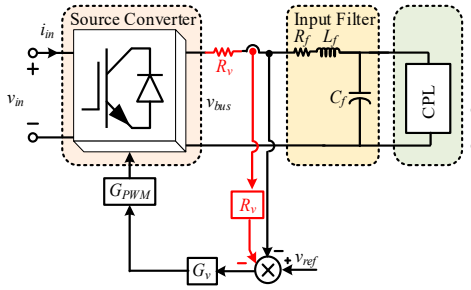
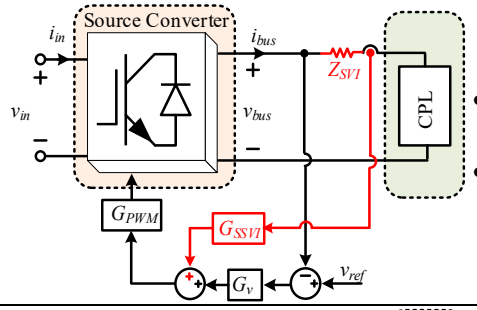
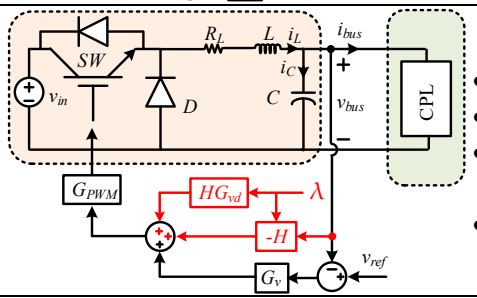
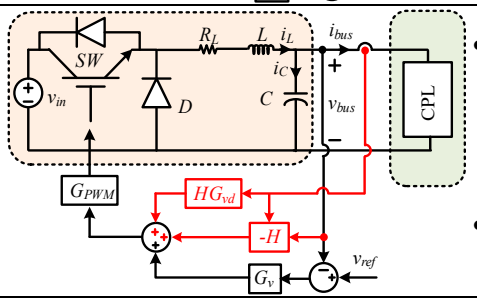
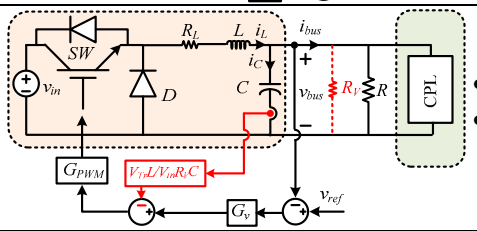


Figure 13. Output voltage using parameter given in [87].

The salient features and drawbacks of source-side CPL compensation techniques are summarized in Table 1. Some authors are considering that when CPLs are connected to nearby source-side converters, there is no need for an LC input filter [24,52,85,86]. This is because the source-side converter's output filter can provide the same function as the LC input filter, which reduces the noise caused by switching. Moreover, some authors are considering a cascaded DC system that comprises a source converter and input filter in series with a load converter [60,88]. Both types of structures are presented in Table 1.

Table 1. Summary of source-side CPL compensation techniques.

Ref.	Stabilization Structure	Salient Features	Drawbacks
[24]		• It is easy to set the control parameters, and the control strategy is simple. • Higher efficiency and reliability	• Increasing the virtual capacitance value will adversely affect the speed of system dynamic responses. • The controller's gain is not adaptable to system changes.
[52]		• It features an intrinsic control parameter for self-tuning. • No change in the hardware.	• This may interfere with the main control objectives. • Effectiveness is affected by frequency switching. • Difficult to implement due to the PD controller.
[60]		• It exhibits a superior dynamic response to external disturbances. • Fast response.	• It is incapable of adapting to changes in system parameters.
[85]		• Easy to tune the control parameter. • It is tested on all three basic DC–DC converters.	• It has poor dynamic and transient performance. • It is incapable of adapting to changes in system parameters. • Energy efficiency is slightly reduced.

[86]		• The particle swarm optimization algorithm was used to find the best values for the active damper's parameters. • Root locus was used to place system poles appropriately.	• The calculation is complex to find the value of damping elements. • No experimental results are provided. • Computation delay and PWM delay are not included.
[88]		• Preserved stability. • The performance of the CPL is not degraded.	• To make the virtual resistor to effectively dampen the unstable LC input filter resonant oscillation, the closed-loop control bandwidth of the source-side converter must be greater than the LC input filter resonant frequency. • The LC input filters of the different CPLs should have different resonant frequencies.
[89]		• It Improves source converter performance. • The experimental results are provided.	• It cannot handle multiple load converters. • Poor transient characteristics.
[90]		• Preserved stability. • Less settling time. • It reshapes the output impedance of the source converter. • It can handle multiple loads.	• It is incapable of adapting to changes in system parameters. • Lacks speed and robustness.
[91]		• This approach can be applied to both minimum and non-minimum phase converters employing linearized feedback control techniques. • It reshapes the output impedance of the source converter.	• Poor transient performances. • Long settling time.
[92]		• Fast response. • Optimized virtual resistance is inserted.	• Effect of R_L is neglected. • The controller gain is not adaptable to system changes.

4.2.2. CPL Side Active Damping

When the source side of a cascaded system consists of an LC filter or an uncontrolled converter with no closed loop, active control strategies on the source side cannot be employed to increase system damping [88]. In such circumstances, there are two options for CPL compensation: one is CPL side compensation and the other, use of an active shunt damper between the feeder and the load subsystems. Active damping techniques based on CPL side compensation will be reviewed in this section. To meet Middlebrook's stability criteria, these techniques adjust the CPL control loops' input impedance by injecting a compensating current or power. The main issue with this strategy is that the dynamics of the extra compensating loop may disrupt the primary control loop of CPL, resulting in a trade-off between load performance and stability margin. On the other hand, this method is beneficial because CPL itself is used to reduce the negative impedance instabilities. In [93], authors proposed a CPL-side active damping control in which virtual impedance is inserted to damp the oscillation caused by CPL. The cascaded system used in this work is shown in Figure 14. The output impedance of the LC input filter is given in (14) and input impedance can be expressed as (15), where $y_{in\_ol}(s)$, $G_{vd\_ol}(s)$, D, $T(s)$ are the open loop input admittance, control-to-output voltage transfer function, duty cycle and loop gain of the voltage loop of the CPL converter, respectively.

$$Z_o(s) = \frac{sL_f + R_f}{s^2 L_f C_f + sR_f C_f + 1} \tag{14}$$

$$Z_{in}(s) = \left(\frac{y_{in_{ol}}(s)}{1 + T(s)} - \frac{P_{CPL}}{V_{bus}^2} \cdot \frac{T(s)}{1 + T(s)} \right)^{-1} \tag{15}$$

where

$$\begin{cases} y_{in\_ol}(s) = \dfrac{sC_L D^2 + \dfrac{D^2}{R_{Ld}}}{s^2 L_L C_L + s\dfrac{L_L}{R_{Ld}} + 1} \\ T(s) = G_C(s) * G_{PWM} G_{vd\_ol}(s) \\ G_{vd\_ol}(s) = \dfrac{V_{bus}}{s^2 L_L C_L + s\dfrac{L_L}{R_{Ld}} + 1} \end{cases} \tag{16}$$

As we can observe in Figure 4, if the output impedance (i.e., LC input filter) resonance frequency is inside the closed loop bandwidth of the CPL's input impedance, in such a circumstance, instability occurs beyond the threshold power of the CPL. The threshold power expression is calculated by (17) [60,94].

$$P_{th} \simeq \frac{R_f \times C_f}{L_f} \times v_{bus}^2 \tag{17}$$

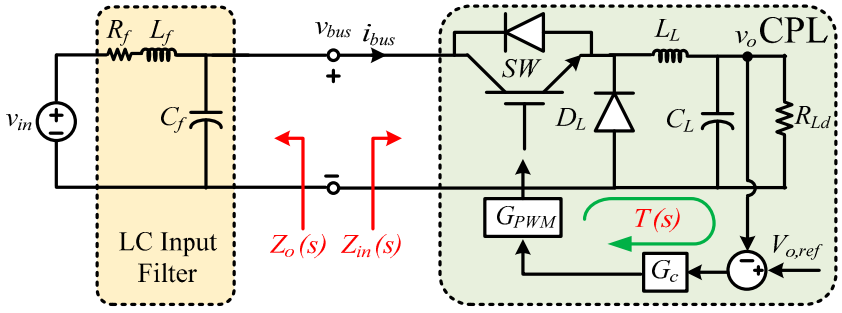


Figure 14. Cascaded system given in [93].

A typical DC-coupled hybrid microgrid is reported in the literature [95] as depicted in Figure 15. Because the power consumed from the DC bus is constant for a given AC load, the bidirectional interlinking converter (BIC) appears as CPL to the DC bus during the islanded mode of operation. As a result, voltage oscillation at the DC bus interface of the BIC occurs due to impedance interaction (i.e., Z_{ip} interacts with Z_{ot}) [96,97]. In [95], a control strategy based on active damping is suggested to address the aforementioned CPL instability without impairing the BIC's AC voltage regulation performance. However, the implementation of this control method requires six AC sensors, which increases the capital cost of the BIC. The output impedance (Z_{ot}) and the input impedance (Z_{ip}) can be expressed as follows:

$$Z_{ot} = \frac{sL_{DC} + R_{DC}}{s^2 L_{DC} C_{DC} + sR_{DC} C_{DC} + 1} \tag{18}$$

$$Z_{ip} = \left[\frac{A(s)}{B(s)} - \frac{i_{bus}}{v_{bus}}\right]^{-1} \tag{19}$$

where

$$\begin{cases} A(s) = 1.5[(v_d + i_d \times (R_f + sL_f)) \times (sC_f + 1/R_L) + i_d] \times \dfrac{v_d}{v_{bus}} \\ B(s) = v_{bus}[(sC_f + 1/R_L)(R_f + sL_f + G_C(S)) + G_C(S)G_v(S)] \end{cases} \tag{20}$$

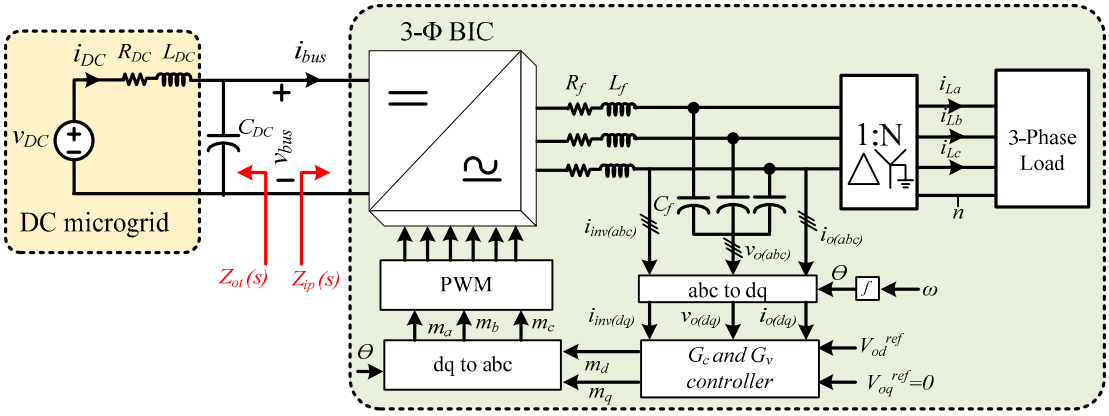
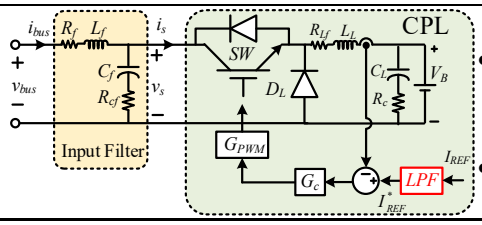
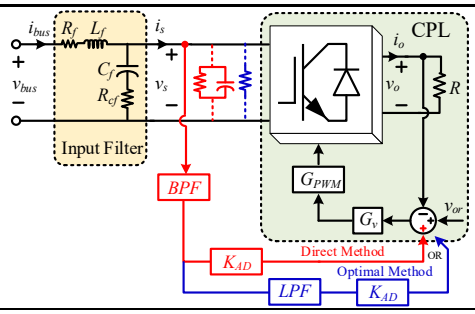
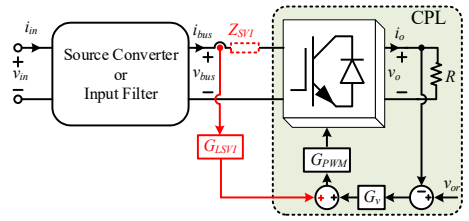
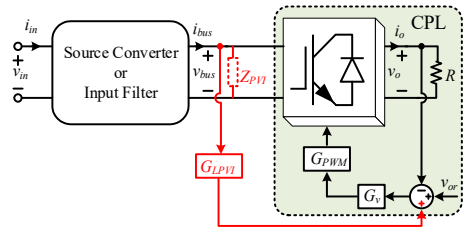
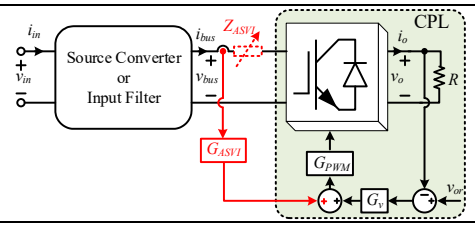
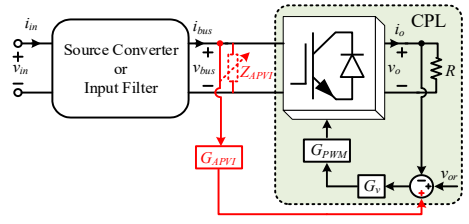
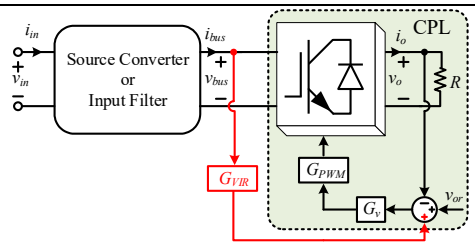


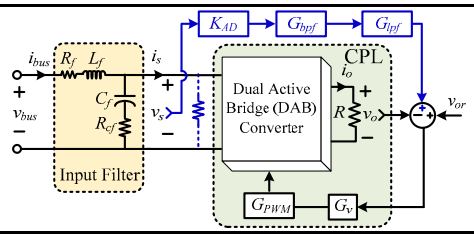
Figure 15. Cascaded system given in [95].

The salient features and drawbacks of the CPL side active damping methods are summarized in Table 2.

Table 2. Summary of CPL side active damping.

Ref.	Stabilization Structure	Salient Features	Drawbacks
[25]		• Changes caused by the load will be taken into account by its control. • No change in the hardware.	• The DC bus alterations are not considered. • Can only compensate for a limited amount of CPL.

[61]		• It presents direct and optimal LPVI control techniques for the CPL based on the buck converter. • Implementation of compensation controllers is simple.	• It involves complex calculations and cannot possess load power adaptability. • Tuning parameters are converter-dependent, and they would vary from one converter to another.
[93]		• A virtual impedance is to be connected in series with the input impedance of the load converter. • The load converter's input impedance is modified only in a small frequency range.	• It degrades the CPL's dynamic performance, such as response time. • It is incapable of adapting to changes in system parameters.
[98]		• Making a total separation between the output impedance of the source converter and the input impedance of the load converter. • Preserved stability.	• This scheme has an inherent limitation while using SAC across the entire load and input voltage range of the load converter. • The trade-off between dc link dynamics and performance in load regulation. • It is incapable of adapting to changes in system parameters.
[99]		• It reshapes the input impedance of the load converter. • The experimental results are provided. • It can handle multiple loads.	• A separate power detection circuit is needed. • The blocks require knowledge of the plant parameters, making their implementation relatively complex.
[100]		• It Improves source converter performance. • It reshapes the input impedance of the load converter at low frequencies.	• The control sampling rate, which has a locked ratio to the switching frequency, limits the POL converter's bandwidth. • Controller order is more than 3. • The complex calculation is required.
[101]		• Power adaptive control technique is presented. • Less sensors are required compared to APVI. • Easy to implement.	• Increase in overshoot. • More dynamic response time.

[102]		• Implementation is easy. • Increase the peak of the input impedance at resonance frequency.	• Deteriorates the performance of the load converter. • Tuning parameter is converter dependent.

4.2.3. Using Auxiliary Circuits or Intermediate-Level Active Damping

In this strategy, an extra circuit is added between the source and load subsystems to mitigate the effect of CPLs, while the source and load subsystems remain unchanged. This auxiliary circuit is often a regulated DC–DC converter as seen in Figure 16 that injects the required compensatory current over the entire operating range of the main system [103]. However, this method eliminates the challenges of the previous two approaches (i.e., source side and CPL side). While it increases the overall complexity of the system, it also imposes additional cost and power losses. In [104], the authors proposed an auxiliary circuit active damping method which is connected to the output of the load side converter as depicted in Figure 17. It improves the transient performance of the cascaded system. However, the implementation is complex and also imposes an extra cost.

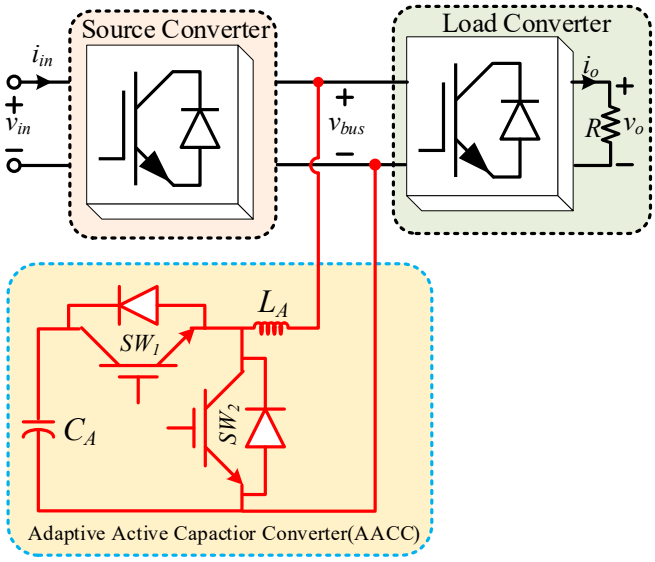


Figure 16. Intermediate-level active damping by adding an adaptive active capacitor converter (AACC) [103].

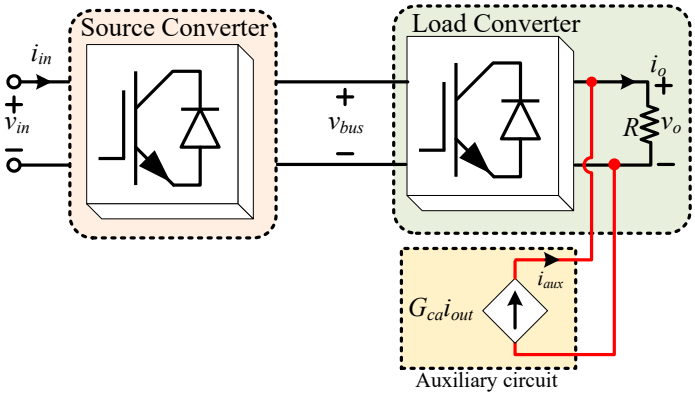


Figure 17. Using auxiliary circuit active damping [104].

5. The Delays in Digitally Controlled Systems and Their Effect on Active Damping Control

Implementation of the AD techniques in the digital domain is an important practical aspect that needs to be taken care of. The control system in the digital platform consists of two types of delays: computational delay and pulse width modulation (PWM) delay [24,105-107]. As synchronous sampling is frequently employed in digitally controlled systems; the computation delay is represented by the interval of time (T_s) between two samples, which is expressed as

$$G_{d,COM} = e^{-sT_s} \tag{21}$$

The PWM delay may be due to zero-order hold (ZOH), which is expressed as [105]

$$G_{d,PWM}(s) = \frac{1 - e^{-sT_s}}{s} \tag{22}$$

$G_{d,PWM}(s)$ can be expressed in the frequency domain as (23)

$$G_{d,PWM}(j\omega) = \frac{1 - e^{-j\omega T_s}}{j\omega} = \frac{\sin(0.5\omega T_s)}{0.5\omega} e^{-j0.5\omega T_s} \approx T_s e^{-j0.5\omega T_s} \tag{23}$$

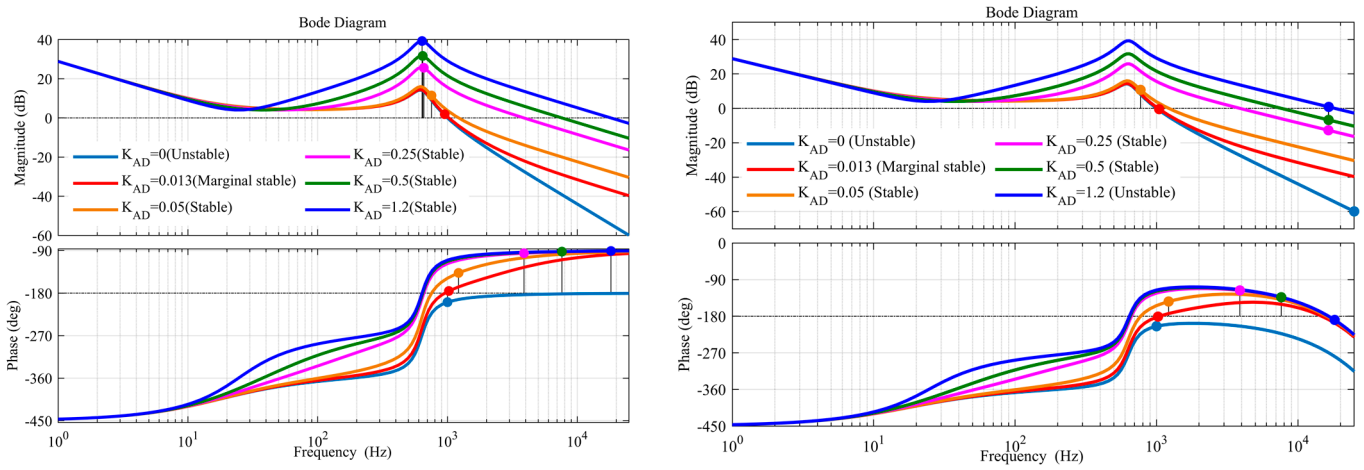
From (23), $G_{d,PWM}(s) \approx T_s e^{-0.5sT_s}$, which may be responsible for the delay of half of the sample time. These delay effects are incorporated in the control loop of the digitally controlled converter by cascading ZOH (for PWM delay) and Z^{-1} (for computational delay) blocks. By combining the abovementioned delays, the net delay in the digital control system can be considered as $e^{-(1.5sT_s)}$. The bode plot of the open-loop gain $\hat{V}_o(s)/\hat{d}(s)$ of a buck converter with the parameters given in [87] is shown in Figure 18, where,K_{AD} is the gain of the active damping controller and its minimum value (i.e., $K_{(AD(\min))}$) is calculated by using (13). In Figure 18a, for $K_{(AD(\min))}$, the system is approaching the marginal stability scenario. Increasing K_{AD} improves the phase margin of the system, indicating an increase in system damping as shown in Figure 18a. In this way, the stability of the closed-loop control system is ascertained. Figure 18b shows that, while considering computational and modulation delays, increasing K_{AD} by a specific amount gradually reduces the system's phase margin until the system becomes unstable. This implies that K_{AD} must have a stable range between $\left[K_{(AD(\min)),}K_{(AD(max))}\right]$. The stable range of K_{AD} can also be increased by decreasing T_s. $K_{(AD(max))}$ can be easily calculated by solving the (24) and (25) [21,107]:

$$\angle[e^{-j\omega T_s}G(s)] = -\pi \tag{24}$$

$$\left|e^{-j\omega T_s}G(s)\right| = 1 \tag{25}$$

$$G(s) = \frac{\hat{V}_{bus}(s)}{\hat{d}(s)}|_{open-loop} = e^{-j0.5\omega T_s} \cdot [Equation\ (7)] \cdot \left(G_{PI}(s) - G_{AD}(s)\right) \tag{26}$$

where $G_{AD}(s)$ is the resulting active damping gain and $G_{PI}(s)$ is the PI controller (i. e., $K_p + K_I/s$)



(**a**) (**b**)

Figure 18. Bode diagram of $\frac{\hat{V}_o(s)}{\hat{d}(s)}$ of buck converter: (**a**) without delay; (**b**) with delay [87].

The delay-induced phase lag effect reduces the phase margin in the high-frequency region. However, because of the minimal quantity of T_s, the delay in the low-frequency zone has no effect and only restricts the upper band of K_{AD} to a certain value. Figure 18b shows a significant flexibility in selecting an appropriate damping gain K_{AD}, which may change based on the designer's viewpoint. To provide the system roboustness under abrupt changes in input voltage and load, K_{AD} should be much larger than $K_{AD(min)}$ (i.e., 15 to 20 times of $K_{AD(min)}$).

6. Challenges and Future Research Directions

This article contributes to the prospects of the various stabilization techniques for cascaded systems in DC microgrids based on the active damping approach. The benefits and drawbacks of various active damping approaches have been discussed extensively in the preceding sections. This section summarises the overall findings of this review work as well as recommendations for future work.

Load-side active damping*:* Active control strategies on the source side cannot be used to increase the system damping when the source side is an LC filter or an uncontrolled converter in a cascaded system. In these situations, CPL-side compensation is a viable choice. However, the main issue with this strategy is that the dynamics of the extra compensating loop may disrupt the primary control loop of the CPL, resulting in a trade-off between load performance and stability margin.

Source-side active damping*:* This method's major advantage is that the system can be stabilized without affecting load performance. However, it is not applicable when the source converter operates in an open loop.

Intermediate-level active damping*:* In this strategy, an extra circuit is added between the source and load subsystems to mitigate the destabilizing effect of CPLs, while the source and load subsystems remain unchanged. However, this method eliminates the challenges of the previous two approaches (i.e., source-side and CPL-side). While it increases the system's overall complexity, it also imposes additional costs and power losses.

From the above explanation in Tables 1 and 2, it can be inferred that each damping control technique has merits and drawbacks. The recommendations are as follows.

1. An investigation of the generalization of active stabilizing techniques is required for the complex DC MGs. Moreover, the stability issues for DC MGs in the presence of dynamic loads and CPLs need to be addressed.
2. The linear active damping techniques are operating point-dependent and can compensate only a limited amount of CPL. Therefore, non-linear damping techniques can be investigated to address the above problem.

3. Further, the tuning parameters of active damping techniques are converter-dependent and they would vary from one converter to another. Thus, converter-free active damping techniques need to be developed to address the problems of converter dependence.
4. The performance of damping techniques depends on converters and the modelling of the complex system and the perfect design of parameters. Therefore, to make model-free stabilization, one can look into data-driven control techniques to improve the stability of the DC MGs.
5. In a more complicated DC network with several source converters, interactions between their control loops have an impact on the converter performance. Therefore, the modelling and stability analysis of the much more practical systems, e.g., multi-terminal DC MG with CPL, is required to investigate.
6. Research on the optimal placement of CPL (e.g., fast DC chargers for EVs) is further required to ensure the stability of the DC MGs, a practical scenario in an EV parking lot with incoming and outgoing EVs.
7. When addressing the effects of CPL in cascaded systems, the majority of active damping techniques focused on small-signal stability, which can only ensure stability for small disturbances. However, the system under large disturbances is also important. Thus, further exploration with large-signal stability is required to ensure the global stability of the system over a wide dynamic range.
8. Based on the observations above, we can conclude that the majority of the work is based on a cascaded DC–DC converter system. However, there has been very little work with cascaded DC–AC converter systems or in islanded MGs. Future research is still needed.
9. Finally, research that aims to reduce the number of sensors, controller order and implementation complexity is required.

7. Conclusions

This paper has presented a comprehensive review of the active damping stabilization method for cascaded systems in DC microgrids. Because of the negative impedance properties of CPLs, oscillation occurs in voltage response at DC bus. Therefore, a reliable control system is essential. Thus, this paper focuses on active damping control techniques. First, this paper discussed the CPL modelling and the analysis of cascaded systems in DC MGs. Furthermore, classification of CPL compensation techniques and their merits and drawbacks was summarized. It is envisaged that it would be useful, directing researchers in the appropriate path for developing damping stabilisation in DC microgrids. More research on active approaches is required in the future to increase the dynamics and robustness of the cascaded system.

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Nomenclature

AD	Active damping
$DGMGs$	Direct Current microgrids
CPL	Constant power load

EVs	Electric vehicles
POL	Point of load converter
DOE	Department of Energy
ZOH	Zero-order hold
AD	Active damping
MGs	Microgrids
REG	Renewable energy generation
$SSVI$	Source-side series virtual impedance
$LSVI$	Load-side series virtual impedance
$LPVI$	Load-side parallel virtual impedance
$ASVI$	Adaptive series virtual impedance
$APVI$	Adaptive parallel virtual impedance
LPF	Low pass filter
HPF	High pass filter
BPF	Bandpass filter
K_{AD}	Gain of active damping
$LVDC$	Low voltage direct current
PWM	Pulse width modulation
MEG	Microgrid exchange group
MEA	more electric aircraft
NII	negative incremental impedance
$GMPM$	Gain and phase margin
$ESAC$	Energy source analysis consortium
MPC	Maximum peak criterion
LFR	Loss-free resistance
$AACC$	Adaptive active capacitor converter

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