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GaAs/Si Tandem Solar Cells with an Optically Transparent InAlAs/GaAs Strained Layer Superlattices Dislocation Filter Layer

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Abstract: Epitaxial growth of III–V materials on Si is a promising approach for large-scale, relatively low-cost, and high-efficiency Si-based multi-junction solar cells. Several micron-thick III–V compositionally graded buffers are typically grown to reduce the high threading dislocation density that arises due to the lattice mismatch between III–V and Si. Here, we show that optically transparent n-In_{0.1}Al_{0.9}As/n-GaAs strained layer superlattice dislocation filter layers can be used to reduce the threading dislocation density in the GaAs buffer on Si while maintaining the GaAs buffer thickness below 2 μm. Electron channeling contrast imaging measurements on the 2 μm n-GaAs/Si template revealed a threading dislocation density of $6 \times 10^7 \text{ cm}^{-2}$ owing to the effective n-In_{0.1}Al_{0.9}As/n-GaAs superlattice filter layers. Our GaAs/Si tandem cell showed an open-circuit voltage of 1.28 V, Si bottom cell limited short-circuit current of 7.2 mA/cm², and an efficiency of 7.5%. This result paves the way toward monolithically integrated triple-junction solar cells on Si substrates.

Keywords: solar cell; Si tandem cell; monolithic integration; molecular beam epitaxy



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1. Introduction

Si-based solar cells currently dominate the photovoltaic market because of their low manufacturing cost and mediocre efficiencies. The theoretical efficiency of a single-junction Si solar cell is limited to 29.4% [1], and the best record-high laboratory Si cell efficiency is currently reported to be 26.1%, which is approaching its theoretical limit. However, III–V solar cells have demonstrated much higher 1-sun efficiencies of up to 39.5% by constructing monolithically grown multi-junction structures [2]. Those high-efficiency III–V multi-junction solar cells have been primarily used for space applications due to their expensive fabrication cost by growing on costly Ge or GaAs wafers. Alternative approaches for low-cost and high-efficiency solar cells include Si-based multi-junction solar cells via either III–V wafer bonding [3] or epitaxial growth [2,4–6]. While the former already reached ~35.9% efficiency in a four-terminal structure, the latter is recently drawing more attention because of its strong potential for low fabrication cost and high efficiency.

Several studies have reported Si-based dual-junction solar cells. Soga et al. demonstrated 21.4% efficient AlGaAs/Si tandem solar cells using metal-organic chemical vapor deposition (MOCVD) [7]. More recently, other III–V materials such as GaAsP with a 1.72 eV bandgap energy were also employed for monolithic current-matched III–V/Si tandem solar

cells by several research groups [5,8]. On top of these dual-junction solar cell research efforts, triple-junction solar cells have also been investigated since a combination of energy bandgaps of 1.12 eV, 1.50 eV, and 2.01 eV can theoretically surpass the efficiency of optimal dual-junction solar cells [1,6,7]. The first Si-based monolithic InGaP/GaAs/Si triple-junction cells were reported in 2018 with an efficiency of 19.7% [9]. They used $\text{GaAs}_x\text{P}_{1-x}$ step-graded buffers to bridge the lattice mismatch between Si and GaAsP top cell. The $\text{GaAs}_x\text{P}_{1-x}$ step-graded buffers were also found to be effective in lowering the threading dislocation density (TDD) to $1.4 \times 10^8 \text{ cm}^{-2}$. Afterward, the researchers further improved the efficiency to 22.3% and 25.9% by lowering the TDD to $2.2 \times 10^7 \text{ cm}^{-2}$ and switching to AlGaAsP step-graded buffers [1].

Direct growth of GaAs buffer on Si has also been used as a virtual template for high-performance optoelectronic devices [10–12]. In particular, 1.3 μm InAs quantum dot lasers grown with a TDD of $\sim 6 \times 10^7 \text{ cm}^{-2}$ in high-quality GaAs/Si template boasted low threshold current, high peak power, and impressive reliability [13]. The advantages of directly growing GaAs on Si rather than the step-graded buffers with ternary compounds such as $\text{GaAs}_x\text{P}_{1-x}$ materials are straight-forward device design, epitaxial growth, and a potentially lower TDD. To reduce TDD, compressively strained dislocation filter layers (DFLs), e.g., InGaAs with In ~ 10 –20% are commonly used [14,15]. However, the effective $\text{In}_x\text{Ga}_{1-x}\text{As}$ DFLs cannot be applied for Si-based tandem cells because the Si bottom cell would suffer from undesirable parasitic absorption. Therefore, developing an optically transparent DFL with a high dislocation filter efficacy is needed for high-performance triple-junction solar cells on Si.

In this paper, we show that 10 nm n- $\text{In}_{0.1}\text{Al}_{0.9}\text{As}$ /10 nm n-GaAs strained layer superlattices can serve as an efficient dislocation filter layer while being optically transparent to the Si bottom subcell. The proposed filter layer enables a threading dislocation density of $6 \times 10^7 \text{ cm}^{-2}$ and smooth surface morphology, which are necessary for III-V top cell growth. Our GaAs/Si tandem solar cell shows an open-circuit voltage of 1.28 V, a fill factor of 81.7%, and 7.5% efficiency with a short-circuit current of 7.2 mA/cm^2 which is limited by the Si bottom subcell. The results obtained in this study pave the way towards high efficiency, crack-free triple-junction solar cells epitaxially grown on Si substrate.

2. Epitaxial Growth

All samples were grown in a solid source molecular beam epitaxy chamber. The GaP/Si substrate was purchased from NAsP GmbH corp. The Si wafer consists of unintentionally n-doped ($n = 1 \times 10^{16} \text{ cm}^{-3}$) 200 nm Si emitter. It should be noted that the Si wafer structure is not optimized for III-V/Si tandem cell application. A 40 nm GaP layer was grown by MOCVD for an anti-phase domain-free III-V growth. Three different dislocation filter layers were investigated, 200 nm n- $\text{In}_{0.1}\text{Ga}_{0.9}\text{As}$, 200 nm n- $\text{In}_{0.1}\text{Al}_{0.9}\text{As}$, and $15 \times (10 \text{ nm n-}\text{In}_{0.1}\text{Al}_{0.9}\text{As}/10 \text{ nm n-GaAs})$ strained layer superlattices as shown in Figure 1a–c). After oxide desorption at 650 °C under As_2 over-pressure, a 50–100 nm GaAs layer was first grown at a low temperature (500 °C) and low growth rate (0.1 $\mu\text{m/h}$). Then, the growth temperature was raised to 580 °C to grow a 1200–1300 nm GaAs layer. Thermal cycle annealing (TCA) from 350 °C to 700 °C was performed four times to facilitate dislocation movement and to improve GaAs buffer crystalline quality. The growth was interrupted to change the substrate temperature for DFL growth as indicated in the sample schematics. Finally, an n-GaAs layer was grown to complete the GaAs buffer growth on Si. We doped the entire GaAs buffer structure at $1 \times 10^{18} \text{ cm}^{-3}$ using Si to be able to electrically interconnect the top subcell and bottom subcell. A moderate doping level of $1 \times 10^{18} \text{ cm}^{-3}$ was used because an excessive n-type doping can prohibit dislocation movement and the dislocation reduction process [16].

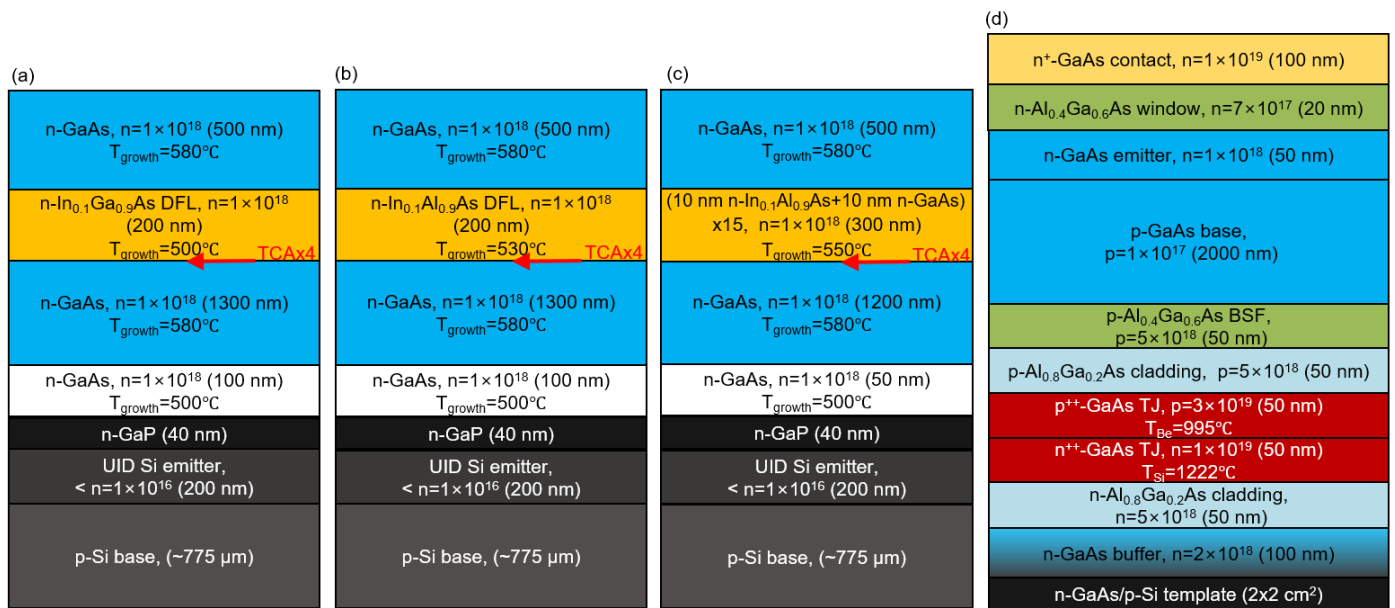


Figure 1. Schematics of the GaAs/Si templates with (a) n-In_{0.1}Ga_{0.9}As DFL, (b) n-In_{0.1}Al_{0.9}As DFL, (c) 10 nm n-In_{0.1}Al_{0.9}As/10 nm n-GaAs SLS, and (d) GaAs/Si tandem solar cell.

Figure 1d illustrates the entire structure of GaAs/Si tandem solar cell. The GaAs/Si buffer sample with the strained layer superlattice DFL was reloaded to our MBE reactor to grow the GaAs tunnel junction (TJ) and top GaAs cell. We have adopted an Al_{0.8}Ga_{0.2}As cladding structure surrounding the 50 nm n⁺⁺GaAs and p⁺⁺GaAs TJ to inhibit dopant diffusion during the top cell growth [17]. The GaAs TJ and upper p-Al_{0.8}Ga_{0.2}As cladding layer were grown at 500 °C at a slow growth of GaAs 0.1 $\mu\text{m}/\text{h}$ to achieve a high n-type doping concentration and smooth surface morphology. The rest of the GaAs top cell layers were grown under typical growth conditions. During the entire tandem cell growth, the reflection high energy electron diffraction showed streaky patterns, indicating smooth surface morphology of the TJ and GaAs top cell growths.

3. Material Characterizations

Figure 2 shows the Nomarski micrographs of the as-grown GaAs/Si buffer with 200 nm n-In_{0.1}Ga_{0.9}As DFL, 200 nm n-In_{0.1}Al_{0.9}As DFL and $15 \times (10 \text{ nm n-In}_{0.1}\text{Al}_{0.9}\text{As}/10 \text{ nm n-GaAs})$ DFL at 1000 $\times$ magnification. In Figure 2a, the surface of GaAs/Si with the 200 nm n-InGaAs DFL exhibits a qualitatively smoother surface, which is correlated with the absence of ternary phase separation. Even though the InGaAs DFL considerably improved the surface morphology, it is not desirable for Si bottom cells due to parasitic absorption since it has a lower band gap than GaAs. On the other hand, Figure 2b shows the surface of the GaAs/Si buffer with 200 nm n-In_{0.1}Al_{0.9}As DFL, which was designed to be optically transparent to minimize parasitic absorption. However, the sample surface looks very rough due to phase separation similarly observed by previous studies demonstrating phase separation and ordering of InAlAs [18]. Consequently, the growth of a high-quality n-In_{0.1}Al_{0.9}As DFL is difficult on a GaAs/Si template. To achieve optically transparent DFL while maintaining smooth surface morphology, periodically strained layer superlattice (SLS) of 10 nm n-In_{0.1}Al_{0.9}As and 10 nm n-GaAs were inserted in GaAs buffers. Compared to the InAlAs DFL only, Figure 2c shows a smoother surface from the n-InAlAs/n-GaAs SLS DFL. Finally, a relatively smooth surface morphology was achieved without using InGaAs, indicative of a relatively high-quality grown GaAs/Si template with optically transparent $15 \times (10 \text{ nm InAlAs} + 10 \text{ nm GaAs})$ DFL.

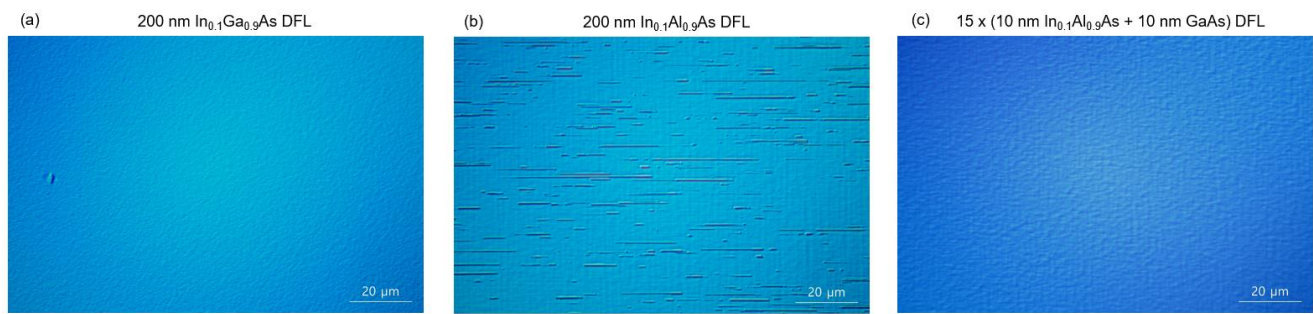


Figure 2. Optical microscope images of GaAs/Si buffer surface with (a) n-In_{0.1}Ga_{0.9}As DFL, (b) n-In_{0.1}Al_{0.9}As DFL and (c) n-In_{0.1}Al_{0.9}As/n-GaAs DFL.

Prior to GaAs top cell growth, electron channeling contrast imaging (ECCI) measurement was performed to investigate if the n-InAlAs/n-GaAs SLS DFL had successfully filtered TDs during the 2 μm GaAs/Si template growth. We chose the ECCI technique because it involves a simple, rapid, and non-destructive process commonly used to characterize TDD [14]. It takes advantage of the dark-bright contrast resulting from the strong backscattering of electrons at defects such as TDs [19]. ECCI was performed using an FEI Inspector F50 scanning electron microscope (SEM) operating at an accelerating voltage of 20 kV with a spot size of 5.0 and a working distance of 5.9 mm. Figure 3 shows a representative ECCI image of the GaAs/Si template with an optically transparent n-In_{0.1}Al_{0.9}As/n-GaAs superlattice filter layer. An average of 150 TDs were detected by surveying a total area of 230 μm^2 . Incorporating n-In_{0.1}Al_{0.9}As/n-GaAs SLS and thermal cycling annealing to the sample structure reduced the TDD to $6 \times 10^7 \text{ cm}^{-2}$, which is more than a factor of four lower compared to the un-optimized GaAs buffer with TDD of $2.8 \times 10^8 \text{ cm}^{-2}$ [14]. This result suggests that InAlAs/GaAs SLS can apply compressive stress and efficiently prevent TDs from propagating upward by bending them into the growth planes [20]. In addition to this dislocation movement, TCA can increase the mobility of TDs, allowing them to interact more with each other. The mechanism of TD reduction by using TCA is based on thermal stress as a consequence of the differential thermal expansion coefficients. It can enhance TDs to glide and combine with existing TDs, causing self-annihilation. Based on the ECCI analysis, we concluded that optically transparent n-In_{0.1}Al_{0.9}As/n-GaAs SLS and TCA have a significant impact on improving the quality of n-GaAs/Si template via TD reduction process.

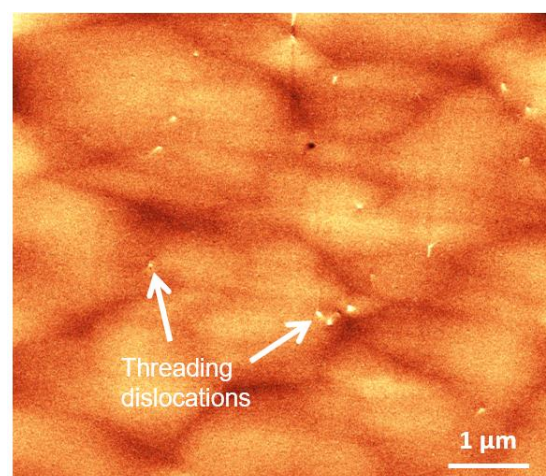


Figure 3. ECCI image of the GaAs/Si template with In_{0.1}Al_{0.9}As/GaAs SLS showing threading dislocations.

Figure 4a shows a cross-sectional transmission electron microscopy image of the GaAs top cell grown on GaP/Si with n-In_{0.1}Al_{0.9}As/n-GaAs SLS. Multiple crystalline defects

such as misfit and threading dislocations were observed at the bottom of the GaAs buffer due to the highly defective GaAs/Si heterointerface. However, beyond the InAlAs/GaAs SLS DFL, threading dislocations were not visibly penetrating into the adjacent GaAs buffer and GaAs subcell on this scale. Shown in the enlarged marked area in Figure 4b are arrays of misfit dislocations formed at the interfaces between the InAlAs/GaAs SLS and GaAs buffers as indicated by the white arrows. The low density of misfit dislocations within the interface provides a good platform for the growth of high-quality GaAs top cells. Consequently, these observations agree with the low threading dislocation density acquired using ECCL.

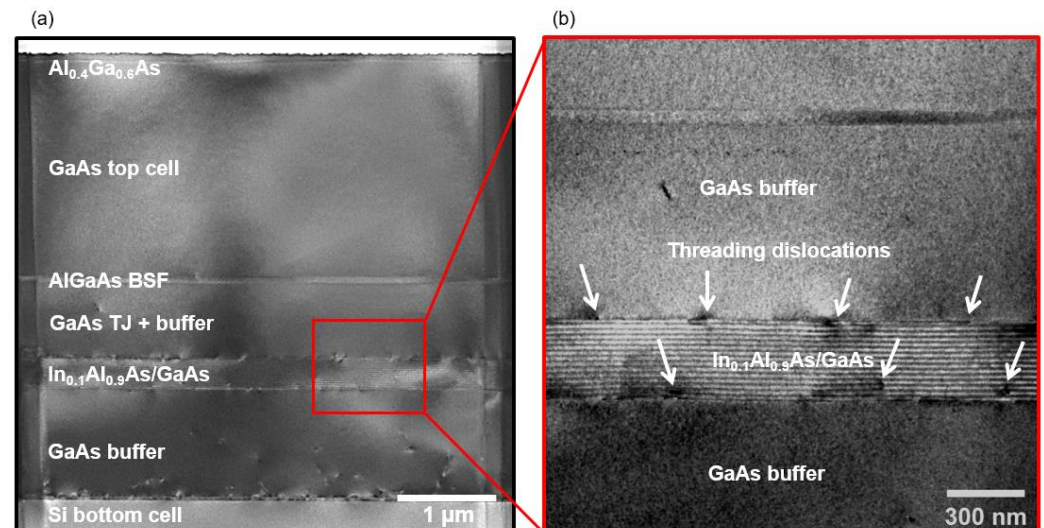


Figure 4. (a) Cross-sectional TEM image of the GaAs/Si tandem solar cell. (b) A high magnification image of the red rectangle in (a), showing effective TD reduction by In_{0.1}Al_{0.9}As/GaAs SLS.

4. Cell Fabrication and Measurement

Standard cleanroom procedures were carried out for the fabrication of the GaAs/Si tandem solar cells as shown in Figure 5. To increase the light absorption of the tandem solar cell, the Si backside was randomly textured using an aqueous KOH solution for 25 min at 70 °C. The addition of IPA is known to slow down the etching rate and help produce stable pyramid structures [21]. A 200 nm aluminum metal contact was deposited on the backside via a thermal evaporator, followed by thermal annealing at 500 °C for 20 min. Then Ti/Au (20/300 nm) was deposited via an electron beam as a p-type electrode. For the top grid metal, Pd/Ge/Au (10/20/200 nm) was deposited via electron beam evaporation. Individual GaAs top cells were isolated by wet etching using H₃PO₄/H₂O₂/DI water (1:1:10). Top cells were etched past the GaAs TJ and until the n-GaAs buffer, and Pd/Ge/Au (10/20/200 nm) was deposited as middle-metal contact after the patterning process. Having the middle metal enabled us to measure the top GaAs cell and the Si bottom cell individually. Si bottom cells were mesa-defined by a combination of wet chemical etching for the remaining III-V buffer layers and inductively coupled plasma-reactive ion etching 2 μm past the n-type Si emitter for the Si bottom cell. Finally, the fabricated sample underwent rapid thermal annealing at 300 °C for 1 min to improve Ohmic contact.

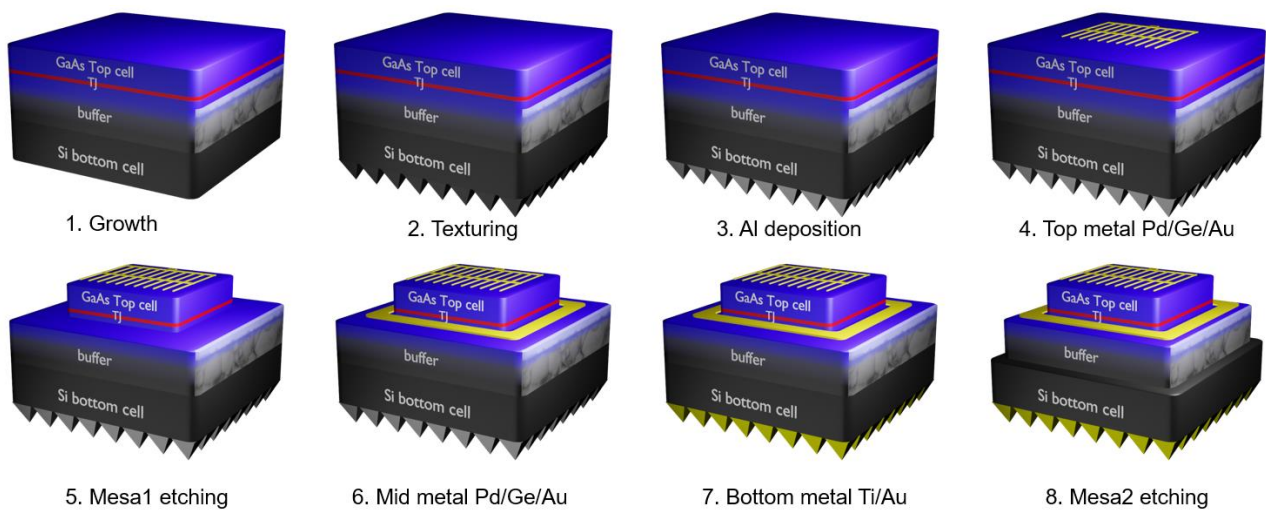


Figure 5. Fabrication procedure of the GaAs/Si tandem solar cell.

Figure 6a shows an SEM image of textured Si. Surface texturing using KOH produced uniform pyramids with an average size of 12 μm on the entire Si back surface. As a consequence of this light trapping effect, the surface reflectance of the textured Si back surface was lowered to about 12% in the wavelength range of 820–1100 nm compared to bare Si as shown in Figure 6b. This surface texturing can maximize the surface reflection for the solar spectrum in the Si subcell and increase the optical path of the incident light by the multiple reflections between the pyramids, enhancing the probability of e^-h^+ pair collection [21].

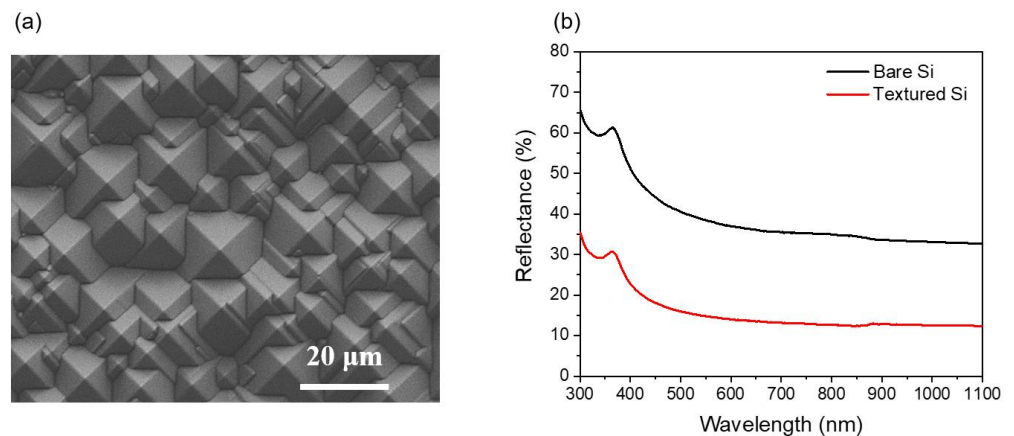


Figure 6. (a) SEM image of randomly textured Si backside. (b) The reflectance curves of bare Si wafer and textured Si in the wavelength range of 300–1100 nm.

The tandem cells were measured under AM 1.5G condition as shown in Figure 7a after applying $\text{TiO}_2/\text{SiO}_2$ anti-reflective coatings on devices. To avoid any contributions of photo-generated carriers outside the dedicated bottom Si cell area, we used a metal aperture mask with an opening size equivalent to that of the GaAs top cell. Figure 7b shows the performance of the GaAs top cell, Si bottom cell, and GaAs/Si tandem cell with and without the metal aperture. First, the GaAs top cell without aperture demonstrated an efficiency of 7.8% with $V_{oc} = 0.78$ V, $J_{sc} = 17.4$ mA/cm^2 , and $\text{FF} = 58.7\%$. Please note that the GaAs top cell was measured through the GaAs TJ by probing the top metal and middle metal as illustrated in Figure 5. In addition, the Si bottom cell and tandem cell without aperture both exhibited $J_{sc} = 7.84$ mA/cm^2 , clearly showing that the tandem cell is current-limited by the Si subcell. Our GaAs/Si tandem cell with an aperture demonstrated a similar $V_{oc} = 1.28$ V, equivalent to the measured V_{oc} without an aperture. However, the

measured J_{sc} value was lower with $J_{sc} = 7.19 \text{ mA/cm}^2$. This indicates that the J_{sc} of the Si bottom cell without aperture was overestimated due to the contribution of charge carriers from outside the dedicated Si mesa as mentioned beforehand. Table 1 summarizes the results of individual subcells and tandem cells. The external quantum efficiency (EQE) curve in Figure 7c reveals a peak efficiency of $\sim 80\%$ at 680 nm and decreasing efficiencies in the blue and red wavelength regimes. Our in-house GaAs baseline solar cell grown on GaAs with a nominally identical cell structure ($\text{Al}_{0.4}\text{Ga}_{0.6}\text{As}$ window and BSF) achieved internal quantum efficiency (IQE) of 90% at 650 nm and maintained 80% up to 870 nm cut-off wavelength. Therefore, the relatively poor blue and red response can likely be attributed to the unoptimized design and growth sequence, resulting in parasitic absorption in $\text{Al}_{0.4}\text{Ga}_{0.6}\text{As}$ window and non-radiative recombination at the interface between the p- $\text{Al}_{0.4}\text{Ga}_{0.6}\text{As}$ BSF and TJ. Especially, on the blue response regime, $\sim 20\%$ higher EQE can be expected by replacing the $\text{Al}_{0.4}\text{Ga}_{0.6}\text{As}$ window with an InGaP layer, which is Al-O defects-free with a higher bandgap [20]. The EQE response for the bottom Si cell could not be measured due to difficulties in probing in our current EQE setup. Potential parasitic absorption of the SLS structure is also going to be studied by measuring EQE on the Si subcell in the future.

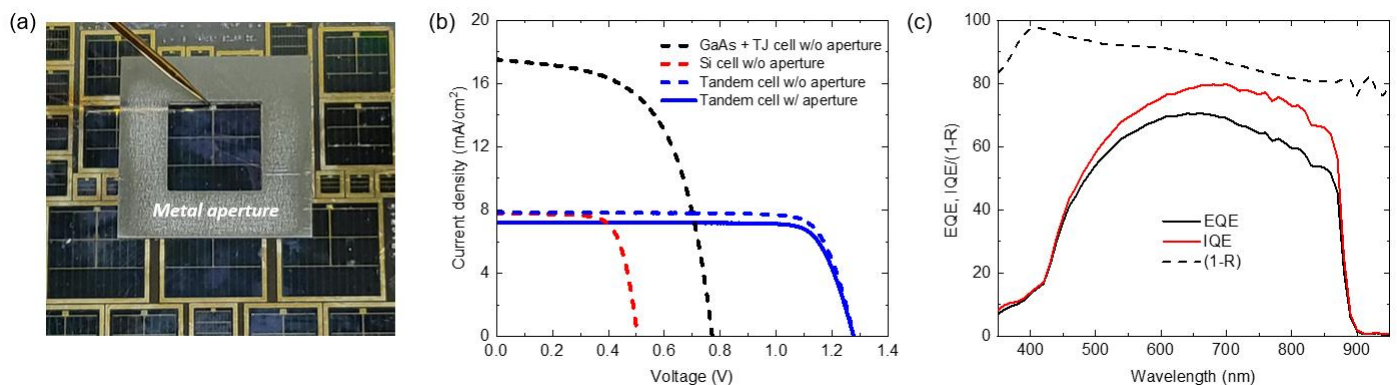


Figure 7. (a) LIV measurements of tandem cells with aperture mask. (b) LIV curves of GaAs top cell (black), Si bottom cell (red) and GaAs/Si tandem cell (blue). The solid and dash lines represent measurements with and without the aperture, respectively. (c) Quantum efficiencies of the GaAs top cell in the tandem device.

Table 1. Summary of GaAs/Si tandem cell performance.

Cells (5 mm × 5 mm)	V_{oc} (V)	J_{sc} (mA/cm²)	FF (%)	Eff. (%)
GaAs cell w/o aperture	0.78	17.4	58.7	7.8
Si cell w/o aperture	0.50	7.76	72.7	2.8
Tandem cell w/o aperture	1.28	7.84	80.8	8.0
Tandem cell w/aperture	1.28	7.19	81.7	7.5

Future work should focus on improving GaAs top cell efficiency by reducing crack formation with optimized growth conditions and structure. In addition, improved J_{sc} of Si bottom cell can be achieved by applying thinning and then pyramid texturing for light trapping in Si bottom cell to obtain higher J_{sc} . Furthermore, slight tuning of the GaAs cell bandgap by adding aluminum is requisite since the optimal energy bandgap for the middle cell in a triple-junction structure is 1.50 eV. Incorporating high-efficiency organic solar cells with the Si tandem cell can also be considered. [22,23]

Table 2 compares our GaAs/Si tandem cell result with the previously reported works. Feifel et al. reported monolithically integrated InGaP/GaAs/Si triple-junction solar cells using GaAsP-graded buffers. We extrapolated the subcell V_{oc} values from their electroluminescence measurements. Since our current tandem cell does not have a top cell, the

performance of GaAs middle and Si bottom cells is compared to each other. We would like to emphasize the fact that the GaAs middle cell $V_{oc} = 0.78$ V reported in this study is higher than the previously reported values (0.70 V and 0.76 V). We believe that this is because of the low TDD of $\sim 6 \times 10^7 \text{ cm}^{-2}$ in the GaAs middle cell grown on Si. However, the relatively low V_{oc} of our Si bottom cell compared to the references was observed, and this can be attributed to the GaP/Si interface nonradiative recombination rates [6,9].

Table 2. Comparison of GaAs/Si tandem cell performance.

V_{oc} (V)	Top (InGaP)	Middle (GaAs)	Bottom (Si)	Tandem (3 J)	Tandem (GaAs + Si)
Ref. [9]	1.07 V	0.70 V	0.55 V	2.32 V	1.25 V
Ref. [6]	1.23 V	0.76 V	0.63 V	2.62 V	1.39 V
Our work	N/A	0.78 V	0.50 V	N/A	1.28 V

5. Conclusions

In this paper, we have demonstrated a GaAs/Si tandem solar cell by using optically transparent n-In_{0.1}Al_{0.9}As/n-GaAs strained-layer superlattices in the GaAs buffer. The optically transparent dislocation filter layer not only efficiently decreased the threading dislocation density to $6 \times 10^7 \text{ cm}^{-2}$ but also allowed smooth surface morphology without InAlAs phase separations. The high-quality GaAs/Si template enabled a GaAs top cell with an open-circuit voltage of 0.78 V and short-circuit current of 17.5 mA/cm². Eventually, our GaAs/Si tandem cell showed an open-circuit voltage of 1.28 V, short-circuit current of 7.19 mA/cm², fill factor of 81.7%, and efficiency of 7.5%. The tandem cell is current-limited by the Si bottom cell, and this current-mismatching will be avoided by incorporating a proper third cell with a bandgap of ~ 1.9 eV. Further improvements in the tandem cell performance can be achieved via the reduction of threading dislocations and optimization of growth conditions. We believe that this work is very promising for high-efficiency triple-junction solar cells monolithically integrated on Si wafer.

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Conflicts of Interest: The authors declare no conflict of interest.

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