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Linear-in-dB Logarithmic Signal Strength Sensor Circuit for Wireless Power Transfer Receivers

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Abstract: Tracking systems for wireless power transfer are becoming a necessity. The received target signals are sometimes weak, which is why it is critical to have a dedicated received–signal–strength indicator (RSSI) for signal detection. It can also be used for transmitter localization and automatic gain control (AGC) to ensure continuous coverage. In this paper, a logarithmic detector coupled with a high-speed full-wave rectifier is designed for an RSSI system. The aim is to place the RSSI on the receiver side of unmanned aerial vehicles used, for example, as agricultural drones. This system is intended to operate in a scenario where multiple drones in a smart farm are charged wirelessly whilst airborne. An RSSI is placed in the receiver to detect and track wireless signals and to ensure the drone is charged while in motion. The RSSI system operates at 5.8 GHz, reported for the first time, and is capable of detecting signal strengths from −60 dBm to 0 dBm with a sensitivity level of 17 mV/dBm. A logarithmic error of 0.4 dB with a dynamic range of 34 dB was achieved. The proposed RSSI system was designed using 65 nm TSMC CMOS technology, and it exhibits high sensitivity, better efficiency, and lower power consumption than those in other reported works.

Keywords: agricultural drones; received-signal-strength indicator (RSSI); logarithmic detector; wireless power transfer; wireless system tracking; unmanned aerial vehicles

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1. Introduction

Although wireless charging has existed since the 1960s, only in the past two decades has it become of utmost importance due to the increasing use of portable devices. In recent years, the use of wireless charging has increased rapidly in many fields, especially in the field of smart technology [1]. The wireless power transfer (WPT) technologies used for wireless charging are classified into radiative and nonradiative [2]. Nonradiative technologies include inductive coupling, magnetic resonance coupling, and capacitive coupling; however, they all have a limited effective charging distance [2]. Thus, WPT using radio frequency (RF) beams is the most efficient charging topology for applications where the distance is higher (in the range of meters) [3]. Drones or unmanned aerial vehicles (UAVs) used in long-range applications and operations in extreme climatic conditions, such as to identify diseased plants, reduce water consumption, and complete other Internet of Things (IoT)-sensor-related tasks, would be more effective if charged wirelessly [4]. Different methods have been investigated for charging the batteries of UAVs to enhance their flight time, such as by (i) increasing the capacity of their batteries, which could add extra weight to the drones; (ii) swapping the discharged batteries with new ones once the drone lands, which would be fairly complex and likely expensive to implement; and (iii) recharging the batteries at the base station of the drone using either a wired link or WPT links. The contact-based conductive charging technique, the most popular charging method used in drones today, requires extremely accurate alignment with the charging station, making it ineffective in harsh weather conditions. Thus, charging UAVs through WPT links using RF beams is a strong, viable solution for the efficient design of UAVs, due

to the longer charging distance and feasible operation in harsh weather conditions [5]. This research analyzes a scenario where multiple drones in a smart farm are charged wirelessly whilst airborne, which requires the receiver in the drone to successfully track and detect wireless signals and ensure the drone is charged while in motion. For such a mechanism to be effective, it is essential to have a highly efficient and precise received–signal–strength indicator (RSSI) block at the receiver. The signals received at the receiver have varying amplitudes, sometimes below the receiver's sensitivity level; therefore, an RSSI is important for signal detection.

In reference [6], an RSSI system is used for the collection of tolls by integrating it with a unit on board. The design incorporates a mixture of rectifiers and amplifiers (limiting in nature); the filter is integrated into the chip using active components, and the output currents are combined through summation. However, in this system, no WPT mechanism is used at all. The RSSI system described previously [7] is used to detect and issue warnings to drones regarding the authenticity of the received signals with a focus on programmed calculations for achieving its objectives, and no description of a circuit design for RSSI implementation is provided. An in-depth analysis of an RSSI system for a wireless network is presented in [8], functioning at 30 KHz whilst receiving a single-tone sinusoidal waveform. This reference presents formulas for key parameters for the understanding of the system's performance characteristics. An RSSI system for a software-defined radio application is showcased in [9], with a conventional arrangement of limiting amplifiers and rectifiers to detect the carrier signal power within a broad frequency range, spanning from 100 KHz to 20 MHz. Similarly, ref. [10] introduces an RSSI system tailored for wireless communication setups to gauge signal strength and facilitate adjustments for RF front-end and baseband processors. An RSSI circuit aiming to assess signal strength and, consequently, regulate transmitter power for mobile communications is presented in [11], showcasing the mechanism for detecting the received signal strength and using that information to make adjustments. For an application involving a 10.7 MHz intermediate frequency (IF), ref. [12] presents an RSSI design that employs a folded diode load with an in-depth analysis of its suitability within the specified IF application. Reference [13] showcases a design of an RSSI system tailored to gauge the intensity of an IF input in terms of its power. The system's purpose is to enable adjustments to optimize performance within wireless communications setups.

Logarithmic detectors are a good choice for RSSI systems because of their fast impulse response and settling time, and, if designed effectively, they can have a linear behavior, which is ideal for detection. The objective of this work is to integrate these into UAVs powered with a 5.8 GHz WPT transmitter signal for the purpose of tracking and maintaining the uninterrupted charging of agricultural drones. This paper proposes a logarithmic detector designed using a 65 nm CMOS process, which acts as an RSSI system with high sensitivity and low power consumption in the WPT receiver. The input power for the RSSI system that needs to be detected is sent from the combination of a frequency synthesizer [14] and an antenna array system [15] acting as a WPT transmitter system (Figure 1). WPT is a technology that enables energy to be transmitted wirelessly to various devices which need their batteries to be charged whilst in motion. Various charging methods using magnetic induction have been used for charging the batteries of mobile, bioimplants, or wearable sensor devices [16,17]. However, these methods require a very precise alignment between the receiver and the transmitter. For drone charging, WPT systems are based on RF wave radiation in the Industry–Science–Medical (ISM) band using antenna arrays through which a radiated beam can be formed and focused on an arbitrary location or position of the receiver [18]. The WPT transmitter system comprises several key components, which include a microprocessor, a modular unit used for the up-conversion of the input signal, a phase-locked loop acting as a frequency synthesizer tasked with generating a fixed oscillating signal, filters, and a power amplifier designed to amplify the output signal and match its output impedance to the antenna.

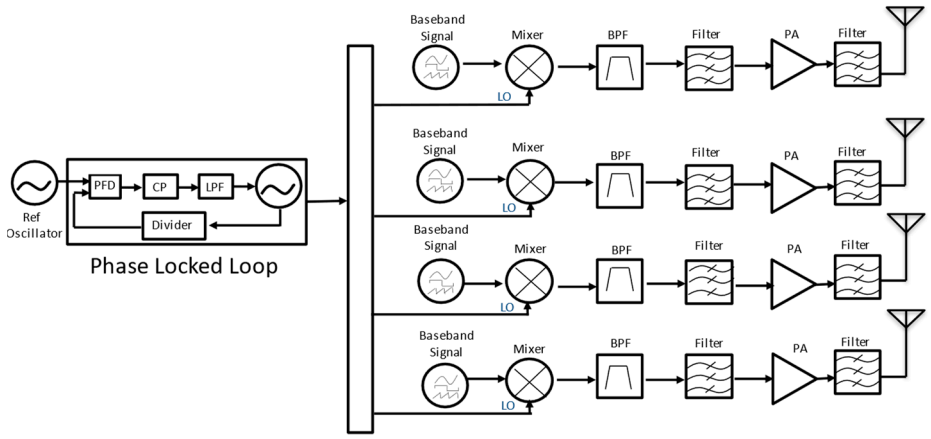

Figure 1. WPT transmitter architecture.

In this paper, first, the behavior and functionality of the RSSI system are presented, and its key parameters are defined, followed by the methodology of how the system specifications are calculated and obtained. Furthermore, the functioning of the RSSI circuits (limiting amplifier and full-wave current–rectifier design) is explained. Finally, the simulation results are discussed at the end of the paper.

2. RSSI System

An RSSI is typically employed to represent the strength of the signal that has been received. This indicator serves the dual purpose of adjusting the amplification levels in both the RF front-end and baseband processors and powering down the receiver when there is no signal. To accommodate the wide dynamic range of received signals within a limiting range of indications, an RSSI is typically implemented in logarithmic form. The logarithmic amplifier, utilized in a successive-detection architecture, is a fundamental component for achieving this. It consists of multiple full-wave rectifiers and a low-pass filter, working in tandem with existing limiting amplifier circuits. Consequently, the successive-detection approach is recognized for its power efficiency [12]. The RSSI circuit presented in Figure 2 is based on a successive-detection architecture.

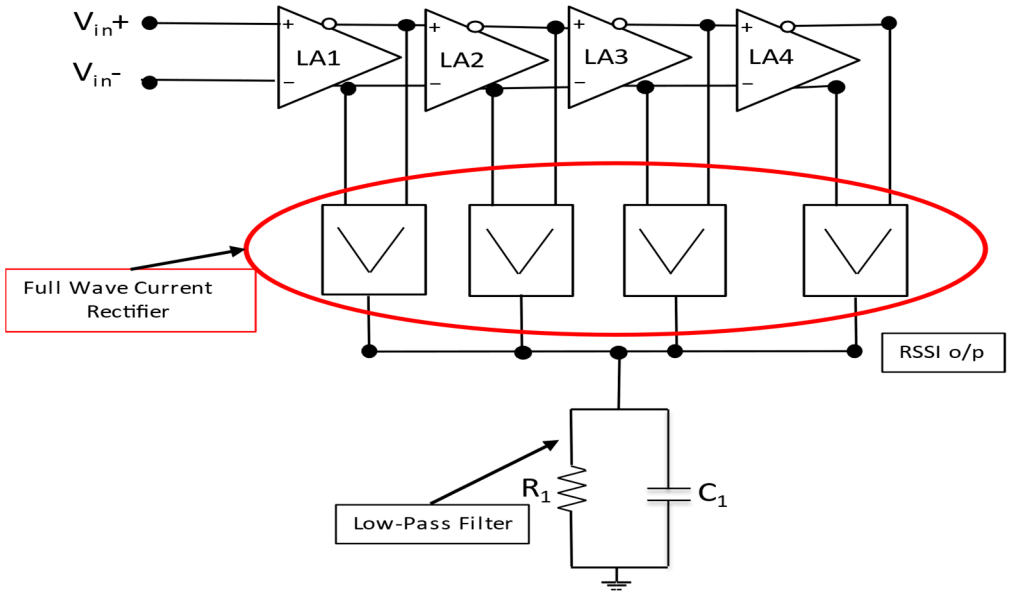

Figure 2. RSSI conventional circuit architecture.

This architecture consists of (a) multistage limiting amplifiers with the same saturation voltage that produce an output with logarithmic behavior, (b) a rectifier after each limiting amplifier yielding the magnitude of its input, and (c) a low-pass filter (LPF) that generates an output proportional to the level of the input. In the successive-detection architecture, the *RSSI* value is the sum of the output of all the branches. This is indicated in the equation below:

$$RSSI(V_I) = \sum_{i=0}^{N} x_i(V_I) \quad (1)$$

where N is the number of limiting amplifiers and $x_i(V_I)$ is the DC-level output of each limiting amplifier used with the rectifier's output, given by $A^i v_I(t)$.

Moreover, the RSSI dynamic range is the range of the input power that can be detected [10]. In other words, the RSSI dynamic range is where the RSSI output is linear in dB. Assuming all the limiting amplifiers have the same gain A, the dynamic range of an RSSI system is usually obtained by using Equation (2), where A is the gain of each limiting gain cell and N is the number of limiting stages.

$$20log_{10}(A^N) \quad (2)$$

The system proposed in this paper is a highly effective RSSI with linear behavior designed using CMOS 65 nm technology. The architecture used for the proposed RSSI is a successive-detection logarithmic amplifier (SDLA) such as the one shown in Figure 2. This was chosen due to its wide dynamic range and its ability to provide a DC output, unlike other types of logarithmic amplifiers. It consists of limiting amplifiers, full-wave current rectifiers, and a low-pass filter at the end to remove the ripples at the output. In order to have minimum logarithmic error and a good dynamic range despite the variations in the power being converted to DC, four stages of identical amplifiers are used with reduced gain.

The RSSI system can be placed on the receiver side of a flying drone to detect the signal from the WPT transmitter. The transmitter is designed to emit a signal of 20 dBm power at 5.8 GHz. Assuming the transmitter and antenna gains are equal to 10 dB, we can deduce using Equations (3) and (4), using the free space propagation loss (*FSPL*) equation, that the power received by the designed RSSI system at 10 m from the transmitter is around −55 dBm.

$$FSPL = 20log_{10}(d) + 20log_{10}(f) + 20log_{10}\left(\frac{4\pi}{c}\right) - G_t - G_r \quad (3)$$

$$A = P_t - P_L(d) \quad (4)$$

In Equation (3), *FSPL* is the free space path loss, d is the distance from the transmitter, f is the frequency, c is the speed of light in a vacuum, and G_t and G_r are the antenna gains of the transmitter and receiver. In Equation (4), A is the received power, P_t is the transmitted power, and $P_l(d)$ is the free space path loss at the specified distance d.

The power specification is subsequently converted to voltage, assuming the input impedance to be 50 ohms, resulting in a received voltage of 0.41 Mv. We set the sensitivity level specification to 0.3 Mv in order to have 0.11 Mv as a safety margin. The desired specifications for RSSI are shown in Table 1.

Table 1. Desired RSSI specifications.

Specification	Value
Supply voltage	1 V
Frequency	5.8 GHz
Power	<30 Mw
Sensitivity level	<0.3 Mv
Dynamic range	50 Db
Technology	65 nm

3. RSSI Circuits

RSSI blocks, as mentioned earlier, have a set of liming amplifiers and rectifiers, with their outputs summed at the low-pass filter, to generate a voltage output proportional to the incoming input power. A limiting amplifier design is shown in Figure 3.

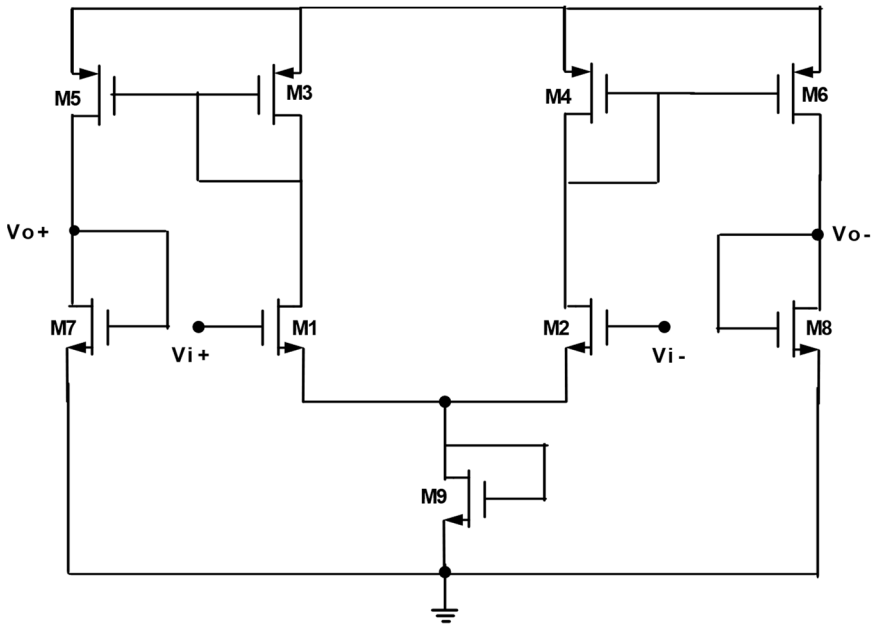

Figure 3. Limiting gain cell circuit schematic.

A limiting amplifier (LA) was chosen in this design rather than an automatic gain loop (AGC)-based design because (a) an LA structure is open-loop, (b) a cascaded LA saturates the output to a constant voltage level, and (c) an LA design is the most suitable for applications where the dynamic range required is large [10].

A traditional LA design with NMOS as the load transistor [11] has certain advantages; for example, it is easy to adjust its gain. However, the LA shown in Figure 3 is more convenient for the proposed application, as the NMOS load transistors in the limiting cells [12] suffer from the body effect, which impacts the gain and threshold voltage [18], resulting in (i) the need for higher power supply voltages to keep the transistor in the saturation region and (ii) higher power consumption for the given specification. The LA used in our design (Figure 3) has current mirrors formed by the combination of M_3–M_5 and M_4–M_6 which eliminate the body effect, enabling it to operate with a low power supply. However, by carefully choosing the transistor widths of the limiting cell shown in Figure 3, the gain of the amplifier is designed to be less than 1 (~0.3), unlike those in previous works where the limiting cell gain is more than 1 [9,10]. This is to ensure the proper rectification of the full-wave current rectifier (subsequent stage), as the input levels required are small in magnitude. Another reason for choosing such a design is it provides a high common-mode rejection ratio, a high power supply rejection ratio, and a large dynamic range due to its differentiality in nature [19,20].

An RSSI output in DC is more accurate to provide a rough estimate of the level of output power on the receiver side, as there is no phase contribution; only a fixed amplitude is present. Hence, the full-wave rectifier is an essential block of an RSSI system, as it converts the incoming AC signal to DC voltage. Moreover, a DC output is also easier to digitize, and it can be read on any system. Apart from these factors, full-wave current rectifiers are implemented in RSSI systems as the output of each individual stage can be easily summed without the use of any other block and as they convert voltage signals to current signals.

The full-wave rectifier design in Figure 4 involves one of the differential pairs (M_1–M_8 or M_2–M_6) scaled n times higher than the other. When the input voltage is low, the larger transistors (M_1 and M_8) primarily handle the current. Consequently, their respective current mirror experiences a higher current flow compared to the one connected to the smaller transistors. As the input voltage gradually increases, the smaller transistors (M_6 and M_2) begin to take on some of the current flow from the current mirror associated with them. This redistribution results in a decrease in the current flowing through the current mirror for the larger transistors [11]. When passed through a load, I_{out} provides a proportional DC voltage. This is represented in Equation (5).

$$I_{out} = (I_2 + I_3) - (I_1 + I_4) \tag{5}$$

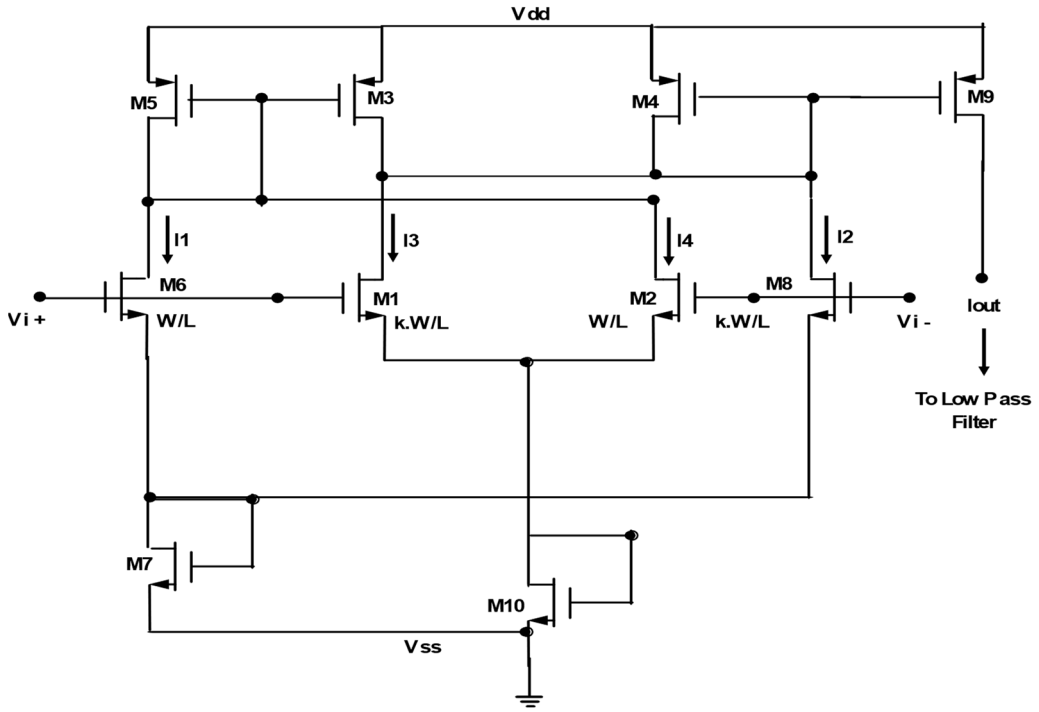

Figure 4. Full-wave current-rectifier circuit schematic.

4. Simulation Results and Analysis

An RSSI system employing multiple stages of a limiting amplifier and a full-wave rectifier was designed using TSMC (Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan) 1P9M 65 nm CMOS process technology, and the simulation results are presented based on individual blocks as well as the whole system. These simulations were carried out on schematics as well as on a post-layout extracted schematic, including all the parasitic capacitances and resistances, the pad capacitances, and the bond wire modeling, in order to ensure that the results are as close as possible to the measured result.

4.1. Limiting Cell

Simulations of the limiting cell, shown in Figure 3, were carried out in order to select the widths of the transistors corresponding to the gain and frequency performance. First, the size of the load transistors was varied to study its effect on the output. Figure 5 represents the V_{out} vs. V_{in} behavior of a limiting cell for different sizes of load transistors. It is clear in Figure 5 that the smaller the width of the load transistors (M_5 and M_6 in Figure 3), the higher the gain.

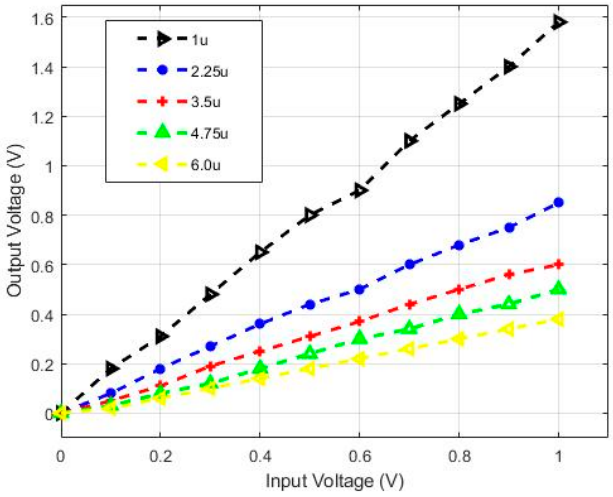

Figure 5. V_{out} vs. V_{in} of a limiting cell for different widths of NMOS load transistors.

The frequency response of a single-stage limiting cell is shown in Figure 6; its gain was adjusted to be 0.3 and the operating frequency is 5.8 GHz.

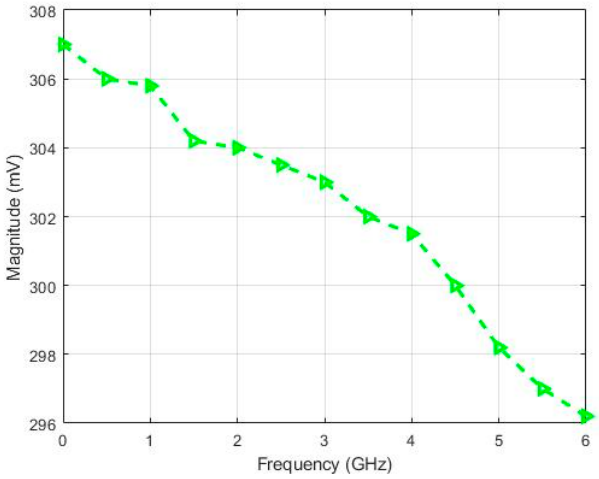

Figure 6. Frequency response of a single limiting cell.

The dynamic range of the designed system was calculated based on Equation (2). As a successive-detection architecture was used in the design, where the outputs of the stages are summed, the ideal dynamic range is calculated as below:

A = 0.3

N = 4

0.3^4 = 8.1 m

Dynamic Range = $20\log_{10}(8.1\text{ m}) = -40$ dB = 40 dB

4.2. Full-Wave Current Rectifier

Simulations were performed on the full-wave current rectifier in order to determine the transistor widths and the input signal at which the proper rectification takes place. For the tail current of the full-wave current rectifier shown in Figure 4, the diode-connected NMOS, M_7, and M_{10} were used instead of an ideal current source or NMOS with a voltage bias through the gate to consume less power.

To understand the input requirements of the rectifier before integrating it with the limiting amplifier, its output response is simulated for various sets of input voltages. It can be seen in Figure 7 that as the input of the rectifier increases beyond 100 µV, the rectification is not particularly strong, which is the reason that the gain of the limiting cell is set to 0.3—in order to obtain the proper rectification of the input signal.

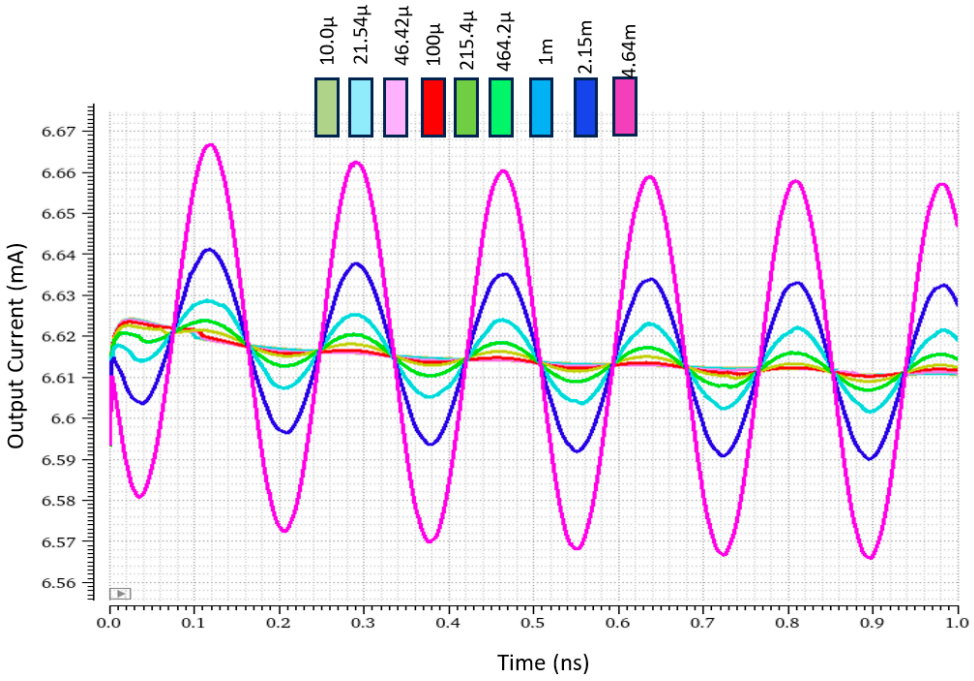

Figure 7. Output current given different input levels.

4.3. RSSI Circuit

Figure 8 represents the output response to the changes in the input voltage in all the stages, individually. It can be noticed that the output saturates faster with every additional stage, creating the desired logarithmic behavior (Figure 9). However, this behavior was observed when diodes were placed as rectifiers; hence, they have a very small dynamic range due to the required voltage drop across each diode. This means that the output must be greater than 0.7 V, which is why efficient full-wave rectifiers with high sensitivity are greatly desired.

The proposed cascaded RSSI system shown in Figure 2 was simulated to study the response between its output and input. As observed from Figure 10, input levels greater than 83 mV start producing an output with AC behavior rather than a rectified output. Figure 11 shows the RSSI output after each stage, respectively, through which it can be inferred that the output saturates faster with every additional cascaded stage. This fast impulse response is a result of the linear-in-dB behavior from the piece-wise logarithmic amplifier, which leads to the desired fast settling time. There is a slight delay due to the increased number of transistors in the propagation path.

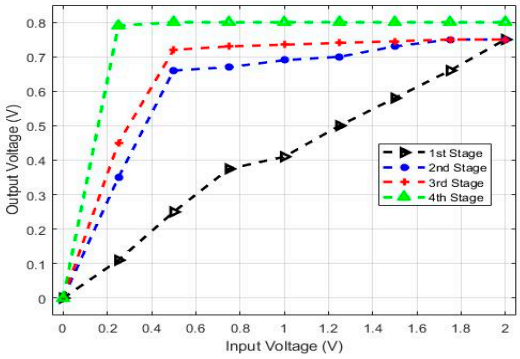

Figure 8. V_{out} vs. V_{in} at the individual stages in an RSSI circuit (1–4).

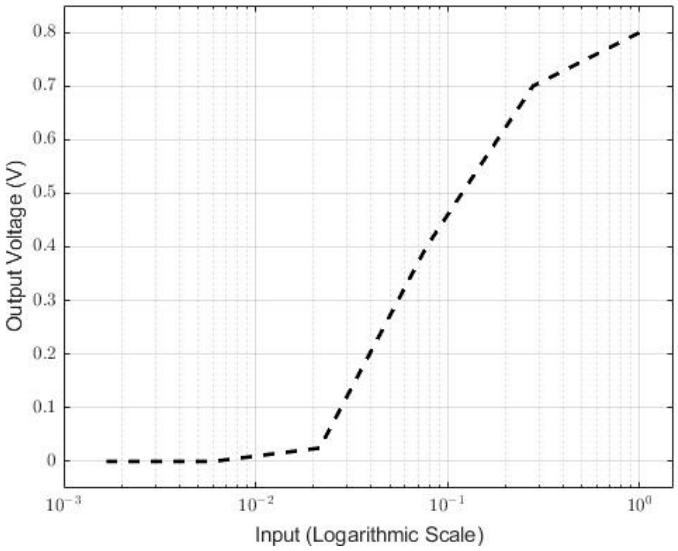

Figure 9. Output vs. input of the RSSI system showing logarithmic behavior.

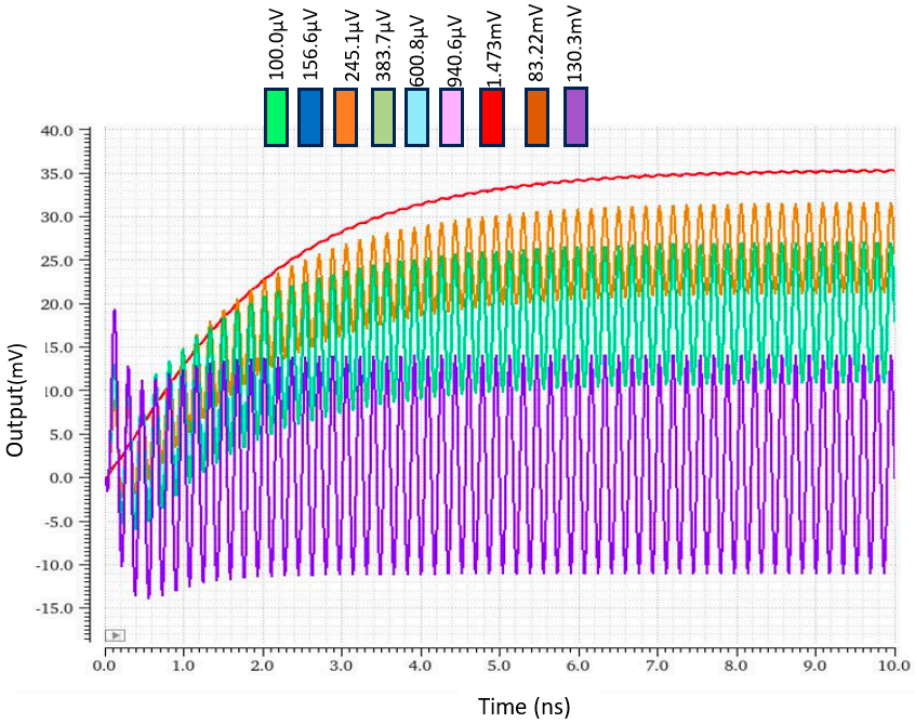

Figure 10. RSSI output over time at various input levels.

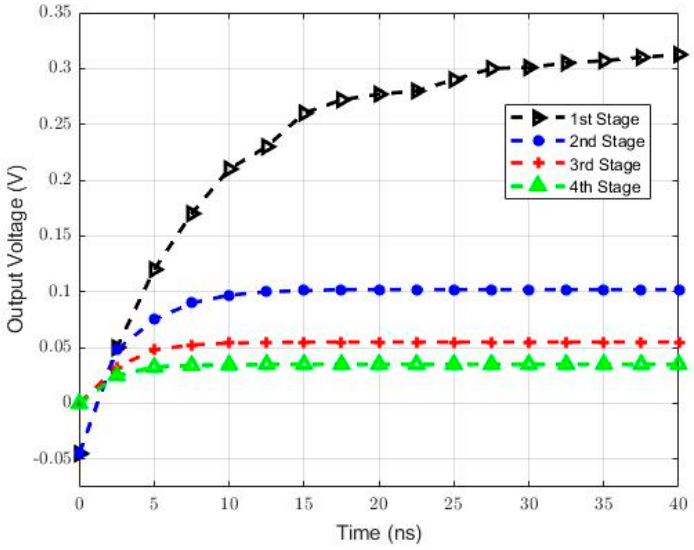

Figure 11. RSSI output from stages 1 to 4, respectively.

The proposed RSSI layout for this work, using a TSMC 65 nm GP process, is shown in Figure 12, where four cascaded limiting stages are followed by four full-wave current rectifiers in a successive-detection format. The output currents from all four full-wave current rectifiers are summed and the output is obtained from the low-pass filter, which is connected externally. The total area consumed by the layout, without the input/output pads, is 0.008 mm^2.

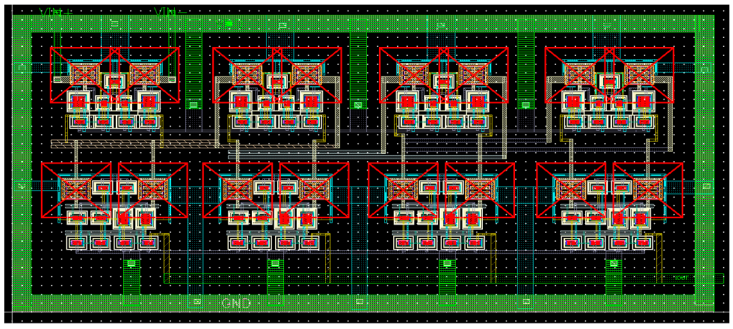

Figure 12. Proposed RSSI layout.

The V_{out} vs. V_{in} behavior of the schematic simulation and post-layout extracted simulation is shown in Figure 13. We can observe that the desirable linear-in-dB behavior is present in both simulations. Figure 14 represents the RSSI output of the schematic simulation and post-layout extracted simulation. It is clear that the settling time slightly increased in the post-layout simulation. Figures 15 and 16 represent the thermal and process variations in the output voltage. Temperature variation (Figure 15) was simulated between 0 and 85 °C for three process variations: FF (both NMOS and PMOS have high doping), TT (both NMOS and PMOS have typical doping), and SS (both NMOS and PMOS have minimal doping). The output voltage for each input voltage for all three processes, as mentioned earlier, is presented in Figure 16, with logarithmic input scaling, so as to show the logarithmic behavior of the RSSI circuit.

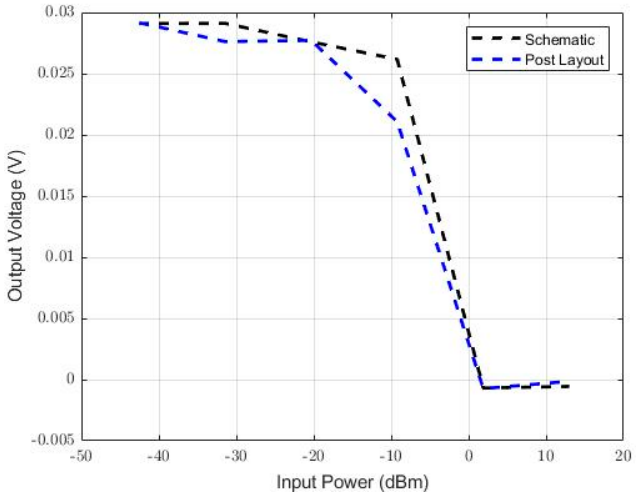

Figure 13. V_{out} vs. V_{in} of the schematic simulation and post-layout extracted simulation.

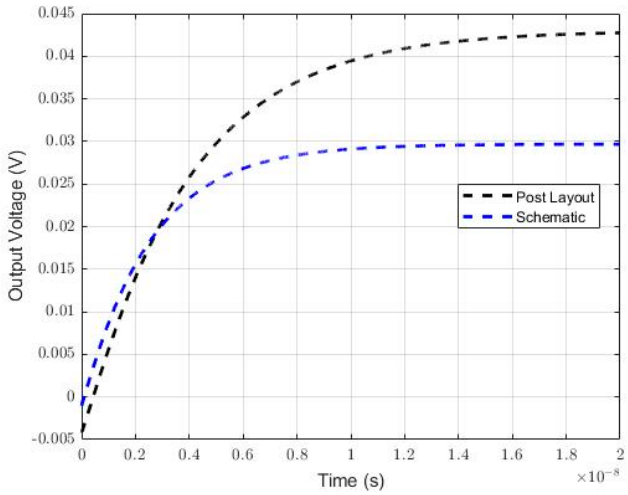

Figure 14. RSSI output of the schematic simulation and post-layout extracted simulation.

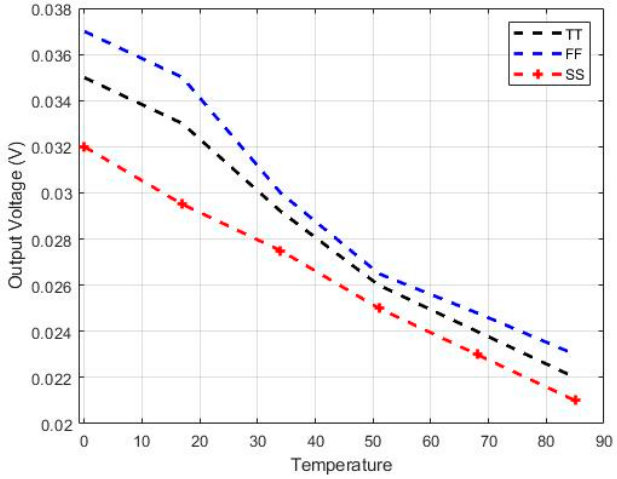

Figure 15. RSSI output across various temperatures for the three process corners.

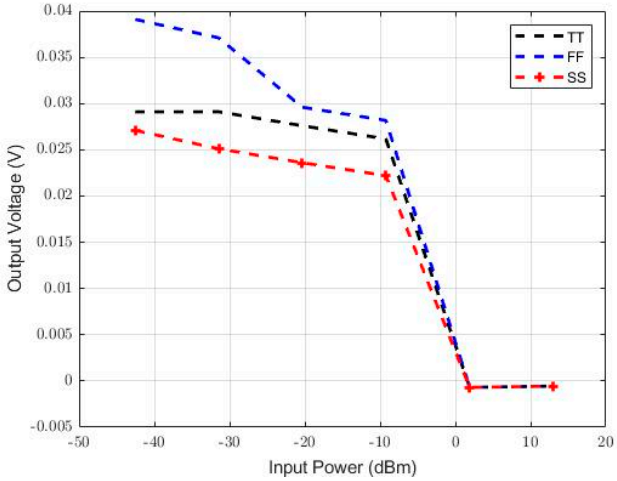

Figure 16. RSSI output at the three process corners.

As can be observed from Table 2 above, this is the first reported RSSI system implemented for WPT receivers operating at 5.8 GHz with the targeted application of charging drones midair. The performance of the system shows similar or better values for sensitivity, dynamic range, power, and logarithmic error, in comparison to the other referenced research. The dynamic range achieved is lower than that in previous works, but this is due to the fact that the other designs operated at much slower device speeds. In terms of sensitivity, the system presented in [9], designed and simulated using a similar 65 nm node, has the highest sensitivity level (30 mV/dBm), whereas the proposed system achieves 17 mV/dBm; however, the operating speed of the system in [9] is 290 times lower than that of the proposed system. The RSSI system designed in this work has a lower logarithmic error (0.4 dB) than those in other reported works. The power consumption of the proposed work (~2 mW) is also very similar in magnitude to that in other referenced research work, presented in Table 2.

Table 2. RSSI performance comparison of previous studies and this study.

	[9] Simulated	[10] Measured	[12] Measured	[13] Measured	[21] Measured	This Work: Simulated
Frequency	0.1–20 MHz	0.3–17 MHz	10.7 MHz	40 MHz	0.03–2.4 GHz	5.8 GHz
Dynamic Range	80 dB	56 dB	75 dB	56 dB	29–48 dB	34 dB
Power (mW)	1.2–2.9	1.8	6.2	9	30–44	2
Area (mm^2)	0.06	0.16	0.4	0.05	-	0.008
Logarithmic Error	1.4 dB	0.5 dB	1 dB	1 dB	-	0.4 dB
Sensitivity Level	30 mV/dBm	-	10 mV/dBm	-	13 mV/dBm	17 mV/dBm
Technology	65 nm	130 nm	0.6 um	130 nm	90 nm	65 nm

5. Conclusions and Future Work

In this paper, an RSSI system using TSMC CMOS 65 nm was designed and investigated for a wireless power transfer receiver. It is observed that the proposed RSSI design is a good choice due to its low number of performance errors, better sensitivity, linear-in-dB behavior, and higher frequency operation. This work successfully rectifies the targeted WPT signal at 5.8 GHz even with very small amplitudes, showing a sensitivity level of 17 mV/dBm, power consumption of 2 mW, a dynamic range of 34 dB, and logarithmic error of just 0.4 dB.

The results in this paper can be further improved by using delay-reduction techniques. In the future, RSSI can be implemented for real-time localization, and programmable reference bias currents can be used for the rectifiers to control the tradeoff between the dynamic range and detection sensitivity. The RSSI system can also be used for cybersecurity pur-

poses in wireless sensor networks for node authentication, localization, anomaly detection, jamming detection, attacks on the physical layer, and energy-efficient security [22,23].

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