

## Article

# Voltage Sag Mitigation Effect Considering Failure Probability According to the Types of SFCL

Joong-Woo Shin <sup>1</sup>, Young-Woo Youn <sup>1,\*</sup> and Jin-Seok Kim <sup>2,\*</sup><sup>1</sup> Korean Electrotechnology Research Institute, Gwangju Metropolitan City 61751, Republic of Korea<sup>2</sup> Department of Electrical Engineering, Osan University, Osan 18119, Republic of Korea

\* Correspondence: ywyoun@keri.re.kr (Y.-W.Y.); redwolf832@gmail.com (J.-S.K.);

Tel.: +82-10-8818-7439 (Y.-W.Y.); +82-10-4514-6494 (J.-S.K.)

**Abstract:** The development of industrial technology is based on electronic devices that are sensitive to power quality. Thus, the demand for high-quality and reliable power supplies is increasing. Voltage sag results in severe problems in the manufacturing process of power quality-sensitive industrial loads. When a fault occurs in a multi-ground power distribution system, the magnitudes of the fault current and voltage sag in the faulted and nonfaulted feeders become high. Hence, installing a superconducting fault current limiter (SFCL) is an effective method of compensating for fault current limitation and voltage sag. This study evaluates the effects of improving the magnitude, duration, and frequency of the voltage sag according to the type of SFCL used. First, a fault in the power distribution system is analyzed using PSCAD/EMTDC, a power system simulation software, according to the fault current-limiting element (CLE) and the type of SFCL. Second, the expected voltage sag frequency caused by a feeder fault in the power distribution system is assessed. Finally, the voltage sag improvement effect according to the CLE and the type of SFCL are compared. The trigger-type SFCL with a resistor as a CLE has been evaluated and found to be effective in improving voltage sag.

**Keywords:** superconducting fault current limiter (SFCL); voltage sag; power quality; power distribution reliability



**Citation:** Shin, J.-W.; Youn, Y.-W.; Kim, J.-S. Voltage Sag Mitigation Effect Considering Failure Probability According to the Types of SFCL. *Energies* **2023**, *16*, 625. <https://doi.org/10.3390/en16020625>

Academic Editors: Juan-José González de la Rosa, Olivia Florencias-Oliveros and Sara Sulis

Received: 6 December 2022

Revised: 22 December 2022

Accepted: 30 December 2022

Published: 4 January 2023



**Copyright:** © 2023 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

## 1. Introduction

The fault current and voltage sag in a power distribution system increase due to the increase in the power generation capacity and the parallel operation of the power system for a stable power supply. Voltage sag affects industrial loads that are sensitive to power quality, such as PLCs (programmable logic controllers) and magnetic contactors [1]. Therefore, the applications of the distribution static synchronous compensator, energy storage system, unified power quality conditioner, and dynamic voltage regulator to improve voltage sag have been investigated [2–4].

Most voltage sags occur under fault conditions [1–7], thus studies have been conducted to identify the relative location and types of faults that cause voltage sag [6] and to calculate the voltage sag [7]. Superconducting fault current limiters (SFCLs) play an important role in limiting fault currents and mitigating voltage sag in a power distribution system, and various studies have been conducted on these protection devices [8–11]. Recently, using these characteristics of SFCLs, studies on the low voltage ride-through enhancement effect have been conducted [12–14]. Previous studies have only evaluated the mitigation effect of voltage sag magnitude. However, the quantitative effectiveness analysis of the voltage sag mitigation was insufficient because no assessment of the expected frequency of voltage sag was performed.

Voltage sags occur on a nonfaulted feeder in the event of a fault. Therefore, the expected frequency of the voltage sag in the nonfaulted feeder can be evaluated using the

expected frequency of the feeder fault [5]. Reference [15] evaluated voltage sag mitigation resulting from resistive-type SFCL installation in terms of magnitude and frequency. However, because the fault current and voltage sag characteristics differ according to the R/X ratio of the fault impedance, the analysis of various current-limiting elements (CLEs) is required. Thus, this study analyzes the installation effect of the resistive- and trigger-type SFCLs in a power distribution system in terms of voltage sag. The CLE of the trigger-type SFCL comprises an inductor; thus, the fault impedance R/X ratio of this SFCL and that of the resistive-type SFCL differ. Hence, the voltage sag is different even if the impedances are equal. Additionally, the frequency of the voltage sag of a nonfaulted feeder was evaluated based on the failure rate, which is determined by the fault location on the faulted feeder. Thus, we analyze the magnitude, duration, and frequency of the mitigation effect on the voltage sag of the power distribution system according to the type of SFCL, which assists in selecting the SFCL type based on the load requirements.

## 2. Impact of SFCL Types on Power Distribution Systems

Here, the effects of SFCL installation on the distribution system are introduced from the perspective of fault analysis. The modeling of a simple test power distribution system and the effect of improving the magnitude of the voltage sag according to the SFCL type are discussed.

### 2.1. Test Power Distribution System Model

In this study, the effect and failure probability of a feeder depending on the fault location in a simple power distribution system have been evaluated. If the fault is far from the bus, the magnitude of the voltage sag is reduced because of the fault impedance. Conversely, if the fault is close to the bus, the magnitude of the voltage sag increases. Figure 1 illustrates a simple 22.9 kV power distribution system that is used to simulate various fault locations. This distribution system consists of long, medium, and short-distance feeders, as well as the main transformer, bus, circuit breakers, distribution transformers, and SFCLs. Feeder 1 (F1), with its long length and light loads, supplies power to loads in rural areas. Feeder 2 (F2), which has a shorter line than F1 and can handle larger loads, supplies power to a suburban area. Feeder 3 (F3) is a short, heavily loaded feeder that supplies power to urban areas. SFCLs at the starting point of the feeder limit the fault current in the case of a fault and compensate for the voltage sag of the bus [8–11]. The faulted feeder undergoes a power outage, whereas the nonfaulted feeder experiences a voltage sag during a fault. The load loss of the faulted feeder can be evaluated using a probabilistic approach. Therefore, the voltage sag frequency of the nonfaulted feeder can be analyzed using the failure rate of the faulted feeder location [5].

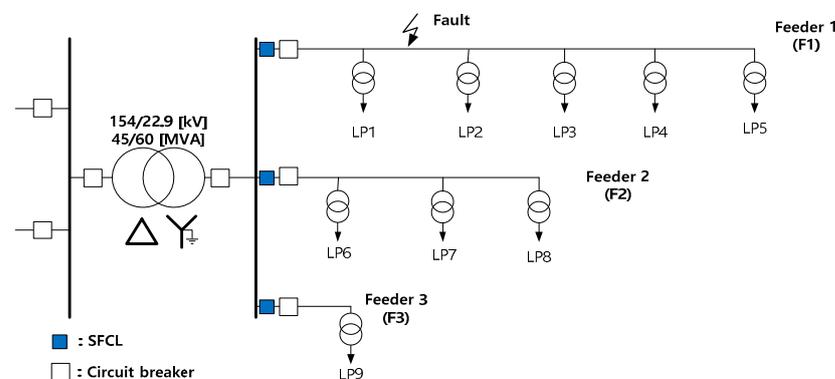


Figure 1. Test power distribution system model with SFCLs on each feeder [16].

Tables 1 and 2 list the parameter settings of the 22.9 kV multi-ground power distribution system and the data for the load points [10,15]. The parameters in Table 1 are input data of the PSCAD/EMTDC simulation in the event of a feeder fault, and the load data in

Table 2 is used to assess the probability of the feeder fault and the acceptability affected by the fault. The impact of the fault is evaluated as a voltage sag.

**Table 1.** Parameter settings of the test power distribution system.

Component	Specification	Value	Unit
	Source	Voltage	154
	Impedance	j0.87	%
M. Tr	Capacity	45	MVA
	Primary voltage	154	kV
	Secondary voltage	22.9	kV
	Impedance	j15	%
Line (ACSR 160 mm <sup>2</sup> )	Z <sub>0</sub>	10.8 + j23.6	%/km
	Z <sub>1</sub> , Z <sub>2</sub>	3.48 + j7.44	%/km

**Table 2.** Data of load points.

Load Point	Data	Load [MVA]	Number of Customers	Line Length [km]
	F1 (rural)	LP1	1.5	414
LP2		1.5	345	4
LP3		1.5	366	3.5
LP4		1.5	320	8
LP5		1.5	150	6
F2 (suburban)	LP6	2.5	690	5
	LP7	2.5	620	4.5
	LP8	2.5	575	5.5
F3 (urban)	LP9	5.5	1375	3
Total		20.5	4855	46.5

## 2.2. Modeling of an SFCL

In this study, the SFCL model was considered based on quenching and recovery characteristics. The resistance of the SFCL with time  $t$  is represented using Equation (1), where  $R_n$  represents the saturated resistance and  $T_F$  is the time constant until the saturation resistance is reached.  $t_0$  and  $t_n$  represent the times of quench initialization and  $n$ th recovery, respectively.  $a_n$  and  $b_n$  are the slopes of the  $n$ th recovery and values of the initial resistance [8–10,16,17].

$$R_{SC}(t) = \begin{cases} \text{and } 0 & (t \leq t_0) \\ \text{and } R_n \left[ 1 - \exp\left(-\frac{t-t_0}{T_F}\right) \right]^{\frac{1}{2}} & (t_0 \leq t \leq t_1) \\ \text{and } a_1(t-t_1) + b_1 & (t_1 \leq t \leq t_2) \\ \text{and } a_2(t-t_2) + b_2 & (t \geq t_2) \end{cases} \quad (1)$$

As shown in Figure 2, the trigger-type SFCL comprises a high-temperature superconductivity (HTSC) element that senses and limits fault currents, a mechanical switch (SW) that switches the current path, and a CLE that limits fault currents [18].

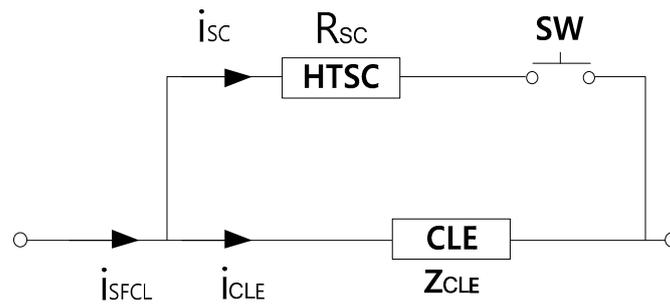


Figure 2. Configuration of the trigger-type SFCL.

In fault situations, the HTSC detects a fault and limits the fault current through quenching. After a few cycles, the SW operates, and the CLE, which is in parallel with the HTSC, operates as shown in Figure 3. After the SW is operated, the magnitude of the bus voltage sag depends on the impedance of the CLE.

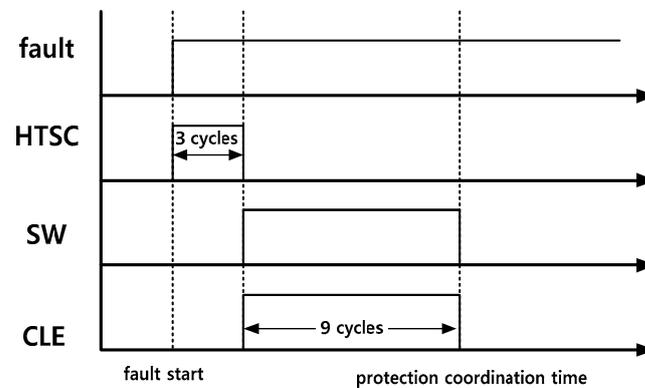


Figure 3. Operation sequence of a fault: HTSC, SW, and CLE.

The voltage sag index evaluates the voltage sag maintained for at least one cycle [19]. In this study, despite permanent faults, after the protection coordination time, the bus voltage sag recovered to the rated voltage. The parameters of the SFCL are listed in Table 3.

Table 3. Parameter settings of the SFCL.

HTSC Element	Value	Unit
Convergence resistance ( $R_n$ )	1.5	$\Omega$
Current-limiting reactor, resistor (CLE)	2, j2	$\Omega$
Switching operation time (after quench)	3	cycles
Time constant ( $T_F$ )	0.01	s
Critical current ( $I_C$ )	1200	A
1st and 2nd recovery slopes ( $a_1, a_2$ )	-80, -160	1/s

### 2.3. Voltage Sag Mitigation

When a fault occurs on a feeder, among the lines of the main transformer in a power distribution system, the bus voltage is represented by Equation (2). The faulted feeder undergoes a power outage, whereas the nonfaulted feeder experiences a voltage sag during the fault duration.

$$v_{bus.f} = \frac{Z_l}{Z_S + Z_t + Z_l} \times v_{rate} \tag{2}$$

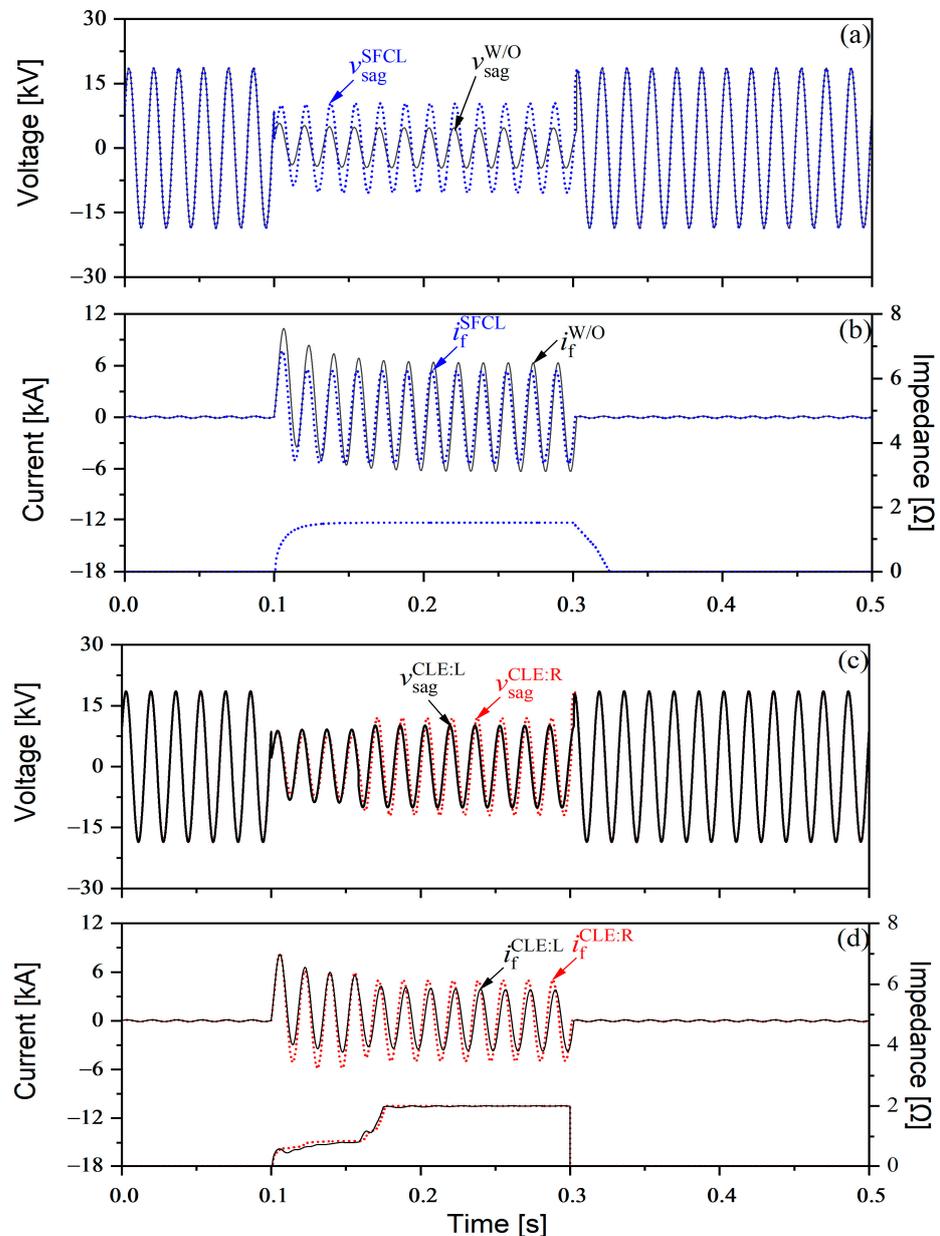
where,  $Z_S$  is the impedance of the source,  $Z_t$  is the impedance of the main transformer,  $Z_l$  is the line impedance from the bus to the fault location, and  $v_{rate}$  is the rated voltage of the bus.

The impedance of the SFCL is maintained at zero in the steady state. However, when a fault occurs on the feeder with a fault current higher than the critical current of the HTSC element, the SFCL changes the impedance from zero to the design value. Subsequently, the SFCL limits the fault current and compensates for voltage sag on the bus.

$$v_{bus.f}^{SFCL} = \frac{Z_l + Z_{SFCL}}{Z_s + Z_t + Z_l + Z_{SFCL}} \times v_{rate} \quad (3)$$

where,  $Z_{SFCL}$  denotes the impedance of the SFCL. A single line-to-ground fault (SLGF) is the most frequent type of fault in a power distribution system.

The simulation results from PSCAD/EMTDC, in which the voltage is analyzed at the bus and the fault current is measured at the faulted feeder according to the design of the SFCL, 1 km away from the bus, are shown in Figure 4.



**Figure 4.** Bus voltage sag and fault current waveforms. (a) Bus voltage waveforms obtained when a resistive SFCL is applied. (b) Current waveforms obtained when a resistive SFCL is applied. (c) Bus

voltage waveforms obtained when a trigger-type SFCL (CLE: R, L) is applied. (d) Current waveforms obtained when a trigger-type SFCL (CLE: R, L) is applied.

The permanent SLGF was generated in 0.1 s, and the circuit breaker operated in 0.3 s to eliminate the SLGF.  $v_{\text{sag}}^{\text{SFCL}}$ ,  $v_{\text{sag}}^{\text{W/O}}$ ,  $i_{\text{f}}^{\text{SFCL}}$ , and  $i_{\text{f}}^{\text{W/O}}$  denote the voltage sag of the bus and the fault current when the resistive-type SFCL is and is not applied at F1, respectively.  $v_{\text{sag}}^{\text{CLE:R}}$ ,  $v_{\text{sag}}^{\text{CLE:L}}$ ,  $i_{\text{f}}^{\text{CLE:R}}$ , and  $i_{\text{f}}^{\text{CLE:L}}$  denote the voltage sag of the bus and the fault current, with the SFCL having different characteristics according to the CLE: R (resistor) and CLE (inductor) of the trigger-type SFCL, respectively. At various installation locations, despite the effectiveness of the SFCL in reducing the fault current, the voltage sag is only improved on the feeder [20].

### 3. Analysis of the Effect of SFCL Types on the Frequency of Voltage Sags

Here, the installation effects of different types of SFCLs were analyzed through failure analysis and probabilistic methods. For the application of probabilistic methods, we only consider the SLGF, the most common type of fault in power distribution systems. The magnitude and duration of the voltage sag due to the SLGF, evaluated through PSCAD/EMTDC, are associated with the expected frequency experienced per customer using probabilistic methods.

#### 3.1. Method of Evaluating the Frequency of Voltage Sag

The voltage sag frequency index (SFI) represents the frequency of the bus voltage sag, with a certain magnitude and duration; it is denoted as  $SFI_x^y(i_k)$  with a magnitude of less than  $x\%$  at time  $y$ , which has fault distance  $k$  in feeder  $i$  [21]. The SFI is evaluated as the sum of feeder fault rates from the bus at  $k$ . The SFI is evaluated as the RMS value at which the voltage sag is maintained for at least one cycle [19,22]. Therefore, in this study, the voltage sag compensated through the HTSC has a single RMS value because the duration of the voltage sag variation from quenching to convergence resistance is too short. The cases and results of evaluating the SFI with both characteristics by fault location in the test power distribution system are listed in Table 4. As shown in Case 0, when a fault occurs at 0.33 km from the bus, the magnitude of the bus voltage is less than 10% of the rated bus voltage in the steady state. Simultaneously, loads of other nonfaulted feeders experience a power outage. In Case 1, the resistive-type SFCL at the starting point of the feeder prevents voltage sags for magnitudes of 0–50%, because the HTSC element compensates for up to 50%. In Cases 2 and 3, as shown in Figures 2 and 3, the durations of the voltage sag are divided into two states: before and after operating the SW. According to the operation of the SW, the voltage sag is compensated through the HTSC element and CLE. Despite the SFCL, a voltage sag with a magnitude of 40–50% occurs in Case 3. In contrast to Cases 1 and 2, the voltage sag is only shown when the inductance of the SFCL is applied. Thus, the voltage sag mitigation achieved using the resistor was more effective than that achieved using the inductor. In Cases 2 and 3, as the magnitude of the voltage sag increases, the difference between cycles 3 and 9 increases because the fault impedance increases according to the distance of the fault location from the bus.

#### 3.2. Impact of SFCL Types on Power Distribution Systems

The System Average RMS Variation Frequency Index (SARFI) is a conventional index of voltage sags measured anywhere [19,22]. However, in this study, we evaluated the mitigation effect of voltage sags on customers in a power distribution system using a feeder fault with the sensitivity of SARFI (S-SARFI) [15].

$$S - \text{SARFI}_x^y(i_k) = \frac{SFI_x^y(i_k) \times (N_T - N_T^i)}{N_T}, \quad (4)$$

where,  $N_T$  is the total number of customers in the power distribution system, and  $N_T^i$  is the customer supplied through feeder  $i$ .

**Table 4.** Voltage sag by fault location.

Case 0 (without SFCL)																		
x * [%]	0~10		10~20		20~30		30~40		40~50		50~60		60~70		70~80		80~90	
y [cycles]	12		12		12		12		12		12		12		12		12	
Fault location [km]	0.33		0.75		1.28		1.95		2.9		4.3		6.6		1.16		26.4	
Case 1 (with resistive-type SFCL, 1.5[Ω])																		
x * [%]	0~10		10~20		20~30		30~40		40~50		50~60		60~70		70~80		80~90	
y [cycles]	12		12		12		12		12		12		12		12		12	
Fault location [km]	-		-		-		-		-		2.05		4.75		11		26.4	
Case 2 (with trigger-type SFCL, HTSC: 1.5[Ω], CLE: resistor 2[Ω])																		
x * [%]	0~10		10~20		20~30		30~40		40~50		50~60		60~70		70~80		80~90	
y [cycles]	3	9	3	9	3	9	3	9	3	9	3	9	3	9	3	9	3	9
Fault location [km]	-	-	-	-	-	-	-	-	-	-	2.05	-	4.75	3.63	11	8.85	26.4	26.4
Case 3 (with trigger-type SFCL, HTSC: 1.5[Ω], CLE: inductor j2[Ω])																		
x * [%]	0~10		10~20		20~30		30~40		40~50		50~60		60~70		70~80		80~90	
y [cycles]	3	9	3	9	3	9	3	9	3	9	3	9	3	9	3	9	3	9
Fault location [km]	-	-	-	-	-	-	-	-	-	0.4	2.05	2.0	4.75	4.5	11	9.4	26.4	26.4

\* Percentage relative to the rated bus voltage in case of a fault.

Tables 5 and 6 show the expected frequency of voltage sag in load as evaluated in cases 2 and 3, respectively. The results of the voltage sag in the three cycles of Cases 2 and 3 are like those in Case 1. The voltage sag duration of the trigger-type SFCL was evaluated as a voltage sag with three and nine cycles, and it was compensated for by the HTSC element and CLE, respectively. The fault rate per kilometer of the feeder is given in Reference [23]. As shown in Table 5, when the CLE has a high resistance, no fault occurs where the magnitude of the bus voltage is less than 50% in another feeder. However, as shown in Table 6, when the CLE of the trigger-type SFCL is an inductor, faults occur, and the magnitude of the bus voltage is less than 50% after SW is opened. When each CLE has the same impedance, the fault current limitation and voltage compensation, depending on the R/X ratio of the power distribution system, differ. Consequently, as shown in Table 6, the voltage compensated through the HTSC element does not result in a voltage sag of 40–50% of the bus voltage magnitude. However, when the voltage is compensated using the inductor, the voltage sag becomes 40–50% of the bus voltage. This indicates that a 1.5 Ω resistor can improve the voltage sag better than a j2 Ω inductor, depending on the impedance at the fault distance. Generally, a power distribution system has a high R/X ratio. The results of F1, F2, and F3 converged to different values because the feeder lengths differed. In the case of a fault in F3, the frequency of the voltage sag that is greater than 70% equals the frequency of the voltage sag with a magnitude of 60–70%. The faults on F3 occur near the bus owing to its length and the absence of significant fault impedance.

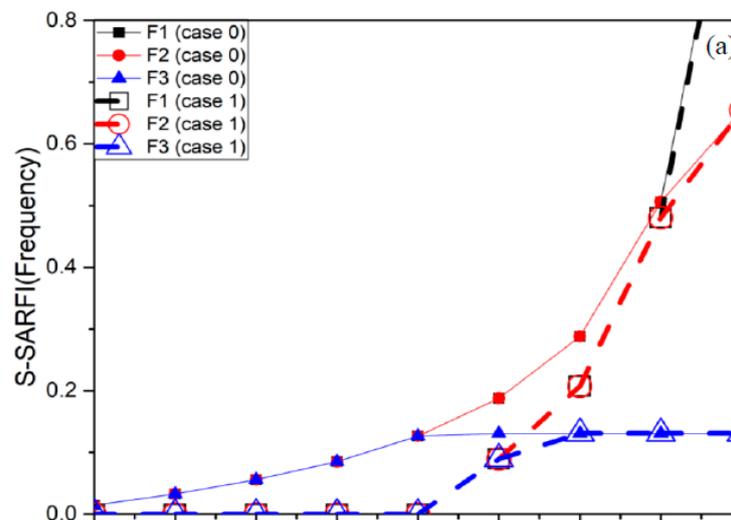
**Table 5.** S-SARFI frequency according to the voltage sag with the magnitude and duration given in Case 2.

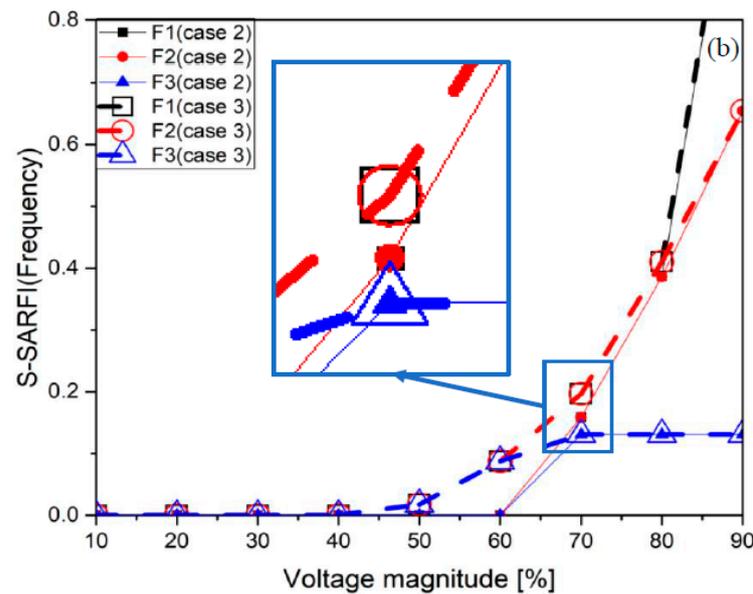
K		F1				F2				F3					
y[cycles]		3		9		3		9		3		9			
x[%]															
0~40		-		-		-		-		-		-		-	
40~50		-		-		-		-		-		-		-	
50~60		0.089		-		0.082		-		0.096		-		-	
60~70		0.207		0.158		0.189		0.144		0.140		0.140		0.140	
70~80		0.480		0.386		0.437		0.352		0.140		0.140		0.140	
80~90		1.152		1.152		0.596		0.596		0.140		0.140		0.140	

**Table 6.** S-SARFI frequency according to the voltage sag with the magnitude and duration given in Case 3.

		F1		F2		F3	
		3	9	3	9	3	9
x[%]	y[cycles]						
0~40		-	-	-	-	-	-
40~50		-	0.017	-	0.016	-	0.019
50~60		0.089	0.087	0.082	0.080	0.096	0.093
60~70		0.207	0.196	0.189	0.179	0.140	0.140
70~80		0.480	0.410	0.437	0.374	0.140	0.140
80~90		1.152	1.152	0.596	0.596	0.140	0.140

The results of Tables 5 and 6 and the resistive-type SFCL are shown in Figure 5. As shown in Figure 5a, the resistive-type SFCL installed on F3 improves the voltage sag of 50% or less of the bus voltage by 0.12 frequency/customers per year. In the test power distribution system, 3480 customers were expected to experience voltage sags owing to the F3 fault, and voltage sags of 417.6 per year were expected to be reduced when installing the resistive-type SFCL. As shown in Figure 5b, when the voltage is at least 70% of the steady-state bus voltage, the voltage sag frequency in Case 2 is lower than that in Case 1. As the impedance ratio increased according to the fault position, the voltage sag mitigation effect increased compared with the fault current reduction effect. Therefore, the effective configuration of the SFCL can be determined using the impedance ratio of the system.

**Figure 5.** Cont.



**Figure 5.** S-SARFI by cases: (a) applying a resistive-type SFCL, and (b) applying a trigger-type SFCL with a resistor and inductor as a CLE.

#### 4. Conclusions

This study analyzed the mitigation effect of voltage sag by SFCLs through a fault analysis and probabilistic evaluation of the power distribution system to evaluate the types of SFCLs and the installation priority of the feeder constituting the power distribution system. Based on the analyses, the CLE, which is a resistor, had a higher voltage sag mitigation effect than an inductor. However, in the case of the inductor, the frequency of the voltage sag did not change rapidly with magnitude. Therefore, an inductor can effectively improve voltage deflection in a certain voltage range. This is due to the change in the fault impedance ratio based on the CLE. The ratio of the fault impedance was not absolute because the fault-impedance ratio varied with fault position.

The SFCL was mainly installed for fault current reduction. However, the installation of the SFCL next to a feeder is an excellent option for protecting power quality-sensitive loads in a power system. The installation of an efficient SFCL power distribution system requires a quantitative evaluation of the fault current and voltage sag mitigation effects through fault and probabilistic analyses of various power distribution facilities. In addition, in this study, all types of faults were considered SLGFs. Because the magnitude of the voltage sag varies depending on the type of fault, it is necessary to evaluate the voltage sag mitigation effect of the magnitude and expected frequency of the SFCL for various types of faults.

**Author Contributions:** Methodology and formal analysis, J.-S.K.; Writing—original draft preparation and writing—review and editing, J.-W.S.; Project administration and funding acquisition, Y.-W.Y. All authors have read and agreed to the published version of the manuscript.

**Funding:** This work was partially supported by the Korea Institute of Energy Technology Evaluation and Planning (KETEP) grant funded by the Korean government (MOTIE) (20193610100010) and an Osan University research grant in 2022.

**Institutional Review Board Statement:** Not applicable.

**Informed Consent Statement:** Not applicable.

**Data Availability Statement:** Not applicable.

**Conflicts of Interest:** The authors declare no conflict of interest. The funder had no role in the design of the study, including the collection, analyses, or data interpretation, writing of the manuscript, or decision to publish the results.

## References

1. Santiago, A.-G.; Oscar, A.R.-G.; Garcia-Arias, L.P.; Maria, J.-G.; Cardona-Orozco, P.D.; Armando, J.U.-F.; Eduardo, A.C.-P.; Salazar-Jiménez, A.F. Analysis of Voltage sag severity case study in an industrial circuit. *IEEE Trans. Ind. Appl.* **2016**, *53*, 15–21.
2. Haque, M.H. Compensation of distribution system voltage sag by DVR and D-Statcom. In Proceedings of the 2001 IEEE Porto Power Tech Proceedings, Porto, Portugal, 10–13 September 2001; Volume 1.
3. Samineni, S.; Johnson, B.K.; Hess, H.L.; Law, J.D. Modeling and analysis of a flywheel energy storage system for voltage sag correction. *IEEE Trans. Ind. Appl.* **2006**, *42*, 42–52. [[CrossRef](#)]
4. Vilathgamuwa, D.M.; Ranjith-Perera, A.A.D.; San, S.C. Voltage sag compensation with energy optimized dynamic voltage restorer. *IEEE Trans. Power Deliv.* **2003**, *18*, 928–936. [[CrossRef](#)]
5. Heine, P.; Lehtonen, M. Voltage sag distributions caused by power system faults. *IEEE Trans. Power Syst.* **2003**, *18*, 1367–1373. [[CrossRef](#)]
6. Yalman, Y.; Uyanık, T.; Tan, A.; Bayındır, K.Ç.; Terriche, Y.; Su, C.-L.; Guerrero, J.M. Implementation of Voltage Sag Relative Location and Fault Type Identification Algorithm Using Real-Time Distribution System Data. *Mathematics* **2022**, *10*, 3537. [[CrossRef](#)]
7. Patra, J.; Pal, N. A Mathematical Approach of Voltage Sag Analysis Incorporating Bivariate Probability Distribution in a Meshed System. *Energies* **2022**, *15*, 7592. [[CrossRef](#)]
8. Moon, J.F.; Kim, J.S. Voltage sag analysis in loop power distribution system with SFCL. *IEEE Trans. Appl. Supercond.* **2013**, *23*, 561504.
9. Moon, J.F.; Lim, S.H.; Kim, J.C.; Yun, S.Y. Assessment of the impact of SFCL on voltage sags in power distribution system. *IEEE Trans. Appl. Supercond.* **2010**, *21*, 2161–2164. [[CrossRef](#)]
10. Kim, J.S.; Lim, S.H.; Kim, J.C.; Moon, J.F. A study on bus voltage sag considering the impedance of SFCL and fault conditions in power distribution systems. *IEEE Trans. Appl. Supercond.* **2013**, *23*, 5601604.
11. Zheng, Z.; Xiao, X.; Huang, C.; Li, C. Enhancing transient voltage quality in a distribution power system with SMEs-based DVR and SFCL. *IEEE Trans. Appl. Supercond.* **2018**, *29*, 5400405. [[CrossRef](#)]
12. Yoon, K.-H.; Shin, J.-W.; Kim, J.-C.; Lee, H.-J.; Kim, J.-S. Simulation of a Low-Voltage Direct Current System Using T-SFCL to Enhance Low Voltage Ride through Capability. *Energies* **2022**, *15*, 2111. [[CrossRef](#)]
13. Komijani, A.; Sedighzadeh, A.; Kheradmandi, M. Improving Fault Ride-Through in meshed microgrids with wind and PV by Virtual Synchronous Generator with SFCL and SMES. *J. Energy Storage* **2022**, *50*, 103952. [[CrossRef](#)]
14. Gireeshma, K.; Chandramohan, S. Enhancing LVRT capability of DFIG using cooperative control of BTFCL and RPC. *Automatika* **2022**, *64*, 1–12. [[CrossRef](#)]
15. Shin, J.W.; Kim, J.C.; Lee, H.J.; Yoon, K.H.; Chai, H.S.; Kim, J.S. Impact of SFCL according to voltage sags based reliability. *IEEE Trans. Appl. Supercond.* **2021**, *31*, 5600905. [[CrossRef](#)]
16. Kim, H.R.; Yim, S.W.; Oh, S.Y.; Hyun, O.B. Recovery in superconducting fault current limiters at low applied voltages. *IEEE Trans. Appl. Supercond.* **2008**, *18*, 656–659.
17. Lee, B.W.; Sim, J.; Park, K.B.; Oh, I.S. Practical application issues of superconducting fault current limiters for electric power systems. *IEEE Trans. Appl. Supercond.* **2008**, *18*, 620–623. [[CrossRef](#)]
18. Kim, J.S.; Lim, S.H.; Kim, J.C. Comparative analysis on current limiting characteristics of hybrid superconducting fault current limiters (SFCLs) with first half cycle limiting and non-limiting operations. *J. Electr. Eng. Technol.* **2012**, *7*, 659–663. [[CrossRef](#)]
19. Sabin, D.D.; Bollen, M.H. Overview of IEEE Std. 1564-2014 guide for voltage sag indices. In Proceedings of the 2014 16th International Conference on Harmonics and Quality of Power (ICHQP), Bucharest, Romania, 25–28 May 2014; pp. 497–501.
20. Kim, J.S.; Lim, S.H.; Kim, J.C. Bus-voltage sag suppressing and fault current limiting characteristics of the SFCL due to its application location in a power distribution system. *J. Electr. Eng. Technol.* **2013**, *8*, 1305–1309. [[CrossRef](#)]
21. Safdarian, A.; Fotuhi-Firuzabad, M.; Lehtonen, M. A general framework for voltage sag performance analysis of distribution networks. *Energies* **2019**, *12*, 2824. [[CrossRef](#)]
22. Arias-Guzman, S.; Ustariz-Farfan, A.J.; Plata, E.C.; Salazar-Jimenez, A.F. Implementation of IEEE Std 1564-2014 for voltage sag severity analysis on a medium voltage substation. In Proceedings of the 2015 IEEE Workshop on Power Electronics and Power Quality Applications (PEPQA), Bogotá, Colombia, 2–4 June 2015; pp. 1–6.
23. Chai, H.S.; Kang, B.W.; Kim, J.S.; Moon, F.F.; Kim, J.C. Study of drawing optimum switch automation rate to minimize reliability cost. *Trans. Korean Inst. Electr. Eng. P* **2015**, *64*, 297–302. [[CrossRef](#)]

**Disclaimer/Publisher’s Note:** The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.