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A Bidirectional Grid-Tied ZVS Three-Phase Converter Based on DPWM and Digital Control

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Abstract: In this paper, a bidirectional grid-tied ZVS three-phase converter is proposed. The circuit operation principle in both the rectifier and inverter modes was analyzed. The proposed topology could achieve zero-voltage switching in the six main switches and the auxiliary switch both in the rectifier mode and inverter mode. In addition, the reverse recovery current of body diodes in the main switches was also suppressed. Furthermore, in order to realize the ZVS control scheme under the grid-tied bidirectional power flow condition and reduce the number of switchings, a modified carrier-based discontinuous PWM was proposed to fit the bidirectional switching sequence. Finally, a 3 kW prototype was constructed. Some simulation and experimental results are presented to verify the validity of the proposed circuit topology and PWM control scheme.

Keywords: zero-voltage switching (ZVS); discontinuous pulse-width modulation (DPWM); bidirectional power flow; reverse recovery current; grid tied

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1. Introduction

In order to overcome the intermittency and instability of renewable energy, energy conversion plays an important role in the grid-tied and/or storage energy system.

In such a system, the bidirectional power flow converter highly affects the efficiency of the whole system. The three-phase, six-switch converter is the best choice and is widely used for bidirectional power flow control in many application fields, including motor drive, energy storage systems, uninterruptible power systems and renewable energy [1]. It has several advantages, such as lower current stress, high efficiency and a small input filter. However, the conventional hard switching scheme causes a significant switching loss [2]. In addition, due to the reverse recovery process, the body diodes of all switches will suffer higher loss and EMI problems. As a result, many techniques have been developed to make the converter operate in the soft-switching condition to reduce the switching loss and improve the conversion efficiency.

In recent years, numerous ZVS techniques have been extensively studied in AC/DC and DC/AC converters. The more common method is to add an auxiliary resonant circuit in these converters. According to the locations of the auxiliary circuit, the ZVS techniques can be divided into two categories, i.e., AC-side or DC-side auxiliary circuits [3]. The auxiliary circuit on the AC side is mainly connected in parallel with the AC side of the converter, and thus, the auxiliary circuit has lower voltage stress. However, the system needs three auxiliary circuits for three phases, making it require more space and components. For the DC-side auxiliary circuit, the auxiliary circuit is placed between the DC bus and the main switches, and only one set of auxiliary circuits is needed. However, different auxiliary circuit structures will result in varying voltage stresses on the main switches that are approximately 1 to 3 times the DC link voltage in the rectifiers [4–8] and inverters [2,9–21]. Active clamping ZVS rectifiers [7,8] and ZVS inverters [2,17–21] with low voltage stress (about 1.01~1.1 times the DC link voltage) were proposed. Nevertheless, extra components,

including an active switch, resonant inductor, and clamping capacitor, are required to compose a DC-side auxiliary circuit to achieve zero-voltage switching. Therefore, the ZVS converters without an auxiliary circuit were proposed [1,22–25]. The advantage of these ZVS converters is not requiring additional components. However, those converters based on critical conduction mode endure high current stress on the main six switches, requiring a third-order LCL filter or even three-phase output current ripple cancellation [25] to eliminate the current ripples. In addition, a bidirectional power flow ZVS operation mechanism in inverter and rectifier modes needs to be carefully considered.

Although the active clamping ZVS method has less current stress on the main switches and only a low-order filter is required, it still suffers from high current stress on the auxiliary switch. In addition, the controls of the six-switch converter for the rectifier mode [7,8] and inverter mode [2,17] are different, and it is not easy to use the same control method to accomplish zero-voltage switching in the bidirectional power flow system. Therefore, in order to realize the bidirectional power flow and maintain fixed switching frequency, the current study combined the active clamping ZVS converter topologies with DPWM and the carrier-based method to reduce the number of switchings and control complexity with the same circuit parameters in both rectifier and inverter modes. The proposed topology can also achieve zero-voltage switching in the six three-phase switches and the auxiliary switch, both in the rectifier mode and inverter mode operations, and only one auxiliary switch is adopted. The reverse recovery currents of body diodes in the main switches were also suppressed. In order to gain a deeper understanding of the development of ZVS techniques, the comparisons of the different ZVS methods in the literature for the ZVS three-phase six-switch converters are summarized in Table 1.

Table 1. Comparisons of different ZVS methods in the three-phase converters.

Structure	Extra Elements (Structure)	Switching Frequency (f_s)	Switch Voltage Stress on Main and Auxiliary Switches	Switch Current Stress on Main/Auxiliary Switches	Filter Design	Bidirectional Operation
[7] Rectifier	LC + switch (3ϕ/3w)	Fixed	$V_{dc} + V_{cc} \approx V_{dc}$	Low/Low	LC	None
[8] Rectifier	LC + switch (3ϕ/3w)	Fixed	V_{dc}	Low/High	LC	None
[2] Inverter	LC + switch (3ϕ/3w)	Fixed	V_{dc}	Low/High	LC	None
[17] Inverter	LC + switch (3ϕ/3w)	Fixed	$V_{dc} + V_{cc} \approx V_{dc}$	Low/Low	LC	None
[19] BTB	LC + switch (3ϕ/4w)	Fixed	$V_{dc} + V_{cc} \approx V_{dc}$	Low/Low	LC	None
[20] Inverter	LC + switch (3ϕ/3w)	Fixed	$V_{dc} + V_{cc} \approx V_{dc}$	Low/Low	LC	None
[21] Inverter	LC + switch (3ϕ/4w)	Fixed	$V_{dc} + V_{cc} \approx V_{dc}$	Low/Low	LC	None
[22] Inverter	None (3ϕ/3w)	Variable	V_{dc}	High/X	LCL	None
[1] Converter	None (3ϕ/3w)	Variable	V_{dc}	High/X	LCL	√
[23] Inverter	None (3ϕ/3 or 4w)	Variable	V_{dc}	High/X	LCL	None
[24] Inverter	None (3ϕ/3w)	Variable (quasi-constant)	V_{dc}	High/X	LCL	None (inverter full ZVS range)
[25] Inverter	3 passive filters (current ripple cancellation) (3ϕ/3w)	Variable	V_{dc}	High/X	Transformer, L and C	None
Proposed converter	LC + switch + D (3ϕ/3w)	Fixed	$V_{dc} + V_{cc} \approx V_{dc}$	Low/High	LC	√

The remainder of this paper is organized as follows. In Section 2, the proposed bidirectional ZVS three-phase converter topology and the modified carrier-based DPWM control scheme are introduced. Based on the topology and DPWM control scheme, the circuit operation principles in the rectifier mode and inverter mode are analyzed in detail, respectively. Some simulation and experimental results are given to verify the validity of the proposed circuit topology and control scheme in Sections 3 and 4. Finally, some conclusions are offered in Section 5.

2. Proposed Bidirectional ZVS Three-Phase Converter

A bidirectional three-phase AC/DC converter is commonly used as an interface between the AC grid and distributed energy resources (DERs) and/or energy storage systems to facilitate bidirectional power flow and maintain proper AC shaping and DC voltage regulation. As a result, the performance of grid-tied bidirectional three-phase AC/DC converters has received significant attention in renewable energy systems, particularly concerning efficiency.

2.1. Proposed Circuit Topology and PWM Strategy

The proposed bidirectional grid-tied ZVS three-phase converter is shown in Figure 1, which is composed of a standard six-switch converter with an LC filter on the AC side and a bidirectional auxiliary resonant circuit on the DC side. In order to achieve bidirectional power flow, the voltage-oriented control (VOC) method is used to control the converter. In order to achieve soft switching, the proposed pulse-width modulation strategy ZVS DPWM shown in Figure 2 is used, where the control signals can be divided into 12 sectors during each line cycle. The positive/negative slope of the sawtooth carrier is decided using the DPWM and operation mode to generate the switching sequence and the selected zero vectors both in the rectifier mode and inverter mode, as shown in Figure 2a. While the converter is operated in the rectifier (inverter) mode and the controlled DPWM signals reach the maximum value, the slope of the sawtooth carrier is positive (negative). In contrast, when the DPWM signals reach the minimum value, the slope of the sawtooth carrier is negative (positive). While the DPWM control signal is a generalized DPWM (GDPWM) method, DPWM1 [26] was adopted in this study. By adding the zero-sequence signal to the three original modulation waves V^*_a, V^*_b and V^*_c, the GDPWM waves V^{**}_a, V^{**}_b and V^{**}_c are generated. Assuming $|V^*_a| \geq |V^*_b|$ and $|V^*_c|$, then the zero sequence signal is $v_0 = (\text{sign}(V^*_a))(V_{dc}/2) - V^*_a$.

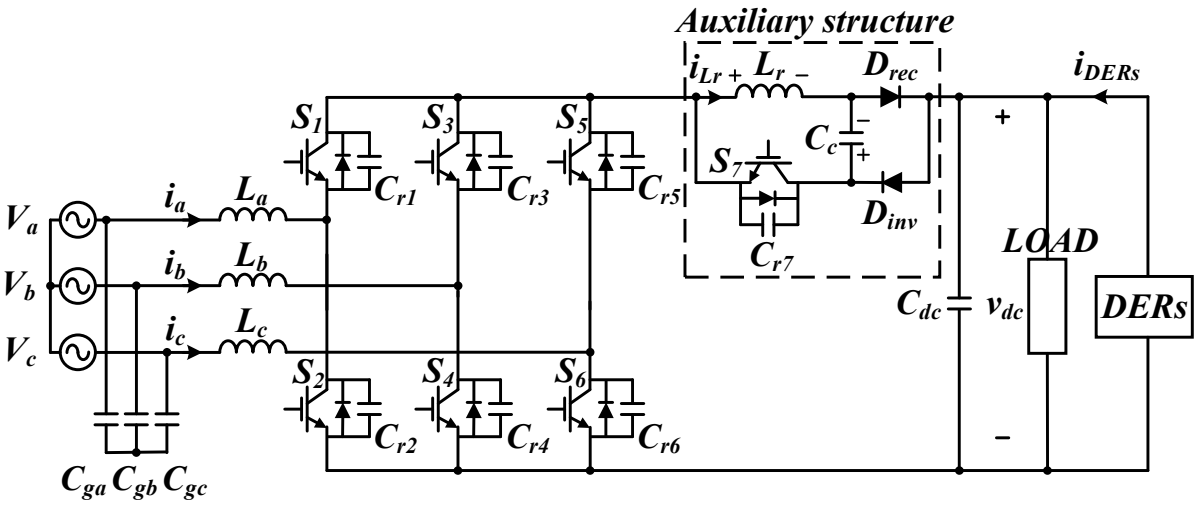

Figure 1. The circuit topology of proposed bidirectional grid-tied ZVS three-phase converter.

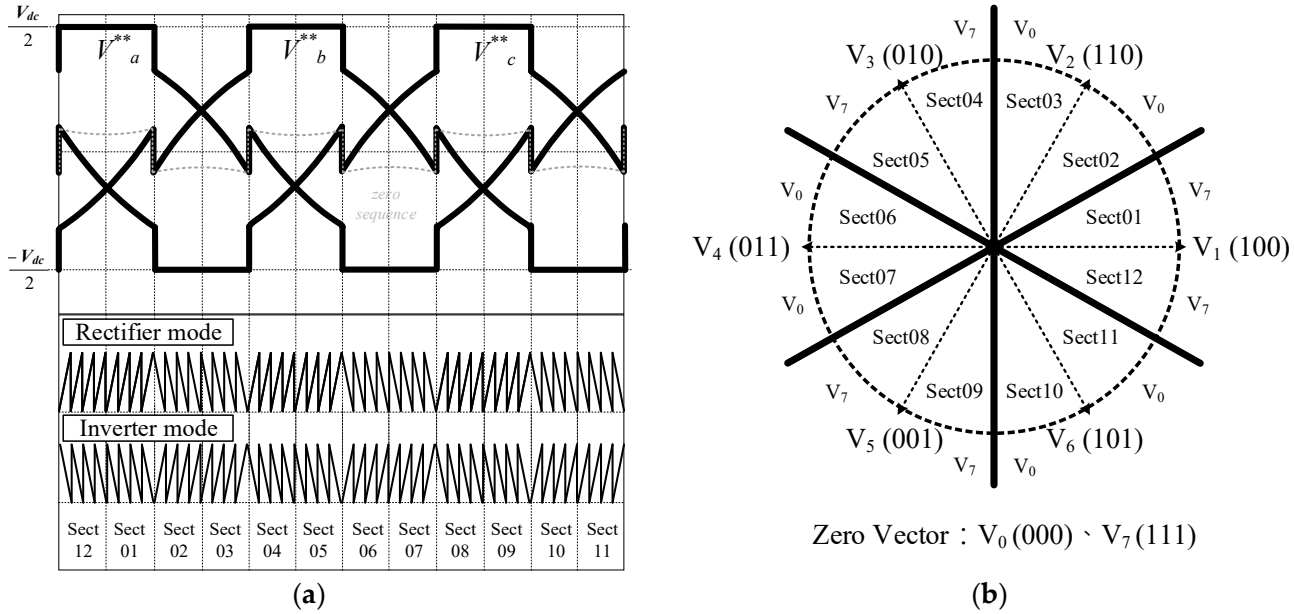

Figure 2. Proposed DPWM strategy and carrier waveform diagram: (**a**) time domain illustration and (**b**) space vector illustration.

Within the proposed carrier-based control strategy, the choice of zero vectors, namely, V_0 and V_7, is depicted in Figure 2b. The control signal for the auxiliary switch S_7 is then computed to achieve ZVS in both the main S_1–S_6 switches and the auxiliary S_7 switch during both rectifier and inverter operational modes.

A. Rectifier Mode

In the rectifier mode, the switching scheme of the carrier is illustrated in Figure 2. When the control signal is clamped at $+V_{dc}/2$, the falling sawtooth waveform is employed for that interval, whereas when the voltage clamp is set at $-V_{dc}/2$, the rising sawtooth waveform is used for that interval. Combining this with DPWM1, the switching sequence shown in Table 2 is generated. Taking interval 01 as an example for analysis, the modulation sequence of the switches is 111 → 110 → 100 → 111.

Table 2. Switching sequence operated in the rectifier mode.

Sector	Vector
1	111 → 110 → 100 → 111
2	000 → 100 → 110 → 000
3	000 → 010 → 110 → 000
4	111 → 110 → 010 → 111
5	111 → 011 → 010 → 111
6	000 → 010 → 011 → 000
7	000 → 001 → 011 → 000
8	111 → 011 → 001 → 111
9	111 → 101 → 001 → 111
10	000 → 001 → 101 → 000
11	000 → 100 → 101 → 000
12	111 → 101 → 100 → 111

B. Inverter Mode

For the inverter mode, the switching scheme of the carrier is depicted in Figure 2. When the voltage clamp is set at $+V_{dc}/2$, the rising sawtooth waveform is utilized for that interval, while when the voltage clamp is positioned at $-V_{dc}/2$, the falling sawtooth waveform is employed for that interval. As a result, the sawtooth waveform undergoes a transition every 60 degrees. Combining this with DPWM1, the switching sequence illustrated in Table 3 is generated. Taking interval 01 as an example for analysis, the modulation sequence of the switches is 111 → 100 → 110 → 111.

Table 3. Switching sequence operated in the inverter mode.

Sector	Vector
1	111 → 100 → 110 → 111
2	000 → 110 → 100 → 000
3	000 → 110 → 010 → 000
4	111 → 010 → 110 → 111
5	111 → 010 → 011 → 111
6	000 → 011 → 010 → 000
7	000 → 011 → 001 → 000
8	111 → 001 → 011 → 111
9	111 → 001 → 101 → 111
10	000 → 101 → 001 → 000
11	000 → 101 → 100 → 000
12	111 → 100 → 101 → 111

By employing the proposed DPWM strategy and the zero-vector selection illustrated in Figure 2, it becomes feasible to derive a twelve-sector switch modulation sequence within a line cycle. Take sector 1 as an example, and assume the three-phase current $i_a > 0 > i_b > i_c$. For a convenient explanation of how the proposed modulation scheme works, the theoretical key waveforms during the sector 1 operation in both rectifier and inverter modes are illustrated in Figure 3 and the following assumptions are made to simplify the operation principle analysis of the bidirectional grid-tied ZVS three-phase converter.

(1) The main switches S_1–S_6 and auxiliary switch S_7 are considered ideal switches with their anti-paralleled diodes (body diodes). The body diodes of switches S_1~S_7 are named D_1~D_7, respectively.
(2) All of the parasitic capacitances C_{r1}–C_{r7} are in parallel with the switches S_1–S_7, respectively. Suppose $C_{r1} = C_{r2} = \cdots = C_{r6}$.
(3) The clamping capacitor C_c possesses a substantial capacitance, resulting in a minor voltage ripple across it. As a consequence, the voltage v_{Cc} can be treated akin to a voltage source.
(4) The operational frequency of the converter is significantly higher than the resonant frequency of the LC filter on the AC side.
(5) The current i_{sx}, where x belongs to the set {1, 2, . . ., 7}, characterizes the switch current incorporating the parasitic capacitor current. Meanwhile, the current i_{cex}, with x also within the set {1, 2, . . ., 7}, represents the switch current after eliminating the parasitic capacitor contribution. The voltage v_{cex}, $x \in$ {1, 2, . . ., 7}, represents the switch voltage. v_{cr} denotes the resonant capacitor voltage.

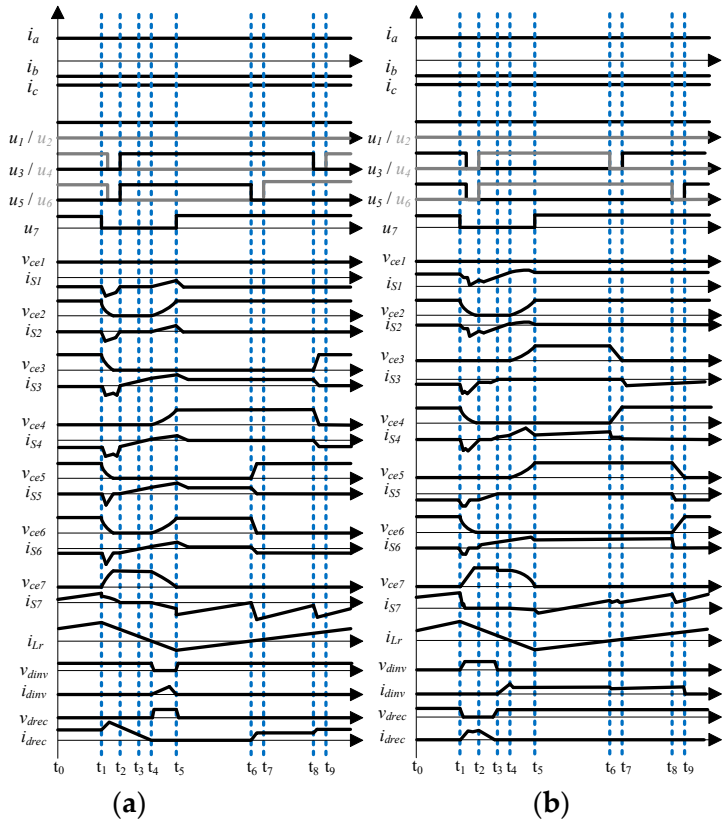

Figure 3. The theoretical key waveforms during the sector 1 operation in the (**a**) rectifier mode and (**b**) inverter mode.

2.2. Rectifier Mode Operation

In order to understand the proposed control strategy in this topology operated in rectified mode, the steady-state key waveforms in sector 1 are shown in Figure 3a. The vector sequence during this sector is 111-110-100-111, as shown in Figure 4a. The corresponding operation state is explained as follows, and the equivalent circuit in each state is illustrated in Figure 5a.

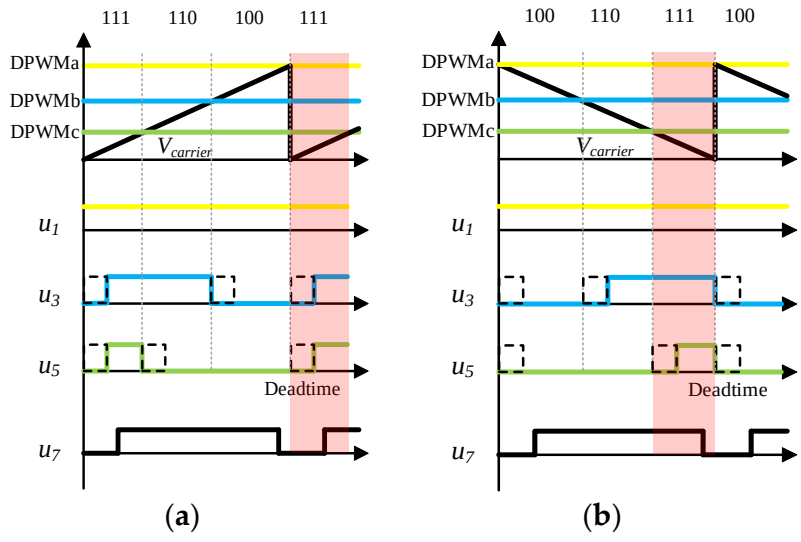

Figure 4. The corresponding vector sequence in sector 1 in Figure 3 operated in the (**a**) rectifier mode and (**b**) inverter mode.

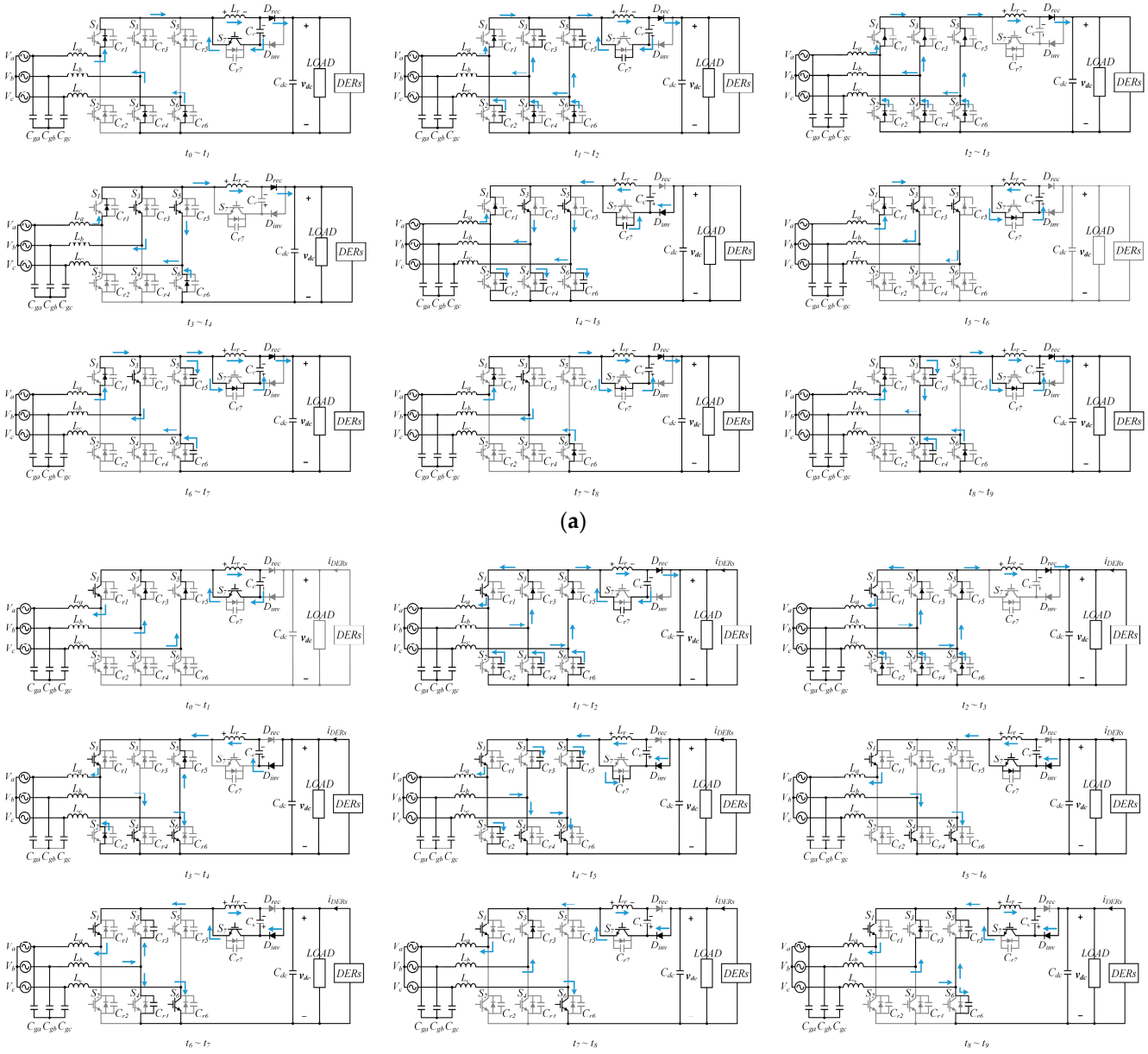

Figure 5. The equivalent circuit in each state of the proposed bidirectional soft-switching converter operated in the (**a**) rectifier mode and (**b**) inverter mode.

State 1 (t_0~t_1): The circuit state is operated in vector $V_1(100)$. D_1, D_4, D_6, D_{rec} and S_7 are in the conducting state; D_{inv} is turned off; and the resonant inductor L_r is magnetized by clamping capacitor C_c, which can be expressed by (1). The energy flows from the AC side to the DC side.

$$\frac{di_{Lr}(t)}{dt} = \frac{v_{Cc}}{L_r} \tag{1}$$

State 2 (t_1~t_2): At instant t_1, S_7 is turned off, and L_r resonates with C_{r2}, C_{r3}, C_{r5} and C_{r7}. C_{r2}, C_{r3} and C_{r5} are discharged and C_{r7} is charged. The energy flows from the AC side to the DC side. The state equations for L_r, C_r and C_C can be expressed as shown in (2) and (3).

$$\frac{di_{Lr}(t)}{dt} = -\frac{(v_{dc} - v_{Cr}(t))}{L_r} \tag{2}$$

$$-3C_r\frac{dv_{C_r}(t)}{dt} + C_{r7}\frac{d(v_{Cc} + V_{dc} - v_{Cr}(t))}{dt} = i_{Lr}(t) - i_a(t) \tag{3}$$

State 3 (t_2~t_3): In this stage, the circuit state becomes vector V_7(111). The voltages on C_{r2}, C_{r3} and C_{r5} drop to zero, and the body diodes on the six main switches are conducting at t_2. Then, S_3 and S_5 are turned on via ZVS at instant t_2. The diode reverse recovery current in S_2 is suppressed by L_r. The voltage on C_{r7} oscillates to be $V_o + v_{Cc}$. The energy flows from the AC side to the DC side. The state equations for L_r and V_{dc} can be expressed as shown in (4).

$$\frac{\mathrm{d}i_{Lr}(t)}{dt} = -\frac{V_{dc}}{L_r} \tag{4}$$

State 4 (t_3~t_4): The circuit is still operated in vector V_7(111) and the body diode of switch S_6 is conducting. The AC-side circuit becomes a loop. The diode reverse recovery current in S_4 is suppressed by L_r. The current of L_r is charged by V_{dc}. The state equations for the L_r can be expressed as shown in (5).

$$\frac{di_{Lr}(t)}{dt} = -\frac{V_{dc}}{L_r} \tag{5}$$

State 5 (t_4~t_5): The circuit is still operated in vector V_7(111) but the body diode of S_6 is turned off. L_r resonates with C_{r2}, C_{r4}, C_{r6} and C_{r7}. The capacitors C_{r2}, C_{r4} and C_{r6} are charged and C_{r7} is discharged. The voltage of switch S_7 is decreased to zero at time t_5. The diode reverse recovery current in S_6 is suppressed by L_r, and the energy of the inductor L_r is restored to the AC side. The diode states in the auxiliary circuit are changed. D_{inv} is conducting and D_{rec} is turned off. The state equations for L_r and C_r can be expressed as shown in (6) and (7).

$$\frac{di_{Lr}(t)}{dt} = -\frac{(V_{dc} - v_{Cr}(t) - v_{Cc})}{L_r} \tag{6}$$

$$3C_r\frac{dv_{Cr}(t)}{dt} - C_{r7}\frac{d(V_{dc} - v_{Cr}(t))}{dt} = -i_{Lr}(t) \tag{7}$$

State 6 (t_5~t_6): The circuit state is still operated in vector V_7(111). S_7 is turned on via ZVS at instant t_5. Both D_{inv} and D_{rec} are turned off. The capacitor C_c is charged by L_r, which can be described by (8).

$$\frac{di_{Lr}(t)}{dt} = \frac{V_{Cc}}{L_r} \tag{8}$$

State 7 (t_6~t_7): The circuit state becomes vector V_2(110). The phase current i_c is discharging C_{r6} and C_{r5}. The D_{rec} is conducting and D_{inv} is turned off. The energy flows from the AC side to the DC side. The state equation relationships between L_r, C_r and C_c can be expressed by (9) and (10).

$$\frac{di_{Lr}(t)}{dt} = \frac{V_{Cc}}{L_r} \tag{9}$$

$$i_c(t) = -C_{r6}\frac{dv_{C_{r6}}(t)}{dt} + C_{r5}\frac{dv_{C_{r5}}(t)}{dt} \tag{10}$$

State 8 (t_7~t_8): The circuit remains in operation within vector V_2(110). The body diode of switch S_6 is in a conductive state. Power continues to transfer from the AC side to the DC side. C_c is charged by L_r, which can be expressed by (11).

$$\frac{di_{Lr}(t)}{dt} = \frac{v_{Cc}}{L_r} \tag{11}$$

State 9 (t_8~t_9): The circuit state changes from vector $V_2(110)$ to vector $V_1(100)$. The phase current i_b is charging C_{r3} and discharging C_{r4}. The energy flows from the AC side to the DC side. The state equations for L_r and C_r can be expressed as shown in (12) and (13).

$$\frac{di_{Lr}(t)}{dt} = \frac{v_{Cc}}{L_r} \tag{12}$$

$$i_b(t) = -C_{r4}\frac{dv_{Cr4}(t)}{dt} + C_{r3}\frac{dv_{Cr3}(t)}{dt} \tag{13}$$

2.3. Inverter Mode Operation

In order to understand the proposed control strategy in the proposed topology operated in inverter mode, the steady-state key waveforms in sector 1 are shown in Figure 3b. The vector sequence during this sector is 111-100-110-111, as shown in Figure 4b. The corresponding operation state is explained as follows, and the equivalent circuit in each state is illustrated in Figure 5b.

State 1 (t_0~t_1): The circuit functions while in vector state 111, where switch S_1, auxiliary switch S_7, and anti-parallel diodes D_3 and D_5 are on. The inverter operates under a zero-vector condition. The resonant inductor L_r is charged through the clamping voltage v_{Cc}. D_{inv} and D_{rec} are turned off. The corresponding equivalent circuit is depicted in Figure 5b, and the relationship between L_r and C_c is described by (14).

$$\frac{di_{Lr}(t)}{dt} = \frac{v_{Cc}}{L_r} \tag{14}$$

State 2 (t_1~t_2): The resonant inductor L_r exhibits resonance, along with C_{r2}, C_{r4}, C_{r6} and C_{r7}. During this state, switches S_3 and S_5 are turned off. Excess energy flows back to the distributed energy storage system or capacitor via D_{rec}. Figure 5b illustrates the corresponding equivalent circuit, and the relationships between C_c, C_r and L_r can be expressed as shown in (15) and (16).

$$\frac{di_{Lr}(t)}{dt} = \frac{(v_{Cr}(t) - V_{dc})}{L_r} \tag{15}$$

$$-3C_r\frac{dv_{Cr}(t)}{dt} + C_{r7}\frac{d(V_{dc} - v_{Cr}(t) - v_{Cc})}{dt} = i_{Lr}(t) \tag{16}$$

State 3 (t_2~t_3): During this state, the circuit functions in vector state 100. The voltages across C_{r2}, C_{r4} and C_{r6} are discharged to zero, while the voltage across C_{r7} is elevated to V_{DC}. The anti-paralleled diodes D_2, D_3, D_4, D_5 and D_6 are on. Under ZVS conditions, at time instant t_2, the switches S_4 and S_6 are turned on, while the resonant inductor L_r mitigates the reverse recovery current in the anti-parallel diode D_3. D_{inv} is still turned off and D_{rec} is still turned on. Excess energy still flows back to the distributed energy storage system or capacitor via D_{rec}. Energy recycling is achieved. Figure 5b illustrates the corresponding equivalent circuit, and the relationship between i_{Lr} and v_{Cc} is expressed by (17).

$$\frac{di_{Lr}(t)}{dt} = -\frac{V_{dc}}{L_r} \tag{17}$$

State 4 (t_3~t_4): The main switches S_1, S_4 and S_6 are held in the on state, while the resonant inductor L_r mitigates the reverse recovery current in the anti-parallel diodes D_2 and D_5. D_{inv} is turned on and D_{rec} is turned off. The power flow is transferred from the DC side to the AC side. The corresponding equivalent circuit is depicted in Figure 5b, and the relationship between i_{Lr} and v_{Cc} is formulated in (18).

$$\frac{di_{Lr}(t)}{dt} = -\frac{(V_{dc} - v_{Cc})}{L_r} \tag{18}$$

State 5 (t_4~t_5): Resonance is established in the resonant inductor L_r in conjunction with C_{r2}, C_{r3}, C_{r5} and C_{r7}. The anti-paralleled diode D_7 prepares to turn on at t_5. During this state, C_{r2}, C_{r3} and C_{r5} are charged and C_{r7} is discharged. D_{inv} is in the on state and D_{rec} is in the off state. The power continues to transfer from the DC side to the AC side. The corresponding equivalent circuit is depicted in Figure 5b, and the relationships between i_{Lr}, v_{cr} and v_{Cc} is described in (19) and (20).

$$\frac{di_{Lr}(t)}{dt} = \frac{V_{Cc} - V_{dc} + v_{Cr}(t)}{L_r} \tag{19}$$

$$3C_r\frac{dv_{Cr}(t)}{dt} + i_a(t) = C_{r7}\frac{d(V_{dc} - v_{Cr}(t))}{dt} - i_{Lr}(t) \tag{20}$$

State 6 (t_5~t_6): At this time, the circuit remains functional in vector state 100, with the main switches S_1, S_4 and S_6 in the on state. The auxiliary switch S_7 is turned on under the ZVS condition. The voltage across the clamping capacitor v_{Cc} is charged through the resonant inductor current i_{Lr}. D_{inv} is conducting, D_{rec} is non-conducting and power is directed from the DC side to the AC side. The equivalent circuit is depicted in Figure 5b, and the relationship between i_{Lr} and v_{Cc} is expressed in (21).

$$\frac{di_{Lr}(t)}{dt} = \frac{v_{Cc}}{L_r} \tag{21}$$

State 7 (t_6~t_7): At this time, the circuit functions in vector state 100. The current in phase i_b results in the discharge of voltage across v_{Cr3} while simultaneously charging the voltage across v_{Cr4}. D_{inv} is conducting, while D_{rec} remains non-conductive, allowing power to transition from the DC side to the AC side. The equivalent circuit is illustrated in Figure 5b, and the relationships between v_{Cr3}, v_{Cr4} and i_{Lr} are shown in (22) and (23).

$$\frac{di_{Lr}(t)}{dt} = \frac{v_{Cc}}{L_r} \tag{22}$$

$$i_b(t) = -C_{r3}\frac{dv_{Cr3}(t)}{dt} + C_{r4}\frac{dv_{Cr4}(t)}{dt} \tag{23}$$

State 8 (t_7~t_8): During this state, the circuit operates in vector state 110. The main switches S_1 and S_6, alongside the auxiliary switch S_7 and the anti-parallel diode D_3, are concurrently conducting. D_{inv} is in the on state and D_{rec} is in the off state. Power continues to transfer from the DC side to the AC side. The corresponding equivalent circuit is displayed in Figure 5b, and the relationship between i_{Lr} and v_{Cc} is shown in (24).

$$\frac{di_{Lr}(t)}{dt} = \frac{v_{Cc}}{L_r} \tag{24}$$

State 9 (t_8~t_9): During this state, the circuit remains in operation within vector state 110. The phase current i_c leads to the depletion of voltage across v_{Cr5}, while simultaneously charging the voltage across v_{Cr6}. D_{inv} is in the on state and D_{rec} is in the off state, allowing power transfer from the DC side to the AC side. The depicted equivalent circuit is illustrated in Figure 5b. Subsequent to this state, the circuit's operation reverts to the initial stage, commencing a new cycle. The relationships between the voltage and current across the inductor and capacitor are shown in (25) and (26).

$$\frac{di_{Lr}(t)}{dt} = \frac{v_{Cc}}{L_r} \tag{25}$$

$$i_c(t) = -C_{r5}\frac{dV_{Cr5}(t)}{dt} + C_{r6}\frac{dv_{Cr6}(t)}{dt} \tag{26}$$

2.4. Control Scheme

In order to control the bidirectional grid-tied three-phase converter via ZVS with the proposed modulation scheme, the control block shown in Figure 6 is used. Based on the voltage-oriented control scheme, the AC grid voltages, the DC DERs/load voltage, and AC-side currents are sensed and fed into the A/D converters, and then the phase lock loop (PLL) is utilized to synchronize the AC grid voltage. Thus, the control signals in the abc nature reference frame are transformed into the d-q synchronous reference frame. To achieve the bidirectional power flow control, the d-axis current command is utilized to judge the power flow direction (PFD) and generate the corresponding DPWM modulation control scheme and main and auxiliary switch control signals to achieve zero-voltage switching, both in the rectifier and inverter operations. Meanwhile, the reverse recovery currents of body diodes in the main switches are also suppressed.

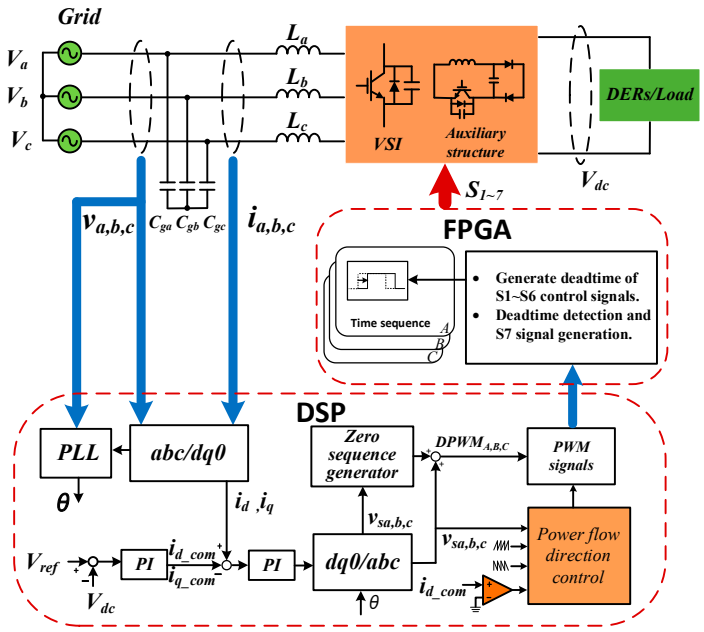

Figure 6. Control block of the proposed bidirectional ZVS three-phase converter.

2.5. Circuit Design

To achieve zero-voltage switching in a bidirectional grid-tied three-phase converter, the state-plane trajectory is considered to design the inductor and capacitor of the proposed circuit.

Considering the system operated at the state 2 (t_1~t_2) in sector 1 under the rectifier mode and according to Equations (2) and (3), one can obtain

$$\begin{cases} v_{Cr}(t) = V_{dc} + V_{Cc}\cos\omega t - Z(i_{Lr.\max} - i_a)\sin\omega t \\ i_{Lr}(t) = i_a + \frac{1}{Z}V_{Cc}\sin\omega t + (i_{Lr.\max} - i_a)\cos\omega t \end{cases} \tag{27}$$

where Z is the characteristic impedance, which is defined as

$$Z = \sqrt{L_r/(3C_r + C_{r7})} \tag{28}$$

While all the sectors 1–12 are considered in the rectifier mode operated in state 2 (t_1~t_2), the generalized circuit expression can be derived:

$$\begin{cases} L_r\frac{di_{Lr}(t)}{dt} = -V_{dc} + v_{Cr}(t) \\ -C_r\frac{dv_{Cr}(t)}{dt} = i_{Lr}(t) - \max(|i_a|, |i_b|, |i_c|) \end{cases} \tag{29}$$

Then, the generalized solution for the ZVS rectifier resonant circuit can be expressed as follows

$$\begin{cases} v_{Cr}(t) = & V_{dc} + V_{Cc}\cos\omega t - Z(i_{Lr.\max} - \max(|i_a|,|i_b|,|i_c|))\sin\omega t \\ i_{Lr}(t) = & \max(|i_a|,|i_b|,|i_c|) + \frac{1}{Z}V_{Cc}\sin\omega t \\ & +(i_{Lr.\max} - \max(|i_a|,|i_b|,|i_c|))\cos\omega t \end{cases} \quad (30)$$

According to (30), the ZVS rectifier resonant circle can be illustrated in Figure 7a, where R_{REC} is the radius of the ZVS rectifier resonant circle.

$$R_{REC} = \sqrt{{V_{Cc}}^2 + (Z(i_{Lr.\max} - \max(|i_a|,|i_b|,|i_c|)))^2} \quad (31)$$

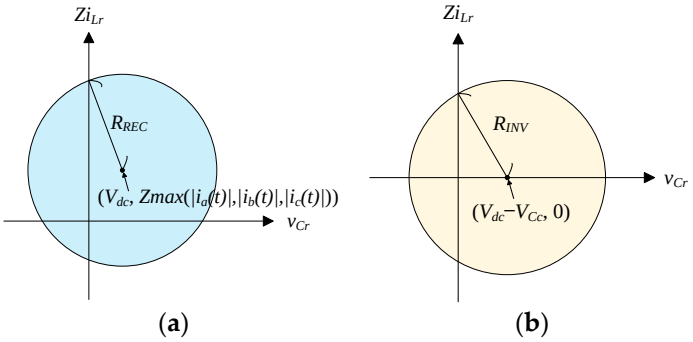

Figure 7. The resonant circles for the (**a**) ZVS rectifier and (**b**) ZVS inverter.

Similarly, considering the system operated under the inverter mode at the state 2 (t_1~t_2) for sectors 1–12, the generalized circuit expression also can be derived as follows:

$$\begin{cases} v_{Cr}(t) = V_{dc} - V_{Cc} + V_{Cc}\cos\omega t - Zi_{Lr.\max}\sin\omega t \\ i_{Lr}(t) = \frac{1}{Z}V_{Cc}\sin\omega t + i_{Lr.\max}\cos\omega t \end{cases} \quad (32)$$

According to (32), the ZVS inverter resonant circle can be illustrated in Figure 7b, where R_{INV} is the radius of the ZVS inverter resonant circle.

$$R_{INV} = \sqrt{{V_{Cc}}^2 + (Zi_{Lr.\max})^2} \quad (33)$$

In order to achieve the zero-voltage switching function, the radii of the ZVS rectifier and ZVS inverter must be greater than V_{dc} and V_{dc}–V_{Cc}, respectively. Therefore, the following equations must be satisfied.

In the ZVS rectifier:

$$\sqrt{{V_{Cc}}^2 + (Z(i_{Lr,\max} - \max(|i_a(t)|,|i_b(t)|,|i_c(t)|)))^2} > V_{dc} \quad (34)$$

In the ZVS inverter:

$$\sqrt{{V_{Cc}}^2 + (Zi_{Lr,\max})^2} > V_{dc} - V_{Cc} \quad (35)$$

For a convenient design, (34) and (35) can be simplified as follows:

In the ZVS rectifier:

$$Z^2 > \frac{V_{dc}^2 - V_{Cc}^2}{(i_{Lr,\max} - \max(|i_a(t)|,|i_b(t)|,|i_c(t)|))^2} \approx \frac{V_{dc}^2 - V_{Cc}^2}{\Delta i_{Lr,REC}^2} \quad (36)$$

In the ZVS inverter:

$$Z^2 > \frac{(V_{dc} - V_{cc})^2 - V_{Cc}^2}{(i_{Lr,\max})^2} \approx \frac{(V_{dc} - V_{cc})^2 - V_{Cc}^2}{\Delta i_{Lr,INV}^2} \tag{37}$$

where $\Delta i_{Lr,REC}$ and $\Delta i_{Lr,INV}$ are half of the peak-to-peak inductor current ripples.

Hence, to accomplish the ZVS bidirectional converter, one can choose a proper capacitor C_C and then the resonant inductor L_r must satisfy both (36) and (37) to achieve $V_{cr} = 0$, as shown in Figure 7, before the switches are turned on.

2.6. Controller Design

In order to achieve bidirectional power flow control with ZVS, a dynamic model is needed. Because the auxiliary circuit is operated during the original switching time of the main six switches, there is no influence on the control of the original six-switch converter. Therefore, the dynamic model of the proposed converter in the d-q frame is

$$v_d = Ri_d + L\frac{di_d}{dt} - \omega L i_q + S_d v_{dc} \tag{38}$$

$$v_q = Ri_q + L\frac{di_q}{dt} + \omega L i_d + S_q v_{dc} \tag{39}$$

$$C_{dc}\frac{dv_{dc}}{dt} = (i_d S_d + S_q i_q) - i_{dc} \tag{40}$$

where R is the equivalent series resistance on the grid side. v_d and v_q are the d-axis and q-axis grid voltages in the synchronous frame, respectively. The i_d and i_q are the d-axis and q-axis grid currents in the synchronous frame, respectively. S_d and S_q are the state-averaged control signals in the d-q frame.

Since the DC output power is only contributed to by the i_d current and the i_q current is negligible, (40) can be rewritten as

$$C_{dc}\frac{dv_{dc}}{dt} = \left[K_P^v(v_{dc}^* - v_{dc}) + \int K_I^v(v_{dc}^* - v_{dc})dt\right]S_d - \frac{v_{dc}}{R_L} \tag{41}$$

where R_L is the DC side load. K_P^v and K_I^v are the DC bus voltage proportional–integral (PI) compensators. Differentiating (41) with respect to time yields

$$C_{dc}\ddot{v_{dc}} = \left[K_P^v\left(\dot{v_{dc}^*} - \dot{v_{dc}}\right) + K_I^v(v_{dc}^* - v_{dc})\right]S_d - \frac{\dot{v_{dc}}}{R_L} \tag{42}$$

Applying the Laplace transform to (42), the outer voltage loop transfer function gives

$$\frac{v_{dc}}{v_{dc}^*} = \frac{(K_P^v s + K_I^v)\frac{S_d}{C_{dc}}}{s^2 + \frac{\left(K_P^v S_d + \frac{1}{R_L}\right)}{C_{dc}}s + \frac{K_I^v S_d}{C_{dc}}} \tag{43}$$

Therefore, the PI compensator K_P^v and K_I^v of the outer voltage control loop can be designed according to (43).

Next, consider the inner current control loop. In (38) and (39), the decoupled terms $\omega L i_d$ and $\omega L i_q$ can be directly added into the d-q control frame, and thus, S_d and S_q have no coupled terms. Therefore, S_d and S_q can be expressed as

$$S_d = K_{Pd}^i(i_d^* - i_d) + \int K_{Id}^i(i_d^* - i_d)dt \tag{44}$$

$$S_q = K_{Pq}^i\left(i_q^* - i_q\right) + \int K_{Iq}^i\left(i_q^* - i_q\right)dt \tag{45}$$

where K^i_{Pd}, K^i_{Id} and K^i_{Pq}, K^i_{Iq} are the d-axis and q-axis PI compensators of the inner current control loop, respectively. Assume the amplitude of the input voltage is constant. Differentiating (38) and (39) with respect to time yields

$$0 = R\dot{i}_d + L\ddot{i}_d + \left[K^i_{Pd}\left(\dot{i}^*_d - \dot{i}_d\right) + K^i_{Id}(i^*_d - i_d)\right]v_{dc} \tag{46}$$

$$0 = R\dot{i}_q + L\ddot{i}_q + \left[K^i_{Pq}\left(\dot{i}^*_q - \dot{i}_q\right) + K^i_{Iq}\left(i^*_q - i_q\right)\right]v_{dc} \tag{47}$$

Applying the Laplace transform to (46) and (47), the inner current-loop transfer functions for d-axis and q-axis gives

$$\frac{i_d}{i^*_d} = -\frac{\left(sK^i_{Pd} + K^i_{Id}\right)\frac{v_{dc}}{L}}{s^2 + \frac{\left(R - K^i_{Pd}v_{dc}\right)}{L}s - \frac{K^i_{Id}v_{dc}}{L}} \tag{48}$$

$$\frac{i_q}{i^*_q} = -\frac{\left(sK^i_{Pq} + K^i_{Iq}\right)\frac{v_{dc}}{L}}{s^2 + \frac{\left(R - K^i_{Pq}v_{dc}\right)}{L}s - \frac{K^i_{Iq}v_{dc}}{L}} \tag{49}$$

The PI compensator of the inner current control loop can be derived by the linear time-invariant dynamic model (48) and (49). It is also important to note that the bandwidth of the inner current loop must be broader than that of the outer voltage loop.

3. Simulation Results

In order to verify the validity of the proposed circuit topology and corresponding modulation strategy, the simulation software Power SIM Version 9.1.1.400 was adopted and the simulation was conducted using the system parameters listed in Table 4 according to the circuit design in Section 2.5. The parameters that were designed and selected could cause both the main and auxiliary switches to achieve soft switching, and the body diode reverse recovery current suppressed by inductor L_r. In this implementation, the IGBT FUJI 2MBI100VA-120-50 was utilized as the power switch. Therefore, a simulated parasitic capacitor C_r = 2 nF, resonant inductor L_r = 40 uH and clamping capacitor C_c = 100 µF were selected.

Table 4. Simulation and experimental parameters of the proposed bidirectional ZVS three-phase converter.

Parameters	Value	Unit
AC grid line voltage (rms)	220	V
DC link voltage, V_{dc}	450	V
Switching frequency, f_s	18	kHz
Three-phase inductors, $L_{a,b,c}$	2	mH
Three-phase capacitors $C_{ga,b,c}$	22	µF
DC-link capacitor, C_{dc}	2200	µF
Parasitic capacitance, C_r	2	nF
Resonant inductor, L_r	40	µH
Clamping capacitor, C_c	100	µF
Power rating, P_{rate}	3	kW

First, consider the proposed bidirectional grid-tied ZVS three-phase converter that was operated in the rectifier mode. The simulation waveforms of the switch voltage and current for the main switches S_3 and S_4 are shown in Figures 8a and 8b, respectively. As

can be observed from Figure 8a,b, S_3 was turned on under the ZVS condition, and the diode reverse recovery current in S_4 could be suppressed when S_4 was turned off. Figure 8c shows the voltage and current waveforms of auxiliary switch S_7, and one can find that S_7 was turned on under the ZVS condition. The voltage of the clamping capacitor v_{Cc} and the current of the resonant inductor i_{Lr} are shown in Figure 8d. As can be seen from Figure 8d, v_{Cc} was much smaller than V_{dc} such that the voltage stress on the main and auxiliary switches was $v_{cc} + V_{dc} \approx V_{dc}$. Figure 8e,f show the voltage and current waveforms of diodes D_{inv} and D_{rec}, respectively. It follows from Figure 8e,f that the diode voltage stress v_{Cc} was much smaller than V_{dc}.

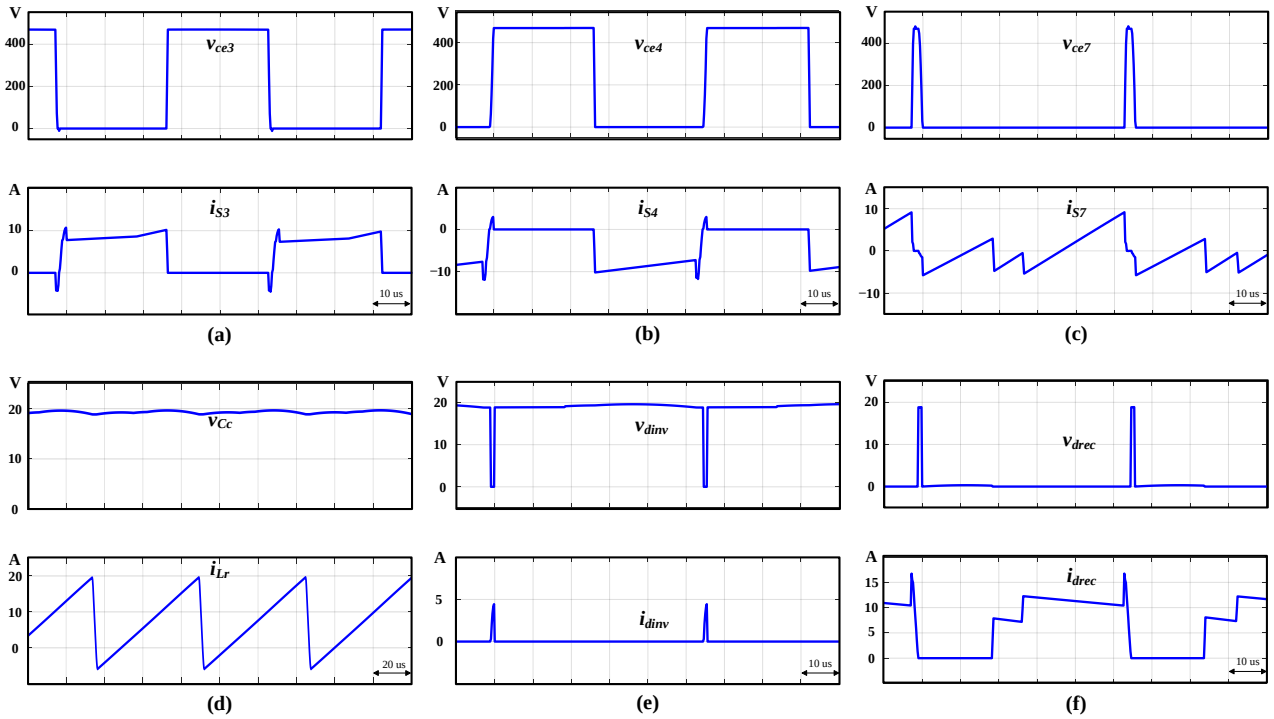

Figure 8. Simulated waveforms of the proposed bidirectional soft-switching converter operating in the rectifier mode: (**a**) voltage and current of switch S_3 (ZVS turn-on), (**b**) voltage and current of switch S_4 (the diode reverse recovery current was suppressed), (**c**) voltage and current of auxiliary switch S_7, (**d**) the clamping capacitor voltage v_{Cc} and resonant inductor current i_{Lr}, (**e**) voltage and current of diode D_{inv}, and (**f**) voltage and current of diode D_{rec}.

Next, consider the proposed bidirectional grid-tied ZVS three-phase converter that was operated in the inverter mode. The simulation waveforms of switch voltage and current for the main switches S_4 and S_3 are shown in Figures 9a and 9b, respectively. As can be observed from Figure 9a,b, S_4 was turned on under the ZVS condition, and the diode reverse recovery current in S_3 could be suppressed when S_3 was turned off. Figure 9c shows the voltage and current waveforms of auxiliary switch S_7, and it can be seen from Figure 9c that S_7 was turned on under the ZVS condition. The voltage of the clamping capacitor v_{Cc} and the current of the resonant inductor i_{Lr} are shown in Figure 9d. It follows from Figure 9d that v_{Cc} was much smaller than V_{dc} such that the voltage stress on the main and auxiliary switches was $v_{cc} + V_{dc} \approx V_{dc}$. The voltage and current waveforms of diodes D_{inv} and D_{rec} are shown in Figures 9e and 9f, respectively. As can be observed from Figure 9e,f, the diode voltage stress was v_{Cc}, which was the same as that in the rectifier mode and was much smaller than V_{dc}.

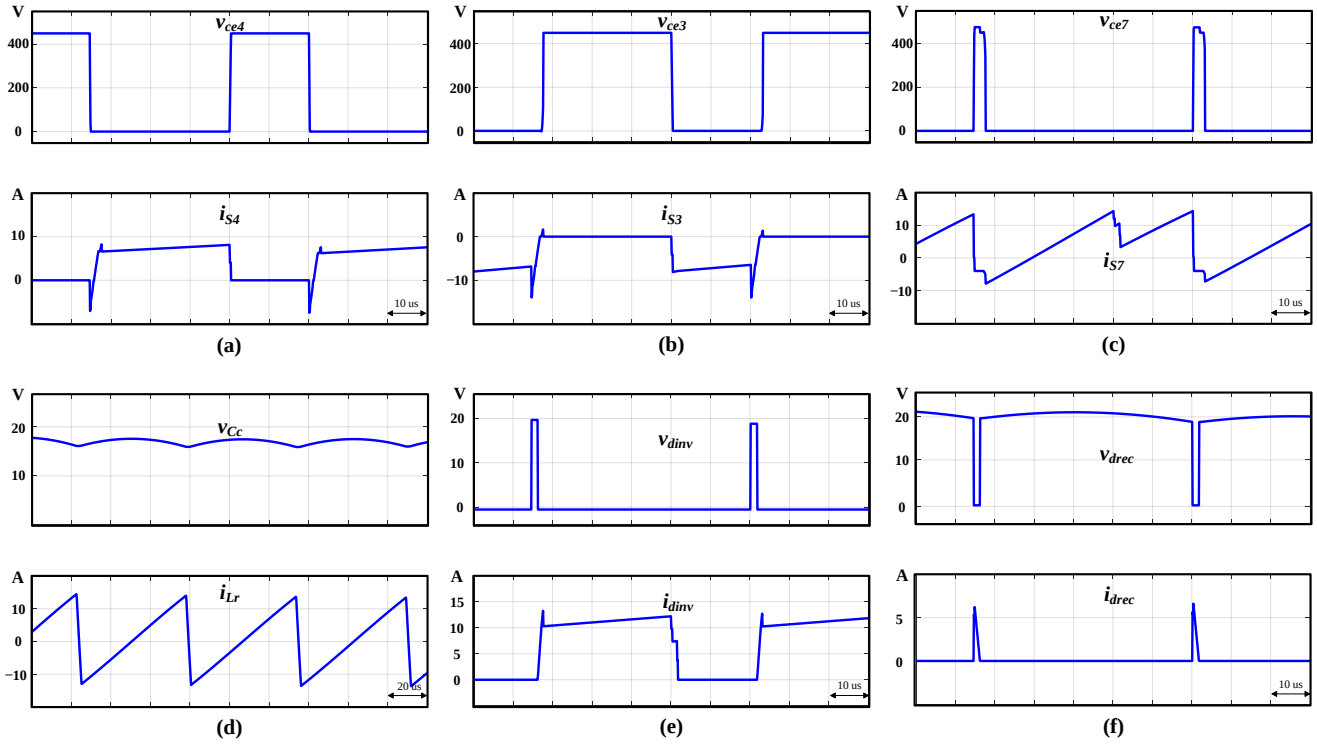

Figure 9. Simulated waveforms of the proposed bidirectional soft-switching converter operating in the inverter mode: (**a**) voltage and current of switch S_4 (ZVS turn-on), (**b**) voltage and current of switch S_3 (the diode reverse recovery current was suppressed), (**c**) voltage and current of auxiliary switch S_7, (**d**) the clamping capacitor voltage v_{Cc} and resonant inductor current i_{Lr}, (**e**) voltage and current of diode D_{inv}, and (**f**) voltage and current of diode D_{rec}.

In order to gain further insight into the operation of zero-voltage switching and the suppression of the reverse-recovery current in the proposed bidirectional grid-tied ZVS three-phase converter, the simulation process was carried out when the system was operated in both rectifier and inverter modes. The simulated ZVS process of switch S_3 in the rectifier mode is shown in Figure 10. It should be noted that the switch current i_{sx}, $x \in \{1, 2, \ldots, 7\}$, was defined as $i_{sx} = i_{cex} + i_{crx}$, which includes the parasitic capacitor current i_{crx}, but the switch current i_{cex} did not include the parasitic capacitor current i_{crx}. The plots of i_{s3} versus v_{ce3}, i_{ce3} versus v_{ce3} and i_{cr3} versus v_{ce3} are shown in Figures 10a, 10b and 10c, respectively. Figure 10d shows the overlap plot of Figure 10a–c. As can be observed from Figure 10, the ZVS on was indeed achieved in the main switch S_3 in the rectifier mode. The simulated reverse-recovery-current suppression of switch S_4 in the rectifier mode is shown in Figure 11. The plots of i_{s4} versus v_{ce4}, i_{ce4} versus v_{ce4} and i_{cr4} versus v_{ce4} are shown in the Figures 11a, 11b and 11c, respectively. Figure 11d shows the overlap plot of Figure 11a–c. As can be seen from Figure 11, the suppression of the diode reverse-recovery process of switch S_4 was indeed completed in the rectifier mode. The plots of i_{s7} versus v_{ce7}, i_{ce7} versus v_{ce7} and i_{cr7} versus v_{ce7} are shown in the Figures 12a, 12b and 12c, respectively. Figure 12d shows the overlap plot of Figure 12a–c. It follows from Figure 12 that the ZVS on was indeed achieved in the auxiliary switch S_7 in the rectifier mode.

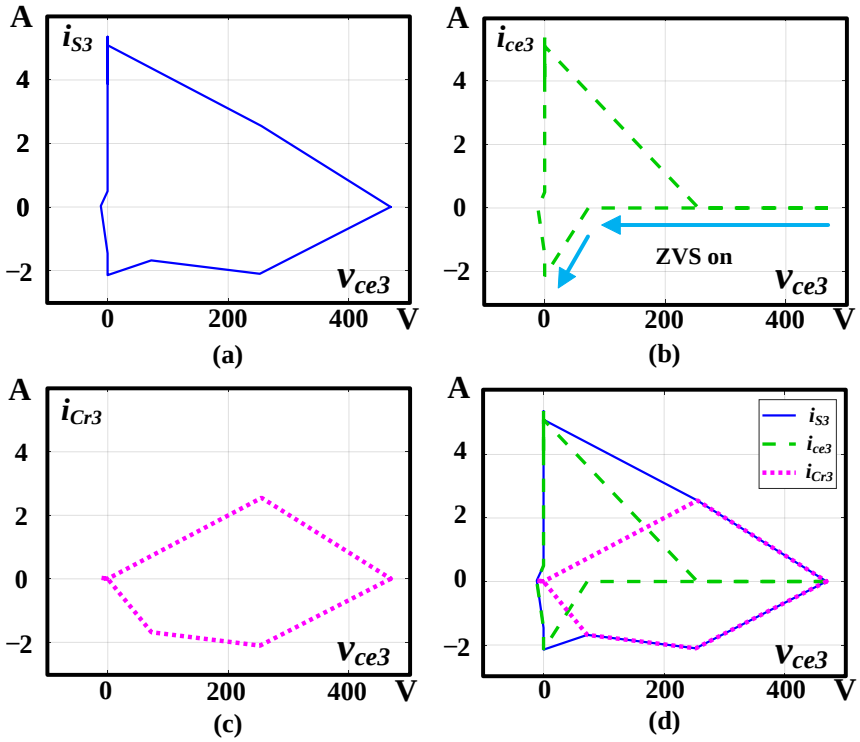

Figure 10. The ZVS process of switch S_3: (**a**) switch current i_{s3} vs. switch voltage v_{ce3}, (**b**) current i_{ce3} vs. switch voltage v_{ce3}, (**c**) capacitor current i_{cr3} vs. switch voltage v_{ce3} and (**d**) the overlap of (**a**–**c**) when the proposed bidirectional soft-switching converter was operating in the rectifier mode.

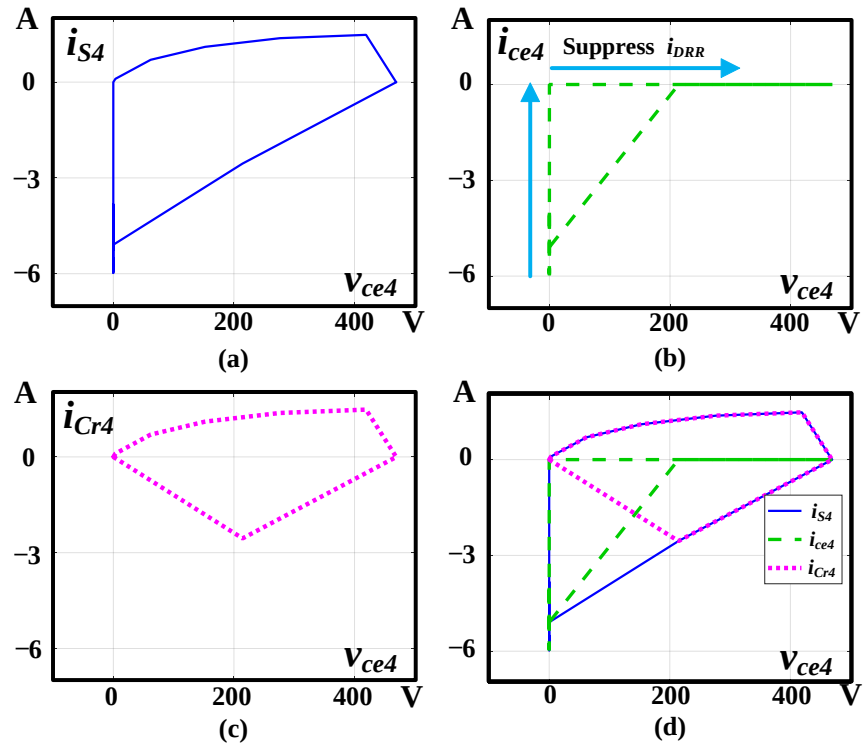

Figure 11. The process of diode reverse-recovery suppression of switch S_4: (**a**) switch current i_{s4} vs. switch voltage v_{ce4}, (**b**) current i_{ce4} vs. switch voltage v_{ce4}, (**c**) capacitor current i_{cr4} vs. switch voltage v_{ce4} and (**d**) the overlap of (**a**–**c**) when the proposed bidirectional soft-switching converter was operating in the rectifier mode.

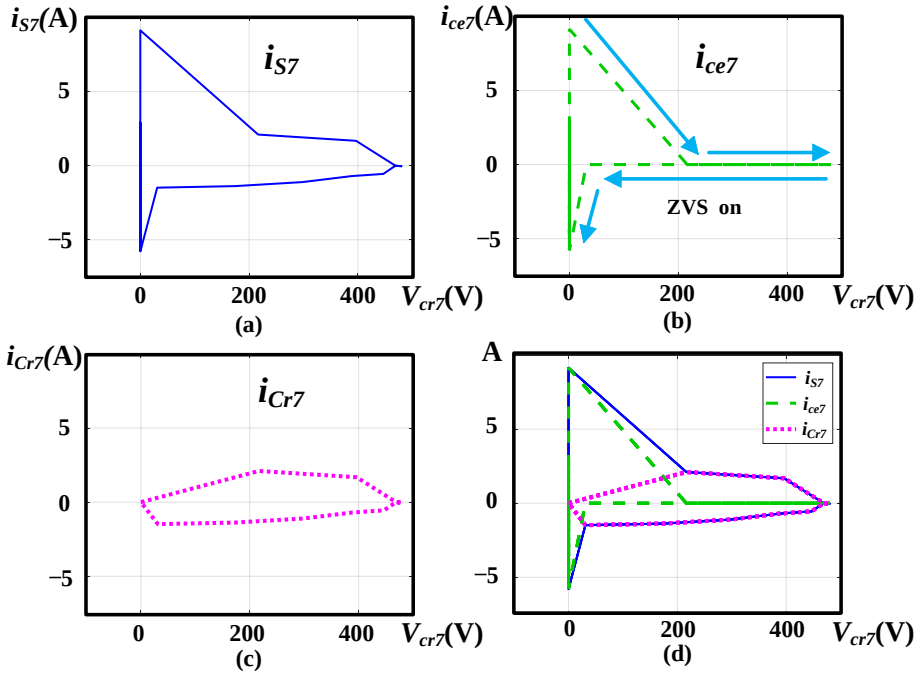

Figure 12. The ZVS process of switch S_7: (**a**) switch current i_{s7} vs. switch voltage v_{ce7}, (**b**) current i_{ce7} vs. switch voltage v_{ce7}, (**c**) capacitor current i_{cr7} vs. switch voltage v_{ce7} and (**d**) the overlap of (**a**–**c**) when the proposed bidirectional soft-switching converter was operating in the rectifier mode.

Similarly, the process of the ZVS operation and reverse-recovery-current suppression in the proposed bidirectional grid-tied ZVS three-phase converter operated in inverter mode are shown in Figures 13–15. As can be observed from Figures 13–15, the ZVS on of main switch S_4, the reverse-recovery-current suppression of main switch S_3 and the ZVS on of auxiliary switch S_7 were indeed achieved in the inverter mode.

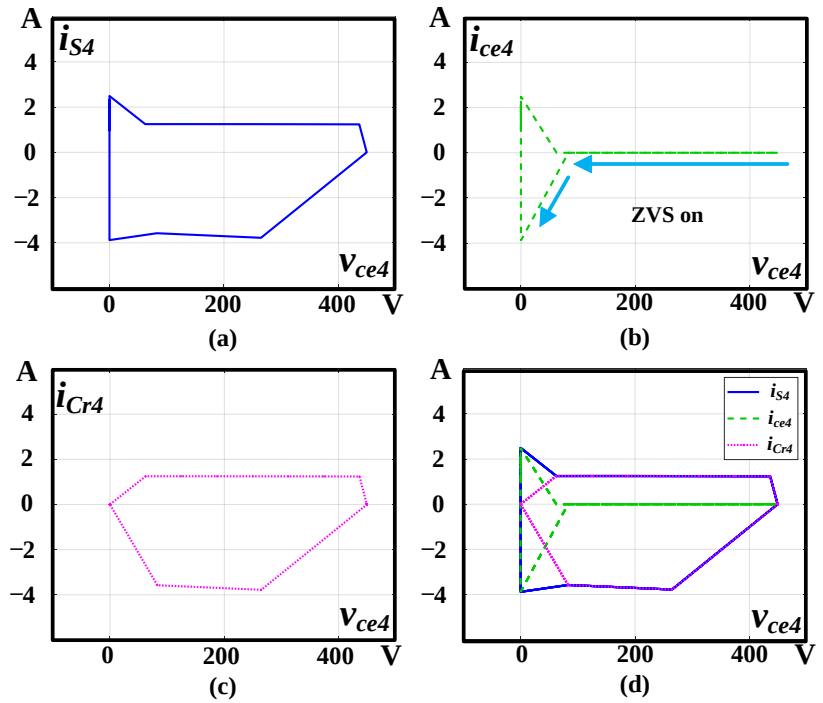

Figure 13. The ZVS process of switch S_4: (**a**) switch current i_{s4} vs. switch voltage v_{ce4}, (**b**) current i_{ce4} vs. switch voltage v_{ce4}, (**c**) capacitor current i_{cr4} vs. switch voltage v_{ce4} and (**d**) the overlap of (**a**–**c**) when the proposed bidirectional soft-switching converter was operating in the inverter mode.

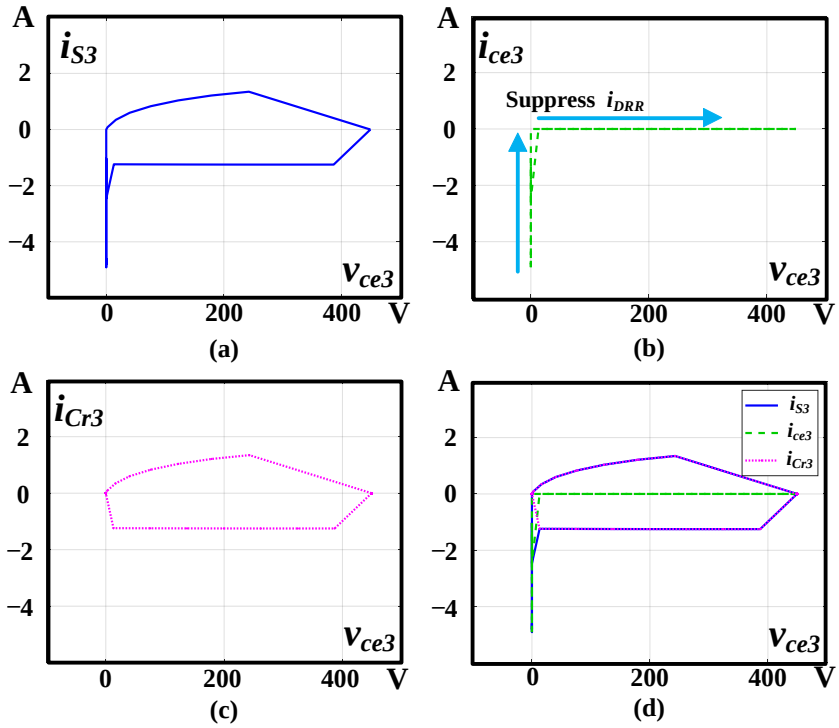

Figure 14. The process of diode reverse-recovery suppression of switch S_3: (**a**) switch current i_{s3} vs. switch voltage v_{ce3}, (**b**) current i_{ce3} vs. switch voltage v_{ce3}, (**c**) capacitor current i_{cr3} vs. switch voltage v_{ce3} and (**d**) the overlap of (**a**–**c**) when the proposed bidirectional soft-switching converter was operating in the inverter mode.

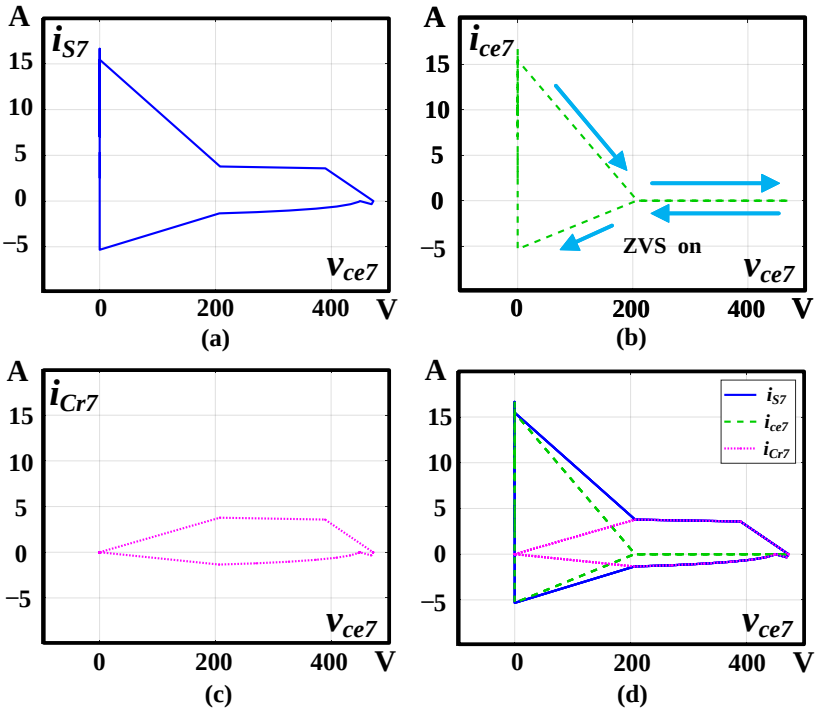

Figure 15. The ZVS process of switch S_7: (**a**) switch current i_{s7} vs. switch voltage v_{ce7}, (**b**) current i_{ce7} vs. switch voltage v_{ce7}, (**c**) capacitor current i_{cr7} vs. switch voltage v_{ce7} and (**d**) the overlap of (**a**–**c**) when the proposed bidirectional soft-switching converter was operating in the inverter mode.

The simulated waveforms of the DC bus voltage V_{dc}, phase-a voltage V_a and current i_a of the proposed bidirectional grid-tied ZVS converter operated in rectifier mode and

inverter mode are shown in Figures 16a and 16b, respectively. As can be seen from Figure 16, when the system was operated in the rectifier mode, the controlled grid-side current was in phase with the grid voltage, and when the system was operated in the inverter mode, the controlled grid-side current was phase-shifted by 180 degrees from the grid voltage.

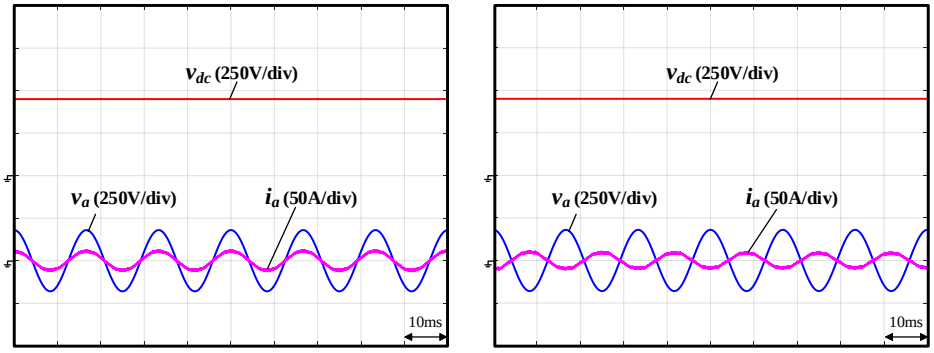

Figure 16. Simulated waveforms of the DC-link voltage, phase-a voltage and phase-a current of the proposed bidirectional soft-switching converter operated in (**a**) rectifier mode and (**b**) inverter mode.

According to the above simulation results, the proposed circuit topology and corresponding PWM control scheme could accomplish zero-voltage switching in the main switches and the auxiliary switch in both the rectifier and inverter modes. Meanwhile, the reverse recovery current of body diodes in the main switches was also suppressed.

4. Experimental Results

To facilitate the understanding of the proposed circuit topology and corresponding modulation control strategy, as well as provide verification, a prototype system was constructed with the parameters listed in Table 4. The adopted active switches were the insulated gate bipolar transistors (FUJI 2MBI100VA-120-50) with a parasitic capacitance C_r = 2 nF, and the system controller was implemented with DSP TMS320F28335/FPGA Cmod-A7-35T.

Figures 17 and 18 show the experimental waveforms when the proposed circuit was operated in the rectifier mode and inverter mode, respectively. While the system was operated in the rectifier mode, the measured switch voltage and current of switches S_3, S_4 and S_7 are shown in Figure 17a–c, respectively. As can be seen from Figure 17a–c, the main switch S_3 and auxiliary switch S_7 were turned on via ZVS, and the diode reverse recovery current of main switch S_4 was also suppressed when the system was operated in the rectifier mode. The voltage v_{Cc} of the clamping capacitor and the current i_{Lr} of the resonant inductor are shown in Figure 17d. It follows from Figure 17d that v_{Cc} was much smaller than V_{dc} such that the voltage stress on the main and auxiliary switches was $v_{cc} + V_{dc} \approx V_{dc}$. The voltage and current waveforms of diodes D_{inv} and D_{rec} are shown in Figures 17e and 17f, respectively. As can be observed from Figure 17e,f, the diode voltage stress is v_{Cc}. It should be noticed that the experimental waveforms of diode voltage and current in Figure 17e,f are in close agreement with the simulation waveforms in Figure 8e,f. The voltage across the two series diodes was $v_{Cc} = v_{dinv} + v_{drec}$.

While the system was operated in the inverter mode, the measured switch voltage and current of switches S_4, S_3 and S_7 are shown in Figure 18a–c, respectively. As can be seen from Figure 18a–c, the main switch S_4 and auxiliary switch S_7 were turned on via ZVS, and the diode reverse recovery current of main switch S_3 was also suppressed. The voltage v_{Cc} of the clamping capacitor and the current i_{Lr} of the resonant inductor are shown in Figure 18d. It follows from Figure 18d that v_{Cc} was much smaller than V_{dc} such that the voltage stress on the main and auxiliary switches was $v_{cc} + V_{dc} \approx V_{dc}$. In addition, the voltage and current waveforms of diodes D_{inv} and D_{rec} are shown in Figures 18e and 18f,

respectively. It follows from Figure 18e,f that the diode voltage stress was v_{Cc}, and the total voltage across the two series diodes was $v_{Cc} = v_{dinv} + v_{drec}$.

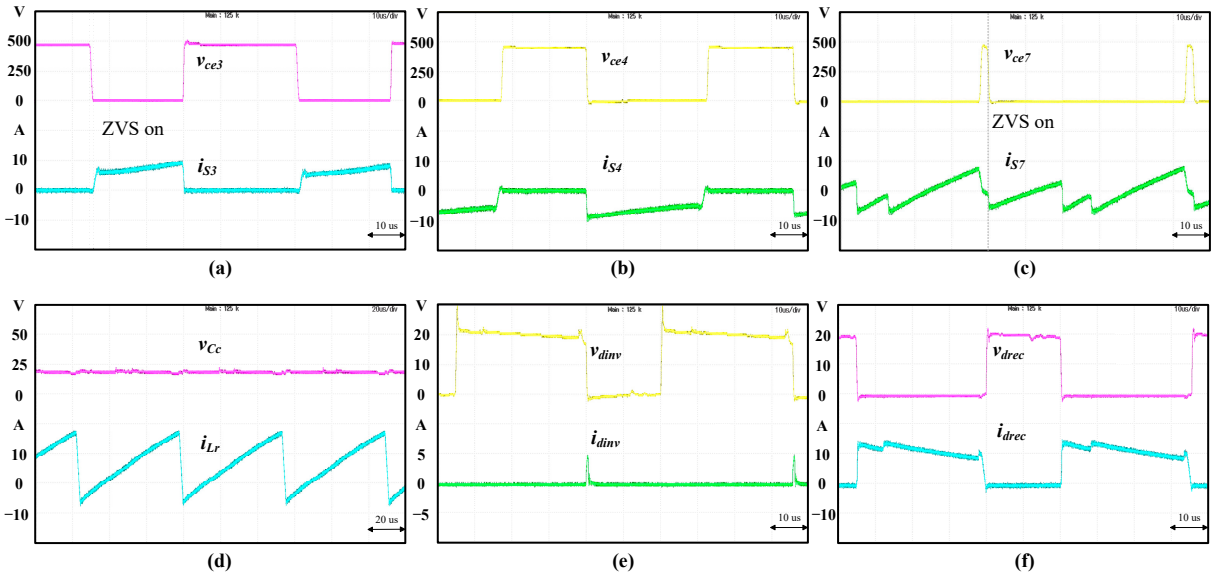

Figure 17. Measured waveforms of the proposed bidirectional soft-switching converter operating in the rectifier mode: (**a**) voltage and current of switch S_3 (ZVS turn-on), (**b**) voltage and current of switch S_4 (the diode reverse recovery current was suppressed), (**c**) voltage and current of auxiliary switch S_7, (**d**) the clamping capacitor voltage v_{Cc} and resonant inductor current i_{Lr}, (**e**) voltage and current of diode D_{inv}, and (**f**) voltage and current of diode D_{rec}.

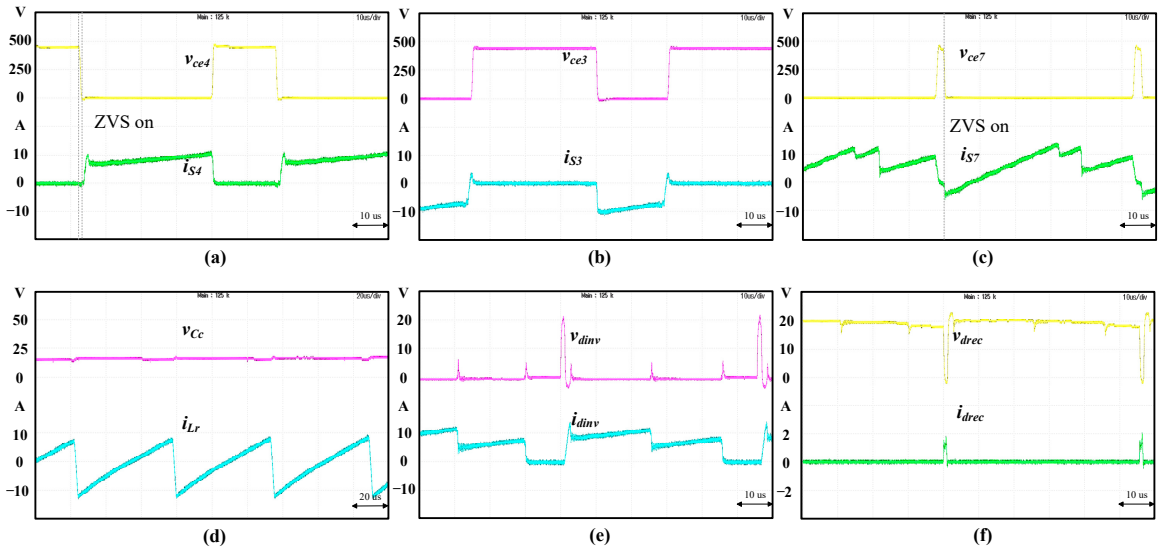

Figure 18. Measured waveforms of the proposed bidirectional soft-switching converter operating in the inverter mode: (**a**) voltage and current of switch S_4 (ZVS turn-on), (**b**) voltage and current of switch S_3, (the diode reverse recovery current was suppressed), (**c**) voltage and current of auxiliary switch S_7, (**d**) the clamping capacitor voltage v_{Cc} and resonant inductor current i_{Lr}, (**e**) voltage and current of diode D_{inv}, and (**f**) voltage and current of diode D_{rec}.

In addition, the light load condition of 300 W for 10% of the rated output power was considered. The rectifier and inverter operations are shown in Figure 19a,b and Figure 19c,d, respectively. As can be observed from Figure 19a,b, the auxiliary switch S_7 and main switch S_3 were turned on via ZCS/ZVS when the converter was operated in the rectifier mode. It

follows from Figure 19c,d that the auxiliary switch S_7 and main switch S_4 were also turned on via ZCS/ZVS when the converter was operated in the inverter mode.

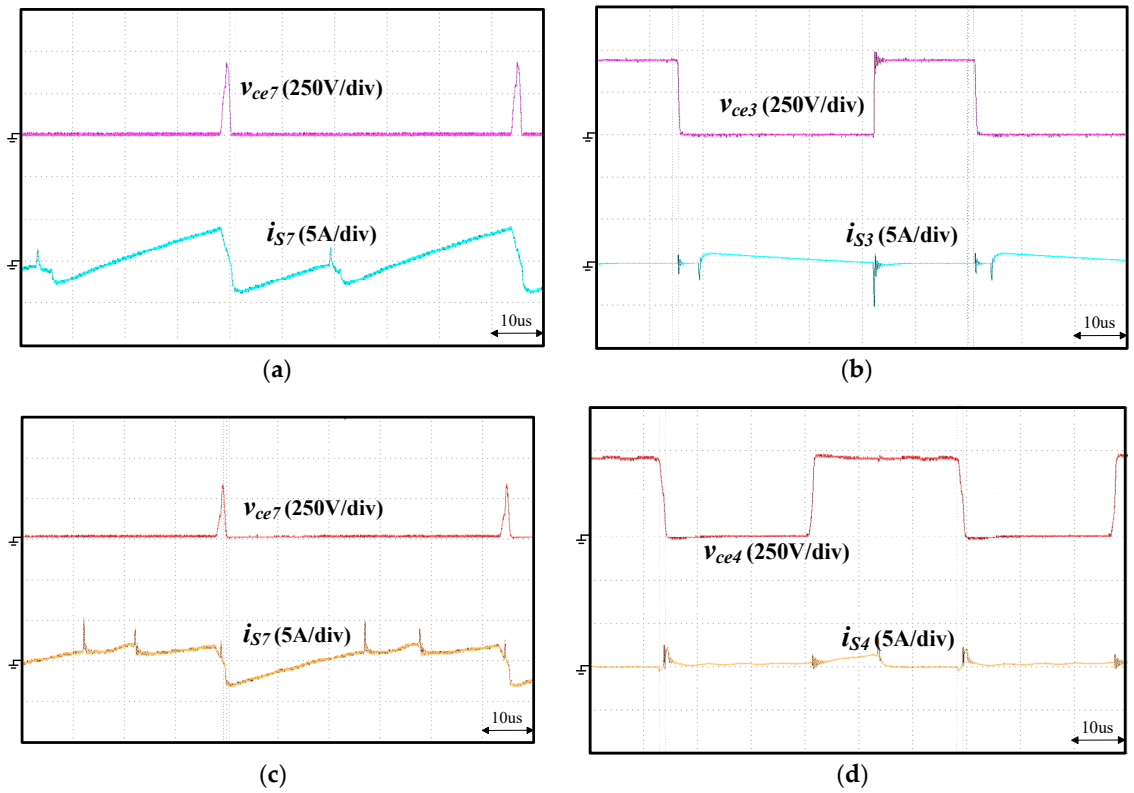

Figure 19. Measured waveforms of the proposed bidirectional soft-switching converter at 300 W while (**a**,**b**) operating in the rectifier mode and (**c**,**d**) operating in the inverter mode: (**a**) voltage and current of auxiliary switch S_7, (**b**) voltage and current of switch S_3, (**c**) voltage and current of auxiliary switch S_7, and (**d**) voltage and current of switch S_4.

Finally, in order to understand the bidirectional power flow functionality of the proposed ZVS grid-tied three-phase converter, the measured waveforms of the DC bus voltage V_{dc}, phase-a voltage V_a and current i_a in both rectifier mode (3 kW) and inverter mode (3 kW) are depicted in Figures 20a and 20b, respectively. According to the control block illustrated in Figure 6, the bidirectional power flow was achieved in the proposed grid-tied ZVS three-phase converter.

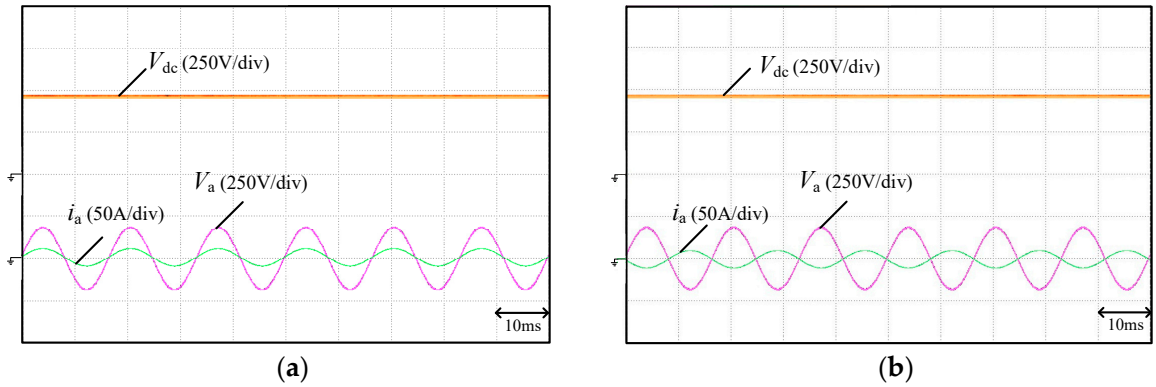

Figure 20. Measured waveforms of DC bus voltage V_{dc}, phase-a voltage V_a and current i_a of the proposed grid-tied ZVS three-phase converter operated in the (**a**) rectifier mode (3 kW) and (**b**) inverter mode (3 kW).

Next, the efficiency was measured using three YOKOGAWA WT310Es. Compared with the traditional hard switching SPWM without an auxiliary circuit, the measured efficiency of the proposed circuit topology and control scheme in the rectifier mode and inverter mode was 3~4% higher than that of the hard switching control scheme, which is illustrated in Figure 21. The realized prototype of the proposed system is shown in Figure 22.

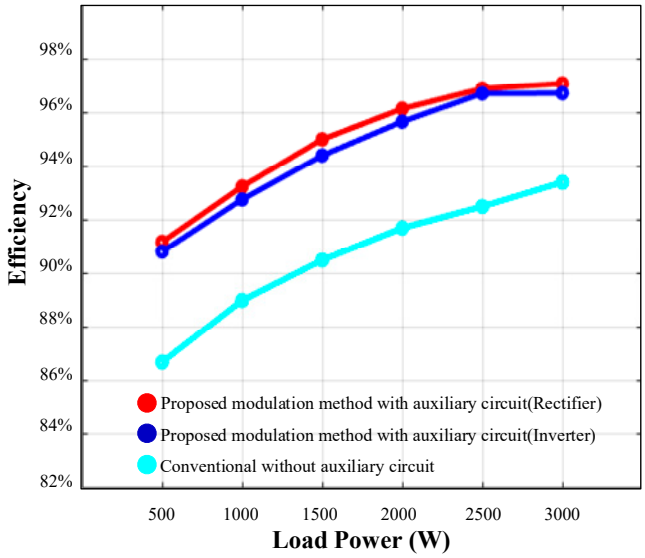

Figure 21. Measured efficiency of the bidirectional three-phase converter operated in hard switching SPWM without auxiliary circuit and proposed ZVS converter during rectifier and inverter modes.

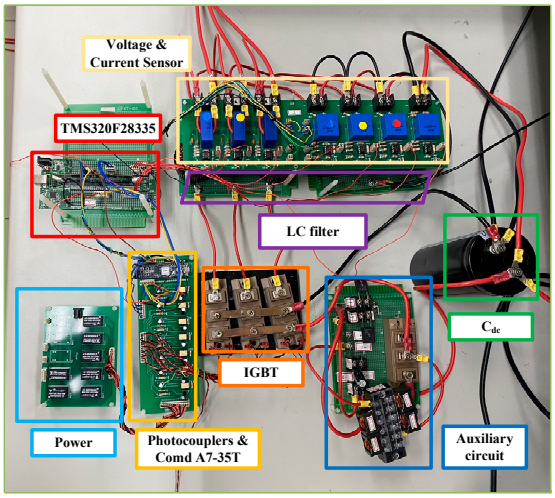

Figure 22. Realized prototype of the proposed system.

Finally, the current total harmonic distortion THD_i and power losses were analyzed. Figure 23 shows the THD_i versus output power for both rectifier and inverter operation. As depicted in Figure 23, it is evident that the higher the output power, the lower THD_i became. Next, the power loss distributions are shown in Figures 24 and 25 for the rectifier mode and inverter mode, respectively. In the power loss distribution, the IGBT Semikron SKM200GB125D and diode Powerex CS240650 were adopted in the simulation software to analyze the conduction loss, turn-off loss, diode loss, copper loss and core loss. As can be seen from Figures 24 and 25, the total power loss during inverter operation was higher than that during rectifier operation due to the difference in auxiliary circuit paths between the inverter and rectifier operations.

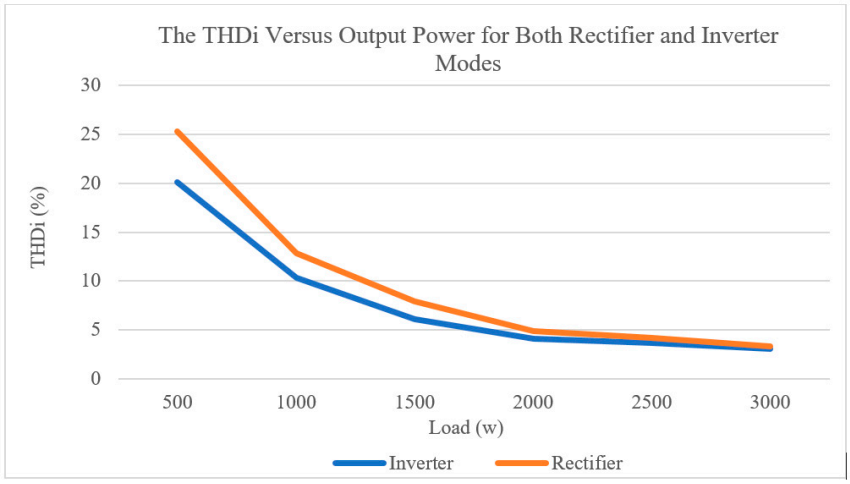

Figure 23. The simulated total harmonic distortion THDi for both rectifier and inverter operations.

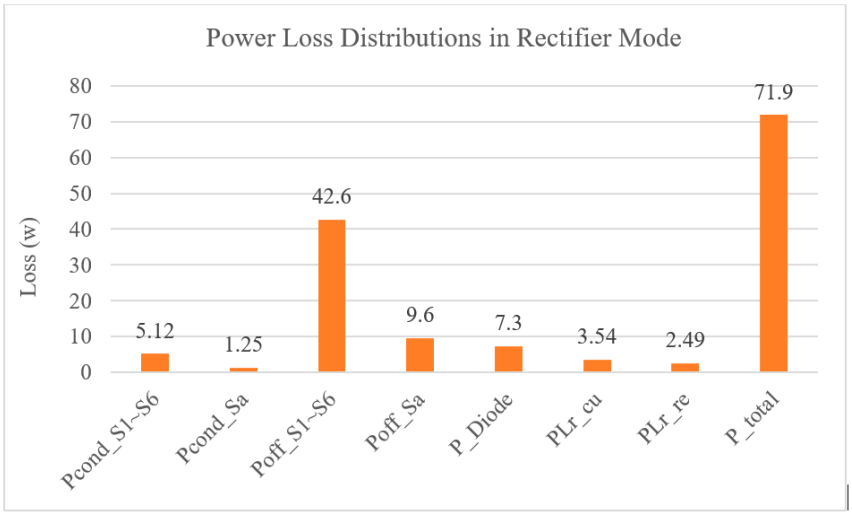

Figure 24. The simulated power loss distribution for rectifier operation.

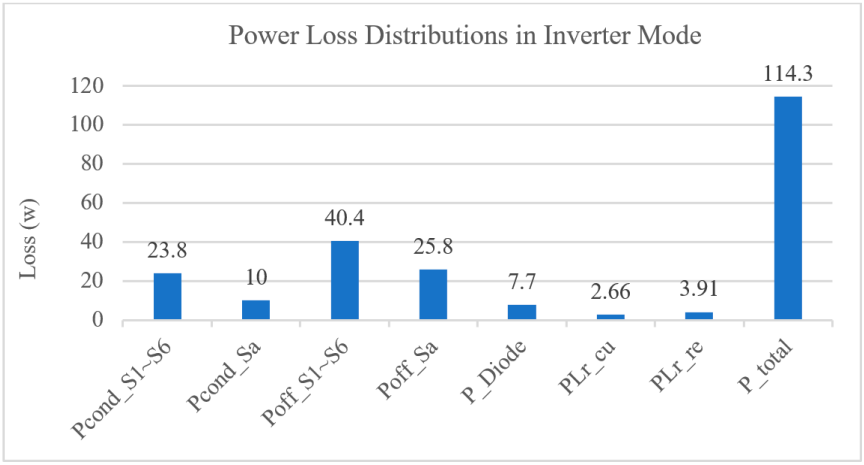

Figure 25. The simulated power loss distribution for inverter operation.

5. Conclusions

This paper proposed a bidirectional grid-tied ZVS three-phase converter topology. In addition, a zero-voltage-switching PWM strategy for a grid-connected three-phase converter is proposed. The control signal for the auxiliary switch is produced using a sawtooth

carrier waveform encompassing both positive and negative gradients. This approach is utilized to attain ZVS across both the main and auxiliary switches. Furthermore, the reverse recovery currents in the anti-parallel diodes of the main switches are effectively mitigated. The operational principles of the circuit are extensively elucidated for both rectifier and inverter modes. Both simulation and experimental results verified the validity of the proposed circuit topology and the proposed ZVS DPWM strategy in the bidirectional grid-tied three-phase system. The measured efficiency of the proposed system was about 3~4% higher than that of a conventional SPWM hard-switching system. It is worth mentioning that the soft switching strategies usually suffer from high voltage and current stress of the semiconductors, which will decrease the power rating of the original design. The proposed topology and PWM control scheme also had those limitations.

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