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Simple Discrete Control of a Single-Phase Voltage Source Inverter in a UPS System for Low Switching Frequency

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Abstract: Previous research has shown that the inverter output voltage distortions are higher for low switching frequencies, and it is impossible to increase the controller gains because it will cause oscillations of the output voltage. The main reason is the real frequency domain characteristic of the PWM modulator and measuring traces, which can be modelled as switching periods delays. The thesis of this paper is that by using the control system that takes care of these delays, it is possible to decrease output voltage distortions for the standard loads for relatively low switching frequencies (e.g., 12,800 Hz). The Luenberger observer was implemented in the multi-input-multi-output passivity-based control of the system with the delay, in order to predict the state variables of the inverter. It is shown that state variable prediction is unnecessary for high switching frequencies (e.g., 51,200 Hz). The theory, simulations and breadboard verification, using the inverter model controlled with the real-time interface MicroLabBox, are presented.

Keywords: voltage source inverter; coefficient diagram method; passivity-based control; real-time interface; Luenberger observer

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1. Introduction

The problem of controlling the voltage source inverter (VSI) is important in UPS systems. These systems should fill the requirements of the EN-62040-3 standard [1], in which the static and dynamic, linear and nonlinear loads are defined. To design such a control system, the inverter should be defined and modelled taking in care the properties of the output filter coil core [2–4]. Linear modelling in the operating point seems sufficient and is commonly used; however, there are many approaches (Section 2) to the nonlinearity of the inverter model [5–7]. Today, sophisticated control is only digital, so discrete models are required. It can be discretised from the continuous model or calculated as a discrete system from state equations [8]. The first parameter of the VSI is the capacitance C_F and ESR (equivalent serial resistance) R_{CF} of the output filter capacitor—typically MKP. The capacitance C_F is tens of μF and it is possible to assign a nominal value as real, whereas ESR is negligible. The inductance L_F of the output filter coil for a high-quality coil core (e.g., Sendust alloy powder [9]) can be assigned as equal to the nominal value. For a cheap coil core (iron powder [10]), the inductance L_F should be measured. In both cases of coil cores, the serial resistance R_{LF}, depending mainly on the power losses in the core, seriously increases with the increase in the magnetizing coil current and its frequency is equal to the switching frequency. The best solution is to measure this resistance. It should be summed with the other serial resistances. Switched-on bridge transistors have a resistance from 50 to 200 mΩ per transistor. Two are always conducting, and the resistance of the PCB traces and connectors is present. Altogether, the sum of serial resistances is called in the paper "equivalent serial resistance" R_{LFe}. The method for calculating the parameters of the VSI from its measured Bode plots enables the creation of the VSI model in the operating point [11–13]. The PWM modulator introduces one switching period

delay. The feedback loop has galvanic isolation in all the voltage and current channels (the isolated amplifier in the output voltage channel, and transducers in the output and inductor channels), difference amplifiers, antialiasing filters, and analogue-to-digital converters. As it can be easily proved, the feedback loop operates efficiently (decreases the VSI output impedance) below the resonant frequency of the output filter [14]. This frequency is usually about 1 kHz. In this frequency range, the Bode plots of the feedback loop have been measured and successfully modelled in experimental models as the delay [15]. The PWM modulator and measuring trace can be modelled as a delay of two to three switching periods. The main thesis of this paper is that by using the control system that takes care of the delay, it is possible to decrease the output voltage distortions of standard loads for a low (≤12,800 Hz) switching frequency. The Luenberger observer [16–19] for the state variables for the multi-input-single-output control will be used. Section 2 presents the simple continuous model of the VSI. Section 3 describes the used modulation scheme for the three-level, double-edge PWM. Section 4 concerns the design of the output filter. Section 5 shows the method of discretizing the continuous model, while Section 6 presents the fully discrete model calculated directly from the state equations. Section 7 describes the identification of the VSI plant and the measuring traces of the VSI. Section 8 presents the theory of PBC control with the prediction of state variables and the simulations for different systems with a low switching frequency in control systems, with and without prediction. Section 9 presents MATLAB/Simulink simulations of the inverter. Section 10 shows breadboard verification. Section 11 presents the results of the simulation and the experimental verification. Section 12 is a discussion. Section 13 contains conclusions.

It is possible to assume that the equivalent serial resistance of the capacitor C_F is $R_{CF} \approx 0$ (for parallel connected MKP metallized polyester capacitors in the experimental inverter, less than 10 mΩ). R_{LFe} is the equivalent serial resistance of the whole inverter—the serial resistance of the filter coil L_F, the switched-on transistors in the bridge and PCB traces. It was shown in [11–13] that R_{LFe} is much higher than the DC resistance of the coil, depending on the switching frequency ($f_s = 1/T_s$), the magnetizing coil current and, very strongly, on the coil core's power losses. It was shown in [11–13] that the worst material is iron powder (e.g., Material Mix −26) and alloy powder (iron, silicon, aluminium); however, MS Sendust (previous name: Super MSS) is a very good material with a reasonable price [9,12].

$$K_{CTRL}(s) = \frac{V_{OUT}(s)}{V_{CTRL}(s)} = e^{-sT_s} K_{INV} = e^{-sT_s} \frac{V_{OUT}(s)}{V_{FIN}(s)} = e^{-sT_s} \frac{{\omega_{F0}}^2}{s^2 + 2\xi_{Fe}\omega_{F0}s + (1 + \frac{R_{LFe}}{R_{LOAD}}){\omega_{F0}}^2}, \quad (1)$$

where

$$\omega_{F0} = \frac{1}{\sqrt{L_F C_F}}, \ \xi_{Fe} = \frac{1}{2}(R_{LFe}\sqrt{\frac{C_F}{L_F}} + \frac{1}{R_{LOAD}}\sqrt{\frac{L_F}{C_F}}). \quad (2)$$

A modification of this simple model is the quasi-continuous transfer function [20,21] of the inverter (including R_{LOAD}), which considers further ZOH discretization for the discrete control purpose (introducing the delay of half of T_s) and one T_s delay of the PWM modulator (3).

$$K_{CTRL}(s) = \exp(-s\frac{T_s}{2})\exp(-sT_s)F_{LC}(s) \approx (1 - s\frac{T_s}{2})\frac{1 - s\frac{T_s}{2}}{1 + s\frac{T_s}{2}} \frac{{\omega_{F0}}^2}{s^2 + 2\xi_F\omega_{F0}s + (1 + \frac{R_{LFe}}{R_{LOAD}}){\omega_{F0}}^2} \quad (3)$$

Modelling the load current as an independent disturbance or state variable has been the standard approach in inverter research for 40 years [22–28]. This allows the load impedance to be neglected in the state matrix. However, we are missing one feedback loop from the output voltage V_{OUT} to the load current I_{OUT}. After designing the control system, it is possible to check how the omission of this loop changes the real position of the poles of the closed-loop system (whether they do not go beyond the unit circle in the z plane). In [24] was shown how the omission of the load resistance shifts poles of the closed-loop system when using the Coefficient Diagram Method of the control [29–31].

2. Continuous Model of the Voltage Source Inverter

Creating the VSI model and its mathematical description is the basic subject of the VSI control design. In [5], the calculation of the nonlinear characteristic of the coil in the LC output filter and its influence on the adaptive control loop were shown. Depending on the inductor core material, its inductance and the equivalent serial resistance varies with the amplitude and the frequency of the magnetizing current [2–4].

The influence of the nonlinear characteristic of the inductor in the inverter output filter on the design of the adaptive control loop (with the calculation of the nonlinear inductance characteristic) was presented in [5]. The change in the coil's inductance and its equivalent serial resistance as a function of the amplitude and the frequency of its magnetizing current depends on the core material [2–4]. The change in inductance is small, 5%, for iron–silicon–aluminium alloy powder materials (e.g., Sendust (MS)/Super-MSS™ [9]). The equivalent serial resistance resulting from power losses in the core, in the core operating point for this core material, is 3–5 times lower than for a cheaper iron-powder material mix −26 [12]. So, the coil core material has an impact on the VSI model. The state–space equations of the VSI with pulse width modulation (PWM) can be solved, resulting in the nonlinear (exponential) dependency of state–space variables on the duty ratio of pulses [8]. In [6], the approximation by the Fourier series of the nonlinear control law was presented. Hammerstein's approach (decomposition of the input–output relationship, where dynamics are represented by a linear transfer function and nonlinearities are represented through the identified black box) to the nonlinear modelling of VSI was presented in [7]. The nonlinear modelling of VSI is a bit more accurate than models with linear approximation of the inverter in the operation point; however, the linear theory results in quite acceptable accordance with the experimental VSI verification. The linear theory enables the simple design of the VSI controller.

The continuous linear model of the single-phase inverter is just the output LC filter and the discrete PWM modulator that can be modelled as a delay with the switching period T_s. The PWM modulator is a digital circuit (e.g., microprocessor) in which we store the duty ratio of the output pulse, and these data are on the output of the modulator in the next period.

The state vector is assigned as $\mathbf{x} = [v_{OUT}\ i_{LF}\ i_{OUT}]^T$, the input vector (in the presented case, one variable) is $\mathbf{u} = v_{FIN}$ and the output vector (in the presented case, one variable) is $\mathbf{y} = v_{OUT}$. The PWM modulator transfer function is $H_{PWM} = \exp(-sT_s)$.

The state matrix, input matrix and output matrix are (4).

$$\mathbf{A} = \begin{bmatrix} 0 & \frac{1}{C_F} & -\frac{1}{C_F} \\ -\frac{1}{L_F} & -\frac{R_{LFe}+R_{CF}}{L_F} & \frac{R_{CF}}{L_F} \\ 0 & 0 & 0 \end{bmatrix},\ \mathbf{B} = \begin{bmatrix} 0 \\ \frac{1}{L_F} \\ 0 \end{bmatrix},\ \mathbf{C} = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix}. \tag{4}$$

The continuous time-invariant state–space equation is (5).

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \tag{5}$$

Finally, for $R_{CF} \approx 0$, the transfer function of the control voltage and the disturbance (the output current) is (6).

$$V_{OUT}(s) = H_{PWM}\frac{{\omega_{F0}}^2}{s^2 + s\frac{R_{LFe}}{L_F} + {\omega_{F0}}^2}V_{CTRL}(s) - \frac{(sL_F + R_{LFe}){\omega_{F0}}^2}{s^2 + s\frac{R_{LFe}}{L_F} + {\omega_{F0}}^2}I_{OUT}(s) \tag{6}$$

The transfer control function of the VSI is (7).

$$K_{CTRL}(s) = \frac{V_{OUT}(s)}{V_{CTRL}(s)} = \exp(-sT_s)K_{INV} = \exp(-sT_s)\frac{V_{OUT}(s)}{V_{FIN}(s)} = \exp(-sT_s)\frac{{\omega_{F0}}^2}{s^2 + s\frac{R_{LFe}}{L_F} + {\omega_{F0}}^2} \tag{7}$$

where the output impedance of the VSI with the open loop, that is, the disturbance transfer function, is (7).

$$Z_{OUT}(s) = -\frac{V_{OUT}(s)}{I_{OUT}(s)} = \frac{(sL_F + R_{LFe})\omega_{F0}{}^2}{s^2 + s\frac{R_{LFe}}{L_F} + \omega_{F0}{}^2} \quad (8)$$

3. Modulation Scheme

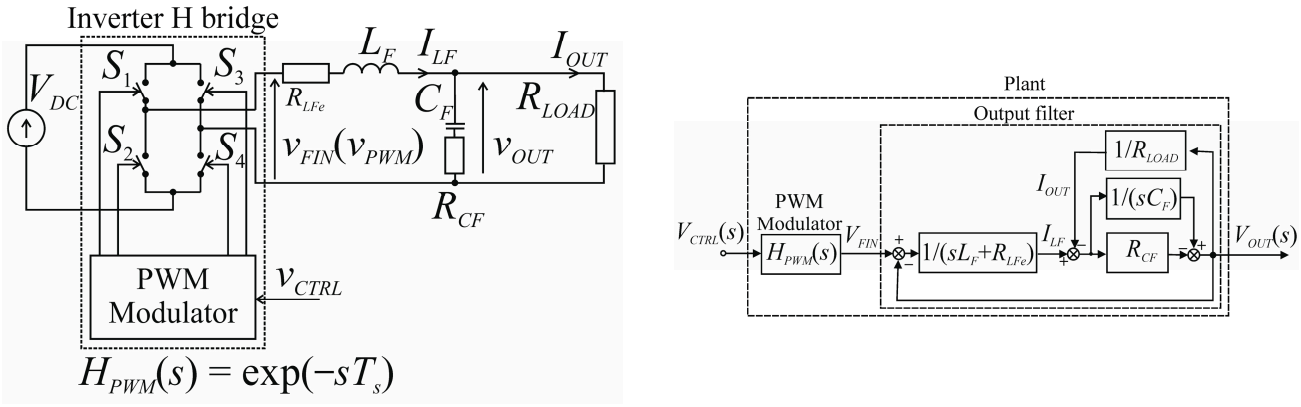
The two-leg H bridge enables two or three levels of single-phase modulation. The three-level modulation results in a much lower level of harmonics than the two levels, in the sinusoidal modulated PWM waveform for the low modulation coefficient [32]. Each microprocessor that can be used to control VSI has the possibility of two-edge modulation that results in lower low-order harmonics than single-edge modulation. There are different modulation schemes—algorithms for driving the transistors in the H bridge in the three-level, two-edge single-phase modulation [32–34]. The best for control purposes is the first PWM scheme, in which it is possible to control the output waveform when it crosses the zero value. The transistors of a (two-leg) H-bridge (Figures 1a and 2a) in the first modulation scheme (Figure 3), are switched with the frequency f_s. The current flows through the serial connection of two switches on the diagonal of the bridge (S_1 and S_4 or S_3 and S_2, Figures 1a and 2a) and the output PWM waveform, which has a double $2f_s$ frequency is a coincidence of switching on two transistors. The control of the switches is described by Equations (9)–(12) and is presented in Figure 3. T_{ON} is the switching-on time. The double-output switching frequency enables one to design an output filter with the lower values of the filter parameters without increasing the switching frequency of transistors. For $k = 1$ to (f_s/f_m):

$$S_1 : T_{ON}(k)/T_s = 0.5M \sin(k\frac{2\pi}{f_s/f_m}) + 0.5M \quad (9)$$

$$S_2 : NOT(S_1) \quad (10)$$

$$S_3 : T_{ON}(k)/T_s = 0.5M \sin((k\frac{2\pi}{f_s/f_m}) + \pi) + 0.5M \quad (11)$$

$$S_4 : NOT(S_3) \quad (12)$$



(**a**) (**b**)

Figure 1. The continuous model: (**a**) inverter model and (**b**) block diagram.

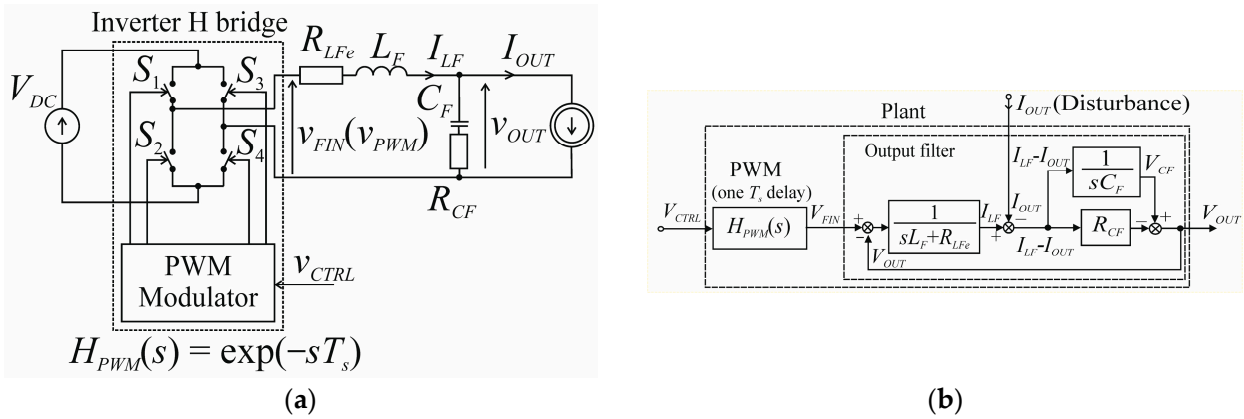


Figure 2. The simple continuous model with I_{OUT} as a disturbance: (**a**) inverter model and (**b**) block diagram for modelling the load current as an independent disturbance.

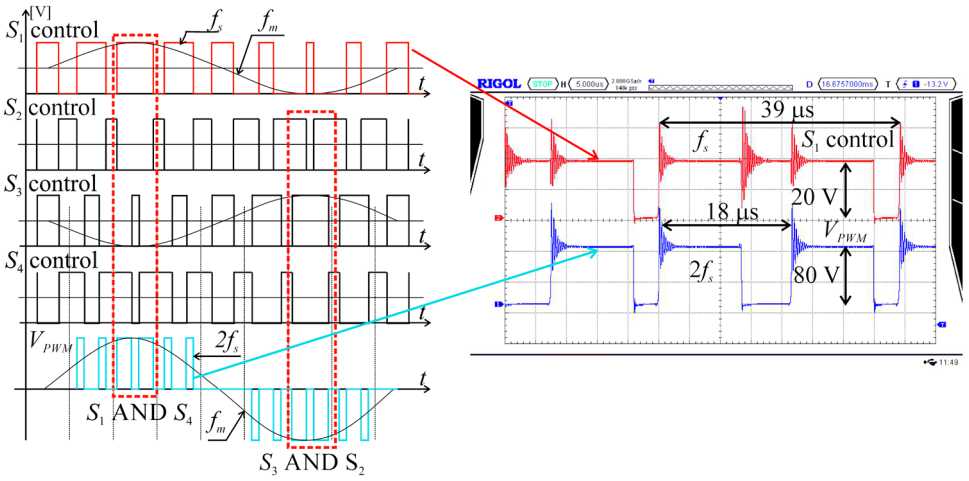


Figure 3. The first schema of the double−edge, 3−level PWM.

4. Design of the Output Filter

The VSI model was based on the output L_FC_F filter. The restriction of the output voltage ripple amplitude (13) $0.5V_{OUTripplepp}$ of up to 3% determines the value of the product of L_FC_F (14). Calculating the quotient L_F/C_F is more ambiguous [8,32,35]. One of the solutions is creating the "cost function" $F_{\cos t}$ (14) as a sum of absolute values of reactive power in the filter components [8,32,35–37]. However, the reactive power of an inductor is sometimes weighted two-times higher than that of the capacitor [36,37], because the reduced L_F value decreases the VSI output impedance for the low frequency and improves the VSI dynamic properties. The presented design of the filter (17) is based on the minimization of the "cost function", with the same weights for both absolute values of reactive powers of the inductor and capacitor [8,35,38]. The case of a single-phase, H-bridge, three-level inverter was presented. The L_F and C_F values depend on the load R_{LOAD} and the switching frequency f_s.

$$0.5V_{OUTripplepp}\Big|_{\max} \le 3\%V_{OUTh1} \tag{13}$$

From (13)

$$L_FC_F \ge \frac{1}{f_s} \tag{14}$$

The cost function $F_{\cos t}$ (15).

$$F_{\cos t} = \omega_m L_F I^2_{LFh1RMS} + \omega_m C_F V^2_{OUTh1RMS} = \omega_m L_F I^2_{LFh1RMS} + \omega_m \frac{1}{f_s L_F} V^2_{OUTh1RMS} \tag{15}$$

$$\frac{\partial F_{\cos t}}{\partial L_F} = 0 \tag{16}$$

The particular values of L_F and C_F from (14) and (16)

$$L_F \approx \frac{1}{f_s} R_{LOAD},\ C_F \approx \frac{1}{f_s} \frac{1}{R_{LOAD}} \tag{17}$$

Similar output filter calculations are the result of calculations presented in [39].

When the effective switching frequency of the V_{FIN} is equal to 51,200 Hz (the double-switching frequency f_s = 25,600 Hz of the bridge transistors, Figure 3), R_{LOAD} = 50 Ω, the result from (17) is L_F = 1 mH, C_F = 0.4 μF; let us use C_F = 1 μF. The feedback is always delayed by at least one switching frequency period T_s = 39 μs (f_s = 25,600 Hz) in the digital PWM modulator. It is possible to assume that the inductor current is constant during one switching period and there is a resistive load. If the amplitude of the output current I_{LFmax} is 5 A and the load is fully decreased in the maximum of output sinusoidal voltage, the increase in the output voltage will be $\Delta V_{OUT} = T_s I_{LFmax}/C_F$ = 195 V. Such an instant increase in the output voltage is unacceptable (and saturates the control unit of VSI which can lead to further oscillations of the output voltage) and the C_F value should be increased to 50 μF. In this case, the increase in the output voltage ΔV_{OUT} = 4 V is acceptable. The presented values, about 1 mH and 50 μF, are typical for the low-output-power VSI.

5. Discretizing the Continuous Model of the VSI

Contemporary VSI is controlled using microprocessors or other digital devices (e.g., FPGA). The simplest approach is to discretize the continuous model of the inverter without delays $K_{INV} = V_{OUT}(s)/V_{FIN}(s)$. The approximation of the transformation $s = (\ln z)/T_s$ should be used. The bilinear transform (Tustin) s = $(2/T_s)(z-1)/(z+1)$ gives the results most similar to the exact logarithmical transformation of the left half plane s into the unity circle in the plane z. The MATLAB c2d function with, e.g., the 'Tustin' discretization method can be used (18) and (19).

$$K_{INV}(s) = \frac{V_{OUT}(s)}{V_{FIN}(s)} = tf([{\omega_{F0}}^2], [1 \ \ 2\xi_{Fe}\omega_{F0}\ {\omega_{F0}}^2]); \tag{18}$$

$$K_{INVc2d}(z) = c2d(K_{INV}, T_s, 'tustin'); \tag{19}$$

Finally, Equation (20) introduces the PWM modulator delay.

$$K_{CTRLc2d}(z) = z^{-1} K_{INVc2d}(z); \tag{20}$$

All the discretisation methods introduce the delay (it was taken care of in model (3)). The disadvantage of this method is the same result for the single- or double-edged modulation, while the double-edged modulation introduces an additional delay (the voltage pulse T_{OFF} time when the transistor is switched off depends on the previous pulse) and a lower THD.

6. The Discrete Model of the VSI

The discrete model of the VSI is created as a linearized solution of the state–space equation of the inverter for a particular method (e.g., single- or double-edged) of PWM [8,32,38,40]. For a multidimensional MIMO system with r inputs, n state variables and p outputs, using the solution of state equations for $\mathbf{x}(t) \in \mathbf{R}^n$, $\mathbf{u}(t) \in \mathbf{R}^r$, $\mathbf{y}(t) \in \mathbf{R}^p$, initial variable conditions $x(t_0)$ and control conditions $u(t_0)$, where $\mathbf{x} = [v_{OUT}\ i_{LF}\ i_{OUT}]^{\mathrm{T}}$, $\mathbf{u} = v_{FIN}$, $\mathbf{y} = v_{OUT}$, it is possible to solve state–space Equation (5).

The general solution in one switching period for $0 \leq t \leq T_s$ is (21).

$$\mathbf{x}(t) = e^{\mathbf{A}(t-t_0)}\mathbf{x}(kT_s) + \int_{t_0}^{t} e^{\mathbf{A}(t-\tau)}\mathbf{B}\mathbf{u}(\tau)d\tau \tag{21}$$

The solution of Equation (21) can be solved in the particular sectors of the switching period T_s for the double-edged PWM [32]. To linearize the solution of the equation the linear approximation (22) is used.

$$e^{\mathbf{A}T_{ONk}/2} = \mathbf{I} + \mathbf{A}T_{ONk}/2 + \mathbf{A}^2T_{ONk}^2/4 \ldots \approx \mathbf{I} + \mathbf{A}T_{ONk}/2 \tag{22}$$

Finally, the linearized state space equations are (23)–(25).

$$\mathbf{x}((k+1)T_s) = e^{\mathbf{A}T_s}\mathbf{x}(kT_s) + e^{\mathbf{A}T_s/2}\mathbf{B}V_{DC}T_{ON}(kT_s) \tag{23}$$

$$\mathbf{x}_{k+1} = \mathbf{A}_D\mathbf{x}_k + \mathbf{G}_DT_{ONk} \tag{24}$$

$$\mathbf{y}_k = \mathbf{C}_\mathrm{D}\mathbf{x}_k \tag{25}$$

The discrete state $\mathbf{A}_D$ and control $\mathbf{G}_D$ matrixes are (26)–(28).

$$\mathbf{A}_D = e^{\mathbf{A}T_s} = \mathbf{\Phi}(T_s) = L^{-1}[(s\mathbf{I} - \mathbf{A})^{-1}]\Big|_{t=T_s} \tag{26}$$

$$\mathbf{G}_D = e^{\mathbf{A}T_s/2}\mathbf{B}V_{DC} = \mathbf{\Phi}(T_s/2)\mathbf{B}V_{DC} \tag{27}$$

$$\mathbf{A}_D = \mathbf{\Phi}(T_s) = \begin{bmatrix} \phi_{11} & \phi_{12} & \phi_{13} \\ \phi_{21} & \phi_{22} & \phi_{23} \\ \phi_{31} & \phi_{32} & \phi_{33} \end{bmatrix},\ \mathbf{G}_D = \begin{bmatrix} g_{11} \\ g_{21} \\ g_{31} \end{bmatrix},\ \mathbf{C}_D = \mathbf{C} \tag{28}$$

where

$$\xi_F = \frac{1}{2}R_{LFe}\sqrt{\frac{C_F}{L_F}};\ \omega_{F0} = \frac{1}{\sqrt{L_FL_F}},$$

$$\phi_{11} = [\cos(\omega_{F0}T_s) + \xi_F\sin(\omega_{F0}T_s)]\exp(-\xi_F\omega_{F0}T_s),$$

$$\phi_{12} = \frac{1}{\omega_{F0}C_F}\sin(\omega_{F0}T_s)\exp(-\xi_F\omega_{F0}T_s),$$

$$\varphi_{13} = -\varphi_{12} + R_{LFe}(\varphi_{11} - 1),$$

$$\phi_{21} = -\frac{C_F}{L_F}\varphi_{12},$$

$$\phi_{22} = [\cos(\omega_{F0}T_s) - \xi_F\sin(\omega_{F0}T_s)]\exp(-\xi_F\omega_{F0}T_s),$$

$$\phi_{23} = 1 - \varphi_{11};\ \phi_{31} = 0;\ \phi_{32} = 0\ \phi_{33} = 1,$$

$$g_{11} = V_{DC}\omega_{F0}\sin(\omega_{F0}T_s/2)\exp(-\xi_F\omega_{F0}T_s/2),$$

$$g_{21} = \frac{V_{DC}}{L_F}[\cos(\omega_{F0}T_s/2) - \xi_F\sin(\omega_{F0}T_s/2)]\exp(-\xi_F\omega_{F0}T_s/2),$$

$$g_{31} = 0.$$

The control transfer function and the output impedance of VSI can be expressed as (29)

$$V_{OUT}(z) = z^{-1}\frac{g_{11}+(\varphi_{12}g_{21}-\varphi_{22}g_{11})z^{-1}}{1-z(\varphi_{11}+\varphi_{22})z^{-1}+(\varphi_{11}\varphi_{22}-\varphi_{12}\varphi_{21})z^{-2}}T_{ON}(z)+ z^{-1}\frac{\varphi_{13}+(\varphi_{12}\varphi_{23}-\varphi_{13}\varphi_{22})z^{-1}}{1-z(\varphi_{11}+\varphi_{22})z^{-1}+(\varphi_{11}\varphi_{22}-\varphi_{12}\varphi_{21})z^{-2}}I_O(z) \quad (29)$$

The delay with one T_s that exists in (29) is the feature of the double-edged modulation. The time between two consecutive pulses depends on the previous switching period control. For single-edged modulation, this delay is absent [32].

The gain of the VSI, with double-edged PWM and a digital modulator inserting a switching period delay T_s, is given by (30), (31):

$$K_{CTRL} = \frac{V_{OUT}(z)}{V_{CRTL}(z)} = z^{-1}K_{INV} = z^{-1}\frac{a_1z^{-1}+a_2z^{-2}}{1+b_1z^{-1}+b_2z^{-2}}, \quad (30)$$

where

$$a_1 = \frac{T_s}{V_{DC}}g_{11};\ a_2 = \frac{T_s}{V_{DC}}(\varphi_{12}g_{21}-\varphi_{22}g_{11})\ ;\ b_1 = -(\varphi_{11}+\varphi_{22});\ b_2 = \varphi_{11}\varphi_{22}-\varphi_{12}\varphi_{21}. \quad (31)$$

For high switching frequencies (e.g., 51,200 kHz), the difference between the discretized control transfer function and the discrete transfer function is low.

7. Measuring Bode Plots of the Inverter and Measuring Traces

To design the control of the VSI, its parameters should be known to define the VSI model. Additionally, Bode plots of the measuring traces should be appointed. The inverter bridge with the output filter can have parameters different from the nominal [11–13]. The parameter values depend mainly on the coil core material in the filter. For an iron powder core, the inductance L_F seriously changes; for the Super MSS, it is almost constant. The power losses in the core cause an increase in the equivalent serial resistance R_{LFe}. Inductance L_F and the equivalent serial resistance R_{LFe} should be measured in the chosen VSI operating point. The fundamental frequency f_m = 50 Hz was set to be constant. Three switching frequencies were checked in the experimental VSI: f_s = 12,800 Hz, 25,600 Hz or 51,200 Hz (the frequency of the voltage pulses on the coil in the presented PWM scheme is double $2f_s$, Figure 3). The DC supply voltage V_{DC}, the load resistance R_{LOAD} and the switching frequency f_s were assigned for the selected operating point. The generated test signal V_{CTRL} (Figure 4) was the sum of the fundamental harmonic and the excitation signal, that is, the n-th harmonic of the fundamental harmonic (32) [11–13].

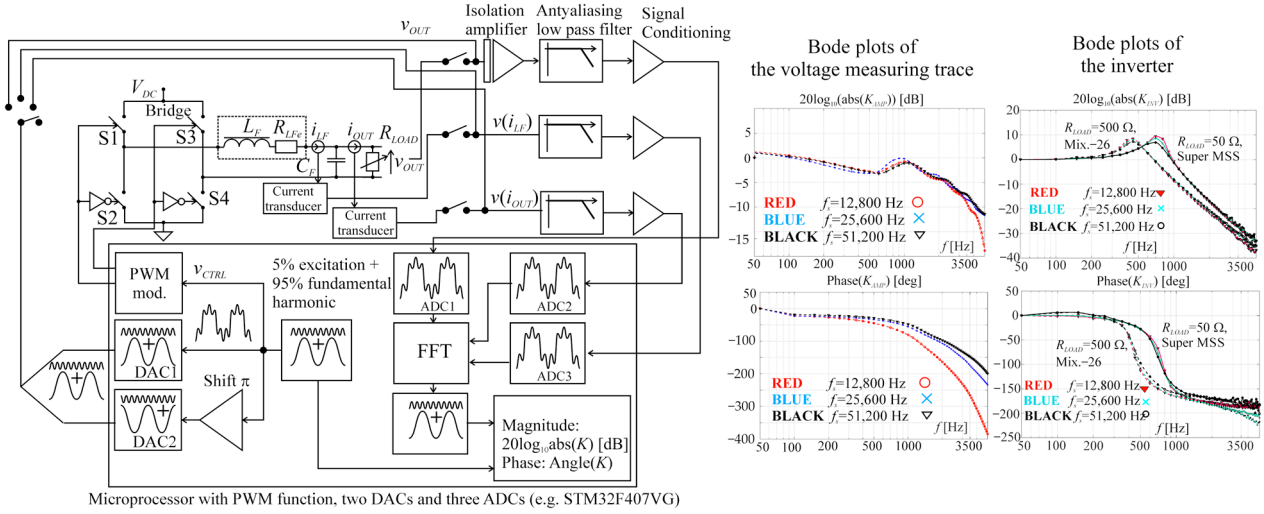


Figure 4. Measurement of the Bode plots of the inverter and the measuring voltage trace.

For $k = 1$ to f_s/f_m

$$V_{CTRL}(k) = round(M \cdot floor\left(\frac{1}{2}\frac{f_{COMP}}{f_s}\right)(A\sin(k\frac{2\pi}{f_s/f_m}) + (1-A)\sin(nk\frac{2\pi}{f_s/f_m}))) \quad (32)$$

where M is the modulation depth (typically $M = 0.9$, to avoid distortions of the fundamental harmonic), f_{COMP} is the input frequency of the PWM unit comparator (in STM32F407VG microprocessor $f_{COMP} = 84$ MHz), A is the relative amplitude of the fundamental harmonic ($A = 0.9$–0.95) and $k = 1\ldots(f_s/f_m)$. The switching frequency f_s is always a harmonic of the fundamental frequency $f_m = 50$ Hz. The reference waveform is represented by $f_s/50$ samples of the sinusoidal reference per the fundamental period $T_m = 20$ ms. The number of samples of the n-th harmonic—the excitation—is equal to $f_s/(n50)$ in one fundamental period. For the minimum number of ten samples per period of the generated harmonics, in the case of $f_s = 12{,}800$ Hz: $n_{max} = 25$, $f_s = 25{,}600$ Hz: $n_{max} = 50$ and $f_s = 51{,}200$ Hz: $n_{max} = 100$. Finally, $n_{max} = 100$ was used for $f_s = 12{,}800$, 25,600 and 51,200 Hz because it has a high attenuation over the 25th harmonics (for $L_F = 1$ mH, $C_F = 51$ µF, the output filter resonant frequency was 705 Hz, below the 25th harmonic) and the error in the measurement of the harmonics close to the 100th harmonic is not practically important. The MKP-type VSI output capacitor $C_F = 51$ µF was the same as in the experimental inverter. The accuracy of appointing the maximum gain is better for the lower-frequency step grid [13]. For lower damping, the frequency step grid should possibly be lower; for high damping, finding the maximum on the Bode plot will be always inaccurate. For the calculation of the L_F and R_{LFe} parameters, the maximum value of the damping coefficient should be ${\xi_F}^2 < (1 + R_{LFe}/R_{LOAD})/2$ for $R_{LOAD} >> R_{LFe}$. The amplitude of the measured fundamental harmonic should be initially adjusted to 50–75% of the ADC range (the used 13-bit bipolar analogue-to-digital converter ADC has a range of −4095 to 4095; the required amplitude of the fundamental harmonic should be 2000–3000 units). The complex test signal v_{CTRL} (35) is generated in the DAC/ADC units from $-floor(0.5f_{COMP}/f_s)$ to $floor(0.5f_{COMP}/f_s)$. It should be checked that for a complex test signal with an excitation component frequency near the VSI filter resonant frequency, the measured value is inside the range of ADC. The amplitude of excitation $|h_{nIN}| = 1 - A$ should have a value of 5 to 10%. It was shown [41] that the lowest comparator frequency is $f_{COMP} = 68$ MHz for $f_s = 25{,}600$ Hz and the double-edged PWM modulation, for which there were no additional distortions caused by the insufficient resolution of the generated waveform (in STM32F407VG, there is $f_{COMP} = 84$ MHz). The main assumption is that the fundamental harmonic is not attenuated in the inverter and it is delayed as all the components of the test signal (the T_s delay in the PWM modulator is not present in the relative calculations because it concerns the whole signal).

The values of the input and output excitations are compared, respectively, with the fundamental harmonic in the input and output. Such a solution solves the problem of the different units in the VSI output (volts) and PWM modulator input test signal (in ADC units). The amplitudes and phases of the excitation harmonic components (33) of the input and output complex signals are calculated using the *fft* transform [14].

For $n = 1\ldots n_{max}$

$$K_{INV}(j2\pi f_n) = \\ = \frac{|V_{OUT}(nf_m)|/|V_{OUT}(f_m)|}{|V_{CTRL}(nf_n)|/|V_{CTRL}(f_m)|}\exp(j\{[\arg(V_{OUT}(nf_m)) - \arg(V_{OUT}(f_m))] - [\arg(V_{CTRL}(nf_m)) - \arg(V_{CTRL}(f_m))]\}) \quad (33)$$

The magnitude Bode plot is (34)

$$|K_{INV}(nf_n)| = 20\log\frac{|V_{OUT}(nf_m)|/|V_{OUT}(f_m)|}{|V_{CTRL}(nf_n)|/|V_{CTRL}(f_m)|} \quad (34)$$

The phase Bode plot is (35)

$$\arg(nf_m) = [\arg(V_{OUT}(nf_m)) - \arg(V_{OUT}(f_m))] - [\arg(V_{CTRL}(nf_m)) - \arg(V_{CTRL}(f_m))] \quad (35)$$

The switching frequency f_s and the load R_{LOAD} are parameters which should be kept constant during one measurement series. The measured row data series—magnitudes and phases of the inverter together with the measurement trace—are sent to PC where the previously measured magnitudes (dB) and phases (degrees) of the measurement trace are subtracted from the corresponding row data. From the magnitude Bode plot, the damping coefficient ζ_F (36), the inductance L_F (37) and the serial equivalent resistance R_{LFe} (38) can be calculated [14] for the assumption $R_{LOAD} >> R_{LFe}$.

$$\xi_F \approx \sqrt{\frac{1}{2}[1 - \sqrt{(1 - \frac{1}{|K_{INV}|_{\max}{}^2})}]} \tag{36}$$

$$L_F = \frac{1 - 2\xi_F{}^2}{\omega_{\max}{}^2 C_F}, \text{ for } \xi_F{}^2 < 0.5 \tag{37}$$

$$R_{LFe} = (2\xi_F \frac{\omega_{\max}{}^2}{\sqrt{1 - 2\xi_F{}^2}} - \frac{1}{R_{LOAD} C_F}) \frac{1 - 2\xi_F{}^2}{\omega_{\max}{}^2 C_F} \text{ for } R_{LOAD} > \frac{\sqrt{1 - 2\xi_F{}^2}}{2\xi_F \omega_{\max} C_F} \text{ and } \xi_F{}^2 < 0.5 \tag{38}$$

The error (41) in the calculation of the damping coefficient ξ_F was caused by the $\Delta\omega_{max}$ error of appointing ω_{max} (39), (40).

$$\omega_{\max}{}^2 = (1 - 2\xi_F{}^2)\omega_{F0}{}^2 \tag{39}$$

$$\Delta\xi_F = \frac{\partial \xi_F}{\partial \omega_{\max}} \Delta\omega_{\max} = -\frac{1}{\sqrt{2\omega_{F0}{}^2}} \frac{\omega_{\max}}{\sqrt{\omega_{F0}{}^2 - \omega_{\max}{}^2}} \Delta\omega_{\max} \tag{40}$$

$$\Delta\xi_F = -\frac{1}{2} \frac{1 - 2\xi_F{}^2}{\xi_F} \frac{\Delta\omega_{\max}}{\omega_{\max}} \tag{41}$$

The measured serial equivalent inductance error is low, and approximately can be assigned $\Delta L_F \approx 0$ (43) because the component errors cancel each other out (42).

$$\Delta L_F = \frac{\partial L_F}{\partial \xi_{Fe}} \Delta\xi_F + \frac{\partial L_F}{\partial \omega_{\max}} \Delta\omega_{\max} = -4 \frac{\xi_F}{\omega_{\max}{}^2 C_F} \Delta\xi_F - 2 \frac{1 - 2\xi_F{}^2}{\omega_{\max}{}^3 C_F} \Delta\omega_{\max} \tag{42}$$

$$\Delta L_F \approx 0 \tag{43}$$

The error of the serial equivalent resistance R_{LFe} (45) depends on the damping coefficient ξ_F and $\Delta\omega_{max}$ that is equal to 0.5 frequency grid.

$$\Delta R_{LFe} = \frac{\partial R_{LFe}}{\partial \xi_F} \Delta\xi_F + \frac{\partial R_{Fe}}{\partial L_F} \Delta L_F \approx 2\sqrt{\frac{L_F}{C_F}} \Delta\xi_F \tag{44}$$

$$|\Delta R_{LFe}| = \sqrt{\frac{L_F}{C_F}} \frac{1 - 2\xi_F{}^2}{\xi_F} \frac{\Delta\omega_{\max}}{\omega_{\max}} \tag{45}$$

Figure 5 presents the error of R_{LFe} as a function of the damping coefficient ξ_F and frequency resolution Δf_{max}. This error ΔR_{LFe} (for L_F = 1 mH, C_F = 51 µF) is serious, up to 1.5 Ω, for the low damping coefficient, which is the case of a low resolution for Δf_{max} = 50 Hz (frequency step grid 100 Hz). The full real value of R_{LFe} is 1 to 2 Ω for the 1 mH coil DC resistance of about 0.2 Ω, the MOSFET bridge transistors with R_{DS} = 0.2 Ω (there are always two serially connected transistors conducting), and the coil core made of Sendust magnetic material [9] with a low power loss. So, ΔR_{LFe} = 1.5 Ω is unacceptable and the frequency step grid should be decreased.

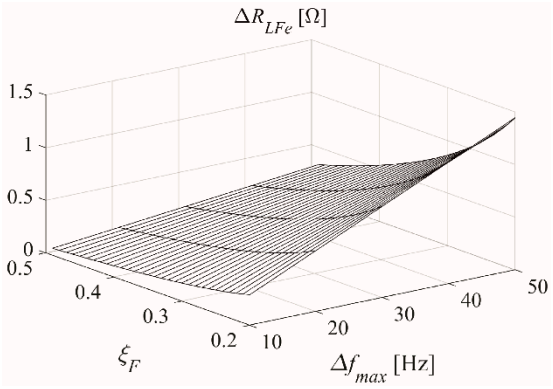


Figure 5. The error ΔR_{LFe} of measurement of the serial equivalent resistance R_{LFe} as a function of damping coefficient ξ_F and frequency resolution Δf_{max} (for L_F = 1 mH, C_F = 51 µF).

Figure 6 presents the Bode plots of two experimental inverters. It can be noticed that in both cases, these frequency domain characteristics can be approximated in the frequency range up to the corner frequency of the output filter (for L_F = 1 mH, C_F = 51 µF, it is 705 Hz) as the simple delay with two switching periods T_s. This approximation (46) of the measuring trace transfer function for f < 1000 Hz will be used in the simulations.

$$K_{TRACE}(s) \approx e^{-s2T_s} \text{ for} \omega \; < \; 2\pi 1000 \; [1/\text{s}] \tag{46}$$

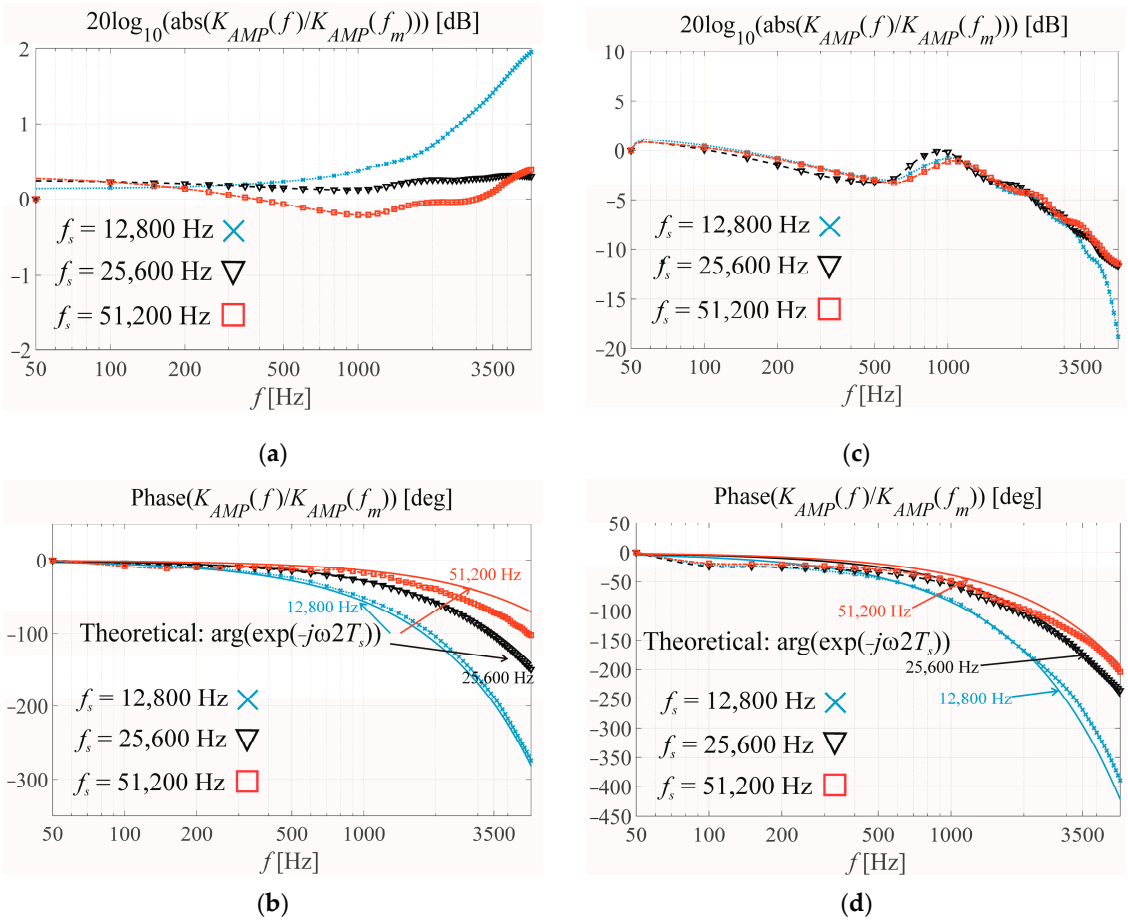


Figure 6. Two exemplary Bode plots: (**a**,**c**) magnitude, and (**b**,**d**) phase of two experimental inverters, (**a**,**b**) the first and (**c**,**d**) the second one.

8. The Prediction of the State Variables

It was shown that the transfer function of the measurement trace and the PWM modulator can be approximated with a simple delay ($2T_s$ is the measuring trace and T_s is the PWM modulator). For the high switching frequency (51,200 Hz and more) this delay is not so important for the design of the control loop [42]. For the lower switching frequency, one of the solutions can be the prediction of the state variable at the next sampling instant [43]. The full-order state Luenberger observer [18,19] will be used. It is quite convenient because we do not need to know exactly the transfer function of the measurement traces.

The discrete state space equations for state variables $\mathbf{x} = [v_{OUT}\ i_{LF}\ i_{OUT}]^T$ and output variable $y(k) = v_{OUT}(k)$ were described in (26), (27). The predicted state variables at the next sampling instant are (47).

$$\hat{\mathbf{x}}(k+1) = \mathbf{A}_\mathrm{D}\hat{x}(k) + \mathbf{G}_\mathrm{D}T_{ON}(k) + \mathbf{L}[\mathbf{y}(k) - \mathbf{C}_\mathrm{D}\hat{\mathbf{x}}(k)] \tag{47}$$

L is discretized observer gain matrix.

The error system is obtained from (48):

$$\mathbf{e}(k+1) = (\mathbf{A}_\mathrm{D} - \mathbf{L}\mathbf{C}_\mathrm{D})[\mathbf{x}(k) - \hat{\mathbf{x}}(k)] = (\mathbf{A}_\mathrm{D} - \mathbf{L}\mathbf{C}_\mathrm{D})\mathbf{e}(k), \tag{48}$$

For three state variables:

$$\mathbf{L} = [l_1 \quad l_2 \quad l_3]^T$$

The characteristic equation of the observer is (49).

$$\det(z\mathbf{1} - \mathbf{A}_\mathrm{D} + \mathbf{L}\mathbf{C}_\mathrm{D}) = 0 \tag{49}$$

According to the principle of separation of estimation and pole placement of the "separation theorem", the roots of the characteristic equation of the observer (49) are independent of the closed-feedback-loop control system. However, the observer eigenvalues should enable a faster convergence to zero of the observation error than that of other transient processes in a closed-loop system. Better observer dynamics are obtained if the roots of their characteristic Equation (49) are closer to zero on the z-plane (their absolute value is lower) than the roots of the characteristic equation without estimation $\det(z\mathbf{1} - \mathbf{A}_\mathrm{D}) = 0$. E.g., in [44], the observer poles are selected to be about 0.8 times closer to the origin than the open-loop poles at the same phase angle. In [45], the Luenberger observer was designed with its dynamics three times faster than the fastest pole of the plant.

The characteristic equation of the open-loop system with the estimation is (50), (51).

$$\det\begin{bmatrix} z - \varphi_{11} + l_1 & -\varphi_{12} & -\varphi_{13} \\ -\varphi_{21} + l_2 & z - \varphi_{22} & -\varphi_{23} \\ 0 + l_3 & 0 & z - 1 \end{bmatrix} = 0 \tag{50}$$

$$\begin{aligned} &1 + z^{-1}[-1 - \varphi_{11} - \varphi_{22} + l_1] + z^{-2}[\varphi_{22} + \varphi_{11} + \varphi_{11}\varphi_{22} - \varphi_{12}\varphi_{21} - (1 + \varphi_{22})l_1 + \varphi_{12}l_2 + \varphi_{13}l_3] \\ &z^{-3}[-\varphi_{11}\varphi_{22} + \varphi_{12}\varphi_{21} + l_1\varphi_{22} - \varphi_{12}l_2 + (\varphi_{12}\varphi_{23} - \varphi_{13}\varphi_{22})l_3] = 0 \end{aligned} \tag{51}$$

Manabe presented the coefficient diagram method (CDM) [29–31] to design a controller where coefficients of the closed-loop characteristic equation are calculated from the Manabe standard form. They depend on the time constant τ of the closed-loop system. Relation (52) is the discretized characteristic equation of the closed-loop system.

$$P(z^{-1}) = \sum_{i=0}^{n} p_{zi}(\tau/T_s)z^{-i} \tag{52}$$

The experimental work [20] showed that for the values of L_F = 1 mH, C_F = 51 µF, and a switching frequency of f_s = 12,800 to 51,200 Hz, the best results of control were for τ/T_s = 5 to 8. So, let us assign $p_{zi}(\tau/T_s)$ for the lower τ/T_s for the characteristic equation of the

observer, which fills the requirement that the observer should be faster than the closed-loop system (the further adjustment—individual decreasing gains from $\tau/T_s = 1$, leads to gains of observer τ/T_s equal to about 7 to avoid system oscillations). Equation (53) should be solved to obtain the gains l_i of the observer for the assigned τ/T_s.

$$\begin{bmatrix} 1 & 0 & 0 \\ -1-\varphi_{22} & \varphi_{12} & \varphi_{13} \\ \varphi_{22} & -\varphi_{12} & \varphi_{12}\varphi_{23}-\varphi_{13}\varphi_{22} \end{bmatrix} \begin{bmatrix} l_1 \\ l_2 \\ l_3 \end{bmatrix} = \begin{bmatrix} p_{z1}+1+\varphi_{11}+\varphi_{22} \\ p_{z2}-\varphi_{22}-\varphi_{11}-\varphi_{11}\varphi_{22}+\varphi_{12}\varphi_{21} \\ p_{z3}+\varphi_{11}\varphi_{22}-\varphi_{12}\varphi_{21} \end{bmatrix} \quad (53)$$

Table 1 presents the gains of the observer in the absolute values of the roots of its characteristic equation for the low switching frequency f_s = 12,800 Hz and relative time constants τ/T_s from 1 to 6. The roots of the characteristic equation of the observer for the lower τ/T_s are closer to zero for the z-plane in Manabe CDM. This research concerns the comparison of operating at a low switching frequency f_s = 12,800 Hz and operating at a high switching frequency f_s = 51,200 Hz, because of the higher values of the switching frequency when the prediction is not necessary (the delay in the inverter system is low).

Table 1. The gains of the observer and absolute values of the roots of its characteristic equation for the switching frequency f_s = 12,800 Hz and relative time constants τ/T_s from 1 to 7 for L_F = 1 mH, C_F = 51 µF, R_{LFe} = 1 Ω.

$\tau/T_s, f_s$	p_{z0}	p_{z1}	p_{z2}	p_{z3}	l_1	l_2	l_3	Abs (Root1)	Abs (Root2)	Abs (Root3)
1, 12.8 k	1	0.043	0.015	−0.007	2.852	−7.780	−9.215	0.211	0.211	0.152
2, 12.8 k	1	−0.866	0.396	−0.082	1.943	−3.194	−3.930	0.459	0.459	0.389
3, 12.8 k	1	−1.456	0.846	−0.189	1.353	−1.392	−1.764	0.595	0.595	0.5332
4, 12.8 k	1	−1.805	1.196	−0.287	1.004	−0.719	−0.917	0.678	0.678	0.624
5, 12.8 k	1	−2.029	1.458	−0.368	0.780	−0.427	−0.531	0.732	0.732	0.686
6, 12.8 k	1	−2.184	1.657	−0.435	0.626	−0.284	−0.335	0.772	0.772	0.730
7, 12.8 k	1	−2.297	1.812	−0.490	0.513	−0.207	−0.223	0.801	0.801	0.764

In [10,20,42,46] the passivity-based control for the voltage source inverters was presented. When the supplied energy in a system exceeds the stored energy, the system is passive. The passive system is stable—this is the idea of PBC. The energy in an inverter is stored in the components of the output filter—the filter coil and the filter capacitor–and can be described by the Hamiltonian function (54) $H(x)$ (sometimes $H(x)$ is called a Lyapunov function [47]).

$$H(x) = \frac{1}{2}(L_F {i_{LF}}^2 + C_F {v_{OUT}}^2) \quad (54)$$

The discrete control law of PBC for the predicted values of state variables is (55), (56), from [42].

$$\hat{v}_{CTRL}(k+1) = -R_i \hat{i}_{LF}(k+1) + (R_i + R_{LF})\hat{i}_{LFref}(k+1) + L_F \frac{\hat{i}_{LFref}(k+1) - \hat{i}_{LFref}(k)}{T_c} + v_{OUTref}(k+1) \quad (55)$$

$$\hat{i}_{LFref}(k+1) = K_v[v_{OUTref}(k+1) - \hat{v}_{OUT}(k+1)] + C_F \frac{v_{OUTref}(k+1) - v_{OUTref}(k)}{T_c} + \hat{i}_{OUT}(k+1) \quad (56)$$

where:

$$\hat{v}_{OUT}(k+1) = \varphi_{11} v_{OUT}(k) + \varphi_{12} i_{LF}(k) + \varphi_{13} i_{OUT}(k) + g_{11} \frac{\hat{v}_{CTRL}(k)}{V_{DC}} T_s + l_1[v_{OUT}(k) - \hat{v}_{OUT}(k)] \quad (57)$$

$$\hat{i}_{LF}(k+1) = \varphi_{21} v_{OUT}(k) + \varphi_{22} i_{LF}(k) + \varphi_{23} i_{OUT}(k) + g_{12} \frac{\hat{v}_{CTRL}(k)}{V_{DC}} T_s + l_2[v_{OUT}(k) - \hat{v}_{OUT}(k)] \quad (58)$$

$$\hat{i}_{OUT}(k+1) = i_{OUT}(k) + l_3[v_{OUT}(k) - \hat{v}_{OUT}(k)] \quad (59)$$

The state–space Equations (57)–(59) are different from (47) because predicted space variables are not directly used in the equations. Using the predicted variables (47) is the typical approach [48]. But our $\mathbf{C_D}$ = [1 0 0], and the output variable is dependent only on the output voltage. So, the measured values of the variables were used directly in (57)–(59) because there was no other way of implementing them in the prediction procedure.

The important problem in PBC is the choice of the current gain R_i and the voltage gain K_v. It was shown in [14,26,47] that the bottom limits of gains are $R_{LFe} + R_i > 0$ and $K_v > 0$. The upper limits of R_i and K_v gains are a result of the limitation of the control voltage v_{CTRL} possible speed. The higher values of the gains cause saturation of the PWM modulator but do not always cause oscillations. Sometimes, slightly increasing the gains over these limits can decrease the distortions of the output voltage for the nonlinear load. But it should be remembered that during saturation, the feedback loop does not work. The derivative of the control voltage in one switching cycle should be lower than the maximum increase in the output PWM signal that is equal to V_{DC}/T_s.

We can assume that $\mathrm{d}(v_{OUTref})/\mathrm{d}t \approx 0$ in one sampling period. The control law without prediction is (60) and (61):

$$v_{CTRL}(kT_s) = -R_i i_{LF}(kT_s) + (R_i + R_{LFe}) i_{LFref}(kT_s) + L_F \frac{di_{LFref}(kT_s)}{dt} + v_{OUTref}(kT_s) \quad (60)$$

$$i_{LFref}(kT_s) = K_v[v_{OUTref}(kT_s) - v_{OUT}(kT_s)] + C_F \frac{dv_{OUTref}(kT_s)}{dt} + i_{OUT}(kT_s) \quad (61)$$

From (61) for the resistive load R_{LOAD}:

$$i_{LFref}(kT_s) \approx K_v v_{OUTref}(kT_s) + (\frac{1}{R_{LOAD}} - K_v) v_{OUT}(kT_s) \quad (62)$$

Let us assume the operation with the load $R_{LOAD} = \infty$.

$$\frac{di_{LFref}(kT_s)}{dt} \approx -K_v \frac{dv_{OUT}(kT_s)}{dt} \quad (63)$$

The absolute value of the derivative of v_{CTRL} for the load $R_{LOAD} = \infty$ is (64).

$$\left|\frac{dv_{CTRL}(kT_s)}{dt}\right| \approx K_v L_F \frac{d^2 v_{OUT}(kT_s)}{dt^2} + K_v(R_i + R_{LFe}) \frac{dv_{OUT}(kT_s)}{dt} + R_i \frac{di_{LF}(kT_s)}{dt} \quad (64)$$

In one switching cycle

$$\frac{di_{LF}(kT_s)}{dt}\bigg|_{\max,\min} \approx \pm\frac{V_{DC}}{L_F}, \quad \frac{dv_{OUT}(kT_s)}{dt}\bigg|_{\max} \approx \frac{i_{LF}}{C_F}, \quad \frac{d^2 v_{OUT}(kT_s)}{dt^2}\bigg|_{\max} \approx \frac{d}{dt}(\frac{i_{LF}}{C_F})\bigg|_{\max} \approx \pm\frac{V_{DC}}{L_F C_F} \quad (65)$$

Finally, the absolute value of the derivative of v_{CTRL} for the load $R_{LOAD} = \infty$ is (66).

$$\left|\frac{dv_{CTRL}(kT_s)}{dt}\right|_{\max} \approx K_v[L_F + (R_i + R_{LFe})T_s]\frac{V_{DC}}{L_F C_F} + R_i \frac{V_{DC}}{L_F} \quad (66)$$

The upper limits of R_i and K_v gains are (67).

$$K_v[L_F + (R_i + R_{LFe})T_s]\frac{1}{L_F C_F} + \frac{R_i}{L_F} < f_s \quad (67)$$

Figure 7a,b presents the graphic visualisation of Equation (67), adequately for f_s = 12,800 and 51,200 Hz, while omitting the delays. When the left side of this equation is lower than the switching frequency, the gains are in the allowable range. The curves of equality of the left side of Equation (67) and the switching frequency—the border values of gains—are presented in Figure 7c for f_s = 12,800 and 51,200 Hz. Taking values of the R_i and K_v gains from these curves below them, we can be sure that there will be no oscillations

in the output voltage. However, it is possible to check experimentally higher values of the gains to decrease the error of the control. The presented values of gains are valid for Simulink simulation because we do not need to scale the voltage and currents. We only divide all the measured variables by the V_{DC} that is on the input of the inverter because the input of the modulator is inside $+1/-1$. The other problem is the modulation index. The lower this index, the higher the dynamics of the modulator. However, in real inverters, the modulation index should be close to unity. Equation (67) does not consider the modulation index M value because the maximum carrier-slope increase does not depend on M. Equation (67) is calculated for $R_{LOAD} = \infty$, the worst case being that the restrictions of the K_v value for the existing load resistance will be slightly lower. The higher value of the gains, the lower the output voltage error and the lower the THD coefficient. That is why it is possible to obtain much lower THD for higher switching frequencies.

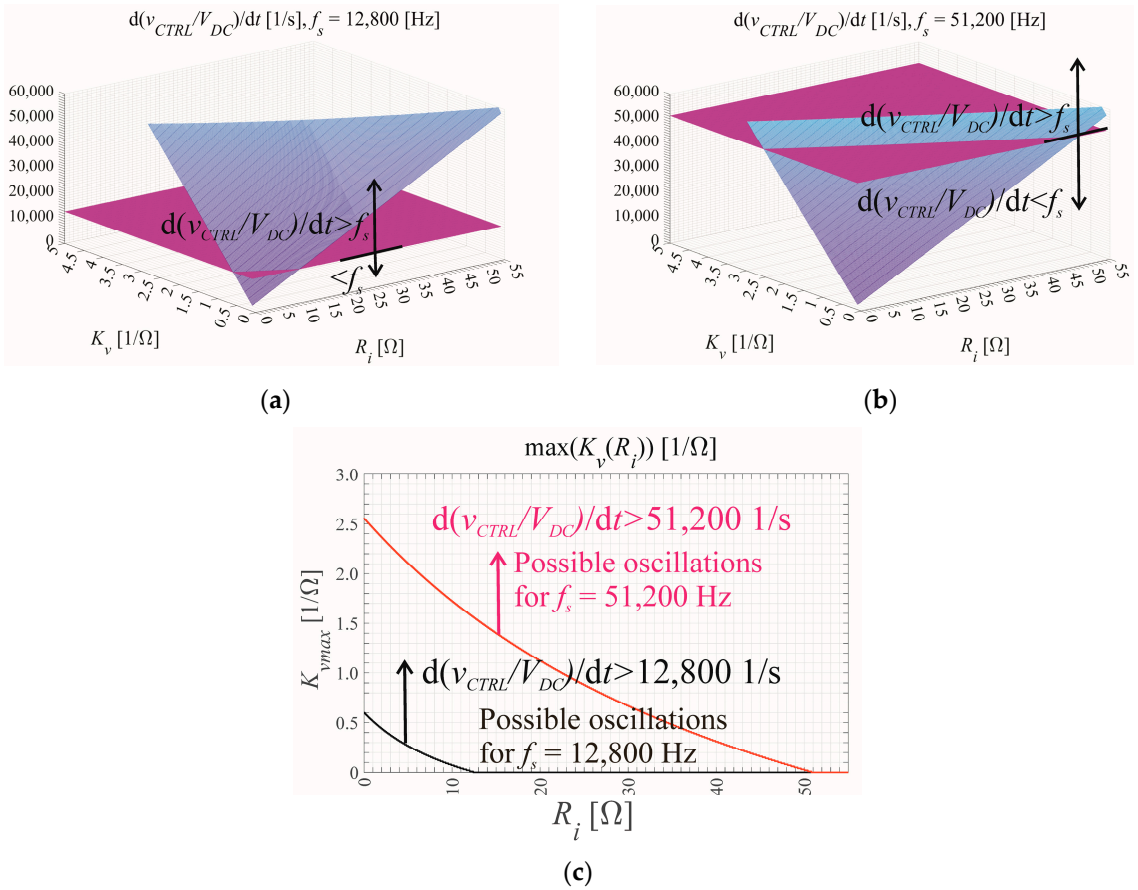


Figure 7. The limits of the voltage and current gains for two switching frequencies f_s = 12,800 (**a**) and f_s = 51,200 Hz (**b**) for L_F = 1 mH, R_{LFe} = 1 Ω, C_F = 51 µF and gain border lines for two switching frequencies (**c**).

9. Simulation of the Inverter with the Delay in the Measurement Traces

Figure 8 presents the output voltage waveform of the open-loop inverter with the nonlinear rectifier load R = 100 Ω and C = 430 µF.

Figure 9a presents the simulation model without the delays in the measuring traces for the low switching frequency f_s = 12,800 Hz. Figure 9b,c presents the output voltage, output current and the control voltage waveforms for L_F = 1 mH, R_{LFe} = 1 Ω, C_F = 51 µF, f_s = 12,800 Hz, the nonlinear rectifier load R = 100 Ω and C = 430 µF, the modulation index M = 0.7, and the PBC control (60) and (61) without prediction. In Figure 9b, K_v = 0.3, and R_i = 4 from the border line from Figure 7b (THD = 2.69%). However, it is possible to increase the gains K_v = 0.5, R_i = 25 (Figure 9c) whilst accepting some oscillations of the control voltage, in order to decrease distortions (THD = 1.04%). In the simulated measure-

ment traces (Figure 8a) there are only ZOH modules simulating the analogue-to-digital converters (ADCs).

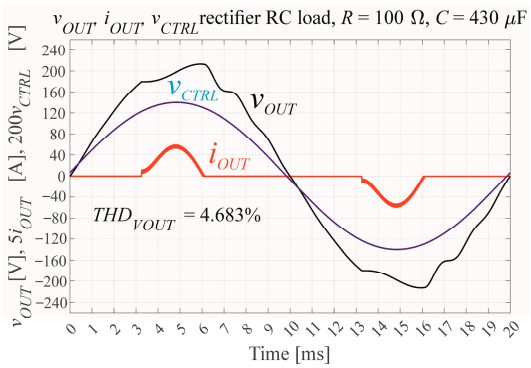
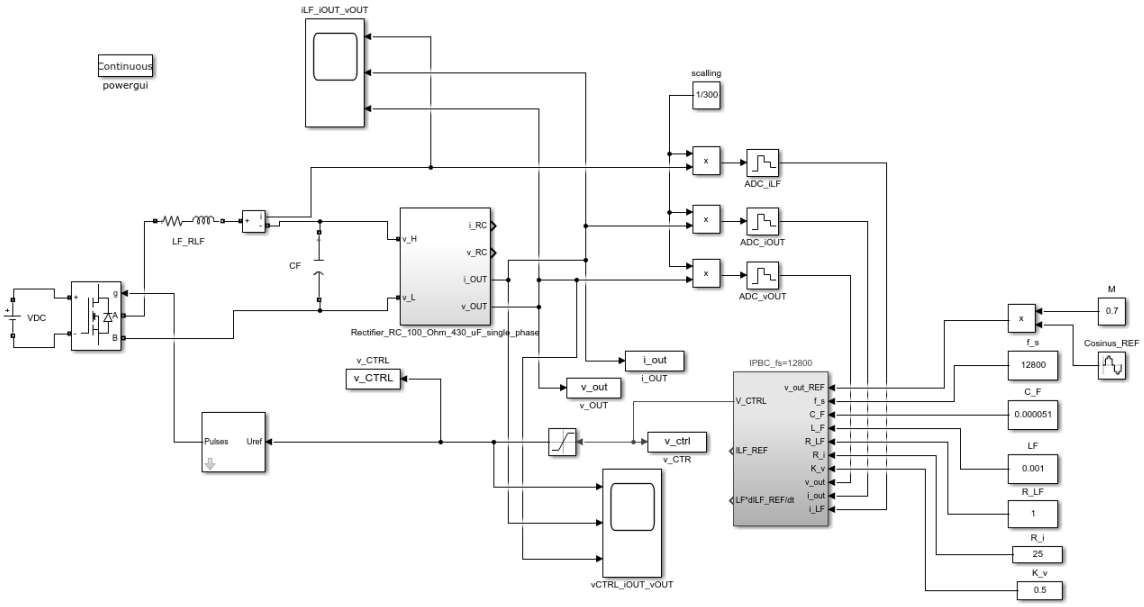
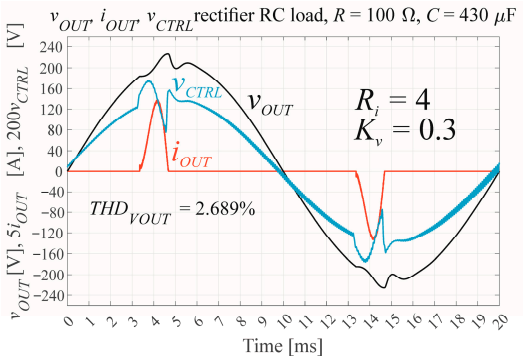


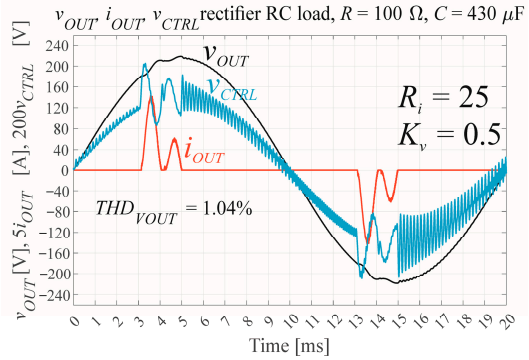
Figure 8. The inverter output voltage, output current waveforms for the open loop and the nonlinear rectifier load R = 100 Ω and C = 430 μF.



(**a**)



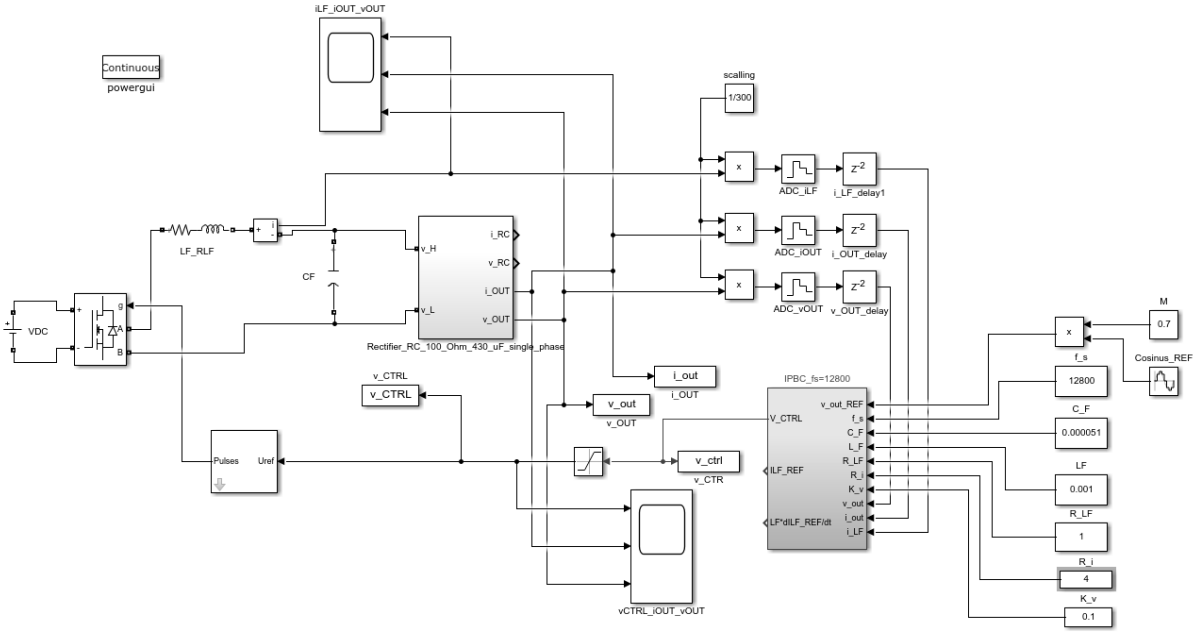
(**b**)



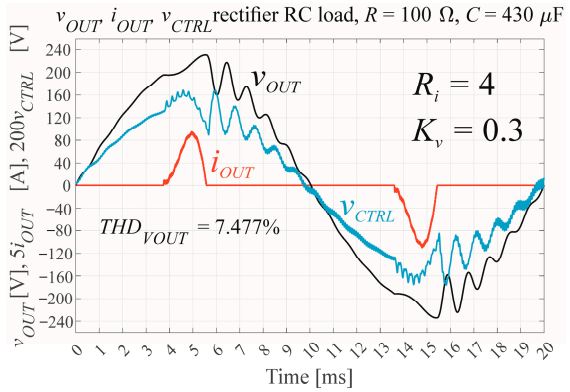
(**c**)

Figure 9. (**a**) The inverter model without delays in the measuring traces; (**b**) the output voltage waveform for the boundary PBC gains; and (**c**) the output voltage waveform for the increased PBC gains adjusted to obtain the minimum distortions (for the acceptable small control-voltage oscillations).

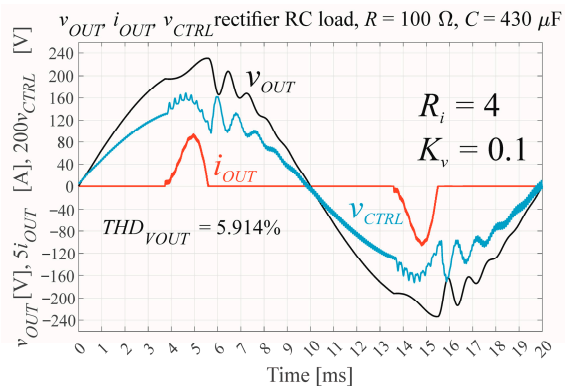
In Figure 10a, the $2T_s$ delays in each of the measuring traces were added to make the simulation model more similar to the experimental model (Figure 6c,d) for f_s = 12,800 Hz. The gains K_v and R_i of PBC were reduced from the border values K_v = 0.3 and R_i = 4 (Figure 10b) to 0.1 and 4 (Figure 10c) to decrease the output voltage oscillations. The controller architecture was the same as in Figure 9a. The controller works wrongly because the output voltage distortions are higher than in the open-loop inverter (Figure 8), which is ridiculous.



(**a**)



(**b**)



(**c**)

Figure 10. (**a**) The inverter model with $2T_s$ delays in the measuring traces with the PBC controller without the prediction; (**b**) the output voltage waveform for the boundary PBC gains; and (**c**) the output voltage waveform for the decreased PBC gains adjusted to obtain the minimum distortions for f_s = 12,800 Hz.

As shown in Figure 11a, the inputs of the PBC controller (55), (56) were predicted (57)–(59). The gains of the observer l_1, l_2, l_3 were initially calculated for τ/T_s = 1 (Table 1) and then reduced to 0.285, −0.778 and −0.092 (the highest values for which there were no oscillations of the output voltage for the particular gains) and the gains K_v and R_i were adjusted to 0.1 and 4. In all the cases, the coefficient of the control quality was the THD of the output voltage.

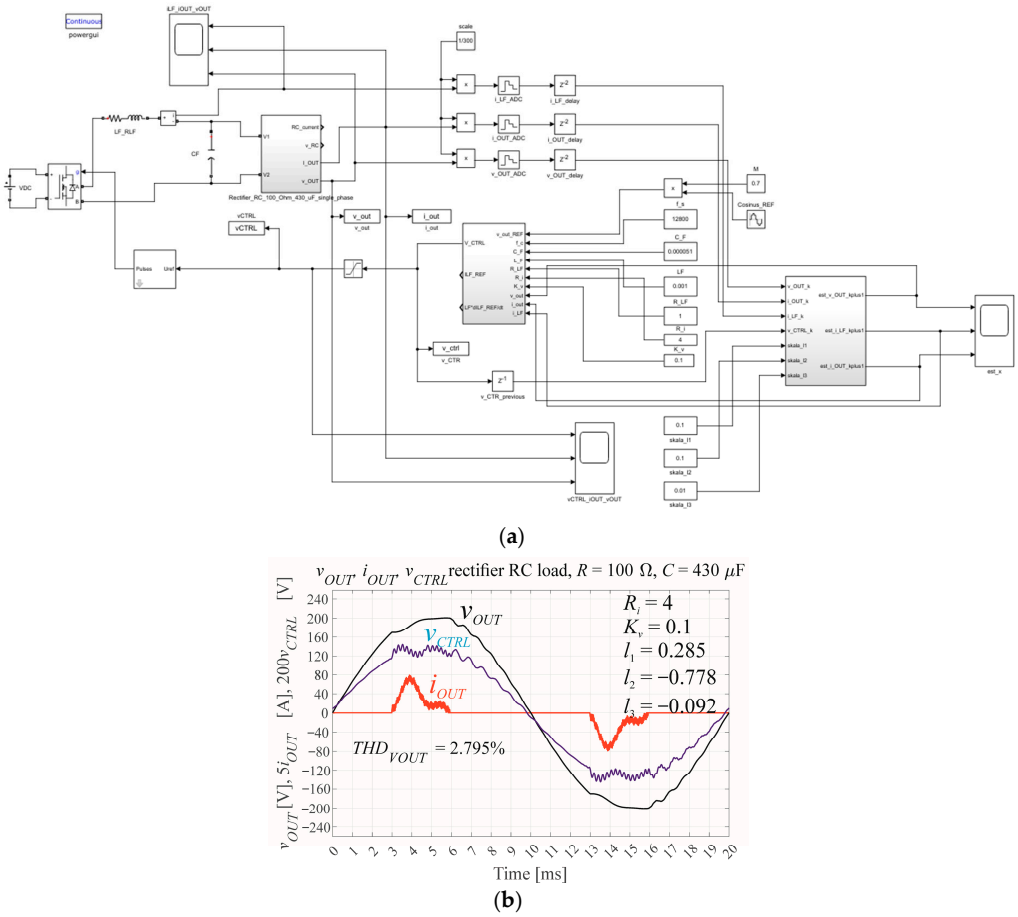


Figure 11. (**a**) The inverter model with $2T_s$ delays in the measuring traces and PBC with the Luenberger observer; and (**b**) the output voltage waveform for the PBC and observer gains adjusted to obtain the minimum distortions for f_s = 12,800 Hz.

To show the influence of delays in the measurement traces (depending on the switching frequency) for the higher switching frequency (51,200 Hz), Figure 12 presents the results of the simulation of the inverter with delays of $2T_s$ in the measuring traces and the PBC controller, without prediction, for f_s = 51,200 Hz. It can be seen that the THD is very low (0.87%), and there is no need to use the observer. Let us compare the shape of the output current waveforms from Figures 11b and 12. The current in Figure 12 is forced to increase immediately even if there are $2T_s$ delays, owing to possible higher controller gains. Table 2 presents the results (THD) of the control in simulations.

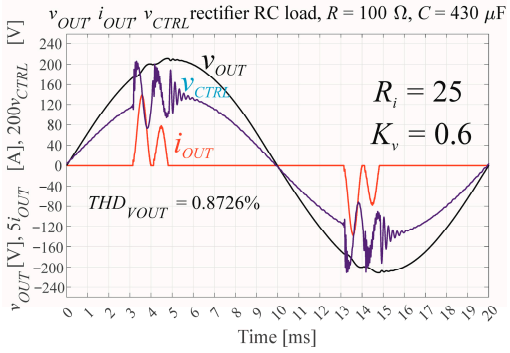


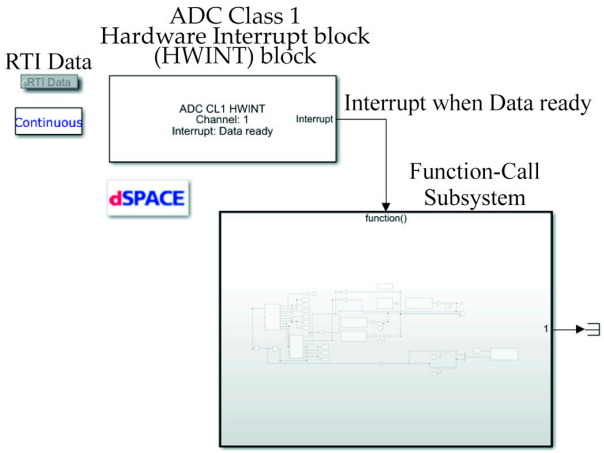
Figure 12. The output voltage waveform for the PBC (without the prediction) gains adjusted to obtain the minimum distortions for f_s = 51,200 Hz.

Table 2. The gains of PBC, gains of the Luenberger observer, and the THD of the simulated inverter output voltage for cases, are presented in Figures 8–12.

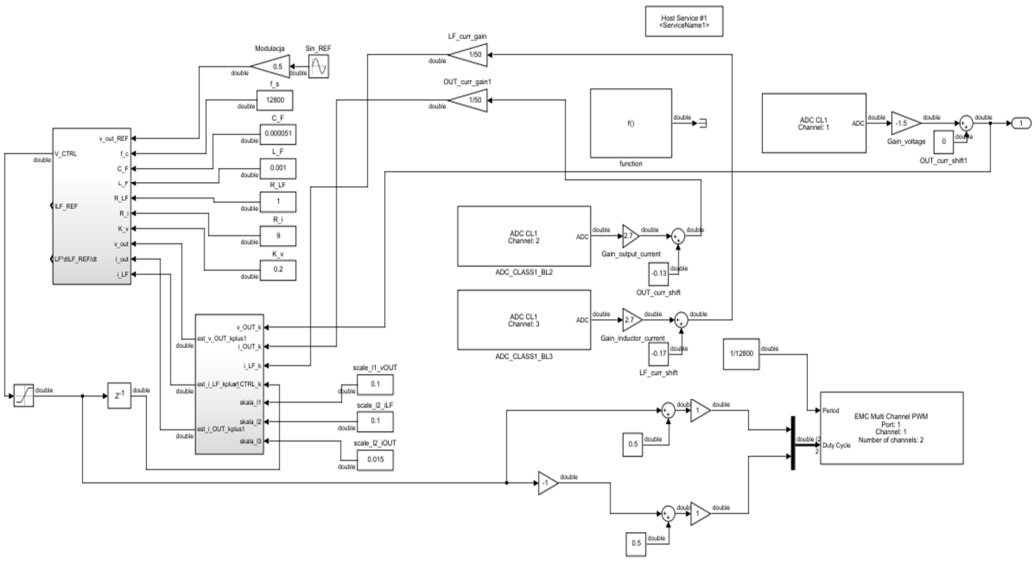
	K_v	R_i	l_1	l_2	l_3	THD
Open loop, f_s = 12,800 Hz	-	-	-	-	-	4.63%
No additional delay, PBC without prediction, f_s = 12,800 Hz	0.5	25	-	-	-	1.04%
Additional delay $2T_s$, PBC without prediction, f_s = 12,800 Hz	0.1	4	-	-	-	5.19%
Additional delay $2T_s$, PBC with prediction, f_s = 12,800 Hz	0.1	4	0.285	−0.778	−0.092	2.80%
Additional delay $2T_s$, PBC without prediction, f_s = 51,200 Hz	0.6	25	-	-	-	0.87%

10. The Experimental Verification of Output Voltage Distortions

Real-time interface (RTI1202 with FPGA—MicroLabBox) with MATLAB 2021b (with the dSpace RTI Electric Motor Control Blockset libraries) is the best choice for experimental verification of the previous SIMULINK simulations [46]. The main trouble of the microprocessor-based (or FPGA-based) control is scaling the measurement trace gain. In the case of the RTI, all the signals can be displayed on a PC monitor using ControlDesk 7.5 (dSpace 2021b) software, and the gains in the Simulink blocks can be adjusted. All the output voltage, output current and inductor current waveform amplitudes (for the modulation coefficient M = 1, the specified sinusoidal output voltage amplitude and the chosen load resistor) should be equal to the specified value 0.5 because the reference output voltage waveform is 0.5 sin (2π50t). The range of the input values of the PWM block was equal to 0–1. Two sinusoidal waveforms shifted mutually 180 degrees in the phase, with the zero level shifted by 0.5 and a maximum amplitude of 0.5 as the inputs of the PWM block to realize the PWM scheme from Figure 3. For a modulation index of M = 0.7, the output voltage scaling gain was −1.5 (it should be reversed), and the output and inductor currents have gains of 2.7. The measured signals were shifted by small constant values to adjust their zero-crossing level. The next step was to divide the current measurements by the load resistance (for the nominal load, scaling was 50 Ω). Experimental verification using RTI is sufficient; however, a further design step is to create software for the microprocessor. This is the reason why the architecture of the RTI1202 software is based on interrupts from the PWM unit, like in the microprocessor. The trigger line 1 events from an EMC multichannel PWM block are handled by an ADC class 1 hardware interrupt block (HWINT), connected to the input port of a function-call subsystem (Figure 13a). The function-call subsystem (Figure 13b) contains all the components of the inverter control loop, such as the EMC multichannel PWM block, the ADC class 1 block and the PBC controller, with amplifiers of all the measured signals. The sample time of all the blocks is inherited from the PWM block triggering event (it can be set only in this block). The experimental inverter bridge transistors are driven with four DIO class 1 3.3 V digital outputs: a noninverted channel 1 (corresponds to S1 from Figure 2) and channel 2 (S3 in Figure 2), and an inverted channel 3 (S2 in Figure 2) and channel 4 (S4). The dead time between switching off and on two transistors in the same leg of the bridge is equal to 500 ns for the Si-MOSFET transistors (IRFP360) and is implemented in IR2184-integrated circuits in the experimental inverter. The output voltage, output current and inductor current are measured via ADC Class 1 channel 1, with a single conversion (−10–+10 V input range) after the trigger event from the PWM block.



(**a**)



(**b**)

Figure 13. The schema of the control using SIMULINK and dSpace, (**a**) the block diagram of control with the function-call subsystem; (**b**) the inside of the function-call subsystem.

Figure 14 presents the same waveforms from the experimental inverter as Figures 8 and 10, Figures 11 and 12 for simulation. The gains and the distortions (THD) of the output signal are presented in Table 3. Figure 15 presents the tested experimental inverter with MicroLabBox (rti1202).

Table 3. The gains of PBC, gains of the Luenberger observer and THD of the experimental inverter output voltage for cases are presented in Figure 14.

	K_v	R_i	l_1	l_2	l_3	THD
Open loop, f_s = 12,800 Hz	-	-	-	-	-	6.35%
PBC without prediction, f_s = 12,800 Hz	0.1	4	-	-	-	7.63%
PBC with prediction, f_s = 12,800 Hz	0.2	9	0.285	−0.778	−0.138	4.09%
Additional delay $2T_s$, PBC without prediction, f_s = 51,200 Hz	0.3	30	-	-	-	1.73%

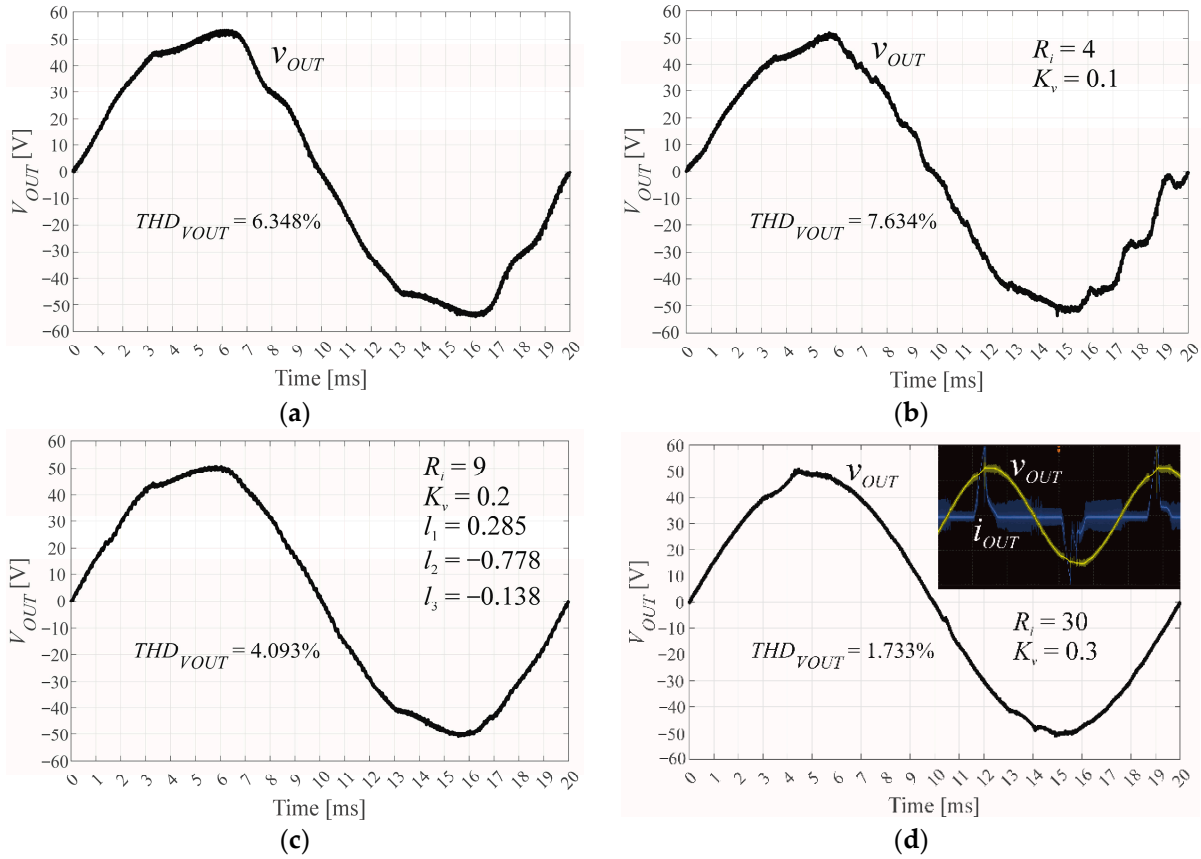


Figure 14. The output voltage waveforms: (**a**) f_s = 12,800 Hz, no feedback; (**b**) f_s = 12,800 Hz, PBC, no prediction; (**c**) f_s = 12,800 Hz, PBC with Luenberger observer; (**d**) f_s = 51,200 Hz, PBC, no prediction.

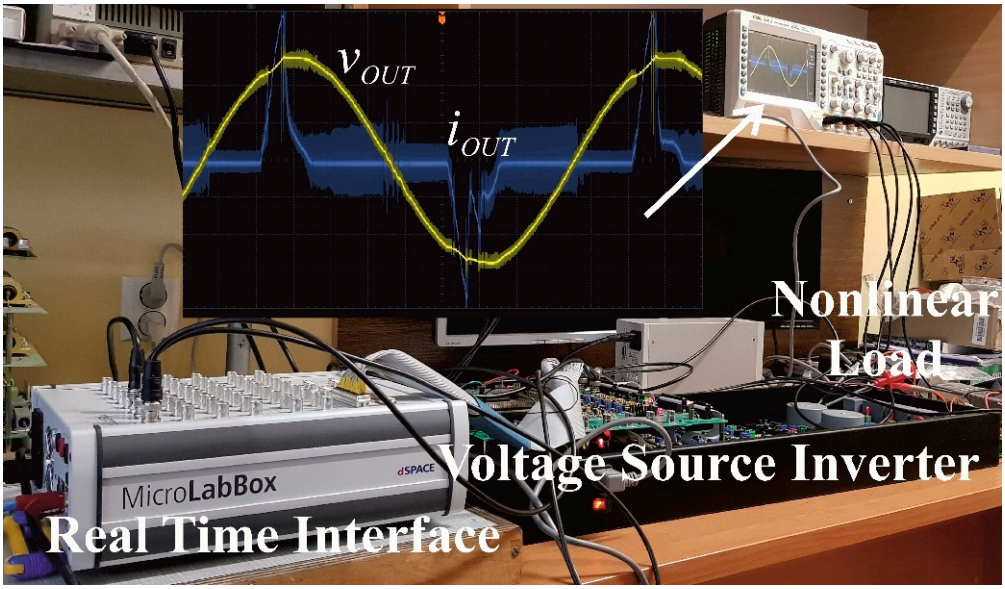


Figure 15. The laboratory equipment.

11. Results

Comparing Tables 2 and 3, it can be seen that the distortions are 1 to 2% higher in the experimental verification than in the simulations. The reason could be the ripple output voltage in the experimental VSI. The controller gains in the simulations and the experimental inverter were adjusted from the initial values from the border lines in Figure 7c

to obtain the lowest THD of the VSI output voltage without oscillations. However, in both cases of the simulation and the experimental verification, it was shown that for the low switching frequency (12,800 Hz), a lack of prediction in the control system can cause higher distortions of the output voltage than in the case of the open loop. For the high switching frequency (51,200 Hz), no prediction is required. Similar results in simulations and experimental verification prove that the approximation of the measuring trace Bode plots in the bandpass 0–1000 Hz, with delays equal to $2T_s$, is appropriate.

12. Discussion

The simulations and the breadboard verification showed that the measurement traces can be modelled as the delay with some switching periods and even using the MISO control (e.g., PBC) is insufficient for a low switching frequency (about 10 kHz). However, this control is perfect for a high switching frequency (about 50 kHz). For a low switching frequency, the delay in the measurement traces causes oscillations of the output voltage even for the low gains of the controller (below the border curve in Figure 7c, because the reason for these oscillations is not considered there). The distortions of the output voltage can be higher than without any instantaneous control. The high switching frequency allows for an increase in the controller gains and decreases the output voltage distortions. Using the prediction of the state variables is the solution for a low switching frequency, e.g., using the state equations with the Luenberger observer. In this way, calculations of the variables are more flexible for the different delays in the measurement traces. The whole time, the theoretical discrete model of the inverter was used. The gains of the Luenberger observer are initially calculated using the coefficient diagram method for the different delays of the closed-loop observer. Initially, one switching period delay of the observer was taken into the calculation of the initial gains and then the gains of the observer were experimentally decreased to obtain the lowest-output voltage distortions. Finally, the adjusted observer dynamics were comparable with the gains of the observer with about seven switching period delays. It can be concluded that for a low switching frequency (about 10 kHz) the observer is necessary because of delays in the measuring traces. The best results can be obtained without the prediction for a high switching frequency (about 50 kHz). The observer is the additional subsystem of the control loop and should be treated as a necessary evil, because it can cause some instability. The gains of the PBC controller were adjusted to the lowest distortions of the output voltage. In some cases, it was able to increase gains over the borderline of gains from Figure 7c and to accept small oscillations in the control voltage. Further increases in the controller gains increase the output voltage distortions.

13. Conclusions

Most of the measuring traces in the inverters have Bode plots that, in the range up to the corner frequency of the output filter, can be modelled as a delay equal to some switching periods. The only possibility for the low-output voltage distortion operation of a MISO instantaneous control loop with a low switching frequency (e.g., 10 kHz), in a real device with delays in the measuring traces, is to use an observer, e.g., the simple Luenberger type. The work with a high switching frequency (e.g., 50 kHz) makes this prediction unnecessary, because the delay in the measuring traces usually depends on the switching frequency, and the prediction unnecessarily complicates the control loop, even increasing the distortions.

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Data Availability Statement: All data files with results of simulations and measurements, the software for VSI simulation and control the experimental inverter are in the private possession of the author.

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Conflicts of Interest: The author declares no conflict of interest.

Abbreviations

VSI	Voltage Source Inverter;
THD	Total Harmonic Distortion;
CDM	Coefficient Diagram Method;
PBC	Passivity-Based Control;
ESR	Equivalent Series Resistance of the capacitor.
The inverter parameters symbols:	
C_F	The output filter capacitor or capacitance (Figures 1 and 2);
L_F	The output filter coil or inductance (Figures 1 and 2);
R_{CF}	The series resistance of the output capacitor (ESR), assigned equal to 0;
R_{LFe}	The equivalent serial resistance of the whole inverter, the sum of the serial resistance of the filter coil L_F, the resistances of two (on the diagonal of the inverter bridge) switched-on transistors in the bridge and the resistance of the PCB traces, connections, etc., strongly depends on the power losses in the output filter coil core;
f_s	The switching frequency;
f_m	The fundamental frequency (50 Hz);
ω_{F0}	The angular resonant frequency of the output filter;
ω_{max}	The angular frequency, for which the magnitude Bode plot has the maximum;
T_s	The switching period;
T_{ON}	The switching-on time.
The load parameters symbols:	
R_{LOAD}	The load resistance (Figure 1) for the pure resistive load;
R, C	the resistance and the capacitance of the nonlinear rectifier RC load (according to EN-62040-3 for PF = 0.7).
The currents and voltages symbols:	
I_{LF}, i_{LF}	The filter coil (inductor) current (Figures 1 and 2);
$I_{LFh1RMS}$	The RMS value of the fundamental harmonic of the inductor current;
I_{OUT}, i_{OUT}	The inverter output current (Figures 1 and 2);
V_{DC}	The DC voltage supplying the inverter (Figures 1 and 2);
V_{CTRL}, v_{CTRL}	The input voltage of the PWM modulator—the control voltage (Figures 1 and 2);
V_{OUT}, v_{OUT}	The output voltage of the inverter (Figures 1 and 2);
V_{OUTh1}	The amplitude of the fundamental harmonic (the first harmonic) of the inverter output voltage;
$V_{OUTh1RMS}$	The RMS value of the fundamental harmonic of the inverter output voltage;
$V_{OUTripplepp}$	The peak-to-peak value of the output ripple voltage;
V_{PWM}, v_{PWM}	The square output voltage waveform of the inverter bridge, the input voltage of the filter;
V_{FIN}, v_{FIN}	The envelope of the inverter bridge input voltage V_{PWM} used in calculations—delayed to v_{CTRL} with T_s.
The transfer functions symbols:	
$K_{CTRL}(s) = \frac{V_{OUT}(s)}{V_{CTRL}(s)}$	The transfer function of the control signal of the inverter with the PWM modulator;

$K_{CTRLc2d}(z)$	The discretized transfer function of the inverter with the PWM modulator;
$K_{INV} = \frac{V_{OUT}(s)}{V_{FIN}(s)}$	The transfer function of the bridge with the output filter without the PWM modulator;
K_{AMP}	The transfer function of the measuring trace;
$F_{LC}(s)$	Transfer function of the output filter, equal to K_{INV}(s);
$Z_{OUT}(s)$	output impedance of the inverter.

The state variables and matrixes symbols:

A, **B** and **C**	The state matrix, input matrix and output matrix of the inverter, respectively;
$\mathbf{x} = [v_{OUT}\ i_{LF}\ i_{OUT}]^T$	The inverter state variables vector;
$\hat{\mathbf{x}} = [\hat{v}_{OUT}\ \hat{i}_{LF}\ \hat{i}_{OUT}]^T$	The predicted state variables vector;
$\mathbf{u} = v_{FIN}$	The inverter input vector (in the presented case one variable);
$\mathbf{y} = v_{OUT}$	The inverter output vector (in the presented case one variable);
$\hat{\mathbf{y}} = \hat{v}_{OUT}$	The predicted inverter output vector;
$\mathbf{A}_D = e^{\mathbf{A}T_s}$	The discrete state matrix of the inverter;
$\mathbf{G}_D = e^{\mathbf{A}T_s/2}\mathbf{B}V_{DC}$	The discrete control matrix of the inverter;
ϕ_{ij}	Coefficients of the discrete state matrix;
g_{ij}	Coefficients of the discrete control matrix;

Luenberger observer symbols:

$\mathbf{L} = [l_1 \quad l_2 \quad l_3]^T$	The discretized Luenberger observer gain matrix;
l_i	Gains in the Luenberger observer gain matrix;

The CDM symbols:

$P(z^{-1}) = \sum_{i=0}^{n} p_{zi}(\tau/T_s)z^{-i}$	The discretized characteristic equation of the closed-loop system (Manabe Standard Form);
τ/T_s	The relative time constant of the closed-loop system.

The PBC symbols:

$H(x)$	The Hamiltonian function (Lyapunov function).

The other symbols:

F_{cost}	The cost function equal to the sum of the absolute values of the reactive powers in the output filter inductor and capacitor;
S_1, S_2, S_3, S_4	The control signals of the bridge transistors;
THD_{VOUT}	Total harmonic distortion of the output voltage.

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