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A High-Voltage-Gain DC–DC Boost Converter with Zero-Ripple Input Current for Renewable Applications

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Abstract: Renewable energy sources in DC microgrids require high-performance conversion systems to increase their capacity and reliability. Among other characteristics in conversion systems, the current ripple is a characteristic that must be considered since it affects the performance of PV panels and batteries. In this paper, a high-voltage-gain DC–DC boost converter for performing current ripple elimination that is based on a variable inductor is proposed. The topology is composed of a diode–capacitor voltage multiplier and a modified cascaded boost converter. To achieve voltage regulation, a reduced-order switched model is obtained considering the switched capacitor's dynamics. To address the inductance variation and external disturbances, the H_∞ control theory is adapted to systematically design a robust proportional–integral (PI) controller. Details of the working principles and the sizing of passive components are presented. The simulation and experimental results demonstrate that the input current ripple of the proposed converter can be removed in both transitory and steady states.

Keywords: DC–DC converters; high voltage gain; zero-ripple input current; variable inductor; H_∞ synthesis

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1. Introduction

Renewable energy sources in DC microgrids, such as PV panels, wind turbines, and bio-electricity, generate electrical power via different principles; however, they generally produce low-voltage buses. High-gain power converters are required to address the low voltage problem and regulate voltage levels [1–4]. To reach an adequate voltage level, a high duty ratio in the traditional boost converter or cascaded converters is used [5]. However, the efficiency and reliability of the power converter are greatly affected.

The voltage gain must be improved via several methods without affecting the overall system operation. These methods include the use of either switched capacitors or switched inductors to store energy. In [6], a replacement methodology was proposed and categorized in four cases: a combination of inductor and switch, a switch alone, a diode alone, and a combination of a switch and a diode. Another alternative reported in the literature is based on voltage multipliers [7–9]. The difference between these two methods is that voltage multipliers do not modify the topology, allowing voltage multipliers to stack up energy and increase the gain through the number of multiplier cells. In [10], some voltage-boosting techniques for PV microinverters were presented. These techniques used switched inductors and capacitors and/or transformers among switches and diodes to create step-up

cells. The main drawback of the above methods is the increase in converter volume. Most of the topologies of the previously mentioned techniques are derived with an input inductor, which requires a large inductance to reduce the input current ripple (ICR) of the converter.

On the other hand, several topologies can achieve a high step-up gain using coupled inductors, which transfer energy from one winding to the other through a common core [11]. In [12], a high voltage level without an extreme duty cycle was obtained; however, these types of boost converter topologies operate with a large ICR. To minimize the current ripple, an input current unit based on a coupled inductor and an auxiliary LC circuit was used [13]. The inductor size is another challenge; therefore, interleaved converters are proposed to eliminate the ICR in certain duty cycles that depend on the number of phases. In [14], a floating interleaved boost with different duty cycles for each phase was presented. The ICR was successfully canceled with a linear dependence of inductance and a duty cycle; however, this condition is restricted to the vicinity of the selected operating point, which is the disadvantage of this technique. This problem may be solved by using a ripple cancellation network based on a tapped inductor [15]. In this case, the input current ripple is removed in all power ranges, but the current stress and power loss are also significantly increased. Switch devices must switch under hard switching conditions, causing voltage and current stress. To address this disadvantage, an auxiliary resonant circuit has been proposed. In [16], an interleaved boost converter with soft switching was presented for electric vehicle applications. The resonance circuit enabled zero-voltage switching for switches and diodes.

Recent research has presented a study of ICR elimination using a variable inductor (VI) [17,18]. The VI is a magnetic device that allows for variation in the inductance based on the current source; therefore, an auxiliary winding is needed [19]. In [20], a detailed design methodology and the possibility of reducing core volume in a power converter were presented. The main advantage of the VI is that only one magnetic component is used to simultaneously achieve power transfer and current ripple manipulation. Moreover, there is galvanic isolation between the power converter and the VI control circuit.

Parameter mismatch is inherent in a real physical system; therefore, the controller design must guarantee operation under real circumstances. The classical control techniques are not completely effective under the influence of model uncertainty. In [21], a robust controller was designed by employing Kharitonov's theorem and considering the parameter variations in a DC–DC converter. A simple controller such as a PI can turn into a robust controller through the correct selection of its parameters. The only disadvantage of the method mentioned above is that the reduction in the output impedance in a nonminimum phase converter is achieved at the expense of the phase margin reduction. To solve the right-half zero problems, model reference adaptive control was incorporated into a conventional classic controller [22]. On the other hand, the robust control of DC–DC converters using the H_∞ control theory has not been fully introduced. This control theory addresses the parameter uncertainty with some fictitious weighting functions added to the nominal model [23,24]. The most difficult task in this approach is the choice of the weighting functions. Moreover, the main advantage of this method is the possibility of guaranteeing some level of performance of the controlled system.

This paper presents a high-voltage-gain DC–DC boost converter with zero-ripple input current using a VI. The primary function of the VI is to regulate the current ripple in one of the inductors to achieve a proportional mirror current, resulting in the total elimination of ICR independent of the operating point. The present study proposes an accurate reduced-order dynamical model that considers the effect of switched capacitor dynamics. The output voltage controller is based on the H_∞ control approach to deal with inductance variation and external disturbances. The main advantages of this proposal compared with other topologies reported in the literature are that a small inductor is required, the output voltage is not floated and grounded to the input voltage, the current ripple cancelation is independent of the operating point, and the system offers ripple elimination even in a transitory state. The proposed converter is very convenient for low-voltage sources such as

batteries, PV, and fuel cell systems, which require high-voltage conversion capability and low-volume topology.

This paper is organized as follows: In Section 2, the operation principle and topology are explained, considering the effects of the VI. Section 3 introduces the analysis and selection of components, including voltage gain, inductor sizing, and capacitor sizing. The nonlinear model, linearized model, and control scheme of the proposed converter are provided in Section 4. Experimental results and the corresponding analysis are described in Section 5. Finally, the paper's conclusion is given in Section 6.

2. Proposed Converter Topology

Figure 1 shows the circuit configuration of the proposed converter. To minimize the ICR, switches S_1 and S_2 operate complementarily. The input current i_s is the sum of inductor currents i_{L1} and i_{L2}, similar to interleaved converters. The voltage gain across the capacitor C_{in} is equivalent to the voltage gain in the traditional boost converter. The voltage multiplier improves the voltage gain and reduces the voltage stress on the switching components. In this case, the output voltage is the sum of V_1 and V_2. The inductor L_2 can be modified to reach a wide operating range with a zero-ripple input current. The current-source converter is incorporated to control the VI (L_2). This converter has a pulsating input current; however, a small input capacitor C_s filters this current and therefore becomes negligible.

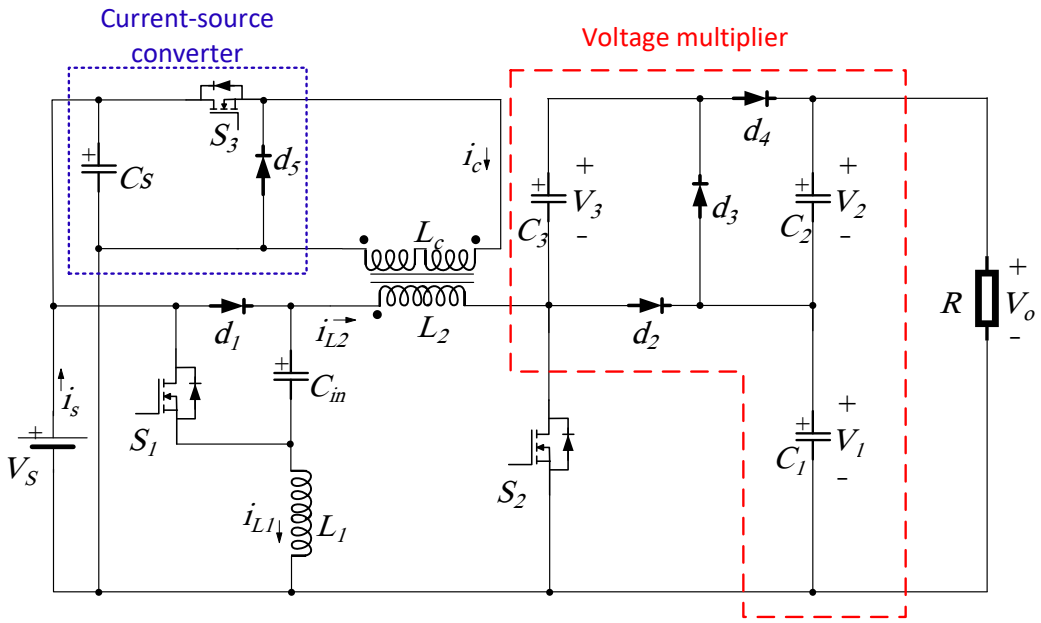


Figure 1. The schematic diagram of the proposed converter and its power stages.

2.1. Analysis of the Operating Principle

The related waveforms of the main converter, in steady-state operation, are shown in Figure 2.

Mode I [t_0, t_2]: During this time, the power switch S_1 is turned on, S_2 is turned off, and d_2 and d_4 are forward-biased. The equivalent circuit is depicted in Figure 3a. In this case, the input voltage V_s charges the inductor L_1, and the capacitor C_{in} and inductor L_2 are discharged to feed the capacitor C_1 and the load. In addition, the capacitors C_2 and C_3 are connected in parallel to deliver energy to the load. From t_0 to t_1, the charge of capacitors C_2 and C_3 starts to balance. From t_1 to t_2, the charge of capacitors C_2 and C_3 is balanced. The voltage level of both capacitors is equal to V_x. The voltage level of V_x is approximately equal to $V_o/2$. When t is equal to t_2, this operational mode is finished.

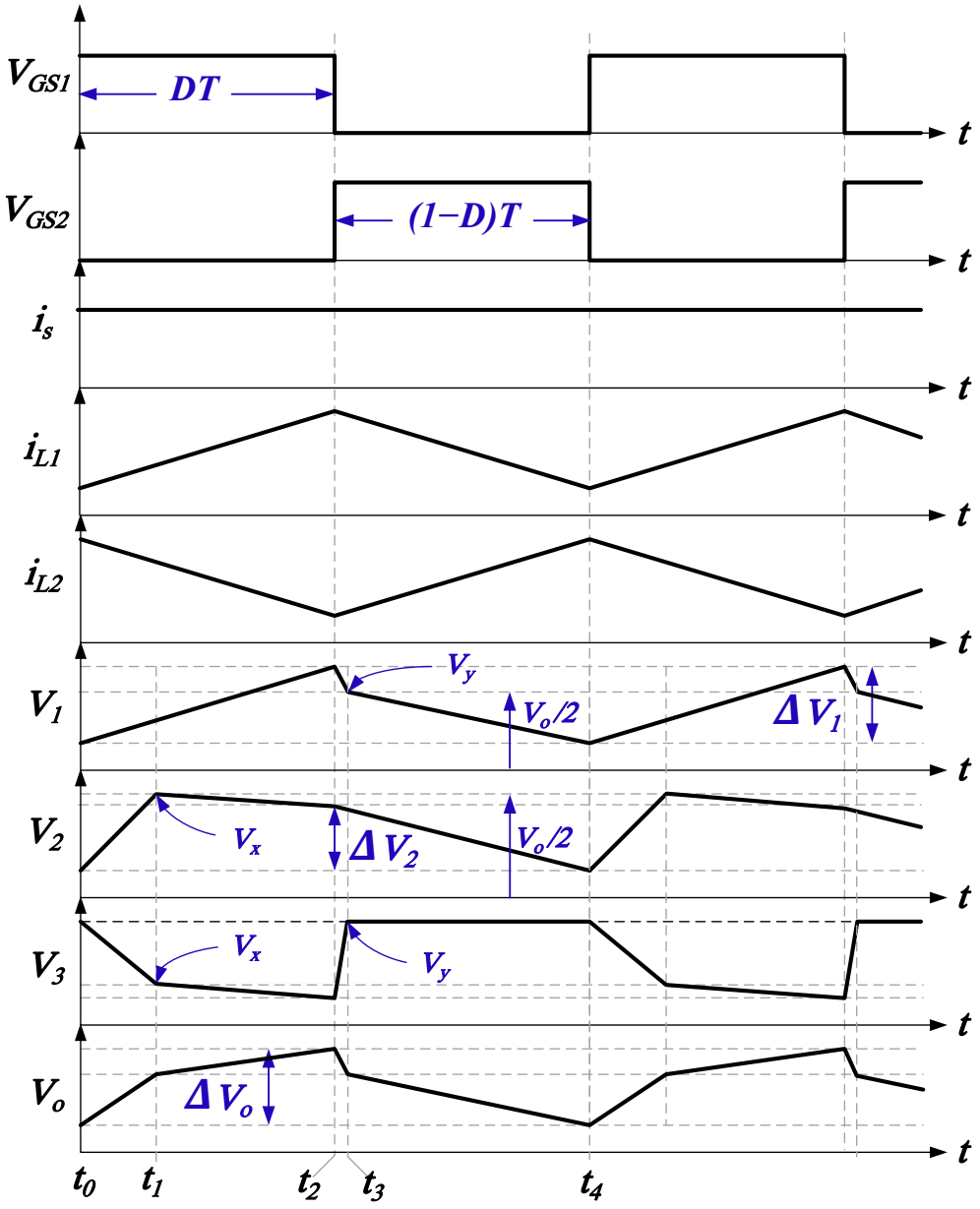


Figure 2. Steady-state waveforms of the main converter.

Mode II [t_2, t_3]: During this time, the power switch S_1 is turned off, S_2 is turned on, and d_1 and d_3 are forward-biased. The equivalent circuit is depicted in Figure 3b. In this case, L_1 is being discharged to feed capacitor C_{in}. The input voltage V_s charges the inductor L_2. Capacitor C_1 is connected in parallel with C_3. The voltage level of both capacitors is equal to V_y. The voltage level of V_y is approximately equal to $V_o/2$. Additionally, capacitors C_1 and C_2 deliver energy to the load. When t is equal to t_3, this operational mode is finished.

Mode III [t_3, t_4]: During this time, the power switch S_1 is turned off, S_2 is turned on, and d_1 is forward-biased. The equivalent circuit is depicted in Figure 3c. In this case, L_1 is discharged to feed capacitor C_{in}. The input voltage V_s charges the inductor L_2. Capacitor C_3 is charged and isolated from the circuit. Capacitors C_1 and C_2 deliver energy to the load. When t is equal to t_4, this operational mode is finished.

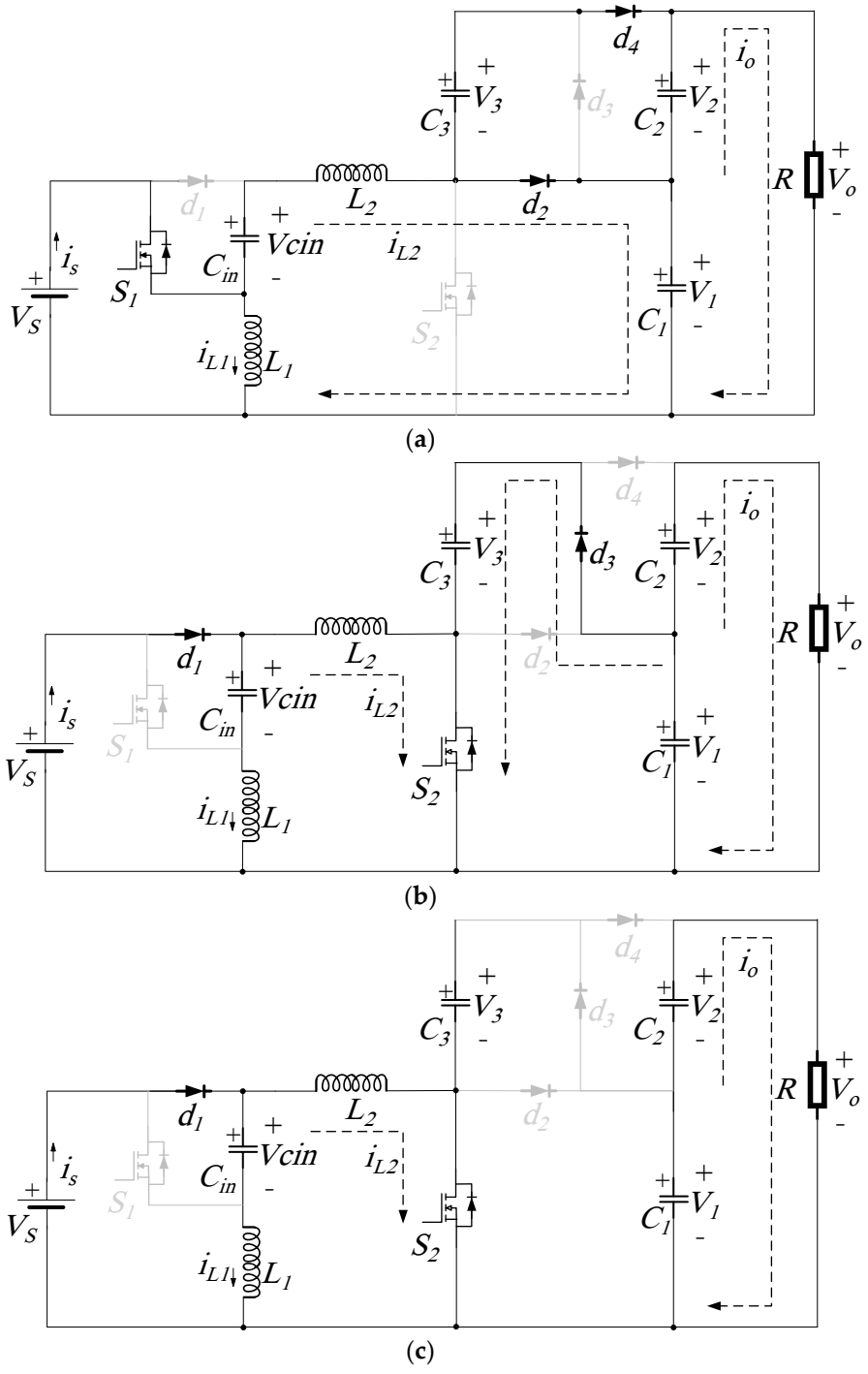


Figure 3. Operating modes during a switching period: (**a**) Mode I; (**b**) Mode II; (**c**) Mode III.

2.2. Variable Inductor Operation

A VI is a current-controlled device. The VI is implemented on a double E-core, which contains an auxiliary winding in the outer arms and the main winding in the center arm, as shown in Figure 4a. The principle of operation is based on the variation in the main winding's inductance through the flux control created by the auxiliary winding, as can be observed in Figure 4b. The amplitude variation in the current ripple is inversely proportional to the inductance of the power inductor. The primary function of the VI is to adjust the ripple in a linear relationship with the duty cycle.

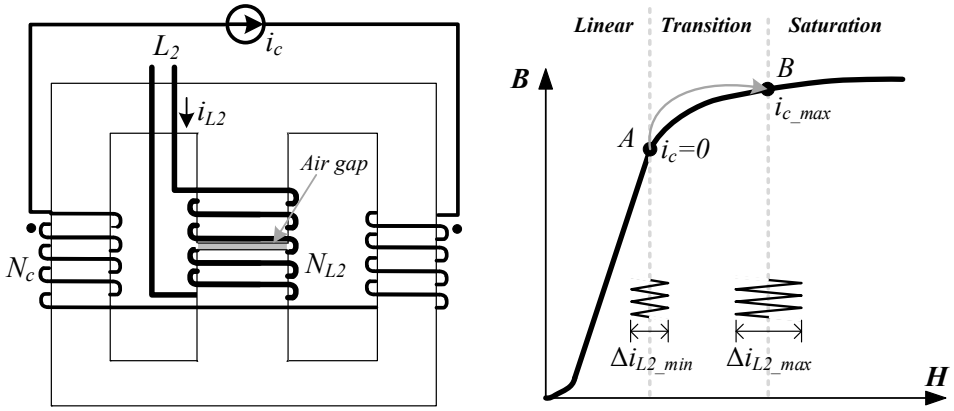


Figure 4. VI structure [18]: (**a**) winding distribution; (**b**) operating points on the B–H curve. Point A represents the limit of the linear region, and point B represents the limit of the transition region.

The controlled current in the auxiliary winding modifies the magnetic flux density of the core and moves the operating point. The current-source converter regulates the inductance using a robust controller since the VI suffers from uncertainties and external perturbations. However, the relationship between controlled current and inductance is nonlinear [20]. A reference estimator relates the controlled current i_c and L_2 to solve the nonlinear relationship. The estimator works over a specified span in the operating region where the VI has a quasilinear behavior. Figure 5 presents a schematic diagram for the practical implementation of the VI control. Details of the control design and implementation are in [18].

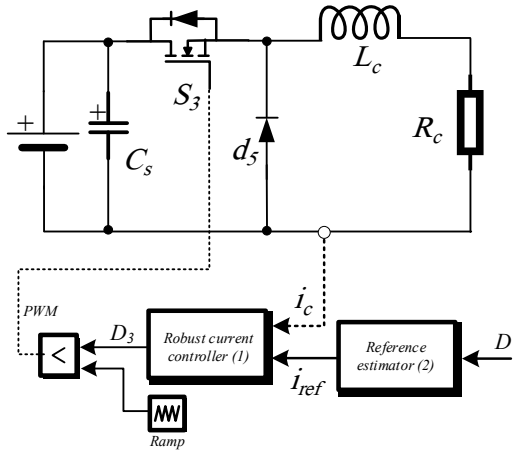


Figure 5. Schematic diagram of the power stage for the VI.

As it has been mentioned before, a robust controller is needed to regulate L_2, and the control input is expressed as [18]:

$$D_3 = \frac{L_c}{V_s}\left(\frac{R_c}{L_c} i_c - \eta sign(e)\right), \tag{1}$$

where L_c and R_c are the inductance and resistance of the auxiliary inductor, respectively; η is a controller gain; i_c is the controlled current; V_s is the voltage source; e is the current error; and D_3 is the control input.

The current reference estimator can be determined as follows [18]:

$$i_{ref} = i_{c\_min} - \frac{\Delta i_c}{\Delta L_2} L_1 \left(\frac{1-2D}{D} \right), \tag{2}$$

where ΔL_2 is the change in the value of L_2, Δi_c is the change in the value of i_c, D is the duty cycle of the proposed boost converter, and i_{c_min} is the minimum control current.

3. Analysis and Selection of Components

3.1. Voltage Gain

Under the assumption that the equivalent series resistance (ESR) is negligible, and by applying Kirchhoff's voltage law in the equivalent circuit of Mode I (Figure 3a), the following equations are obtained:

$$V_{L1} = V_s, \tag{3}$$

$$V_{L2} = V_s + V_{cin} - V_1, \tag{4}$$

where V_{L1} is the voltage across L_1, V_{cin} is the voltage across C_{in}, and V_1 is the voltage across C_1.

Expressions for relating Mode II (Figure 3b) are given as follows:

$$V_{L1} = V_s - V_{cin}, \tag{5}$$

$$V_{L2} = V_s. \tag{6}$$

where V_{L2} is the voltage across L_2.

The following equations can be derived by using the volt–second balance principle for both inductors:

$$\int_0^{DT} V_s dt + \int_0^{(1-D)T} (V_s - V_{cin}) dt = 0, \tag{7}$$

$$\int_0^{DT} (V_s + V_{cin} - V_1) dt + \int_0^{(1-D)T} V_s dt = 0. \tag{8}$$

By solving (7), the voltage across C_{in} can be obtained as follows:

$$V_{cin} = \frac{V_s}{1-D}. \tag{9}$$

By using (8) and (9), and considering output voltage $V_o \approx 2V_1$, the proposed converter gain can be expressed as follows:

$$M = \frac{2}{D(1-D)}. \tag{10}$$

In a practical implementation, the ESR of inductors limits this gain. The next equations consider this limitation.

$$\int_0^{DT} (V_s - r_1 i_{L1}) dt + \int_0^{(1-D)T} (V_s - r_1 i_{L1} - V_{cin}) dt = 0, \tag{11}$$

$$\int_0^{DT} \left(V_s + V_{cin} - r_2 i_{L2} - \frac{V_o}{2} \right) dt + \int_0^{(1-D)T} (V_s - r_2 i_{L2}) dt = 0, \tag{12}$$

where i_1, i_2, r_1, and r_2 are the currents and ESR of L_1 and L_2, respectively.

By applying Kirchhoff's current law in the equivalent circuit of Mode I, the following equations can be written:

$$i_{cin} = -i_{L2}, \tag{13}$$

$$i_{c1} = i_{L2} - 2i_o. \tag{14}$$

where i_{cin} is the current of C_{in}, i_{c1} is the current of C_1, and i_o is the current load; in addition, i_o is assumed to be equal to V_o/R.

The current equations of Mode II are calculated as follows:

$$i_{cin} = i_{L1}, \tag{15}$$

$$i_{c1} \approx -2i_o. \tag{16}$$

By applying the charge–second balance to C_{in} and C_1, the following equations can be obtained as follows:

$$\int_0^{DT} -i_{L2}dt + \int_0^{(1-D)T} i_{L1}dt = 0, \tag{17}$$

$$\int_0^{DT} (i_{L2} - 2i_o)dt + \int_0^{(1-D)T} -2i_o dt = 0. \tag{18}$$

By solving simultaneously (11), (12), (17) and (18), the practical converter gain is expressed as follows:

$$M_p = \frac{1}{(1-D)\left(\frac{2D}{(1-D)^2}\frac{r_1}{R} + \frac{2}{D}\frac{r_2}{R} + \frac{D}{2}\right)}. \tag{19}$$

Figure 6 shows the practical converter gain under the effect of different ratios of load resistance R, r_1, and r_2. As can be seen, the minimum voltage gain is eight and occurs at D = 50%, when the ESR is negligible. The gain increases if the duty cycle is different than 50%.

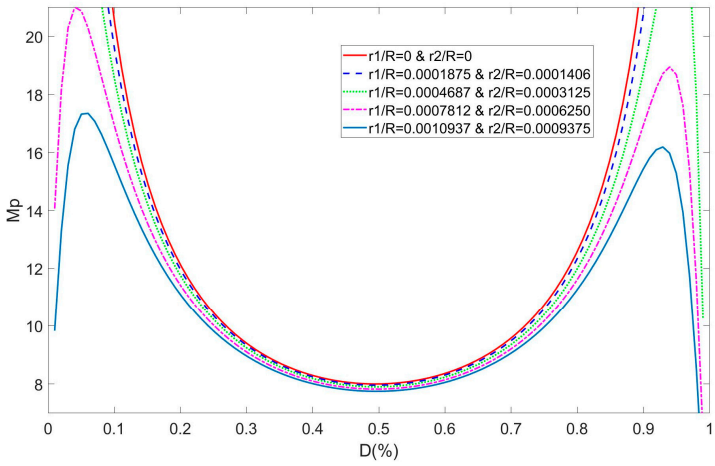


Figure 6. Voltage gain versus duty cycle considering ESR of inductors.

3.2. Inductor Sizing

By using (17) and (18), the average current of inductors L_1 and L_2 can be calculated as follows:

$$I_{L1} = \frac{2V_o}{R(1-D)}, \tag{20}$$

$$I_{L2} = \frac{2V_o}{RD}. \tag{21}$$

To eliminate the ICR, the sum of both inductor current ripples must be zero, considering (3) and (6) and their period yields

$$\frac{V_s DT}{L_1} - \frac{V_s(1-D)T}{L_2} = 0. \tag{22}$$

After some elementary algebraic transformations, Equation (22) yields

$$L_1 = \frac{D}{1-D} L_2. \tag{23}$$

As can be seen, inductors present a linear dependence. Therefore, this condition can be used to calculate the minimum inductance for L_1 in critical conduction mode. The minimum inductor current for L_2 is determined by using (21) and the change in current. This yields

$$i_{2,min} = \frac{2V_o}{RD} - \frac{1}{2}\frac{V_s(1-D)T}{L_2}. \tag{24}$$

Setting to zero and substituting (24) into (23), the minimum inductance is

$$L_{1min} = \frac{RD^2}{4Mf}. \tag{25}$$

Considering f as the switching frequency, the obtained value in (23) is the maximum for the VI, i.e., the minimum inductance for the VI must be fulfilled.

$$L_{2min} < \frac{RD(1-D)}{4Mf}. \tag{26}$$

3.3. Capacitor Sizing

In the study of power converters that use capacitor voltage multipliers, it is rare to present the relationship between capacitance and output voltage ripple. As can be observed in Figure 2, a good approximation is

$$\Delta V_o = \Delta V_1 + \Delta V_2, \tag{27}$$

where ΔV_1 is the voltage change in C_1, ΔV_2 is the voltage change in C_2 at $t = t_1$, and ΔV_o is the output voltage ripple.

The change in the charge in C_2 can be calculated as follows:

$$|\Delta Q_2| = \int_0^{(1-D)T} i_o dt = C\Delta V_2. \tag{28}$$

Assuming capacitors C_1, C_2, and C_3 are equal, and C is the capacitance, solving (28) yields

$$\Delta V_2 = \frac{V_o(1-D)}{RCf}. \tag{29}$$

Additionally, the change in the charge in C_1 can be calculated as follows:

$$\Delta Q_1 = \int_0^{DT} (i_2 - i_o)dt = C\Delta V_1. \tag{30}$$

By solving (30), we have

$$\Delta V_1 = \frac{V_o(2-D)}{RCf}. \tag{31}$$

Finally, substituting (29) and (31) in (27), the capacitance of the voltage multiplier in terms of output voltage ripple is

$$C = \frac{3-2D}{Rf\left(\frac{\Delta V_o}{V_o}\right)}. \tag{32}$$

4. Dynamic Analysis and Control Scheme

4.1. Switched Converter Model

The modeling of DC–DC converters with voltage multipliers involves several challenges. The dynamic of switched capacitors cannot be modeled using the averaging method [25]. A precise reduced-order model solves this problem. The complexity of the model depends on the states of C_3. The main objective of C_3 is to transfer energy from C_1 to C_2. However, this energy transfer occurs suddenly in Mode I. Figure 3a presents the dynamics of Mode I. A set of equations can be obtained as follows:

$$L_1\frac{di_{L1}}{dt} = -r_1 i_{L1} + V_s, \tag{33}$$

$$L_2\frac{di_{L2}}{dt} = -r_2 i_{L2} - V_1 + V_{cin} + V_s, \tag{34}$$

$$C_{in}\frac{dV_{cin}}{dt} = -i_{L2}, \tag{35}$$

$$C_1\frac{dV_1}{dt} = i_{L2} - \frac{(V_1+V_2)}{R}, \tag{36}$$

$$(C_2+C_3)\frac{dV_2}{dt} = -\frac{(V_1+V_2)}{R}. \tag{37}$$

Figure 3b,c present the dynamics of Modes II and III. These modes are modeled by using the following equations:

$$L_1\frac{di_{L1}}{dt} = -r_1 i_{L1} - V_{cin} + V_s, \tag{38}$$

$$L_2\frac{di_{L2}}{dt} = -r_2 i_{L2} + V_s, \tag{39}$$

$$C_{in}\frac{dV_{cin}}{dt} = i_{L1}, \tag{40}$$

$$C_1\frac{dV_1}{dt} = -\frac{(V_1+V_2)}{R} - \frac{(V_1-V_2)}{r_c}, \tag{41}$$

$$(C_2+C_3)\frac{dV_2}{dt} = -\frac{(V_1+V_2)}{R} + \frac{(V_1-V_2)}{r_c}, \tag{42}$$

where r_c is the equivalent resistance inducing losses due to the energy transfer among capacitors.

Considering (33)–(42), the switched model of the converter is as follows:

$$L_1 \frac{di_{L1}}{dt} = -r_1 i_{L1} - V_{cin}(1-u) + V_s, \tag{43}$$

$$L_2 \frac{di_{L2}}{dt} = -r_2 i_{L2} + (V_{cin} - V_1)u + V_s, \tag{44}$$

$$C_{in} \frac{dV_{cin}}{dt} = i_{L1}(1-u) - i_{L2}u, \tag{45}$$

$$C_1 \frac{dV_1}{dt} = i_{L2}u - \frac{(V_1+V_2)}{R} - \frac{(V_1-V_2)}{r_c}(1-u), \tag{46}$$

$$(C_2+C_3)\frac{dV_2}{dt} = -\frac{(V_1+V_2)}{R} + \frac{(V_1-V_2)}{r_c}(1-u). \tag{47}$$

where $u \in \{0,1\}$ is the switching function.

Current i_{L1} is denoted as x_1, current i_{L2} is denoted as x_2, voltage V_{cin} is denoted as x_3, voltage V_1 is denoted as x_4, voltage V_2 is denoted as x_5, and the sum of x_4 and x_5 is the output of the system y. The next expression represents the reduced-order nonlinear model:

$$\begin{aligned} \dot{\boldsymbol{x}} &= f(\boldsymbol{x}) + g(\boldsymbol{x})u \\ y &= h(\boldsymbol{x}) \end{aligned} \tag{48}$$

where

$$f(\boldsymbol{x}) = \begin{bmatrix} -\frac{r_1}{L_1}x_1 - \frac{1}{L_1}x_3 + \frac{1}{L_1}V_s \\ -\frac{r_2}{L_2}x_2 + \frac{1}{L_2}V_s \\ \frac{1}{C_{in}}x_1 \\ -\frac{1}{C_1}\frac{(x_4+x_5)}{R} - \frac{1}{C_1}\frac{(x_4-x_5)}{r_c} \\ -\frac{1}{(C_2+C_3)}\frac{(x_4+x_5)}{R} + \frac{1}{(C_2+C_3)}\frac{(x_4-x_5)}{r_c} \end{bmatrix}; \; g(\boldsymbol{x}) = \begin{bmatrix} \frac{1}{L_1}x_3 \\ -\frac{1}{L_2}(x_3-x_4) \\ \frac{1}{C_{in}}(x_1+x_2) \\ \frac{1}{C_1}\frac{(x_4-x_5)}{r_c} \\ -\frac{1}{(C_2+C_3)}\frac{(x_4-x_5)}{r_c} \end{bmatrix};$$

$$h(\boldsymbol{x}) = x_4 + x_4; \; \boldsymbol{x} = [x_1 \; x_2 \; x_3 \; x_4 \; x_5]^T.$$

Figure 7 shows the comparison between the full-order model and the reduced-order model. As can be observed, the steady-state and dynamic response in the simulation present good agreement.

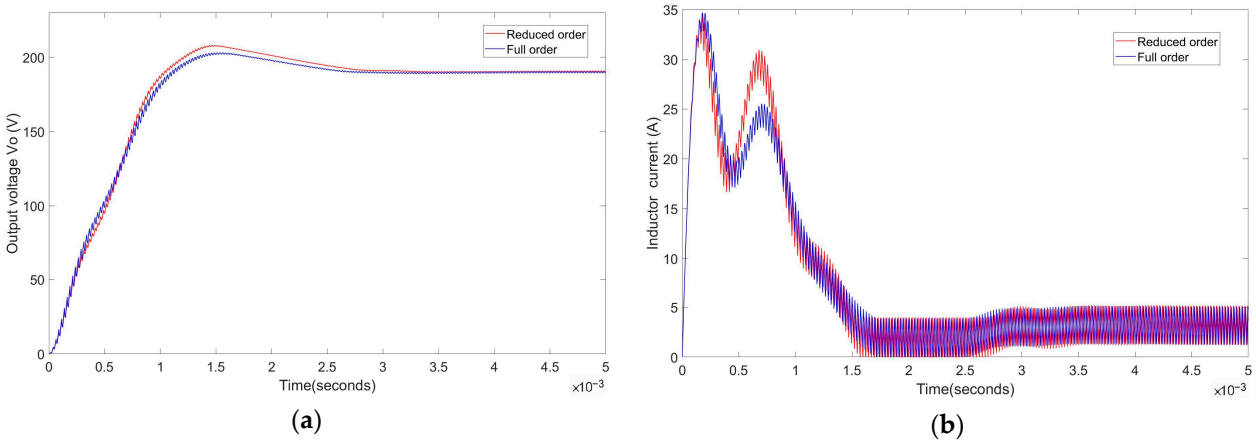


Figure 7. Comparison between the reduced-order model and the full-order model: (**a**) output voltage; (**b**) current of L_2.

The simulation of the full-order model was carried out using PSIM software, while the simulation of the reduced-order model was performed using MATLAB software. The backward Euler method and 10 ns time step were used to solve Equation (48). The parameters involved in this simulation were V_s = 24 V, L_1 = 90 µH, L_2 = 60 µH, C_{in} = 100 µF, $C = C_1 = C_2 = C_3$ = 47 µF, r_c = 100 mΩ, r_1 = 25 mΩ, r_2 = 20 mΩ, R = 200 Ω, and u(average) = 0.6. In the case of r_c, the value is strongly influenced by the ON-state resistance of transistor S_2 and the ON-state of diode d_3.

4.2. Linearized Average Model

The linear state–space model can be linearized from (48) and by replacing the switching function u with its average value u_{av}. Setting the relevant derivatives in (48) to zero, the desired operating values can be obtained as follows:

$$\begin{bmatrix} r_1 & 0 & (1-\overline{u}_{av}) & 0 & 0 \\ 0 & r_2 & -\overline{u}_{av} & \overline{u}_{av} & 0 \\ (1-\overline{u}_{av}) & -\overline{u}_{av} & 0 & 0 & 0 \\ 0 & \overline{u}_{av} & 0 & -\frac{r_c+R(1-\overline{u}_{av})}{r_cR} & \frac{R(1-\overline{u}_{av})-r_c}{r_cR} \\ 0 & 0 & 0 & \frac{R(1-\overline{u}_{av})-r_c}{r_cR} & -\frac{r_c+R(1-\overline{u}_{av})}{r_cR} \end{bmatrix} \begin{bmatrix} \overline{x}_1 \\ \overline{x}_2 \\ \overline{x}_3 \\ \overline{x}_4 \\ \overline{x}_5 \end{bmatrix} = \begin{bmatrix} V_s \\ V_s \\ 0 \\ 0 \\ 0 \end{bmatrix}. \tag{49}$$

From Equation (48), the linearization of the average model around the desired equilibrium point $(\overline{x}_1, \overline{x}_2, \overline{x}_3, \overline{x}_4, \overline{x}_5, \overline{u})$ yields the following state equations:

$$\begin{aligned} \dot{\widetilde{x}} &= \mathbf{A}\widetilde{x} + \mathbf{B}_1\widetilde{u}_{av} + \mathbf{B}_2\widetilde{V}_s, \\ \widetilde{y} &= \mathbf{C}\widetilde{x}, \end{aligned} \tag{50}$$

with $\widetilde{x} = \begin{bmatrix} \widetilde{x}_1 & \widetilde{x}_2 & \widetilde{x}_3 & \widetilde{x}_4 & \widetilde{x}_5 \end{bmatrix}^T$, $\widetilde{x}_1 = x_1 - \overline{x}_1$, $\widetilde{y}_1 = \widetilde{x}_2 = x_2 - \overline{x}_2$, $\widetilde{x}_3 = x_3 - \overline{x}_3$, $\widetilde{x}_4 = x_4 - \overline{x}_4$, $\widetilde{x}_5 = x_5 - \overline{x}_5$, $\widetilde{u}_{av} = u_{av} - \overline{u}_{av}$, and $\widetilde{V}_s = V_s - \overline{V}_s$, where the superscript (~) represents the linearized signal. The matrices $\mathbf{A}$, $\mathbf{B}_1$, and $\mathbf{B}_2$ are obtained via the Taylor first-order development as follows:

$$\mathbf{A} = \frac{\partial(f(\boldsymbol{x}) + g(\boldsymbol{x})u)}{\partial \boldsymbol{x}}; \mathbf{B}_1 = \frac{\partial(f(\boldsymbol{x}) + g(\boldsymbol{x})u)}{\partial u}; \mathbf{B}_2 = \frac{\partial(f(\boldsymbol{x}) + g(\boldsymbol{x})u)}{\partial V_s}$$

The system matrix is given as follows:

$$\mathbf{A} = \begin{bmatrix} -\frac{r_1}{L_1} & 0 & -\frac{(1-\overline{u}_{av})}{L_1} & 0 & 0 \\ 0 & -\frac{r_2}{L_2} & \frac{\overline{u}_{av}}{L_2} & -\frac{\overline{u}_{av}}{L_2} & 0 \\ \frac{(1-\overline{u}_{av})}{C_{in}} & -\frac{\overline{u}_{av}}{C_{in}} & 0 & 0 & 0 \\ 0 & \frac{\overline{u}_{av}}{C_1} & 0 & -\frac{r_c+R(1-\overline{u}_{av})}{r_cRC_1} & \frac{R(1-\overline{u}_{av})-r_c}{r_cRC_1} \\ 0 & 0 & 0 & \frac{R(1-\overline{u}_{av})-r_c}{r_cR(C_2+C_3)} & -\frac{r_c+R(1-\overline{u}_{av})}{r_cR(C_2+C_3)} \end{bmatrix}. \tag{51}$$

While the input matrices are written as follows:

$$\boldsymbol{B}_1 = \begin{bmatrix} \frac{\overline{x}_3}{L_1} & \frac{(\overline{x}_3-\overline{x}_4)}{L_2} & -\frac{(\overline{x}_1+\overline{x}_2)}{L_2} & \frac{\overline{x}_2+(\overline{x}_4-\overline{x}_5)}{r_cC_1} & -\frac{(\overline{x}_4-\overline{x}_5)}{r_c(C_2+C_3)} \end{bmatrix}^T, \tag{52}$$

$$\boldsymbol{B}_2 = \begin{bmatrix} \frac{1}{L_1} & \frac{1}{L_2} & 0 & 0 & 0 \end{bmatrix}^T. \tag{53}$$

In the case of the output matrix,

$$\mathbf{C} = \begin{bmatrix} 0 & 0 & 0 & 1 & 1 \end{bmatrix}. \tag{54}$$

The control voltage gain and audio susceptibility transfer functions corresponding to the state in Equation (50) are, respectively,

$$G_u(s) = \boldsymbol{C}(s\boldsymbol{I} - \mathbf{A})^{-1}\boldsymbol{B}_1, \tag{55}$$

$$G_v(s) = \boldsymbol{C}(s\boldsymbol{I} - \mathbf{A})^{-1}\boldsymbol{B}_2. \tag{56}$$

Figure 8 compares the switched model (48) and the output voltage transfer function (55) using the same parameters as in Figure 7. The input $\widetilde{u}_{av}$ presents a step change of 1% at time t = 0.03 s, and the output voltage changes from 189.6 to 191.2 V.

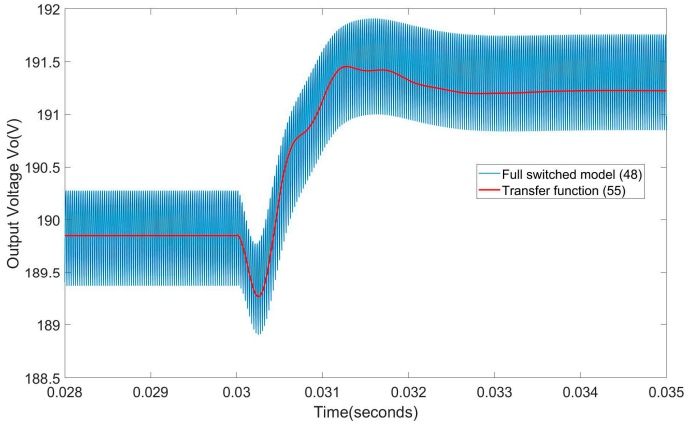


Figure 8. Comparison between the fully switched model and the transfer function $G_u(s)$.

4.3. Control Design

The general philosophy of robust control is to design a controller for a set of models instead of designing for just one model. Compared with the physical system, the open-loop plant $G_u(s)$ presents a plant-model mismatch. In this study, the uncertain model considers a multiplicative uncertainty.

The transfer function of the system in the presence of uncertainty can be expressed as follows:

$$\mathrm{G}_p(s) = G_u(s)(1 + W_d(s)\Delta(s)), \|\Delta(s)\|_\infty < 1, \tag{57}$$

where $\mathrm{G}_p(s)$ is the uncertain plant; $W_d(s)$ is an uncertain weight, which captures the size of the deviation; and $\Delta(s)$ represents the unstructured uncertainty.

The deviation of $G_u(s)$ and $\mathrm{G}_p(s)$ at some frequency ω is measured by the relative error of their frequency response, and the mathematical expression is given as follows:

$$\max_{\mathrm{G}_p \in \boldsymbol{G}} \left| \frac{\mathrm{G}_p(j\omega) - G_u(j\omega)}{G_u(j\omega)} \right| < W_d(s), \quad \forall \omega \geq 0. \tag{58}$$

The main uncertainties are caused by L_2, r_1, r_2, and R. The uncertainty radii are listed in Table 1.

Table 1. Nominal values and uncertainty radii of the proposed converter.

Parameter	Nominal Value	Uncertainty Radius
L_1	95 µH	0
L_2	60 µH	25 µH $\leq L_n \leq$ 95 µH
C	47 µF	0
C_{in}	100 µF	0
r_1	250 mΩ	150 mΩ $\leq r_{n1} \leq$ 350 mΩ
r_2	200 mΩ	100 mΩ $\leq r_{n2} \leq$ 200 mΩ
R	213 Ω	160 Ω $\leq R_n \leq$ 360 Ω

Selecting weighting functions are essential in robust control design techniques. Low frequency requires a high disturbance rejection. The weighting function acts as a low-pass filter. Therefore, the following form of weighting function is selected [26]:

$$W_e(s) = \frac{\frac{s}{H} + W_b}{s + W_b A}, \tag{59}$$

where W_b is allowable bandwidth, A is an allowable steady-state error, and H is an allowable high-frequency error.

The process is presented according to the standard linear fractional transformation (LFT) configuration, as shown in Figure 9.

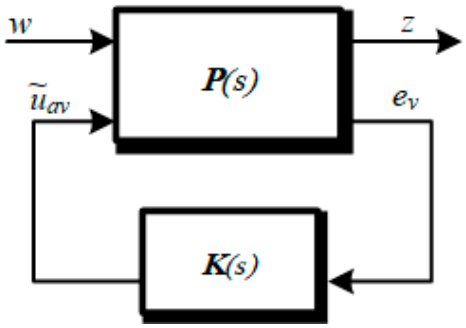


Figure 9. Standard H_∞ control problem.

The generalized plant $\boldsymbol{P}(s)$ has two inputs: the exogenous input $w = \left[V_{ref}\ \tilde{V}_s\right]^T$, which includes the reference signal and disturbance, and the manipulated variable $\tilde{u}_{av}$. There are two outputs: the error signal $z = [V_{oz}\ u_z\ e_z]^T$ and the measured variable e_v.

The closed-loop system can be expressed as follows:

$$\begin{bmatrix} z \\ e \end{bmatrix} = \boldsymbol{P}(s) \begin{bmatrix} w \\ \tilde{u}_{av} \end{bmatrix} = \begin{bmatrix} P_{11}(s) & P_{12}(s) \\ P_{21}(s) & P_{22}(s) \end{bmatrix} \begin{bmatrix} w \\ \tilde{u}_{av} \end{bmatrix}, \tag{60}$$
$$\tilde{u}_{av} = \boldsymbol{K}(s) e_v,$$

where

$$P_{11}(s) = \begin{bmatrix} 0 & -W_d(s) w_i G_v(s) \\ 0 & 0 \\ W_e(s) & W_e(s) w_i G_v(s) \end{bmatrix}; P_{12}(s) = \begin{bmatrix} W_d(s) G_u(s) \\ w_u \\ -W_e(s) G_u(s) \end{bmatrix};$$

$$P_{21}(s) = [I w_i G_v(s)]; P_{22}(s) = [-G_u(s)].$$

Considering w_i as a constant input weight and w_u as a constant output weight, the lower LFT gives the system transfer function matrix from w to z as follows:

$$z = F_l(\boldsymbol{P}, \boldsymbol{K}) w \tag{61}$$

where

$$F_l(\boldsymbol{P}, \boldsymbol{K}) = P_{11} + P_{12}\boldsymbol{K}(I - P_{22}\boldsymbol{K})^{-1} P_{21}.$$

The control objective is to synthesize a stabilizing controller $\boldsymbol{K}$ for all the plant models, i.e., H_∞ control theory involves the minimization of the norm of $F_l(\boldsymbol{P}, \boldsymbol{K})$. The infinity norm can be calculated using the following equation:

$$\left\| F_l(\boldsymbol{P}, \boldsymbol{K}) \right\|_\infty = \sup_\omega \overline{\sigma}(F_l(\boldsymbol{P}, \boldsymbol{K})(j\omega)) \leq \gamma, \tag{62}$$

where $\overline{\sigma}$ is the maximum singular value, and the value of γ implies the disturbance rejection capability.

The output voltage controller is chosen as a proportional–integral controller as follows:

$$\boldsymbol{K}(s) = \frac{K_i + K_p s}{s}, \tag{63}$$

where K_p is the proportional gain, and K_i is the integral gain.

The controller parameters of (63) were obtained with the *hinfstruct* command of MATLAB. This command extends classical H_∞ synthesis to fixed-structure linear control systems [27]. The selection of weighting functions is essential to define the desired performances of the closed-loop control system. Performance weight $W_e(s)$ provides the steady-state error and settling time, using the bandwidth W_b and term A [28]. The control action weight w_u must be adjusted according to the following criteria: A smooth control input is obtained if $w_u > 1$, and aggressive control input is obtained if $w_u < 1$. The effect of $G_v(s)$ must be scaled to obtain a disturbance signal less than one in magnitude, using an input weight w_i. Therefore, this term is inverse to static gain. The weighting functions are selected as follows:

$$\begin{cases} W_d(s) = \frac{0.4623s^3 + 1.428\times10^5 s^2 + 3.222\times10^8 s + 1.163\times10^{12}}{s^3 + 7.638\times10^4 s^2 + 1.057\times10^9 s + 1.071\times10^{13}} \\ W_e(s) = \frac{0.4s+80}{s+0.008} \\ w_u = 1.2 \\ w_i = 0.2 \end{cases} \tag{64}$$

The obtained control gains are K_p = 0.00251 and K_i = 1.642, while the γ value achieved for the closed-loop system is 0.704. Figure 10 shows the behavior of the uncertain plant $G_p(s)$ in a closed-loop system based on its corresponding bode diagram.

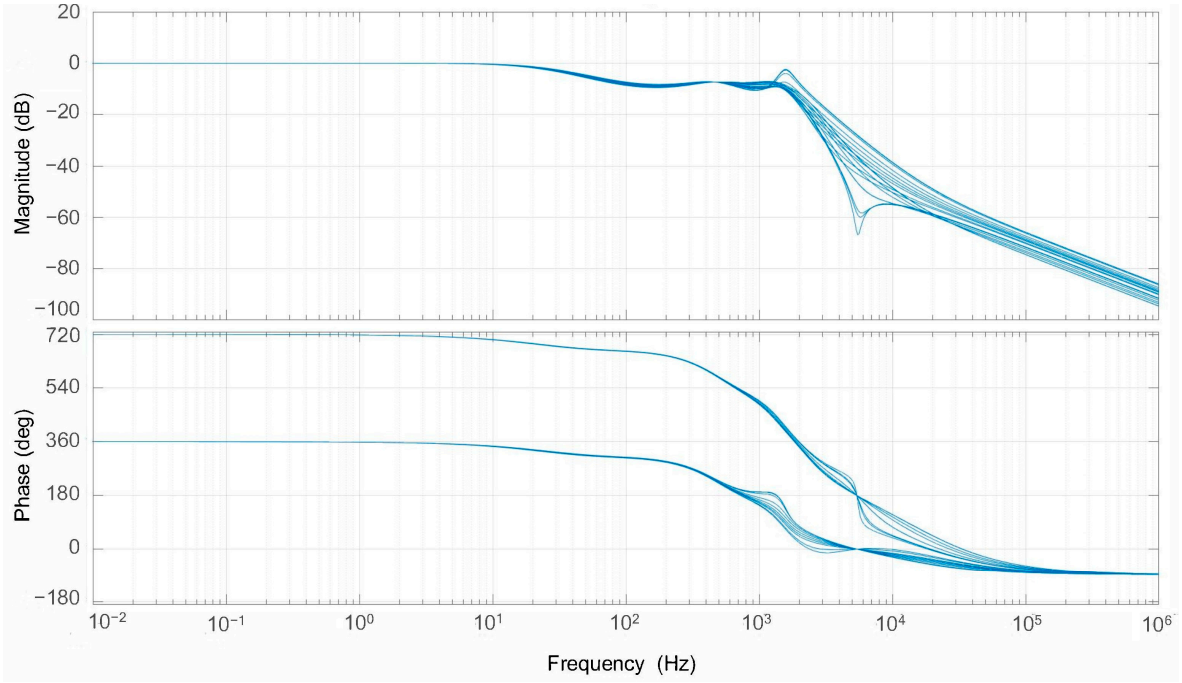


Figure 10. Bode diagram of closed-loop response. From top to bottom: magnitude diagram (top) and phase diagram (bottom).

Figure 11 depicts the waveforms of the simulation with a load change. As can be seen, a good dynamic response was obtained. The simulation of load step change was carried out using Simulink/MATLAB. The nominal plant $G_u(s)$ and V_s= 24 V were used to verify

the performance of the controller $\boldsymbol{K}(s)$. The simulation configuration parameters were as follows: The fixed-step size was 10 ns, with an ODE 5 (Dormand–Prince) solver, and the sampling time of the voltage controller was 10 us. At time t = 0.1 s, the load changed from 60% to 100%. The load returned to 60% at t = 0.3 s. Overshoot and undershoot were 6 V in both cases, and the settling time was 100 ms in both cases. A limiter can be added to avoid inrush current during startup transient. However, it does not affect the performance of the controller when the system is in the vicinity of the equilibrium point. In the present study, the limiter was included and bounded from 0.05 to 0.75.

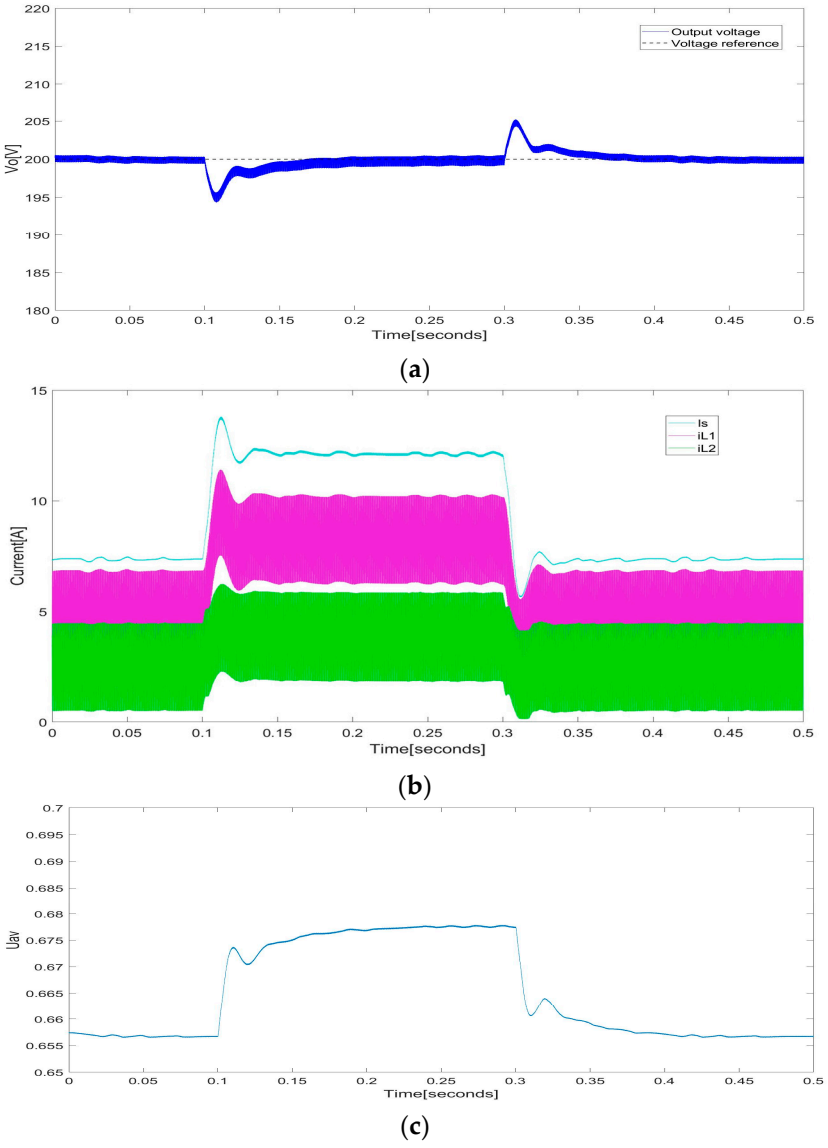


Figure 11. Simulated transient of the proposed DC-DC boost converter under a load step change from 60% to 100% and vice versa: (**a**) output voltage V_o (blue trace) and reference (dotted line); (**b**) from top to bottom: input current i_s (cyan trace), inductor current i_{L1} (magenta trace), and inductor current i_{L2} (green trace); (**c**) control law u_{av}.

Figure 12 shows the block diagram of the DC–DC converter with the overall control system. The power stage, the VI, and the controller are illustrated, for the main boost converter and the current-source converter.

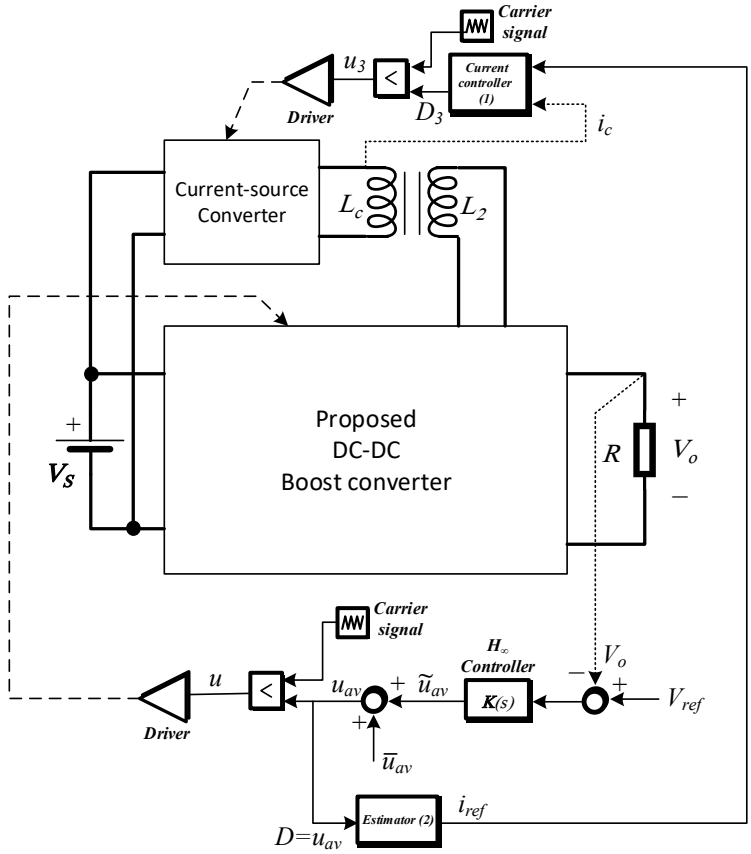


Figure 12. Proposed DC–DC converter and its overall control scheme.

5. Experimental Results and Discussion

The circuit in Figure 1 was implemented to validate the proposed zero-ripple input current method. Figure 13 and Table 2 show the experimental prototype and specifications, respectively. The controllers were implemented using a CompactRIO embedded system with an NI cRIO-9067 chassis, NI 9223 analog input module, and NI 9401 digital output module.

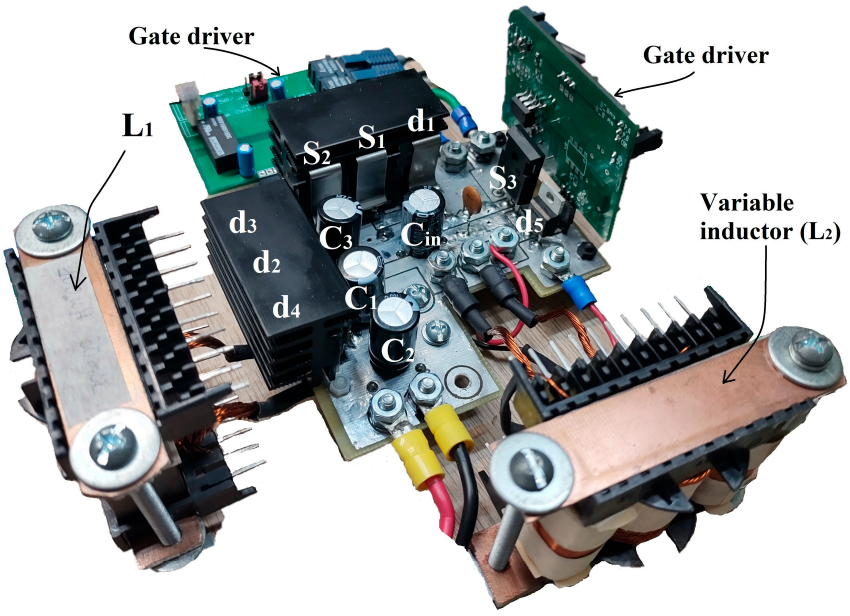
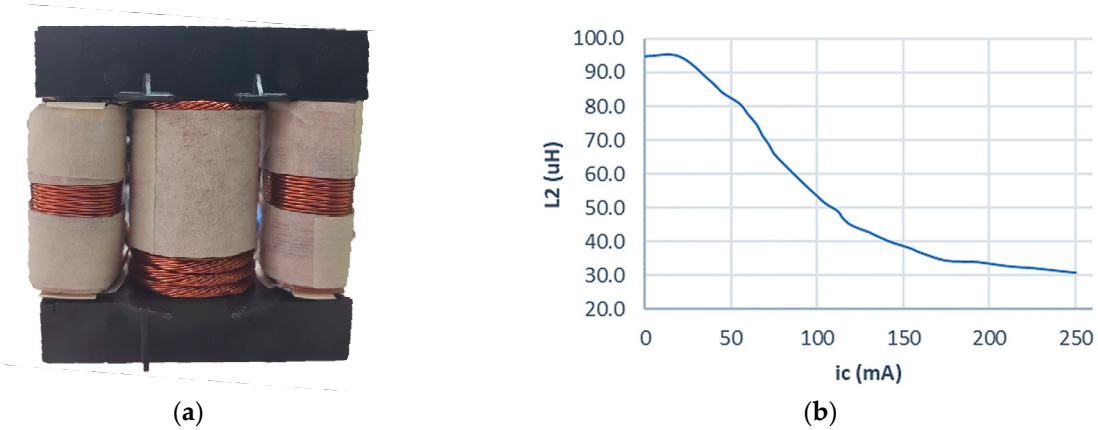


Figure 13. Experimental prototype.

Table 2. Specifications of the prototype.

Parameter Component	Value and Information
Rated power	250 W
Switching frequency f	40 kHz
Input voltage V_s	20–30 V
Output voltage V_o	200 V
Transistors S_1, S_2, and S_3	C3M0065090D
Diodes d_3, d_2, d_3, d_4, and d_5	GE10MPS06A
Electrolytic capacitor C_{in}	100 µF
Electrolytic capacitors C_1, C_2, and C_3	47 µF
Inductor L_1	95 µH
Variable inductor L_2	25–95 µH

The VI was implemented in an ETD 49/25/16 E-core with 3C90 magnetic material (Figure 14a), N_{L2} = 14, N_c= 153, and the switching frequency for S_3 was 20 kHz. The VI controller was set up, incorporating these parameters, with the controller gain η = 7. As shown in Figure 14b, the first test for measuring the variable inductance L_2 was performed. The input voltage was 24 V, and the proposed converter was loaded with a 220 Ω resistance. The estimator values were obtained from the measurements as follows: i_{c_min}= 0.035 A, Δi_c= 0.130 A, and ΔL_2 =65 µH.



(**a**) (**b**)

Figure 14. VI graphical representation: (**a**) prototype; (**b**) inductance curve.

A test with the main converter in an open loop, applying a duty cycle D = 0.6, was carried out. Figure 15 shows the waveforms for the proposed converter when loaded with a 220 Ω resistance and an input voltage V_s = 24 V. The average current of both inductors was different; however, the zero-ripple input current was accomplished. As can be observed, the current ripple Δi_{L2} of the VI is distorted. This is due to many reasons: the core is forced to operate within the limits of the linear and transitional regions, but also with a small unbalanced winding of the arms, which has an impact on the magnetic reluctance and the parasitic capacitance of the windings in high frequency [29].

Figure 16 shows the dynamic response of the proposed converter under the action of the robust PI controller. The output load changed from 60% to 100% and vice versa, while the reference voltage was 200 V. In this test, the inductance L_2 varied in the function of the duty cycle to guarantee the ICR elimination. As can be observed, variation in the inductance parameter value L_2 did not cause a significant change in performance or stability. The voltage overshoot and undershoot was about 8 V. The settling time was about 120 ms, which is a good response for boost converters with high gain, but it should also be noted that the overvoltage or undervoltage was small.

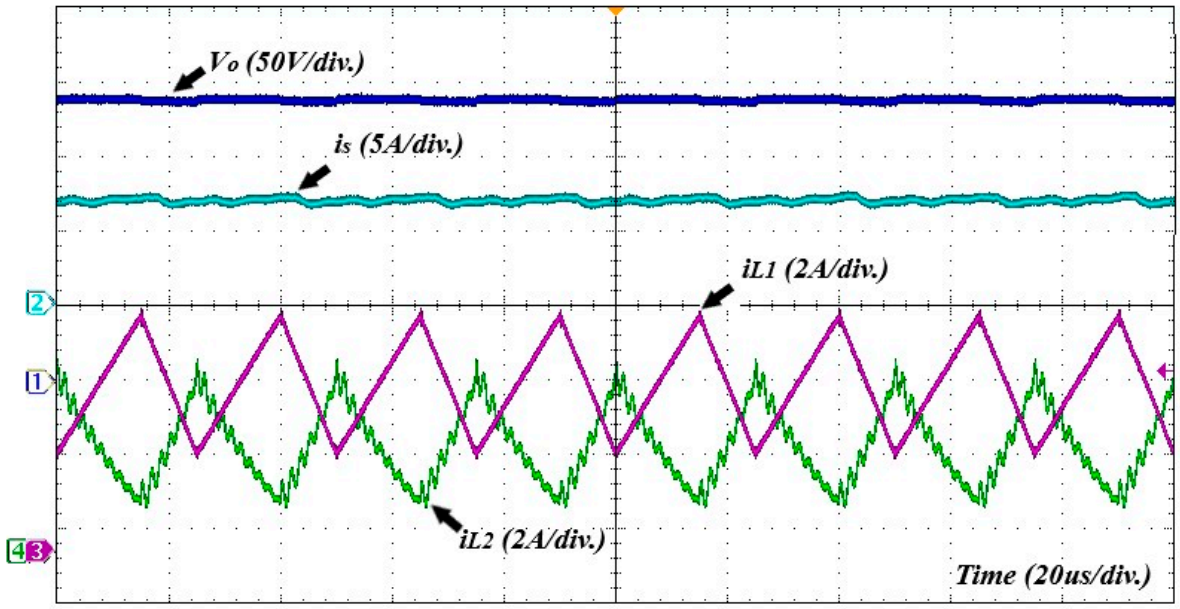
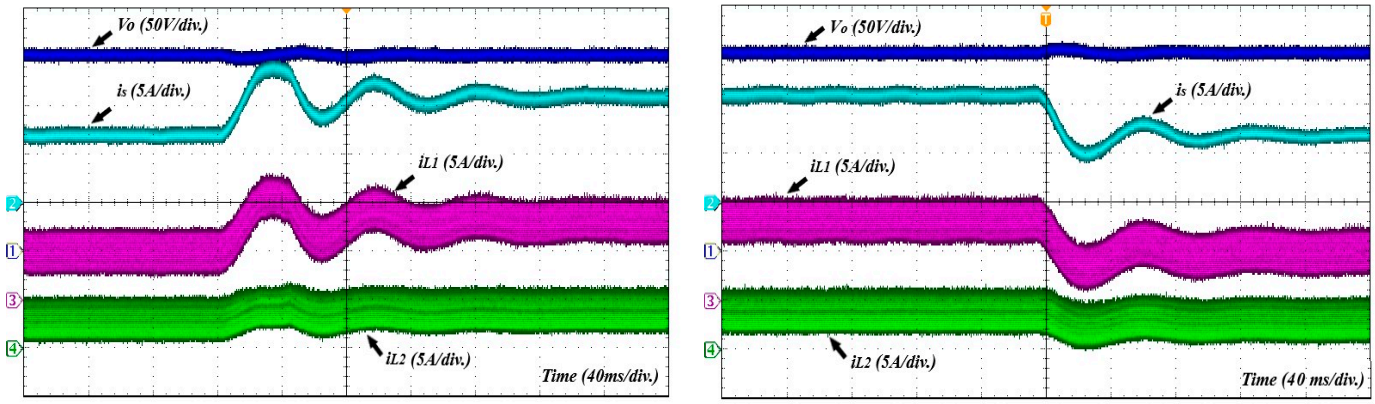


Figure 15. Open-loop waveforms. From top to bottom: output voltage V_o (blue trace), input current i_s (cyan trace), inductor current i_{L1} (magenta trace), and inductor current i_{L2} (green trace); test at $D = 0.6$.



(**a**) (**b**)

Figure 16. Transient response under load variation. From top to bottom: output voltage V_o (blue trace), input current i_s (cyan trace), inductor current i_{L1} (magenta trace), and inductor current i_{L2} (green trace): (**a**) from 60% to 100%; (**b**) from 100% to 60%.

Figure 17 shows the voltage regulation under the robust PI controller. This figure demonstrates the output voltage response when the input voltage changed from 24 V to 21 V. According to the voltage variation test, it can be concluded that the zero-ripple input current during the transient response was maintained.

Figure 18 shows the efficiency test of the proposed boost converter. In Figure 18a, with a constant load of 100 W, the efficiency was tested at different input voltages, which indicates that the higher the input voltage was, the higher the efficiency would be. In this test, the voltage gain was maintained at a constant value of 8. Additionally, a comparison of the measured efficiency with different output powers is depicted in Figure 18b. For this test, two input voltages and a 200 V nominal output voltage were applied. The efficiency values presented were all measured using the Chroma 62204 power meter.

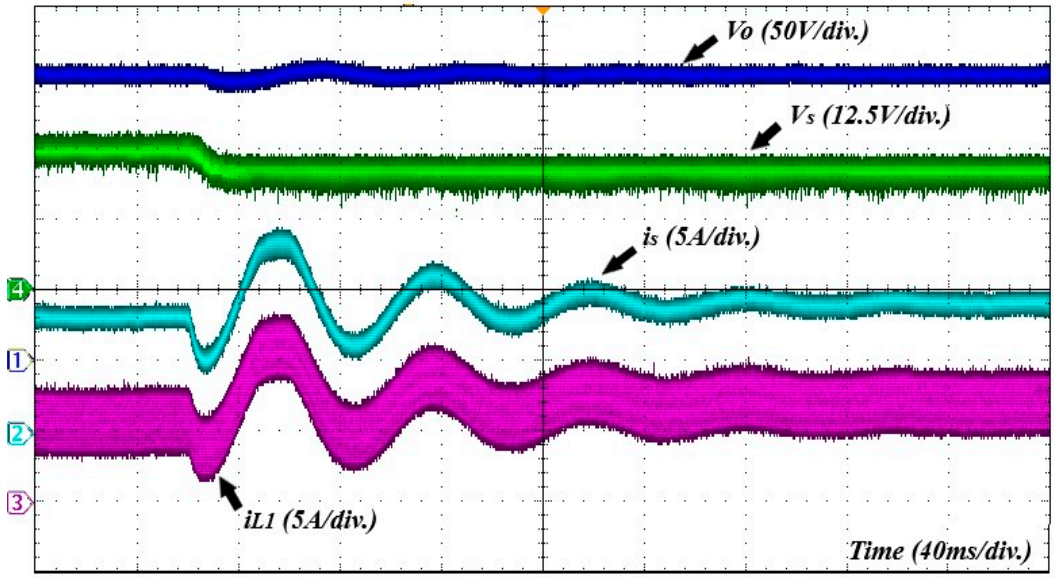


Figure 17. Transient response under input voltage change. From top to bottom: output voltage V_o (blue trace), input voltage V_s (green trace), input current i_s (cyan trace), and inductor current i_{L1} (magenta trace).

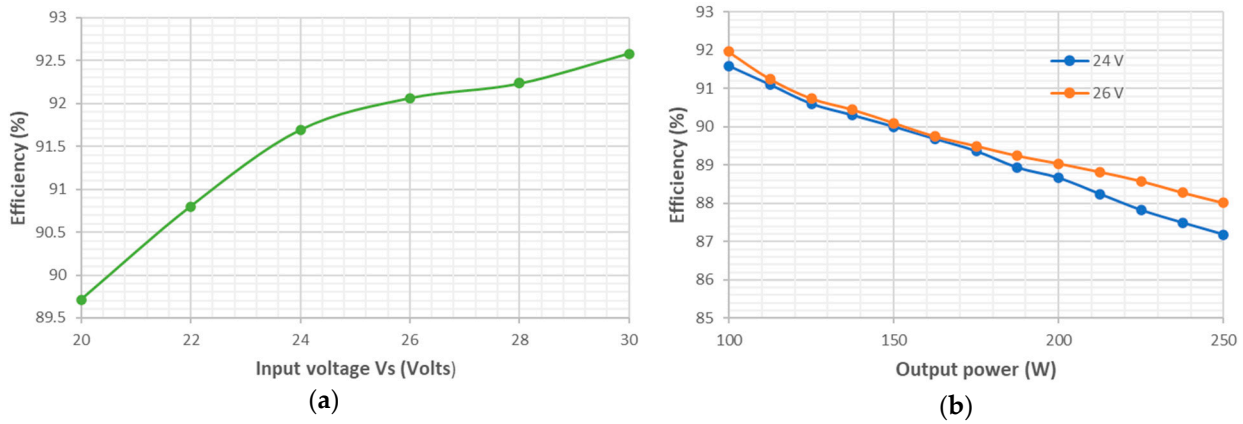


Figure 18. Efficiency test of the converter: (**a**) efficiency test for different input voltages; (**b**) efficiency test for different output loads.

Table 3 compares the proposed DC–DC boost converter with state-of-the-art topologies in terms of gain, the number of power components, ICR elimination, frequency, and efficiency. Considering that the current-source converter power consumption is low, the number of active devices of the proposed converter is similar to other converters. In addition, the proposed topology presents the least number of passive components.

Table 3. Comparison of different types of high voltage gain converters.

Converter	Gain	I	C	S	D	ICR	f	Maximum Efficiency
[1]	$\frac{1+3D-3D^2}{(1-D)^2}$	5	8	1	6	High	50 kHz	90%
[7]	$\frac{(1+D)}{(1-D)^2}$	3	4	1	4	High	100 kHz	88%
[15]	$\frac{1+D}{1-D}$	4	4	2	2	Zero	25 kHz	94%
[16]	$\frac{1}{1-D}$	3	4	6	9	Low	25 kHz	97%
Proposed	$\frac{2}{D(1-D)}$	2	4	3	5	Zero	40 kHz	92%

In [21], a similar converter had a worse performance when the PI controller was tuned using another approach. The proposed PI, which is based on H_∞, exhibited a settling time of 120 ms, whereas the adaptive PI controller in [22] had a settling time of 160 ms.

With this proposal, the input current ripple can be eliminated in a wide operating region in transitory and steady states. Voltage regulation can be attained with a simple control loop. However, a low efficiency at low voltage was obtained due to S_1 and d_1. The inductance, which could be varied, had a superimposed high-frequency ripple. This ripple was noticeable when the control current was zero, and the switching frequency increased.

6. Conclusions and Future Works

In this paper, a zero-ripple input current boost converter using a VI was introduced. The converter presents a high voltage gain and wide operating region with zero-ripple condition. The sizing of the components was introduced to minimize the impact of the volume of the circuit. Moreover, a dynamical model including the effect of switched capacitors in the multiplier cell was presented. All dynamical models were validated via simulation. To address the parameter variation and external perturbations, a robust PI controller was designed based on the H_∞ theory.

Experimental results revealed that a simple control loop should be employed to regulate the output voltage. The current ripple reduction capability occurs not only under the operating point for traditional two-phase interleaved converters but also in a duty cycle greater than 50%. The main feature of the proposed converter is that it has great potential to be used in renewable sources, where high voltage gain and lower current ripple are required.

In future research, it might be possible to study alternative methods to eliminate the high-frequency ripple superimposed in the VI. Additionally, a soft switching method can be included to increase global efficiency. Another type of VI or nonlinear inductor can also be explored as a case study. Additionally, the implementation of another control approach with the advantage of directly using the nonlinear model of the DC–DC converter should be explored.

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Nomenclature

A	Allowable steady-state error
$\mathbf{A}$	System matrix
$\boldsymbol{B}_1$	Input matrix for voltage gain transfer function
$\boldsymbol{B}_2$	Input matrix for audio susceptibility transfer function
$\boldsymbol{C}$	Output matrix
C	The capacitance of each capacitor in the voltage multiplier
D	Duty cycle
$\Delta(s)$	Unstructured uncertainty
ΔV_o	Voltage ripple of V_o
ESR	Equivalent series resistance
η	Current controller gain
$F_l(\cdot)$	Lower linear fractional transformation

$G_p(s)$	Uncertain plant
$G_u(s)$	Voltage gain transfer function
$G_v(s)$	Audio susceptibility transfer function
$h(\cdot)$	Output function
i_c	Control current
ICR	Input current ripple
$\boldsymbol{K}(s)$	Voltage controller
LFT	Linear fractional transformation
M	Ideal gain
M_p	Practical gain
$\boldsymbol{P}(s)$	Generalized plant
PI	Proportional–integral controller
u	Switching function
u_{av}	Average control input
$\widetilde{u}_{av}$	Linearized average control input
$\overline{u}_{av}$	Equilibrium average control input
VI	Variable inductor
w	Exogenous input
$\boldsymbol{x}$	State vector
$\widetilde{\boldsymbol{x}}$	Linearized state vector
$\overline{\boldsymbol{x}}$	Equilibrium point vector
y	System output
$\widetilde{y}$	Linearized output
z	Error signal vector

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