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Review

A Review on Multilevel Converters for Efficient Integration of Battery Systems in Stationary Applications

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Abstract: Recently, multilevel converters (MLCs) have gained significant attention for stationary applications, including static compensators, industrial drives, and utility-grid interfaces for renewable energy sources. Compared to two-level voltage-source inverters (VSI) MLCs feature high-quality AC voltage with reduced harmonic content despite the lower switching frequency of the semiconductor devices. On the DC side, MLCs can integrate multiple isolated/non-isolated battery modules instead of a single battery pack. This helps to keep the system in service in case of a malfunction of one or more battery modules, as well as active balancing among the modules, a feature not possible with two-level VSI. In general, MLCs can be classified into two types: (i) two-port MLCs, which provide a single interface to connect with the battery pack, and (ii) multiport MLCs, which provide multiple interfaces to allow connection at the module or cell level. The classical topologies of both MLC types (e.g., neutral point clamped, flying capacitor, cascaded bridge) face limitations due to the high switch count. Consequently, many hybrid and reduced-switch topologies are reported in the literature. This paper presents a critical overview of both classical and recently reported MLC topologies and offers a better insight of MLC operation for grid-connected and standalone applications. In addition, the analysis thoroughly assesses various high-level control and modulation strategies while considering active balancing among the battery modules. Other salient features such as balancing speed during offtake/grid-injection mode and fault-ride-through capability are also incorporated. In conclusion, the key findings are summarized for a better understanding of the present and future integration of battery systems in stationary applications.

Keywords: multi-level inverters; stationary battery systems; hot swapping; grid; battery-energy storage; active balancing; modulation strategies

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1. Introduction

In recent years, the deployment of battery-based energy-storage systems (BESSs) has been growing exponentially for stationary applications [1–5]. Being one of the core elements of an environmentally friendly and resource-efficient solution, BESSs have assumed the fundamental role of providing sustainable and high-standard energy sources. Grid-connected BESSs enhance grid reliability by stabilizing the power fluctuations caused by intermittent renewable-energy sources (RES), improving self-consumption and peak shaving for prosumers via a coordinated supply-and-demand time-shift [6,7]. In addition, BESSs provide ancillary services that include frequency-containment reserves (FCR), frequency-restoration reserves (FRR), imbalance mitigation, and replacement reserves [8–10]. In the off-grid mode, BESSs serve as the backbone of standalone power systems where there is no access to the utility grid.

Lithium-ion batteries (LiB) account for more than 80% of the installed capacity among different stationary BESS technologies due to their high energy and power density [11].

In a typical LIB BESS, multiple individual cells are first connected in series to make a module. The series connection adds up the individual cell voltages to the desired module-level open-circuit voltage (OCV). A typical module can have OCV in the range of 50–70 V [12]. The modules are then further connected in series and parallel combinations to form the complete battery pack. The parallel connections among the modules increase the usable capacity/energy of the pack, measured in kilowatt hours (kWh), whereas the number of parallel connections is a function of the use case [13–19]. For example, grid ancillary services (FCR, FRR) and prosumer use cases (self-consumption, arbitrage, peak shaving) require high-energy (HE) BESSs and therefore require a large number of parallel modules. On the contrary, decentralized generators require high-power (HP) BESSs to support the black-start capability. Unlike HE, the HP use case does not require many parallel connected modules [20].

The number of series connections impacts the pack OCV, which in turn depends on the number of stages in the PE interface. A single-stage PE interface consists of a single DC-AC inverter and therefore requires high DC-link voltage (>330 V for single-phase AC connection), as shown in Figure 1. This means that at least six modules (each 50–70 V) are required to be connected in series on the DC side. On the contrary, the two-stage PE interface does not apply any voltage restriction on the pack OCV, as there is an intermediate boost-conversion stage before the DC-AC inverter. However, due to the higher cost associated with two stages, a single-stage PE interface is preferred [21–24]. Therefore, this review paper considers the single-stage PE interface as a reference.

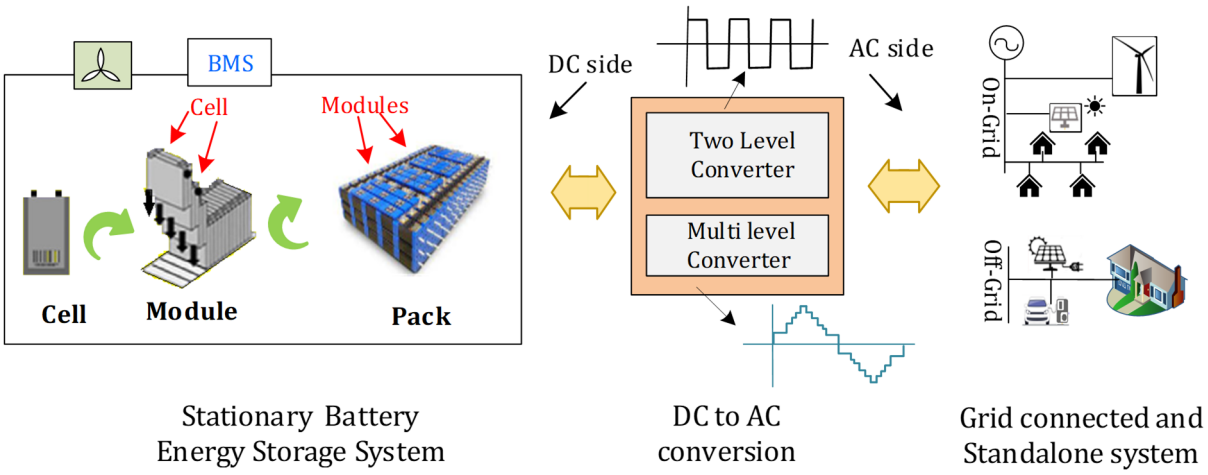


Figure 1. Schematic overview of stationary BESSs, power electronics converter, grid-connected system, and off-grid load.

Another important component of a stationary BESS is a battery-management system (BMS). The BMS continuously monitors the critical pack parameters, which include minimum and maximum cell voltage/current, temperature, and state of charge (SOC). It ensures that the BESS operates inside the safe operating area (SOA). A BMS also provides balancing functionality among the individual cells. The balancing circuit can be passive (switched resistor bank), which results in higher power dissipation, or active (switched capacitors and inductors), which results in high implementation costs [25–28].

Conventionally, a two-level voltage-source inverter (VSI) is used for a single-stage PE interface, as shown in Figure 1. The DC port of the two-level VSI is connected to the battery-pack terminals, whereas the AC port is connected to the grid via the filter inductor or directly to the standalone AC load. Due to fewer switches, the two-level VSI is simple in structure but faces multiple downsides.

Firstly, it faces a potential capacity reduction on the BESS side. As it requires a large number of series connections in the battery pack, the individual cells accumulate differences in SOC and reach the cut-off voltage earlier than other cells. This happens mainly due

to non-homogeneity and different internal impedances/self-discharge rates of individual cells. To avoid damages due to overheating or a deep state of discharge, the BMS must disconnect the whole battery pack.

Secondly, the two-level VSI operates at a higher switching frequency, which exposes the semiconductor switches and interfacing filter to high dv/dt. In the standalone mode where there is no filter inductor, the high dv/dt and small rise times create undesired effects, which include excessive voltage stress on windings, leakage currents, and increased EMI. Furthermore, if long cables are used to connect the drive, the rapid rise times can potentially cause the transmission-line effect, which can double the voltage applied to the drive terminals, as explained in [29].

Considering the downsides of two-level VSI, this review paper focuses on multi-level converters (MLCs) as a reliable BESS interface for on-grid and off-grid applications. MLCs were first introduced in 1975 by Baker and Lawrence as an improved alternative to a two-level VSI in high-power applications [30]. The output AC voltage of MLCs is a synthesized multi-step (greater than two) signal due to the switching of multiple semiconductor switches. The number of levels in the AC voltage is directly proportional to the number of switches. Compared to two-level VSIs, MLCs offer a higher degree of flexibility, as they can be connected at the pack, module, or individual cell level. They offer high-quality AC voltage, lower switching losses, lower voltage stress on semiconductor switches, and reduced filter size for grid connection [30–33]. Some drawbacks include the large number of semiconductor switches and associated gate-driver circuitry, which can lead to a high implementation cost [33].

An important feature of a BESS-fed MLC is the potential to perform active balancing among the battery modules, a feature not possible with a two-level VSI. Active balancing is an added value of the MLC system that eliminates the requirement of a separate BMS. It is an important performance parameter to consider in selecting an efficient MLC topology for stationary BESSs. However, in the MLC literature, no review articles are available that cover this aspect for stationary BESSs [34,35]. Most review articles dedicated to RES-fed MLCs are limited only to PV systems [34–38]. Other review articles have focused on grid-connected BESSs but do not consider the battery-balancing requirements [30–33].

The main contribution of this paper is to present a critical overview of the classical, hybrid, and reduced-switch MLC topologies for stationary BESSs. The topologies are analyzed based on different key performance indicators (KPIs), which include (i) switch/diode count, (ii) passive-component count, (iii) AC-mode support, (iv) active balancing, (v) modularity, (vi) dual-mode support (grid-connected to off-grid transition), (vii) switch utilization, (viii) fault ride through capability, and (ix) DC-microgrid support. In addition, an overview of the latest control and modulation techniques is also presented. The analysis takes into account the dual role of modulation technique for BESS-fed MLCs, which ensures that the operating principle of active balancing does not violate while also maintaining a good-quality AC voltage.

The paper is organized as follows. Section 2 presents and classifies various potential MLC topologies for stationary BESS. It also presents the active-balancing principle and the role of multiport MLCs for stationary BESSs. Section 3 presents the topological comparison based on the aforementioned nine KPIs. Section 4 explains different modulation strategies, and Section 5 presents the higher-level control strategies. A simulation study is conducted in Section 6 to compare various active-balancing modulation techniques. Finally, Section 7 concludes the paper by summarizing the key findings and directions for future research.

2. Topologies of MLC Systems for Stationary BESSs

For grid-connected systems, the main requirement for an independent stationary BESS is to balance the offtake and generation for a specific group of demand (loading) points.

This is normally done by equalizing the fluctuations in the electricity generation and demand by time-shifting the load requirement. For an off-grid system, maintaining an uninterrupted power supply (UPS) is the main requirement [39,40].

Figure 2 reflects the classification of MLCs for a stationary BESS. Depending upon the type, isolation, and arrangement of the battery pack/modules, MLC systems can be broadly classified into two categories: (i) two-port and (ii) multiport MLCs.

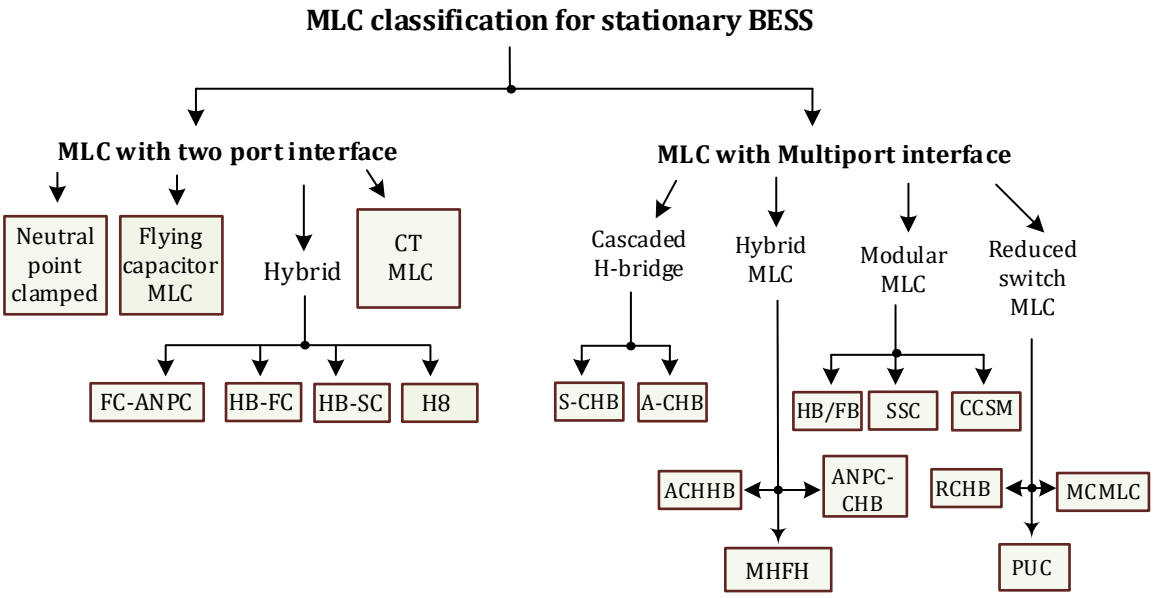


Figure 2. Categories of MLC configurations for stationary BESSs.

The two-port MLC provides a single interface and is connected to the whole battery pack, whereas multiport MLC provides multiple interfaces to connect several modules or individual cells. The two-port MLC does not provide balancing functionality but significantly decreases the THD in the AC voltage compared to a two-level VSI. It also allows a smaller interfacing filter for grid connections. The sub-section below briefly covers the underlying topologies for the two-port MLC system.

2.1. MLC with Two-Port Interface

Figure 3b–g reflect the potential configurations for a two-port MLC. Figure 3a depicts the grid-connected and off-grid AC interface to evaluate both modes of operation for each configuration in stationary applications.

2.1.1. Neutral-Point Diode Clamped (NPC)

In the NPC topology, the input DC voltage is divided into an even number of AC-voltage levels. For x levels in the AC voltage V_{Ac}, the NPC MLC consists of $2(x-2)$ clamping diodes, $(x-1)$ DC-link capacitors, and $2(x-1)$ semiconductor switches [41,42]. Figure 3b reflects the NPC MLC topology for five-level V_{Ac}. It has the advantage of bipolar DC bus operation but lacks modularity and balancing of the DC-link capacitors. In addition, it faces limitations due to uneven power losses and unequal blocking voltage across six diodes.

Another variant of the NPC topology is the active-NPC topology reported by ABB in [43]. It adds up the phase capacitor in a three-level NPC configuration to produce two additional voltage levels. Active-NPC topology finds widespread applications for industrial drives.

2.1.2. Flying-Capacitor MLC

In this topology, the MLC consists of $2(x-2)$ clamping diodes, $(x-1)$ DC-link capacitors, and $2(x-1)$ power electronics switches for single-phase x-level AC voltage [44–46]. Figure 2c depicts the single-phase flying-capacitor MLC topology for five-level V_{Ac}. The single-phase

flying-capacitor topology consists of four identical DC-link capacitors $C_1 - C_4$ of the same voltage rating for splitting the DC bus into four equal voltages.

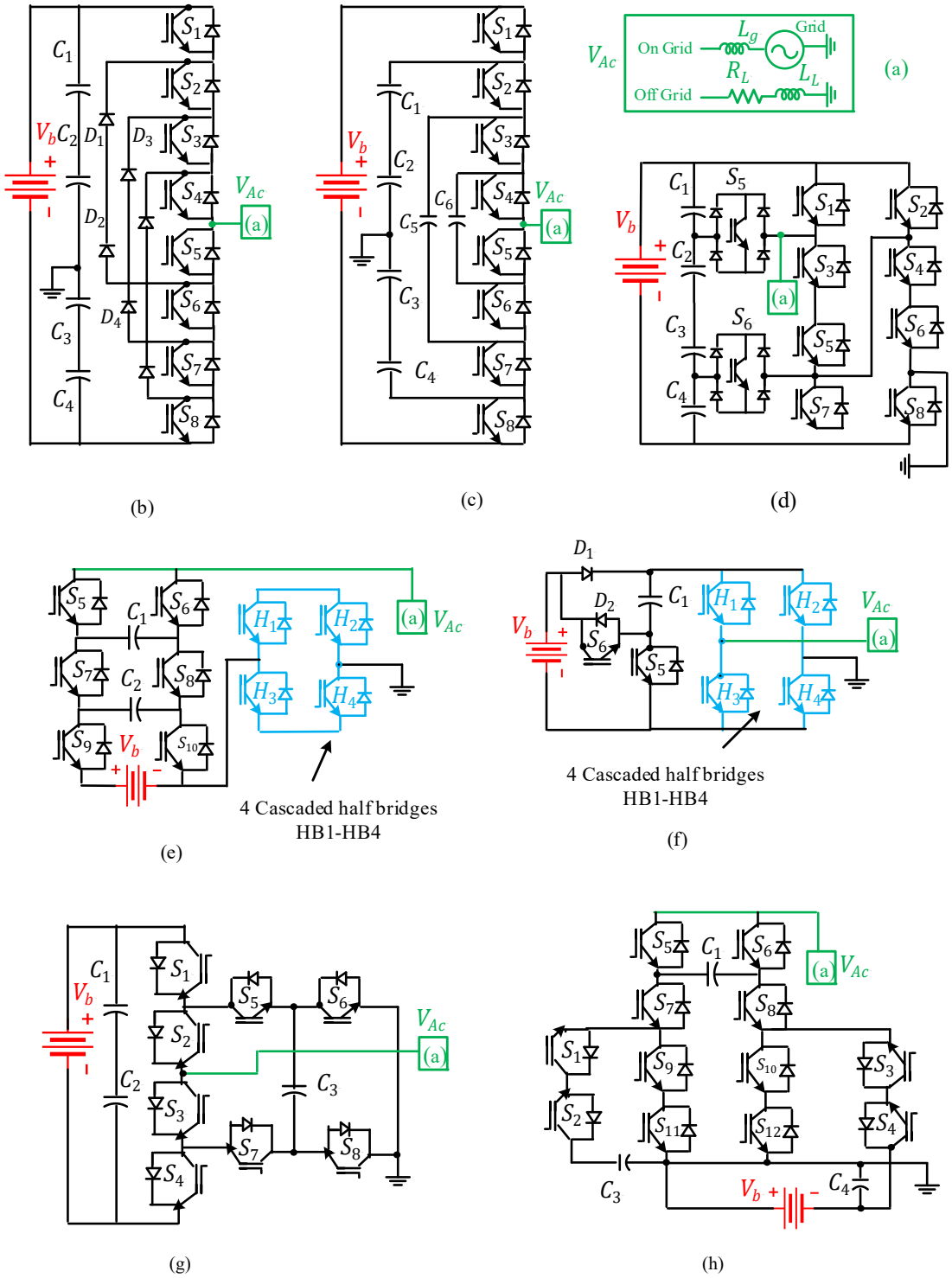


Figure 3. (**a**) Grid-connected and standalone load for MLC. Multiple configurations of the two-port MLC system fed by single/non-isolated BESSs. These include (**b**) NPC topology, (**c**) flying-capacitor topology, (**d**) cascaded-T configuration, (**e**) hybrid HB-FC topology, (**f**) hybrid SC-HB topology, (**g**) hybrid MLC (H8) topology, and (**h**) hybrid FC-ANPC topology.

This topology is similar to NPC topology, as is clear from the comparison of Figure 3b,c, except that there are no clamping diodes.

The flying-capacitor MLC features higher modularity compared to the NPC topology and offers better voltage-forming capability, higher frequency operation, and active and reactive power management. These features make the flying-capacitor MLC a better candidate for a standalone power supply. However, it faces high switching losses while transferring the active power from the DC to the AC side and requires a significant number of capacitors, which reduces its economic viability compared to the NPC MLC [45].

2.1.3. Cascaded-T MLC

As reported in [45,47] a cascaded-T MLC is a reduced-switch MLC topology where a single-phase grid-connected or standalone x-level output consists of $(x + 1)$ semiconductor switches, $(x + 3)$ clamping diodes, and $(x + 3)$ DC-link capacitors. Figure 3d depicts the cascaded-T MLC topology for nine-level output voltage.

2.1.4. Hybrid MLC

This combines two traditional MLC topologies to achieve higher voltage levels for the same number of switches. Ref. [48] reported the HB-FC topology, where four cascaded half bridges are combined with a seven-level flying capacitor MLC to achieve 15 voltage levels, as shown in Figure 3e.

In [49], the authors reported another hybrid MLC topology, where a combination of four cascaded half bridges and a three-level switched-capacitor (SC) converter generates nine levels, as reflected in Figure 3f. Figure 3g depicts another hybrid MLC (H8) topology, as reported in [48], where fewer switches achieve higher voltage levels than either of the parent topologies.

In [50], a combination of an active-NPC (ANPC) and a flying-capacitor MLC is reported, as shown in Figure 3h.

2.2. MLC with Multiport Interface

Multiport MLCs feature higher flexibility compared to two-port configurations, as they also allow connection at the module or individual cell level. Importantly, multiport MLCs can realize the terminal voltage or SOC balance between the battery cells or modules, and therefore do not suffer from capacity reduction due to the series connection among the cells [51–53].

If the MLC is connected at the cell level, the overall switch count becomes too high to be economically viable. As explained in Section 1, a 3.6 V LiB cell implies that more than 100 series-connected cells are needed per phase, which means that at least 400 semiconductor switches are required for single-phase grid connection. In the case of module-level implementation, fewer switches (less than 30) are needed, as each module is composed of multiple series-connected cells. The choice of cells per module is a non-technical constraint and is more based on the commercial availability of battery modules [54,55].

In this paper, 16 series-connected cells are considered in each module. Compared to a cell-level MLC, a module-level MLC faces a tradeoff, as the faulty cell cannot be isolated individually. However, it can be addressed by controlling the charging/discharging current of the module carrying the faulty cell. Moreover, each module still has a cell-level monitoring system (secondary BMS) to monitor the voltage/temperature of individual cells; however, it would not disconnect the faulty cell, as this feature is already supported by the module-level MLC.

2.2.1. Active Balancing with a Multiport MLC

The underlying building block for multiport MLCs is either a full-bridge (FB) or half-bridge (HB) structure that is interfaced with an isolated battery module [56,57]. Figure 4a,b reflect a single battery module with an HB and FB interface, respectively.

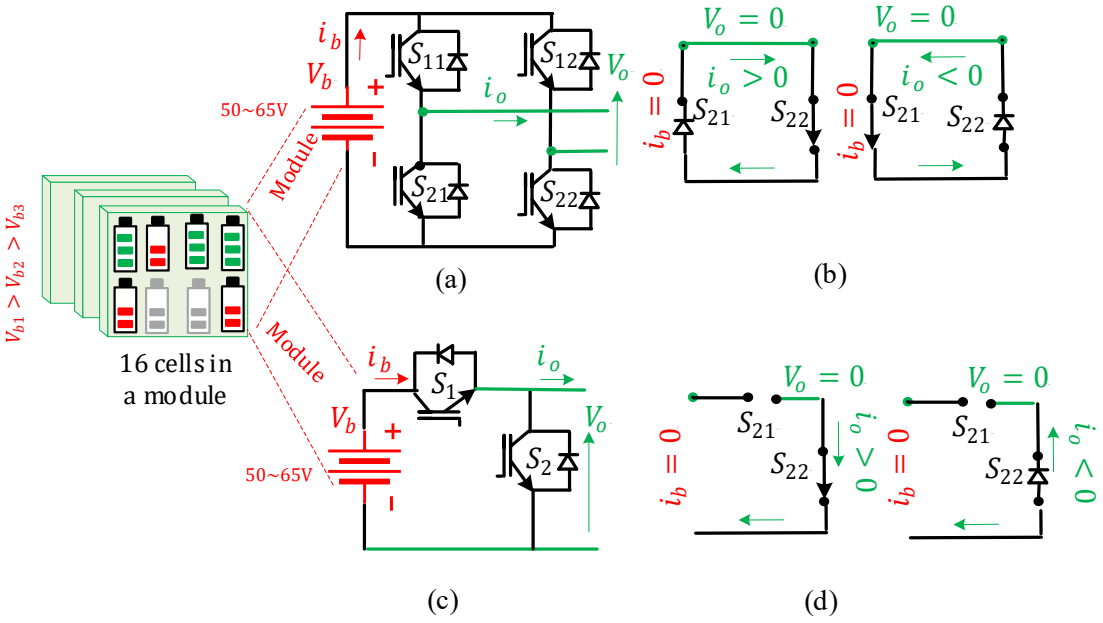


Figure 4. Operating modes of full-bridge and half-bridge interfaces with a single battery module: (**a**) generic full-bridge structure, (**b**) module-bypass state during discharging mode for full bridge, (**c**) generic half-bridge structure, and (**d**) module-bypass state during discharging state for half bridge.

Tables 1 and 2 show the operational modes of FB and HB interface as a function of various switching states, respectively [58].

Table 1. Operational modes of full-bridge interface as a function of switch states.

Mode	State Controller m_n	Output Voltage (V_o)	FB Switch State				Battery-Module State	Battery-Module Current (i_b)	Output Current (i_o)
			S_{11}	S_{12}	S_{11}	S_{22}			
1	1	$+V_B - 2V_d$	1	0	0	1	Charging	Negative	Negative
2	1	$+V_B - 2V_d$					Discharging	Positive	Positive
3	0	0	1	1	0	0	Bypassed	0	Positive
4	0	0	0	0	1	1	Bypassed	0	Negative
5	−1	$-V_B + 2V_d$	0	1	1	0	Charging	Positive	Positive
6	−1	$-V_B + 2V_d$					Discharging	Negative	Negative

Table 2. Operational modes of half-bridge interface as a function of switch states.

Mode	State Controller m_n	Output Voltage (V_o)	HB Switch State		Battery Module State	Battery Module Current (i_b)	Output Current (i_o)
			S_1	S_2			
1	1	$+V_B - V_d$	1	0	Charging	Negative	Negative
2	1	$+V_B - V_d$			Discharging	Positive	Positive
3	0	0	0	1	Bypassed	0	Positive
4	0	0	0	1	Bypassed	0	Negative
5	−1				NA		
6	−1						

Comparing Tables 1 and 2, it can be seen that the FB interface provides three output voltages, $+V_B$, 0, and $-V_B$, through different combinations of S_{11}, S_{12}, S_{21}, and S_{22}. On the other hand, HB can provide two output voltages, $+V_B$ and 0 V, through different combinations of S_1 and S_2.

The state transition is governed by the control parameter m_n, which can take values between -1 and 1. When $m_n = 0$, the output voltage $V_0 = 0$ and the battery module is bypassed from the MLC system, representing a no-charge/discharge state. The module current $i_b = 0$ but the output current (i_o) continues, which can be positive or negative.

Figure 4b,c show negative and positive output-current paths, respectively, for the FB and HB interface during the module-bypass state when $m_n = 0$ *and* $V_0 = 0$. When $m_n = 1$ or -1, V_o and the real power (P_o) of the FB and HB interface can be expressed as follows:

$$V_{o-FB} = V_b - 2V_d \tag{1}$$

$$P_{o-FB} = V_b \cdot i_{AC} \cdot m_n \quad \forall -1 \leq m_n \leq 1 \tag{2}$$

$$i_{o-FB} = \left\{ \begin{array}{ll} i_b & \text{if} \quad m_n = +1 \text{ or } -1 \; \forall \; V_0 \neq 0 \\ > 0 & \text{if} \quad m_n = 0 \; \forall \; V_0 = 0, i_b = 0 \\ < 0 & \text{if} \quad m_n = 0 \; \forall \; V_0 = 0, i_b = 0 \end{array} \right\} \tag{3}$$

$$V_{o-HB} = V_b - V_d \tag{4}$$

$$P_{o-HB} = V_b \cdot i_o \cdot m_n \quad \forall \; 0 \leq m_n \leq 1 \tag{5}$$

$$i_{o-HB} = \left\{ \begin{array}{ll} i_b & \text{if} \quad m_n = +1 \; \forall \; V_0 \neq 0 \\ > 0 & \text{if} \quad m_n = 0 \; \forall \; V_0 = 0, i_b = 0 \\ < 0 & \text{if} \quad m_n = 0 \; \forall \; V_0 = 0, i_b = 0 \end{array} \right\} \tag{6}$$

where V_d is the voltage drop across one switch during the ON state. V_d can be positive or negative based on the direction of i_o. Comparing Equations (1) and (4), it can be seen that FB has a voltage drop two times higher than that of HB. In addition, except for the bypass mode, the output current in both topologies is equal to i_b.

For $0 \leq m_n \leq 1$, the charged or discharged energy of each battery module depends on the period during which the module is connected to the circuit.

Comparing Tables 1 and 2, FB allows an extra mode (Mode 6), where $V_0 = -V_B + 2V_D$. This state allows the generation of negative voltage levels in the output. The HB interface does not have Mode-6; however, it does not impact the balancing potential, as cascaded HBs can operate at a higher frequency than FB.

The choice of m_n can be used for the voltage or SOC equalization among the modules. Since each module is controlled by a dedicated m_n, the switch-in and switch-out time of each module can be controlled independently. The module with higher voltage or SOC can be discharged for longer duration (more $-V_B$ intervals) or charged for a shorter duration (more 0 intervals). m_n can also improve the energy-utilization ratio while avoiding the overcharging or deep discharging of individual modules.

2.3. Subtypes of MLC with Multiport Interface

The subsections below highlight several potential multiport MLC topologies for connections at the module level.

2.3.1. Cascaded H-Bridge (CHB) MLC

CHB topology consists of multiple cascaded FBs and generates AC voltage by switching between several small DC voltage levels using low-frequency switching devices [59–61]. Due to the modular structure, it holds an advantage in fault-tolerant operation over FC and NPC topologies, as there are no clamping diodes, bulky inductors, or capacitors in a CHB configuration. Typically, CHB consists of several FBs (h) connected in series.

Each FB is fed by an isolated battery module. The output voltage V_{AC} and number of levels N_{levels} can be expressed as follows [61]:

$$V_{AC-max} = V_{b-max} \times h \tag{7}$$

$$N_{level} = 2h + 1 \tag{8}$$

where V_{AC-max} and V_{b-max} are the maximum values of output AC voltage and module DC-link voltage, respectively.

Figure 5 reflects a 13-level CHB MLC topology where six FBs are cascaded together. Each FB is connected to an individual battery module. The AC voltage has six levels (V_{b1} *to* $V_{b1} + V_{b2} \ldots + V_{b6}$) in both positive and negative half cycles.

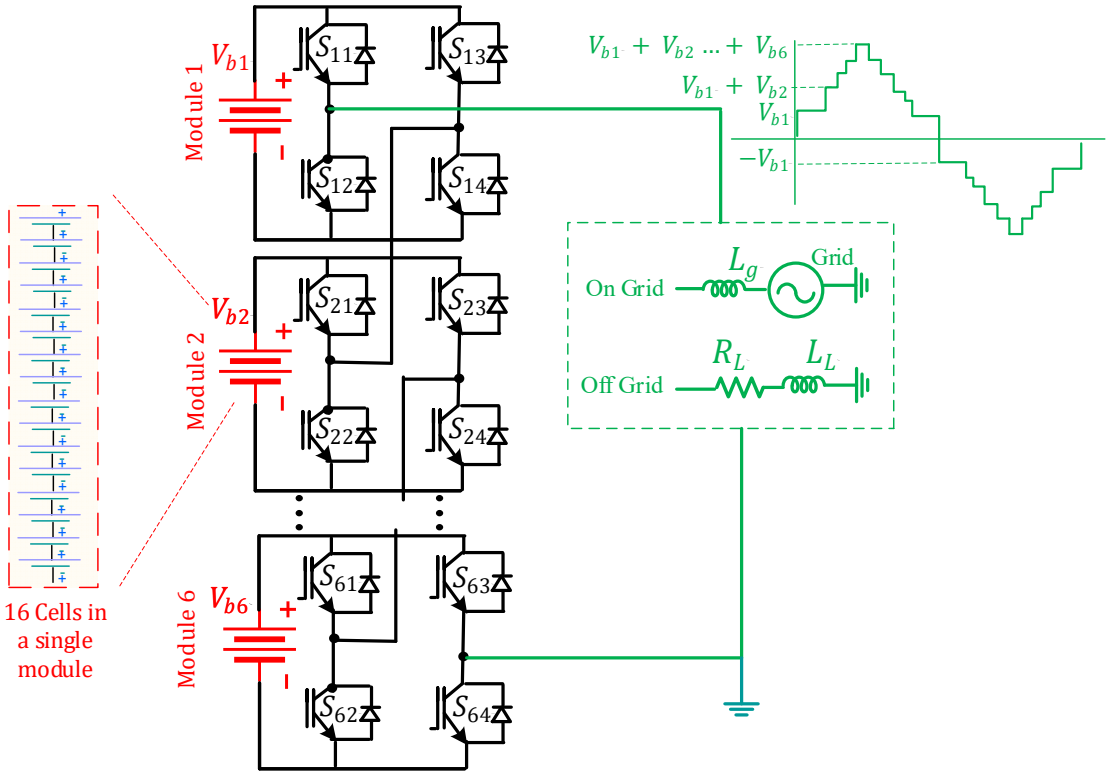


Figure 5. Schematic diagram of a multiport 13-level CHB system comprising six isolated battery modules.

CHB topology can operate at different modulation indexes for the FBs. This feature allows the CHB to perform active balancing, as it can maintain one module DC-link voltage at values independent of other modules. For a multiphase system, it can perform compensation of unbalanced phase currents.

Based on the voltage of the individual battery modules, CHB topology can be sub-classified into symmetrical (SCHB) [62,63] and asymmetrical (ACHB) configurations [64,65].

In S-CHB, all the DC voltages are equal. In terms of components, SCHB needs $2(N_{levels} - 1)$ switches and $(N_{levels} - 1)$/modules to generate N_{levels} in the AC voltage.

In the A-CHB, the DC voltages are kept different based on a geometric progression factor (GPF). The GPF commonly has a value of two or higher to generate more steps in the AC voltage without increasing the number of FBs. Accordingly, N_{levels} can be expressed as follows:

$$N_{level} = 2^{h+1} - 1 \quad \text{if} \quad V_k = 2^{k-1} V_b \; \forall \quad \text{k} \in [1, 2, 3, \ldots, h] \tag{9}$$

$$N_{level} = 3^h \quad \text{if} \quad V_k = 3^{j-1}V_b \; \forall \qquad \text{k} \in [1, 2, \ldots, h] \tag{10}$$

The maximum AC voltage of h FBs can be expressed as:

$$\left.\begin{array}{ll} V_{AC-max} = \left(2^h - 1\right)V_{b-max} & \text{if} \quad V_k = 2^{k-1}V_b \; \forall \quad \text{k} \in [1, 2, \ldots, h] \\ V_{AC-max} = \left(\frac{3^h-1}{2}\right)V_{b-max} & \text{if} \quad V_k = 3^{k-1}V_b \; \forall \quad \text{k} \in [1, 2, \ldots, h] \end{array}\right\} \tag{11}$$

Comparing Equations (6)–(11), it becomes clear that ACHB can generate more voltage levels and a higher amplitude of the AC voltage than SCHB with the same number of FBs. In the reference case, SCHB needs six modules to generate 13 levels with a peak AC voltage of 365 V, whereas AHCB can generate the same voltage with only three modules. However, there is a tradeoff, as ACHB is less modular and fault tolerant compared to S-CHB.

In the case of binary DC-link module voltages, ACHB yields only the additive voltage levels, whereas in trinary sequence selection of DC voltages, both additive and subtractive voltage combinations can be obtained. Another disadvantage is the requirement of modules with higher OCV, which means a large number of series-connected cells per module, thus increasing the balancing problems of the cells within the module.

2.3.2. Reduced-Switch MLC

Recently, many reduced-switch MLC configurations have been reported [35,36,38,66–76] to improve the number of levels and voltage harmonic profile without changing the component rating. Most of the configurations focus on MLCs interfaced with solar PV, where the reduction of switches allows only unidirectional power flow (PV panels to the AC side) and therefore do not support battery-module integration [35,36,38]. Likewise, many topologies do not allow the individual modules to be bypassed or re-ordered in the voltage-building process and therefore do not support the module-balancing feature [35]. The subsections below cover only reduced-switch topologies that are bidirectional and can perform the primary balancing among the isolated battery modules.

Reduced Cascaded Half-Bridge MLC

The reduced cascaded half-bridge (RCHB) MLC consists of one FB and multiple HBs connected in series. It is reported in [77] as an improvement over CHB-MLC because it requires a lower number of semiconductor switches to generate the same levels in AC voltage.

Figure 6 reflects the single-phase configuration of a 13-level RCHB-MLC where each HB is connected to an isolated battery module. The output of these cascaded HBs is connected to an intermediate DC bus. The DC bus exhibits a staircase-shaped periodic-voltage waveform at twice the frequency of the AC voltage. The DC bus is connected to an FB that simply inverts the DC voltage to generate the AC waveform. The FB uses low-frequency semiconductor switches that operate at the base frequency (50/60 Hz) of the fundamental AC voltage.

In RHCB topology, different battery modules can be involved or bypassed in the voltage-building process, as each HB can be controlled independently, thus achieving the primary module-balancing feature. Based on the variation in OCV of different modules (all the same, binary relation or other), the total number of levels ($N_{level-HCHB}$) and maximum valued of the AC voltage ($V_{AC-HCHB-max}$) can be expressed as follows:

$$N_{level-HCHB} = \left\{\begin{array}{lll} n+1 & \text{if} \quad V_{bk} = V_{DC} \; \forall & \text{k} \in [1, 2, 3, \ldots, n] \\ 2^n & \text{if} \quad V_{bk} = 2^{k-1}V_{DC} \; \forall & \text{k} \in [1, 2, 3, \ldots, m] \\ 2n & \text{if} \quad V_{bk} = 2V_{DC} \; \forall & \text{k} \in [1, 2, 3, \ldots, n] \end{array}\right\} \tag{12}$$

$$V_{AC-HCHB-max} = \left\{ \begin{array}{cc} n \times V_{DC} & \text{if} \quad V_{bk} = V_{DC} \; \forall \quad \text{k} \in [1,2,3,\ldots,n] \\ (2^n - 1)V_{DC} & \text{if} \quad V_{bk} = 2^{k-1}V_{DC} \; \forall \quad \text{k} \in [1,2,3,\ldots,m] \\ (2n-1)V_{DC} & \text{if} \quad V_{bk} = 2V_{DC} \; \forall \quad \text{k} \in [1,2,3,\ldots,n] \end{array} \right\} \tag{13}$$

where n is the number of cascaded HBs per phase.

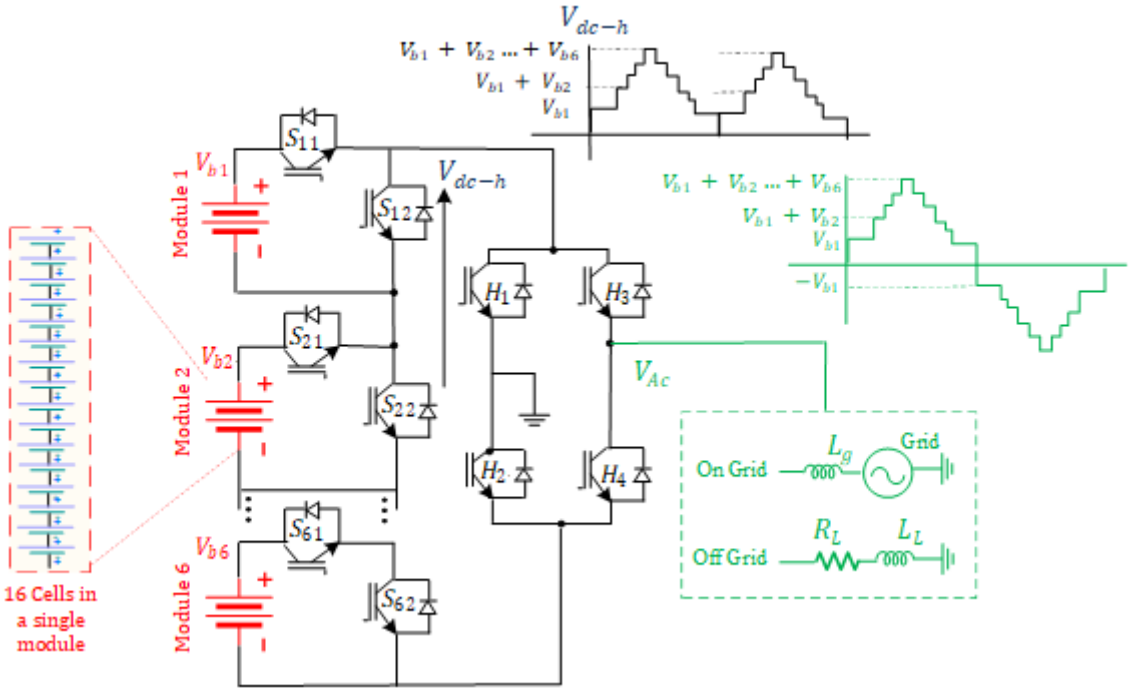


Figure 6. Schematic diagram of multiport 13-level RCHB topology comprising six isolated battery modules.

Comparing Figures 5 and 6, RHCB topology requires two switches per module, whereas CHB topology needs four switches per module to produce the same number of levels in the AC voltage. The total number of switches for both topologies can be expressed as follows [77]:

$$\left. \begin{array}{c} N_{sw-CHB} = 4 \times Modules \\ N_{sw-RHCB} = 2 \times Modules + 4 \end{array} \right\} \tag{14}$$

This means that for a six-module MLC, $N_{sw-CHB} = 24$ and $N_{sw-HCHB} = 16$. The difference becomes larger as the module count increases.

The output of cascaded HBs is the multistep half-sinusoidal-shape DC voltage (V_{DC-h}) with a frequency two times higher than that of the AC voltage, as shown in Figure 6. The final FB converts V_{DC-h} to sinusoidal AC voltage by simply reversing the polarity of alternate cycles.

Despite the switch-count reduction, the RHCB topology faces a critical limitation in grid-connected mode that is not reported in [72,77] or in the available literature on the cascaded HB MLC [69,74]. The limitation is explained as follows.

RHCB uses the front-end FB for polarity generation, which means FB is essentially uncontrolled from the current-control perspective. The switches in FB are synchronously turned on and off at the zero crossings of the AC voltage and therefore lack the ability to inject current in the grid-connected mode.

The synchronous switching allows FB to operate in voltage-control mode, which is possible for standalone/off-grid applications, as explained in [72,77]. However, in the case of grid connection, the RCHB cannot inject power, as active and reactive currents of the

interfacing inductor (L_g) cannot be controlled with synchronous (50 Hz) switching of the semiconductor switches in FB. However, in the offtake mode it draws uncontrolled current, as the FB simply behaves like a diode rectifier due to synchronous switching.

Another option to perform indirect current control via cascaded HBs is also possible but adds high THD in the DC bus voltage V_{DC-h} since each HB operates as an independent DC-DC (synchronous buck) converter. The resulting voltage level in the intermediate DC bus needs a certain settling time before the next level can be added. For a grid-following operation, all six levels must be completed in half-cycle time ($\leq$10 ms). This means that the settling time should be less than 1.6 ms per level for six HBs. Such a requirement creates an underdamped response with high overshoot in each level of V_{DC-h}. As a result, the THD in the AC voltage exceeds the allowable limit by the grid codes.

Modified Cascaded MLC

A modified cascaded MLC (MCMLC) is reported in [66] that allows a wide operating range, smaller THD, and higher efficiency for grid-connected mode. Figure 7a reflects the schematic of MCMLC. In this configuration, there is an auxiliary bidirectional switch S_{aux-1} between two cascaded FBs. The auxiliary switch allows the modules to be connected in both series and parallel configuration. When S_{aux-1} is turned off/bypassed, MCMLC functions as a normal CHB (as in Figure 5) connecting the modules via FBs (cascaded mode). When S_{aux-1} is turned on, the two modules are connected in parallel (HB mode), sharing the same negative DC bus. The parallel connection allows the higher current injection into the grid using the same switches.

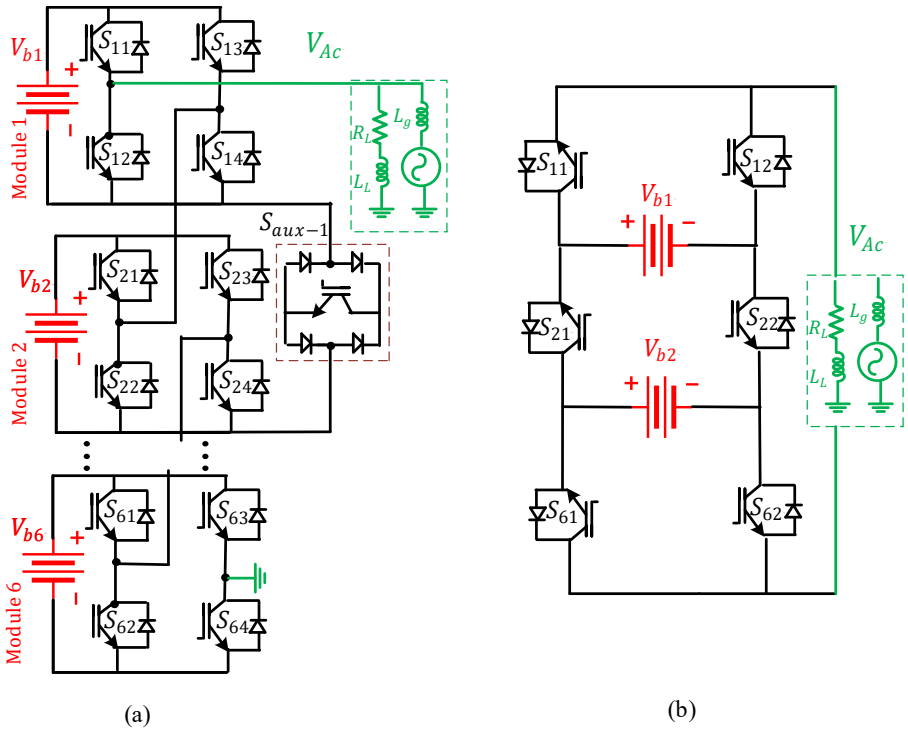


Figure 7. Schematic diagram of reduced-switch MLC for (**a**) modified cascaded CHB and (**b**) packed U-cell configuration.

Despite a wide operational range, the MCMLC configuration has a few downsides. Firstly, the transformation between cascaded and HB mode requires the interruption of the inductor current, which can lead to voltage spikes across the semiconductor switches. To avoid these spikes, the mode transition must be done at zero-crossing points of the reference-modulating signal (zero voltage, zero current), which is only possible if the

voltage and current are in-phase. This means that the MCMLC cannot control the reactive power and must operate at a unity power factor.

Secondly, the zero-voltage–zero-current transition cannot be achieved in a standalone system for stationary applications, as the loads are mostly inductive/nonlinear. As a consequence, the MCMLC can only function either in CHB or HB mode for off-grid applications.

Packed U-Cell MLC

The packed U-cell (PUC) topology is proposed in [75,76] as a reduced-component alternative to the CHB, NPC, and FC configurations. It consists of six semiconductor switches and two isolated battery modules, as shown in Figure 7b. A PUC MLC generates seven-level AC voltage using six switches. The upper switches, S_{11} and S_{12}, operate at the fundamental frequency of the AC voltage. The lower four switches operate at a relatively higher frequency and lower harmonics, thus reducing the switching losses of the PUC MLC. The left set of switches (S_{11}, S_{12}, S_{61}) operates in a manner complementary to the right set of switches (S_{12}, S_{22}, S_{62}).

The PUC topology is capable of operating in both grid-connected and standalone applications [51]. It can provide an uninterrupted power supply (UPS) for a wide range of changes in the load and module voltage. However, a major limitation of PUC topology is the voltage dependency of both modules. The OCV for module−2 (V_{b2}) needs to be regulated at one-third of the magnitude of V_{b1}. Such restrictions reduce the modularity of a PUC MLC.

2.3.3. Modular MLC

The generic implementation of a single-phase modular MLC (MMLC) comprises an AC port, a DC port, and the converting structure, consisting of two identical arms that are connected via two uncoupled inductors. Each arm consists of N submodules (SMs). Each SM constitutes the fundamental building block of the MMLC. The number of SMs per arm indicates the levels in the output AC voltage. Figure 8a reflects the single-phase MMLC schematic for the reference case with six battery modules. As shown in Figure 8a, there are six SMs. Each SM is interfaced with a single-battery module.

In the literature, numerous configurations are reported for SMs [4,78–82]. Two of the most well-known topologies that are widely used in MMLCs are HB and FB configurations [4]. As shown in Figure 8c, HB is relatively simple and cost effective but faces many limitations. It cannot stop the DC fault current in the converting structure. Due to its four switches, it can only produce two voltage levels: V_{b} with S_1 ON, S_2 OFF and 0 with S_1 OFF, S_2 ON. This means that the SMs can only be bypassed in the case of a short circuit but cannot stop the DC fault current. The FB configuration shown in Figure 8b can counter this issue, as it generates three levels: V_{b}, 0, and $-V_{\mathrm{b}}$. Due to an extra level, $-V_{\mathrm{b}}$, FB can offer high impedance and effectively block the DC fault current.

Besides HB and FB topologies, SMs can also use many configurations from a family of two-port or multiport MLC topologies, as reflected in Figure 2. Consequently, SMs will feature the same pros and cons associated with these topologies, as reported in [78].

Recently, [4] reported a compact, low-volume SM topology that uses stacked switched capacitors (SSC) acting as an energy-storage buffer. Figure 8d reflects the SSC configuration, where C_1 and C_2 make the energy buffer in conjunction with the battery module V_{b}. Compared to the HB SM configuration, it can decrease the total volume of SM by more than 40%.

To increase the levels in the SM voltage, cross-connected (CS) SM topology is reported in [83]. Figure 8e reflects the CSSM configuration, where two switches are used to connect back-to-back half-bridge SMs. This configuration has the advantage, as it tolerates the DC fault current by turning off the crossed switches.

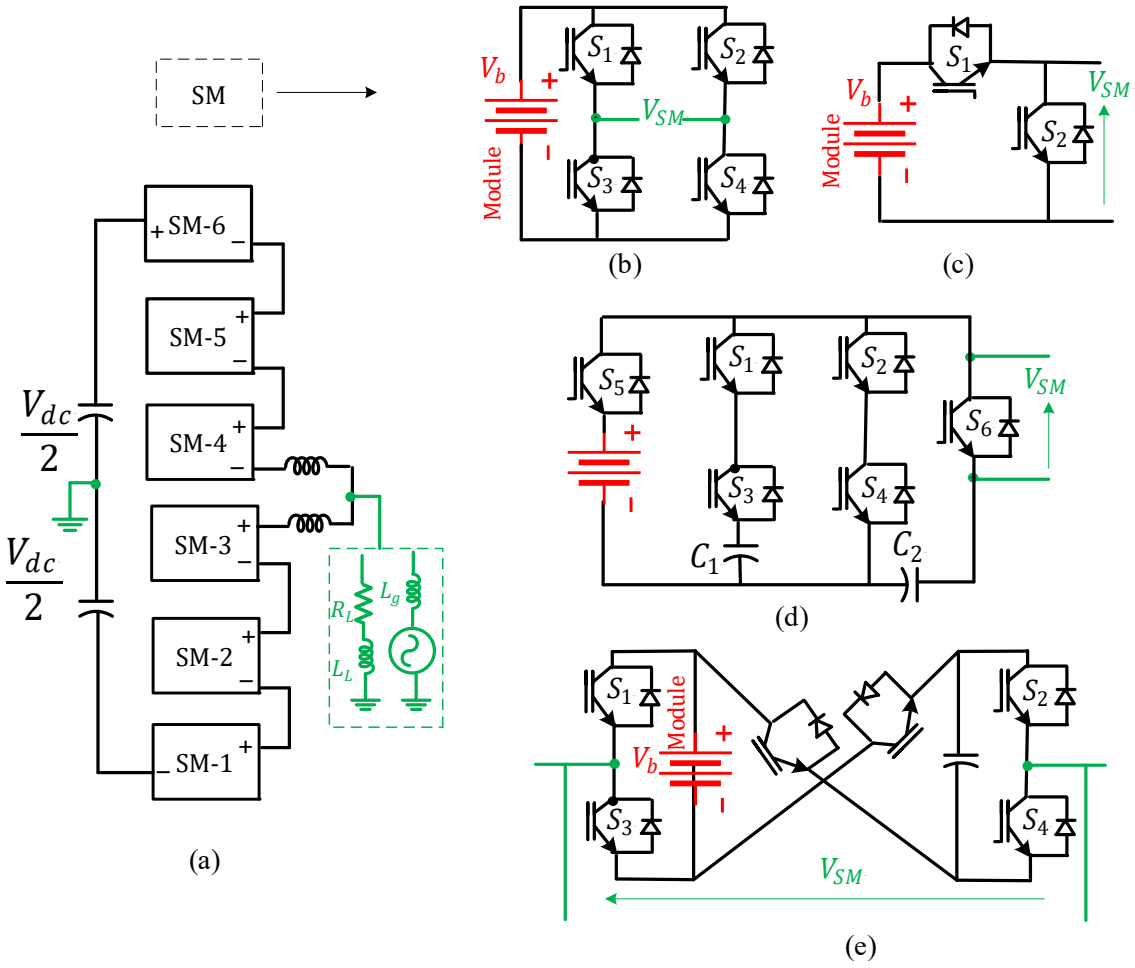


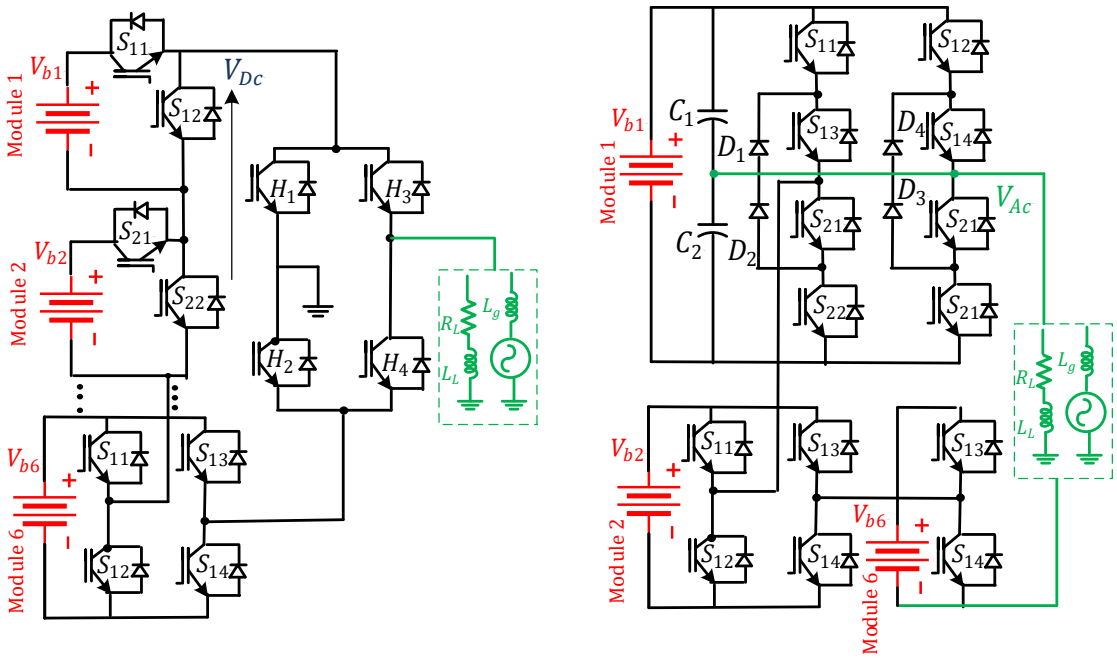
Figure 8. (**a**) Schematic diagram of a modular MLC in a single-phase system. Various configuration of SM, including (**b**) FB, (**c**) HB, (**d**) stacked switched capacitors, and (**e**) cross-connected SM configuration.

Similarly, switched-capacitor (SC) SMs and composite three-level SMs (CSMs) are reported in [84,85], respectively. The SCSM can ride through a DC-link short circuit by turning off all the active switches, whereas the CSM can address the DC fault current together with unbalanced charging of the switched capacitors.

2.3.4. Hybrid MLC

Researchers have proposed the concept of hybrid MLC to combine two or more MLC topologies to achieve higher voltage levels. However, not all the hybrid topologies in the literature [86,87] are relevant for battery-module integration due to the constraint of bidirectional power flow and module-balancing requirements, as explained in Section 2.2.1. This includes the hybrid topology, where the NPC and FC are merged through a coupled inductor [87] and the nine-level T-Type NPC and FCH-bridge configurations reported in [86].

An interesting asymmetric cascaded hybrid MLC configuration (ACHHB) is introduced in [88], where several HBs are cascaded with one FB, as shown in Figure 9a. The DC-link voltage of HBs can be kept equal or follow a binary sequence, keeping the DC source of FB constant. ACHHB can generate up to 13 levels with five HBs and one FB unit, compared to the six FB units required for CHB topology, and considerably improves THD in the output voltage. If the DC voltage of HB units vary in binary or trinary fashion, the number of levels in AC voltage can be much higher [88].



(a) (b)

Figure 9. Schematic diagram of a hybrid MLC for (**a**) asymmetric cascaded configuration and (**b**) ANPC-CHB configuration.

Figure 9b depicts a hybrid ANPC structure with CHB topology. The purpose of introducing CHB units is to increase the number of levels without any variation in overall power. The CHB units act as active power filters to enhance the quality of the AC voltage. Similar to [88], another modular half- and full-bridge hybrid (MHFH) topology is reported in [89], which offers extra levels and can be extended in a cascaded manner. However, due to the presence of two unidirectional switches, this topology cannot charge all the modules simultaneously.

3. Topological Comparison

Table 3 presents a summary of the reviewed two-port and multiport MLC topologies for stationary BESSs. The type of topology and the reporting publication are included for better understanding. For multiport MLCs, the base case of six modules is considered as a reference for each topology. Based on the active-balancing principle in Section 2.2.1, seven state-of-the-art multiport MLC topologies that can perform active balancing among the battery modules were shortlisted. These topologies include (i) symmetric CHB [62,63], (ii) asymmetric CHB [64,65,67,88], (iii) RCHB [35,36,38,66–76], (iv) MCMLC [4,79,85], (v) HB/FB MLC [81], and (vi) ACHHB [90]. The passive-element count in Table 3 also includes the filter inductor for a grid interface.

Table 3. Comparison of core technical features among various MLC topologies.

Topology	Class	Ref	Structure	Switch (Diode) Count	Passive Element (Count)	AC Mode	Active Balancing	AC Levels	Merits/Demerits
NPC	MLC with two port interface	[41–43]	Traditional	8(6)	C(4) L(1)	*G", *O	NA	5	Bipolar DC-bus compatible/uneven switch utilization, lacks isolation
Flying capacitor		[46]	Traditional	8(0)	C(6) L(1)	*G", *O	NA	5	Better standalone and high frequency operation/high implementation cost

Table 3. *Cont.*

Topology	Class	Ref	Structure	Switch (Diode) Count	Passive Element (Count)	AC Mode	Active Balancing	AC Levels	Merits/Demerits
CT-MLC	MLC with two port interface	[45,47]	Traditional	10/8	C(4) L(1)	*G, *O	NA	9	More levels, better fault tolerance/high switch count
HBFC		[48]	Hybrid	14/14	C(2) L(1)	*G″, *O	NA	13	Higher levels, modular/unidirectional
SC-HB		[48]	Hybrid	10/11	C(1) L(1)	*G″	NA	13	Higher levels, modular, unidirectional
G- MLC		[48]	Hybrid	8/8	C(3) L(1)	*G″, *O	NA	11	Scalable, high-power density
FC-ANPC		[49]	Hybrid	12/12	C(4) L(1)	″G″	NA	11	Higher levels/unidirectional
Symmetric CHB	MLC with multi-port interface	[62,63]	Cascaded H bridge	24/24	L(1)	*G″, *O	Module level	13	Higher efficiency, low THD, faster module balancing, supports redundant operation
Asymmetric CHB		[65,67,88]	Cascaded H bridge	24/24	L(1)	*G″, *O	module voltage restriction	>30	Higher levels in AC voltage/large number of cells in module. Uneven steps in the AC voltage.
RCHB		[36,38,66–76]	Reduced Switch	16/16	C(1) L(1)	*O	Module level	13	Higher efficiency, Low THD, modulation limitation, grid-connected mode not possible
MCMLC		[4,79,85]	Reduced Switch	13/17	L(1)	*G″, *O	Module level	13	Wide operational range/voltage spikes on mode transition
PUCMLC		[74]	Reduced Switch	6/6	C(1) L(1)	*G″, *O	NA	7	Modular/voltage dependency of battery modules
HB/FB		[4]	Modular MLC	12/12	C(2) L(3)	*G″, *O	Module level	13	Modular/fault-current blocking limitation for HB
SSC		[84]	Modular MLC	30/30	C(12) L(3)	*G″, *O	Module level	13	Low volume /high switch account
CCSM		[83]	Modular MLC	12/12	C(1) L(1)	*G″, *O	NA	13	Modular/voltage dependency of battery modules
ACHHB		[87]	Hybrid	18/18	C(1) L(1)	*G″, *O	Module level	13	Higher efficiency, low THD, grid mode not possible
ANPC-CHB		[87]	Hybrid	18/20	C(3) L(1)	*G″, *O	NA	13	Low volume/high switch account
MHFH		[87]	Hybrid	12/12	C(3) L(1)	*G″, *O	NA	13	Low volume/high switch account

*G″ (only grid injection possible), *G (gird bidirectional), *O (Off grid).

It can be seen that except for PUCMLC, all multiport MLC topologies can generate 13 levels in the AC voltage. Another exception is the asymmetric-CHB topology, which can generate more than 30 levels due to the asymmetric-voltage profile of the battery modules. However, this large number of levels in AC voltage remains uneven and the resulting THD in the fundamental AC voltage is higher than the limit permitted by the grid codes.

Table 4 highlights the comparative summary of seven multiport MLC topologies reported in [4,35,36,38,62–76,79,81,85,88,90] for different applications. The topologies are divided into three performance categories.

(i) Appropriate with no operational limitation;
(ii) Possible but not efficient due to high switch count, lack of modularity, or high THD in the AC voltage;
(iii) Not suitable at all due to functional limitations.

Table 4. Comparative summary of cascaded MLC topologies, based on [4,35,36,38,62–76,79,81,85,88,90].

Topology Feature	*Symmetric CHB* [62,63]	*Asymmetric CHB* [64,65,67,88]	*RCHB* [41]	*MCMLC* [35,36,38,66–76]	*HB/FB MLC* [4,79,81,85]	*ACHHB* [90]
Grid offtake	🟢	🟢	🟡	🟢	🟢	🟡
Grid injection	🟢	🟢	🔴	🟡	🟡	🔴
Frequency balancing	🟢	🟡	🔴	🟡	🟡	🔴
Standalone (UPS mode)	🟡	🟡	🟢	🟡	🟡	🟡
Scalability	🟢	🟡	🟢	🟢	🟢	🟡
Reliability	🟢	🟢	🟡	🟢	🟢	🟡
Battery fault tolerance	🟢	🟡	🟢	🟢	🟢	🟢
(Dual on-grid and off-grid	🟡	🟡	🔴	🟡	🟡	🔴
Footprint (No: of components)	🟢	🟡	🟢	🟡	🟡	🟢
AC-fault ride-through	🟢	🟡	🔴	🟢	🟢	🔴
Enhancing power quality	🟢	🟢	🔴	🟢	🟢	🔴
Black start	🟢	🟢	🟡	🟢	🟢	🟡
Voltage support	🟢	🟢	🔴	🟢	🟢	🔴
Hot swapping	🟢	🟡	🟢	🟡	🟢	🟢
Capacity extension	🟢	🟡	🟢	🟡	🟢	🟡
Different chemistry integration	🟢	🟢	🟢	🟡	🟢	🟡
DC microgrid support	🔴	🔴	🟢	🟡	🟢	🟡

🟢 Appropriate topology 🟡 Possible but not efficient 🔴 Not suitable topology

The subsection below highlights the merits and demerits of each topology for grid-connected and off-grid systems.

3.1. Off-Grid/Standalone Operation

Comparing all potential topologies from (i) to (vi), it is clear that the RCHB topology holds the advantage due to having the lowest number of semiconductor switches (16) and passive components (1). It can control the discharging of various battery modules independently, reach any number of cascaded HBs/voltage levels, and allow redundant operation. In addition, RHCB has good fault tolerance, as it can bypass the faulty module without affecting the performance of running modules, thus considerably improving the

reliability of the system. Another feature of RCHB and ACHHB topologies is the DC microgrid support. The intermediate multistep DC link can be used to feed an independent load or a DC microgrid.

3.2. On-Grid Operation

Unlike off-grid mode, RHCB lacks the current-control mode due to the synchronous operation of the front-end FB. As a result, it can only offtake power (uncontrolled and non-sinusoidal current) from the grid but cannot inject the power into the grid. The modular MLC topologies (MCMLC, HB, FB) can perform both offtake and injection but suffer from high passive-component counts, as they require two inductors in each arm.

ACHHB works on the same operating principle as RHCB and therefore lacks the ability to inject power into the grid.

SCHB [62,63] and ACHB [64,65,67,88] can perform both offtake and injection with no operational limitation. However, ACHB entails a large string of cells in each module (>30), which leads to large and uneven steps in the AC voltage, ultimately resulting in high THD exceeding the grid codes.

Both SCHB and ACHB topologies hold the advantage of grid-connected applications, including AC-fault ride-through, power quality, and frequency balancing, but are not the best candidates for the standalone system due to their large footprint (i.e., high switch count). However, unlike RHCB, such limitations do not impede the functional ability of SCHB/ACHB to feed a standalone load. On the other hand, the reduced-switch topologies RHCB [35,36,38,66–76] and ACHHB [90] are optimally appropriate for standalone systems but face absolute limitations when it comes to the grid injection.

In a nutshell, it can be deduced that there is no single universal topology that can be considered optimal for both grid-connected and standalone operation; however, SCHB [62,63] can perform reasonably well for dual mode of operation.

4. Modulation Strategies of Multiport MLCs

4.1. Basic Principle

The primary role of an MLC modulation strategy is to enhance the output voltage quality so that it stays close to a pure sinusoidal waveform, as explained in [36,91–96]. For three-phase systems, there can be a circulating current among the legs of an MLC, which needs to be suppressed by the modulation strategy [36]. The switching frequency of the semiconductor switches should be minimized to reduce the switching losses [97,98]. Additional requirements from the distribution system operator (DSO) mandate a grid-connected MLC to comply with the grid codes [99,100]. These requirements include injecting pure sinusoidal current at unity power factor, active and reactive power control, DC-current suppression, total harmonic distortion in current below 5% during grid-injection mode, and fault-ride-through capability for various grid faults and defects in the battery modules.

The modulation technique needs to ensure that the operating principle of active balancing is not violated while also maintaining good-quality AC voltage. This means the injection angle needs to be updated during zero transition of the AC voltage.

Figure 10 depicts the overview of the potential modulation techniques for a multiport MLC in compliance with active balancing among the battery modules.

4.2. Classification of Modulation Strategies

The modulation strategies can be broadly classified into fixed- and variable-frequency modulation, as reported in [36]. The fixed-frequency modulation can be further divided into multicarrier- and fundamental-frequency modulation. Multicarrier PWM is subdivided into level-shifted carrier (LSC)- and phase-shifted carrier (PSC)-based PWM methods, whereas in fundamental-frequency modulation, the underlying methods include selective harmonic elimination (SHE)-, nearest-level control (NLC)-, and optimized control angle (OCA)-based PWM schemes.

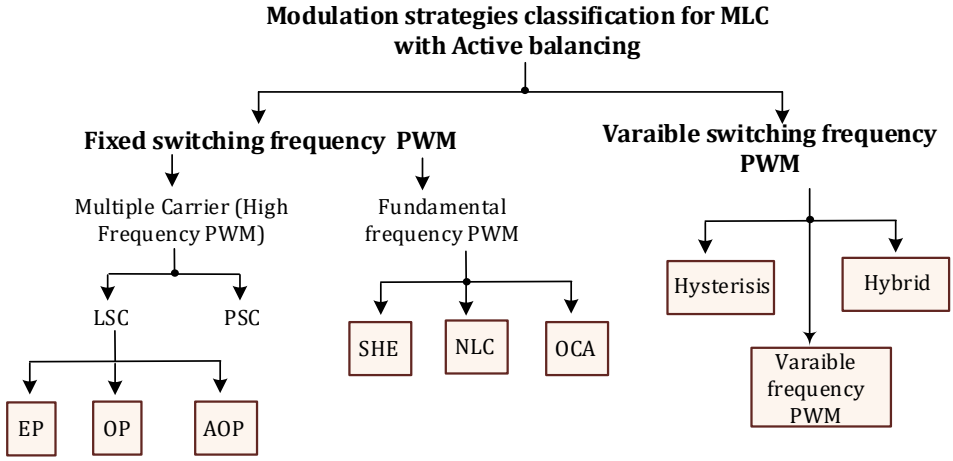


Figure 10. Modulation techniques for the MLC in compliance with the active-balancing role.

The variable-frequency PWM methods include hysteresis and hybrid PWM. They provide a faster dynamic response compared to fixed-frequency-based PWM techniques but are not widely used due to high switching losses.

4.2.1. Multiple-Carrier-Based PWM

In LSC, multiple-carrier signals are generated, which are shifted vertically in the modulation space, as explained in [101–104]. Typically, the carrier signals have a frequency that is 20 to 30 times the fundamental frequency of the AC output voltage. Each carrier signal corresponds to two switches of one leg.

For the FB topology shown in Figure 4, the two carrier signals are used. C_1 corresponds to S_{11}, and S_{21} whereas C_2 correspond to S_{12} and S_{22}. For the HB topology there is a single carrier signal C representing S_1 and S_2. The total number of carrier signals depends on the number of cascaded FB and HB structures (12 for the CHB topology in Figures 5 and 6 for the RHCB topology in Figure 6). A single modulating reference signal coming from higher-level control (explained in the next subsection) is compared with the multiple-carrier signals to generate PWM for the switches.

Figure 11 shows various sub-techniques for LSC-based PWM schemes. A single cycle of the modulating reference signal is considered for better illustration. The x-axis shows the time in seconds, whereas the y-axis reflects different levels of carrier amplitude.

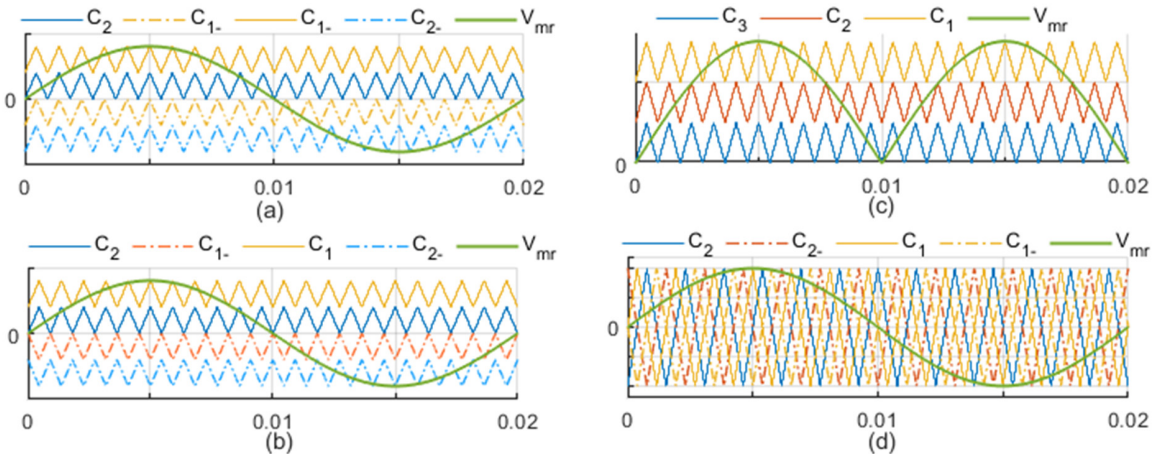


Figure 11. Various sub-techniques for LSC-based PWM scheme [105,106]: (**a**) equal−phase LSC PWM for FB structure, (**b**) opposite−phase LSC PWM for FB structure, (**c**) equal−phase LSC-PWM for HB structure, and (**d**) PSC PWM for FB structure.

In an equal-phase (EP) PWM scheme [105], the multiple-carrier signals are shifted vertically with a DC offset equal to the carrier magnitude symmetrically above and below the mean value of the modulating reference signal, as shown in Figure 11a.

In an opposite-phase (OP) PWM scheme [106], the carrier signals are shifted similar to EP-PWM but with the complementary phases. The carrier waves (C_1, C_2) above the mean value of the modulating reference are out of phase to C_1 lying below, as shown in Figure 11b.

The DC offset corresponds to m_n and therefore directly controls the switch-in time of each module. A lower value of DC offset indicates more turn-on and less turn-off time, and vice versa.

During standalone or grid-injection mode, the battery modules with higher OCV or SOC are placed near the mean value of the modulating reference signal, whereas the modules with lower OCV or SOC occupy the top layer. Figure 10c reflects the concept reported in [70] where the carrier signals are ordered such that $C_1 > C_2 > C_3$. This means that the battery modules at the top layer (C_1) receive less switch-on time, and therefore less energy is consumed from module 1 compared to module 2 and module 3.

To reduce the switching transients, the carrier signals are reordered every half cycle or complete cycle when the modulating wave goes through the zero crossing. The reordered carrier signal becomes effective during the next cycle.

Comparing Figure 11a–c, it can be seen that the modulating reference signal (V_{mr}) for HB has a frequency two times higher than that of FB, so the carrier signals can be re-ordered twice in each cycle of the AC output voltage.

In the PSC-based PWM scheme [106], all carrier signals have the same magnitude and frequency as the modulating reference signal but are phase shifted by $\frac{180^o}{n}$ (where n is the number of modules) in each period of the modulating reference signal.

Unlike amplitude-based carrier-shifting techniques, each carrier signal in PSC occupies the same modulation space, as shown in Figure 11d. This allows PSC to achieve a linear modulation range for all switches and better quality of the output voltage. However, it cannot regulate the switch-in and -out duration of different battery modules due to the fixed period, which means all battery modules supply the same energy at the end of each switching period.

4.2.2. Fundamental Frequency-Based PWM

In this method, the switches are turned on once during each cycle of the fundamental AC voltage. The turning on of each switch is governed by the switching angle, which is calculated using various techniques. Prominent techniques include SHE-, NLC-, and OCA-based PWM.

In the SHE-based PWM method, the undesired odd harmonic components and distortion factor of the AC-voltage waveform is suppressed, as explained in [107,108]. This is achieved by finding the complementary firing angles α_1 and β_1 using non-linear methods.

These complementary angles result in the switch turn-on times that correspond to a pure sinusoidal waveform, as depicted in Figure 12b. The output AC-voltage waveform can be expressed in Fourier series as follows:

$$V_{AC-out} = \sum_{k=1,3,5,\ldots}^{\infty} \frac{4V_B}{k\pi}\{\cos(k\alpha_1) + \cos(k\alpha_2) + \ldots + \cos(k\alpha_6)\}\sin(kwt) \tag{15}$$

where k is the number of the undesired odd harmonics and V_B is the module voltage. The magnitude of the Fourier coefficients for the fundamental voltage $V_{\mathrm{AC}-1}$ ($k = 1$) and maximum value $V_{\mathrm{AC}-1}$ can be expressed as follows:

$$\left.\begin{array}{c} V_1 = \frac{4V_B}{\pi}\{\cos(\alpha_1) + \cos(\alpha_2) + \ldots + \cos(\alpha_6)\} \\ V_{1-\max} = n\frac{4V_B}{\pi}\ for\ \alpha_i = 0 \end{array}\right\} \tag{16}$$

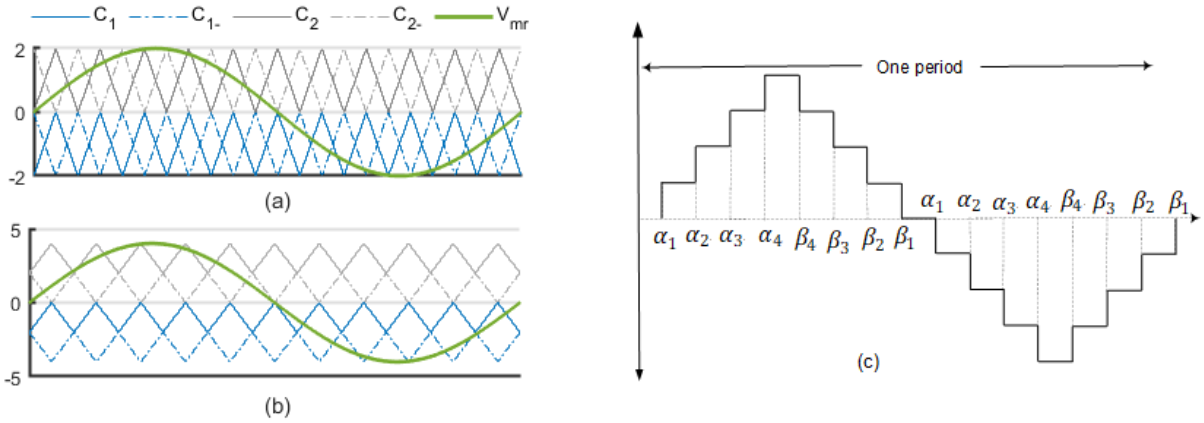


Figure 12. Various sub−techniques for LSC PWM scheme: (**a**) opposite−phase PWM for FB structure [106], (**b**) alternate opposite−phase PWM for FB structure [106], and (**c**) synthesized nine−level voltage waveform for SHE modulation [108].

The modulation index M_{SHE} is then expressed as:

$$M_{SHE} = \frac{\pi V_{AC-1}}{n4V_B} \tag{17}$$

To cancel the odd harmonics, the magnitude of the Fourier coefficients specific to odd ones are set to zero, as shown below [108]:

$$\sum_{k=3,5,7,\ldots}^{21} \{\cos(k\alpha_1) + \cos(k\alpha_2) + \ldots + \cos(k\alpha_6)\} = 0 \tag{18}$$

From Equation (18), it can be seen that there are 10 nonlinear transcendental equations that need to be solved using iterative methods such as the Newton–Raphson method [75] to obtain the optimized value for switching angles.

Once the switching angles are obtained, the energy balance is achieved by alternately reversing the angle assignment in pairs, as explained in [107,108] As a result, $\alpha_1 = \alpha_6$, $\alpha_2 = \alpha_4$, and $\alpha_4 = \alpha_5$ after each period of the fundamental AC voltage. This allows the energy balance to be maintained among the modules. To avoid solving nonlinear equations in each AC voltage, the firing angles were calculated offline in [108] and stored in a look-up table. SHE is applicable for both FB and HB configurations.

In the nearest-level control (NLC) method, a sinusoidal reference is compared with the actual output AC voltage to select the nearest sinusoidal voltage level. NLC is computationally less intensive compared to SHE, as it does not require nonlinear equations to be solved. It also offers a better quality of output voltage and a smaller ripple in the load current [109–111].

In optimal switching angle (OCA), the harmonics are minimized by calculating the optimal value of the switching angle using nonlinear methods [36].

4.2.3. Variable-Frequency-Based PWM

In the underlying methods for this category, the current error signal and fixed-width reference-hysteresis band are compared to generate the switching signals for MLC switches. Refs. [112–114] explain different variable-frequency PWM strategies and assess the impact of filter elements on network harmonics.

4.3. Comparative Analysis

All the fixed-frequency-based modulation techniques explained in Section 4.2 provide adequate performance from the power-quality perspective. However, when the

active-balancing functionality is added, the fundamental-frequency-based PWM methods reported in [107,108] suffer from computational complexity. For example, in the SHE method, the offline calculation of injection angles reported in [108] maintains only the energy balance among the modules. This means that each module supplies the same kWh after a definite time interval T. Therefore, it is effective only as long as all the battery modules have same capacity, initial SOC, and discharge/charge rate (*C*). In the case of a battery pack with different capacity modules, the energy-balancing approach forces the lower-capacity modules to operate at higher *C* rates, resulting in much faster discharging/charging than the rest of the battery modules.

To avoid this issue, the angle assignment needs to be updated during each switching interval based on either the SOC or OCV of each module. As explained in Section 4.2.2, when the angle-assignment time is combined with the time to solve the nonlinear equation in each AC cycle, the computational complexity increases manifold.

The multi-carrier-based PWM methods have the advantage of simple calculation but face other limitations; for example, all LSC techniques reported in [74,103,104] are inherently nonlinear and unbalanced due to the fractional share of modulation space, as shown in Figures 11 and 12. If the battery modules have fresh cells with the same initial voltage/SOC, the LSC always makes the battery modules unbalanced first before performing the active balancing.

The PSC scheme does not undergo this issue and continues the balanced operation for an extended range. However, like SHE, the PSC method can only perform the energy balance among modules and is therefore not effective if the modules are initially unbalanced or do not have the same capacity.

5. High-Level Control

5.1. Main Objective

A robust high-level controller ensures that a good tracking of the active and reactive current reference is achieved for grid-connected (current-control) mode [115,116]. In the standalone (voltage-control) mode the controller must reduce the voltage transients, dv/dt, semiconductor losses, and switching delays. A good estimation of semiconductor voltage drop and compensation of switching delays is also critical to achieve an accurate reference following on the AC side.

The controller must also maintain the system stability during active balancing, module bypassing, or hot swapping. Additionally, it must perform a smooth transition from grid-connected mode to standalone mode.

The output of a high-level controller is a sinusoidal modulating-reference signal that drives the modulation block.

In grid-connected mode the high-level controller can also perform power-quality conditioning, which includes current-harmonics suppression and reactive-power compensation for nonlinear loads to enhance the grid power quality.

5.2. Classification of Higher-Level Control Strategies

Figure 13 provides a classification of various high-level control strategies that can be used for multiport MLCs.

5.2.1. Synchronous Reference-Frame (SRF)-Based Control

In the sub types of SRF-based control methods, voltage-oriented control (VOC) is quite common for grid-connected MLCs [117].

In VOC, all the synchronous quantities are first converted to the orthogonal α–β stationary reference frame using the Park transformation and then to DC components in a rotating *dq* reference frame using the Clark transformation [118,119]. Figure 14 shows the block diagram of VOC control reported in [120] for a single-phase MLC.

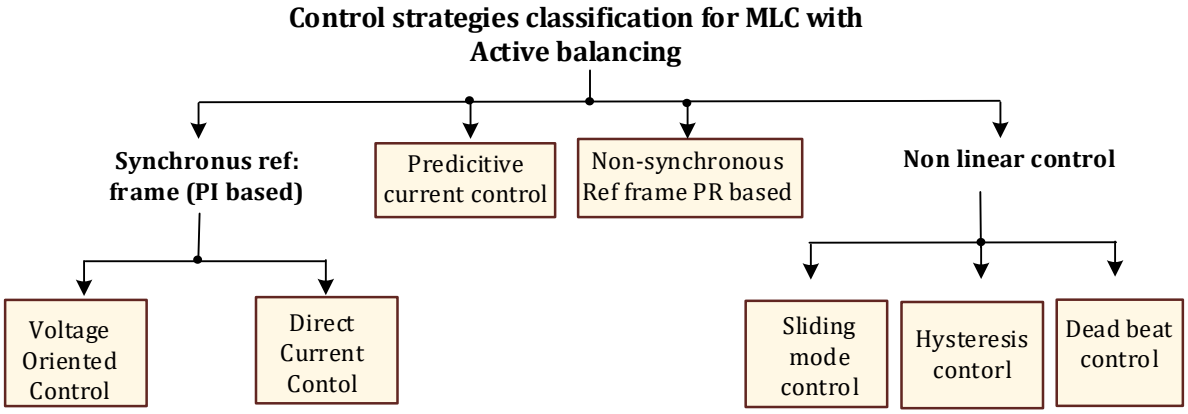


Figure 13. High−level control techniques for MLCs.

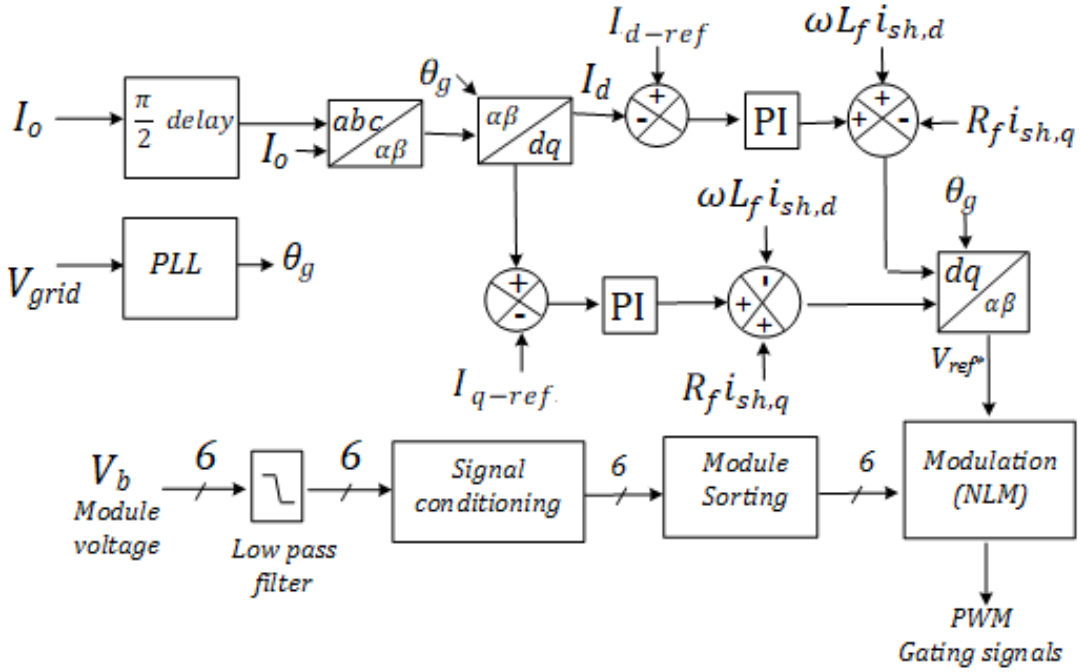


Figure 14. High-level VOC controller for CHB MLC [118].

A single-phase phase-locked loop (PLL) is used to synchronize the rotating dq frame with the angle (θ) of the fundamental grid voltage. For cascaded battery modules a single current-control loop is used.

Two proportional-integral (PI) controllers are used to control the i_d (d-axis component representing active power) and i_q (q-axis component representing reactive power). The output of the PI controllers is added to the feedforward signals for cross-coupling elimination. The output corresponds to V_{ref-d} and V_{ref-q}, which are the dq components of the reference voltage. After the reverse Park transformation, the two orthogonal reference output voltages $V_{ref-\alpha}$ and $V_{ref-\beta}$ are obtained. $V_{ref-\alpha}$ is used as a modulating-input signal for the modulation stage.

The direct current controller (DCC) is reported in [121] for m-level PV-fed MLCs but can be applied to a BESS-fed MLC topology as well. It provides an accurate current control in grid-connected mode and allows for robust performance under system-fault conditions. Figure 15 depicts the controller reported in [122]. DCC uses a sinc filter as reported in [122,123] along with the multiple second-order generalized integrators (multi-SOGI) to filter the measured grid voltage and AC-side current. The output of the current

controller can be used with the module-balancing algorithms, which select the switching vector so as to minimize the distortion in the output voltage.

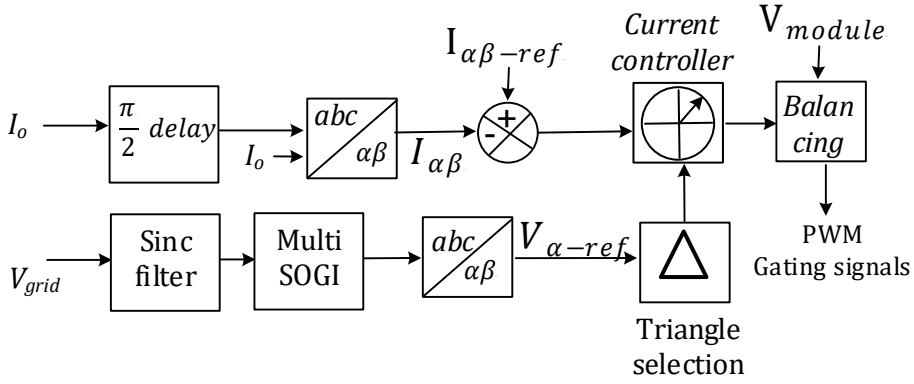


Figure 15. Schematic view of high-level direct-current controller [121].

5.2.2. Predictive Current Control (PCC)

PCC uses the discretized MLC-model behavior in the previous time instant to predict the output at next time instant.

It makes multiple control-index predictions in each sampling interval and chooses the one that leads to the minimum deviation between the desired output and the predicted value. Generally, the control target is to track a pure sinusoidal AC reference in phase with the grid voltage.

PCC is reported in [124–127], where forward Euler discretization is first used to obtain the discrete-time dynamic model of the MLC. The tracking error of predicted-current values is governed by cost function C, which can be expressed as follows:

$$C_{k+1} = i^*_{k+1} - i_{k+1}\left|i^*_{k+1} - i_{k+1}\right|^2_2 \quad (19)$$

where i^*_{k+1} is the desired value at $k+1$ time instant, and $|.|^2_2$ represents the quadratic eucledian norm.

In PCC, the sampling time is kept small to hold the approximation of $i^*_{k+1} = i_k$ true. The resulting actual current i_{k+1} at $k+1$ time instant is the same as i^*_{k+1}.

To avoid common-mode voltage generation for three-phase implementation, PCC incorporates the uncertainty or mismatch between the actual and sampled filter parameters. To reduce the calculation time for PCC, a fast-optimization algorithm based on sphere decoding is reported in [126,127].

5.2.3. Non-Synchronous Reference-Frame (PR)-Based Control

In this method, the frame transformation does not take place. The actual and reference current values are compared in a stationary reference frame and the difference is fed to a proportional resonant (PR) controller [128,129]. The PR controller is tunned at the fundamental frequency of the grid. In the case of harmonic suppression, multiple PR controllers can be used. Each controller is tuned at a frequency that is an odd multiple of the fundamental grid frequency. The output of the PR controller is the modulating reference signal, which drives the modulator block.

PR-based controllers face higher tuning issues than PI-based controllers but offer high speed, as they do not need frame transformation.

5.2.4. Nonlinear Control

Nonlinear controllers feature smaller amplitude variations and offer quick response but face design challenges when load parameters are dynamic and change over time, such

as off-grid systems. The sub-techniques in this category include sliding-mode control (SMC), hysteresis controllers, and deadbeat controllers.

SMC is reported in [130,131] for cascaded three-phase dual-inverter systems and cascaded H-bridge, respectively.

In SMC, first a sliding surface is defined using nonequality constraints such as common-mode voltage reduction and cancellation of higher-order harmonics. Once the constraints are defined, the control variable, which is usually the MLC output current, is squeezed onto the sliding surface $s(t)$, as expressed below:

$$\mathrm{s(t)} = c_1\mathrm{e(t)} + \frac{d}{dt}e(t) \tag{20}$$

where $\mathrm{e(t)} = I_{ref} - i(t)$ is the error signal obtained by comparing the reference and actual MLC output current. Figure 16 reflects the schematic overview of the SMC with a low-pass filter for a CHB MLC, as reported in [132]. The low-pass filter is used to prevent overshoot and slipping around the sliding surface. To define the stability condition for the sliding surface, the Lyapunov stability standard is used in [132] and is expressed below:

$$\frac{d}{dt}e(t) = - \in sign(s) - ks - \omega\frac{R}{L}i(t) + \ddot{i(t)} \tag{21}$$

where $\in > 0$, $sign(s)$ is the signum function, and k is the inequality constraint, which is defined as follows:

$$k > \left[\omega\frac{R}{L}i(t) + \ddot{i(t)}\right] \tag{22}$$

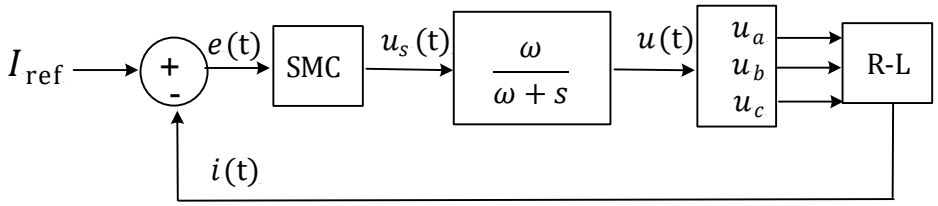


Figure 16. Schematic representation of the sliding-mode control scheme with a low-pass filter, reported in [130,131].

Another important nonlinear controller is a hysteresis controller. This is used in applications where the requirements include fast transient response, unconditional stability, and wide setpoint-tracking bandwidth [133].

In the hysteresis control method, the controlled parameter $i(t)$ (MLC output current) is made to follow the reference current by applying a suitable voltage at the MLC output. Each voltage level corresponds to a single hysteresis limit. If $i(t)$ exceeds the initial hysteresis limit, the next (higher or lower) voltage level is selected to force $i(t)$ again within the specified limit. If $i(t)$ remains out of bounds for all the voltages levels in one direction, the process repeats with reverse polarity and stops only when a particular voltage level is selected that reverses the direction of $i(t)$.

One challenge for hysteresis controllers is to select the correct voltage level that keeps the MLC output current within the desired band. Quite often, a single-band hysteresis controller faces limitations in controlling the current. To solve this issue, a multiband hysteresis-modulation technique is reported in [134,135] that uses multiple symmetrical hysteresis bands to control the output current.

Figure 17 shows the multiband hysteresis controller reported in [134]. In this technique, the inner hysteresis band carries out switching between adjacent levels, whereas the outer band carries out additional switching-level changes.

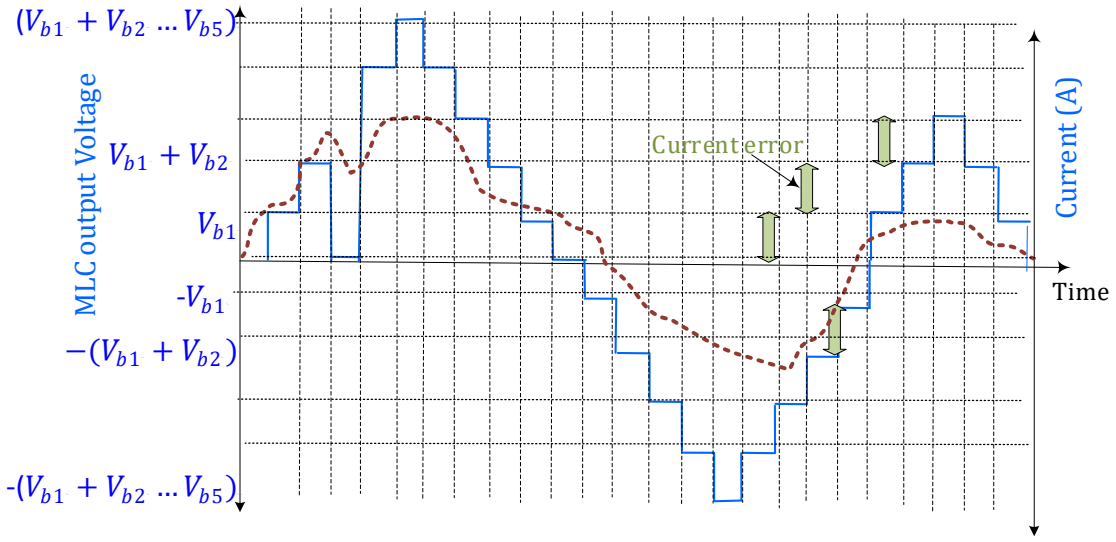


Figure 17. Multiband hysteresis controller reported in [134].

The last nonlinear controller reviewed for MLCs is the deadbeat controller. Deadbeat controllers are reported in [136] as an alternate choice for synchronous reference-frame-based controllers. They are built in stationary alpha-beta reference frames to minimize the complexity and computation burden for transformation to and from *dq* reference frames. Figure 18 reflects the deadbeat controller that is reported in [136].

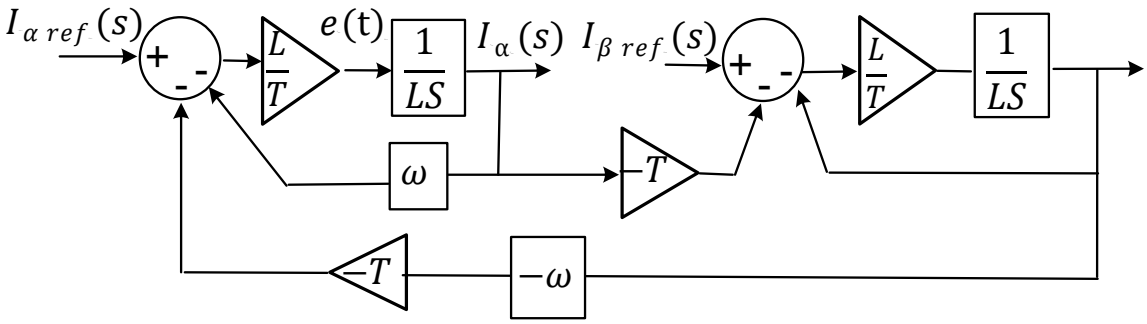


Figure 18. Deadbeat current controller reported in [136].

The deadbeat action forces the MLC current $i(t)$ to follow the reference current in each sampling interval. The deadbeat transfer function for i_{alpha} and i_{beta} can be expressed as follows:

$$\frac{i_{\alpha\beta}}{i_{\alpha\beta-ref}} = \frac{1}{1+\mathrm{Ts}} == \frac{1}{1+(\mathrm{T}+\mathrm{C})\mathrm{s}} \tag{23}$$

where C is a constant and T is the time delay of a single sample. The constant C is set as the same value as T in order to cancel the delay time between reference and actual current, as reported in [137].

5.3. Comparative Summary

Due to simplicity, response speed, and ease of implementation, the hysteresis control method outperforms all other methods. It exhibits robustness and a reduction in system order compared to the rest of the methods. However, it faces a serious drawback due to variable-switching frequency, as it causes non-uniform electrical and thermal stress across all the switches and entails a high cost for the heat sink.

The non-synchronous controller features fast reference tracking, but a capacity mismatch among the battery modules may lead to overmodulation and degraded power quality for standalone applications.

It is important to note that the switching frequency of an MLC is significantly lower than standard two-level VSI, which means a relatively higher sampling time is available to update the reference signal. This means that the steady-state performance and transient stability are more critical parameters than the speed of response.

It is explained in the previous subsection that both VOC- and PCC-based methods [47,119] achieve zero steady-state error and ensure system stability for a dual mode of operation. Therefore, VOC-based high-level control is considered for the simulation study in this review paper.

6. Simulation Study

In this section, a simulation study is conducted using (i) the topology based on the explanation in Section 3, (ii) the modulation methods based on the explanation in Section 4.3, and (iii) higher-level control based on the explanation in Section 5.3.

It can be seen from Table 4 that the CHB MLC topology holds the advantage over other topologies in many features. Therefore, 13-level grid-connected CHB configuration was selected for the study, as depicted in Figure 19. Based on the explanation in Section 5.3, a higher-level closed-loop controller using the synchronous reference frame was developed in a MATLAB environment.

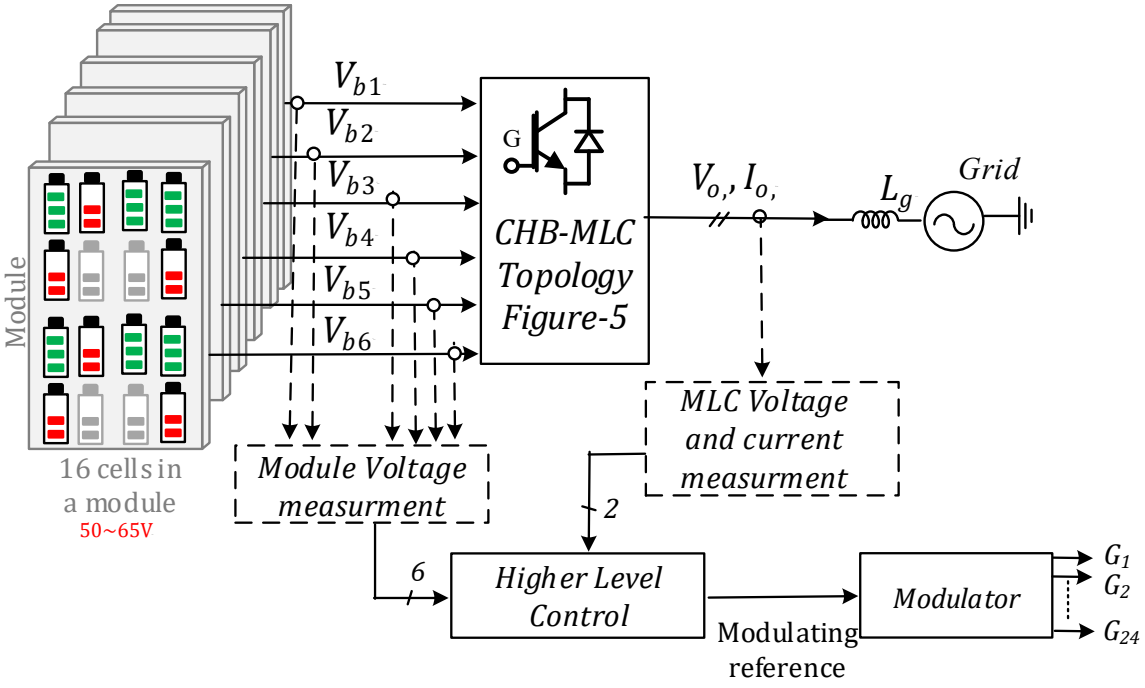


Figure 19. Schematic representation of single−phase CHB-MLC with voltage and current measurements.

Multicarrier-based modulation methods show improved performance compared to other PWM schemes, as explained in Section 4.3, but there are multiple subtypes, and each type has different features.

The simulation study compares these subtypes, including (i) EP-, (ii) OP-, (iii) AOP-, and (iv) PS-based PWM methods.

The performance indicators include balancing speed, voltage THD, current THD, and maximum voltage difference among the unbalanced modules. The THD of MLC voltage and current were measured using fast Fourier-transform (FFT) analysis. Table 5 shows the different system parameters considered for the simulation study.

Table 5. System parameters considered for the simulation study.

System Parameters	
Number of modules	6
Number of cells per module	16
Nominal module voltage	65 V
Cell type	LFP
Rated power	5 kW
Nominal cell capacity	5 Ah
Number of AC voltage levels L_{AC}	13
Carrier-signal frequency f_C	1100 Hz
Fundamental frequency f_o	50 Hz
Modulating ration	{−1,1}
Filter inductance L_{AC}	200 uH
Filter resistance R_{AC}	0.1 mΩ
Full-bridge switch type	MOSFET
Switch ON resistance	10 mΩ
Total number of switches	24
Grid voltage (rms)	230 V
Proportional-gain PI controller	0.4
Integral-gain PI controller	50
Control sampling time	50 µs

To evaluate high-level control and active balancing for different PWM methods, three tests were conducted, as follows:

I. Monitor the AC-side parameters using a short-duration test at low and rated current. The measurements include current-tracking error and voltage/current THD).
II. Monitor the impact of active balancing on the DC voltage of all six battery modules using a long-duration charge–discharge test with balanced modules with the same initial OCV.
III. Monitor the impact of active balancing on unbalanced battery modules with different initial OCV and SOC.

The difference among module voltages was measured at the beginning and end of each cycle. Further details of the balancing algorithm, including the OCV/SOC calculation and a reference-modulating signal update, are beyond the scope of this paper.

Figure 20 reflects various results for the EP-PWM method. Figure 20a shows the MLC output voltage, whereas Figure 20b reflects the MLC output current and grid voltage on the same graph. The grid voltage was scaled down (by a factor of 15) to improve the visualization.

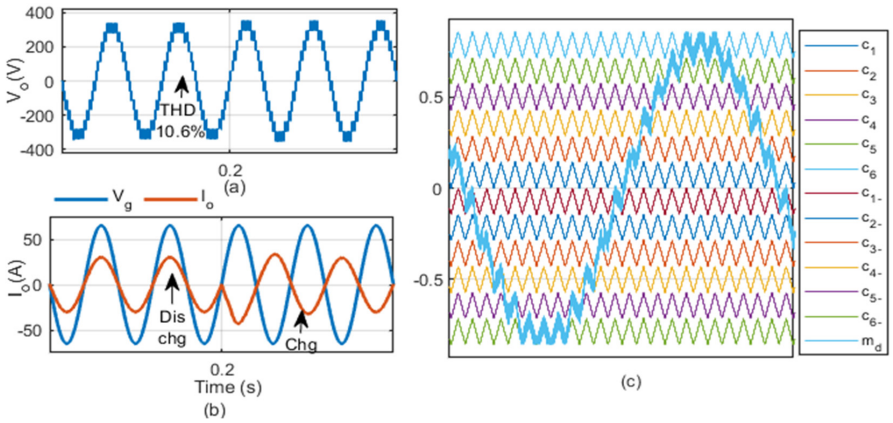


Figure 20. Simulation results for equal-phase LSC modulation: (**a**) MLC output voltage, (**b**) injected current and grid voltage, and (**c**) twelve carrier signals and modulating−reference signal from the high−level controller.

From $t = 0$ s to $t = 0.2$ s, the MLC remained in the grid-injection mode, where it injected a constant active power of 6 kW into the grid at unity power factor. This corresponds to the reference current $I_{d\_ref} = 30$ A and $I_{q\_ref} = 0$ A for the high-level controller. The modulating reference (output of high-level controller) and multiple career signals are depicted in Figure 19c.

It can be seen from Figure 20b that the MLC injected current was in phase with the grid voltage during the grid-injection mode. At $t = 0.2$ s the MLC went into offtake mode and the MLC offtook 6 kW from the grid. The reference current changed from $+30$ A to -30 A. The actual current followed the reference, as is clear from Figure 20b, where the MLC current was 180^o out of phase with the grid voltage. The THD of the MLC voltage was 10.6% throughout t the test, whereas the output current had a THD of 1.6% in grid-injection mode and 2% in offtake mode.

In the second test, the initial OCVs of the battery modules $1 - 6$ were set to the same value of 65 V, whereas the initial SOC of all the modules was kept at 80%. Figure 21a reflects the battery-module voltage profile for a charge–discharge cycle. It can be seen that the module voltages remained balanced, with a small difference (ΔV) of less than 0.01 V throughout the operation.

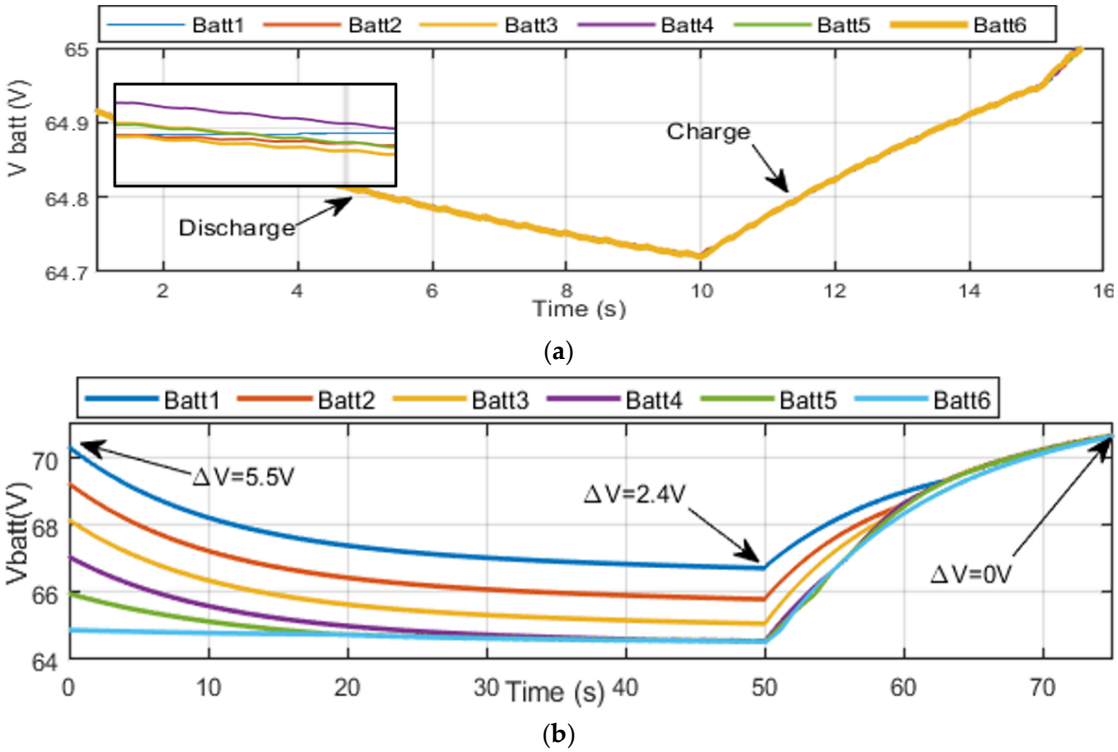


Figure 21. Battery-module voltage profile during a charge–discharge-cycle test for EP-PWM with (**a**) no initial imbalance in the module voltage and (**b**) a maximum initial imbalance of 5.5 V.

In the third test, the initial OCVs and SOC of battery modules $1 - 6$ were set as 70.3 V, 69.2 V, 68.1 V, 67.1 V, 65.9 V and 64.8 V, and 75%, 74%, 73.5%, 72.5%, 71% and 70.5%, respectively. The test ran for a duration of 100 s. The maximum initial OCV difference was measured as $V_{mod1} - V_{mod6} = 5.5$ V. The discharging cycle continued for a duration of 50 s. The EP-PWM method gradually reduced the difference to 2.4 V at the end of the discharging period. The difference was eventually reduced to zero after 24 s of the charging cycle, as shown in Figure 21b.

Figure 22 reflects the different test results of the OP-PWM method. In the test with unbalanced modules, the same initial SOC and OCV profiles as those used for the EP-PWM method were considered.

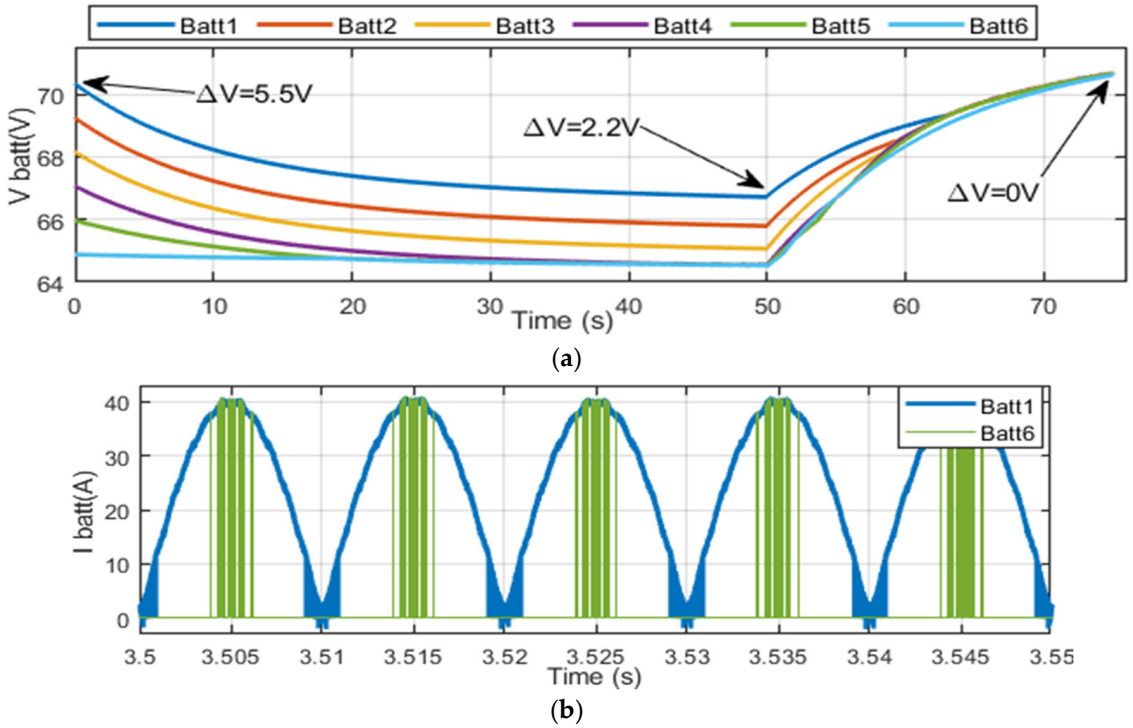


Figure 22. (**a**) Battery-module voltage profile during a charge-discharge-cycle test for OP-PWM method with initial imbalance of 5.5 V and (**b**) battery-module current profile for two modules with maximum and minimum OCV.

Figure 22a depicts the module voltage profile for the test (iii) with unbalanced modules. The initial imbalance was measured as 5.5 V. The maximum difference at the end of the 50 s discharging cycle was measured as 2.5 V, whereas the at the end of the 24 s charging cycle the difference was reduced to 0 V.

To illustrate the impact of active balancing on the current of battery modules, the current profiles of modules 1 and 6 are depicted in Figure 22b. These two modules were selected because module 1 had the highest initial OCV, whereas module 6 had the lowest initial OCV.

It can be seen that battery module 1 had a higher average current in the discharging mode as it conducted throughout the switching period, whereas module 6 only conducted the switching current fractionally (less than 5 ms) during the switching cycle. This means that module 1 underwent rapid discharging compared to module 6, which is clear from the voltage profile of module 6 in Figure 21a.

Figure 23 reflects the battery-module voltage and current profile of the AOP-PWM method for the test (iii) with unbalanced modules. The initial imbalance was measured as 5.5 V. The maximum difference at the end of the 50 s discharging cycle was measured as 2.5 V, whereas at the end of the 24 s charging cycle the difference was not reduced to 0 and was measured as 0.3 V.

Table 6 provides an overview of different parameters for four multicarrier-based PWM methods. Using fast Fourier transform (FFT), the MLC voltage and current THD were calculated at rated and low (less than 20%) power. At rated power, the AOP-PWM method exhibited the highest voltage THD but the lowest current THD, whereas the EP-PWM method showed the lowest voltage THD but the highest current THD.

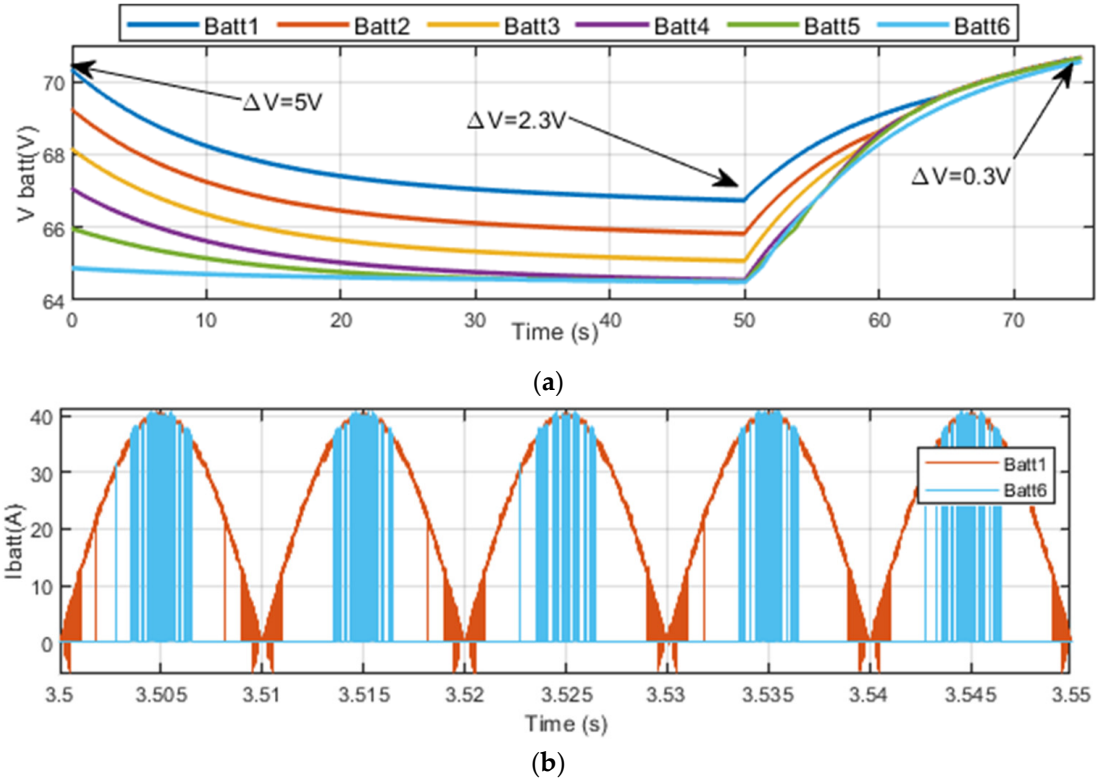


Figure 23. (**a**) Battery-module voltage profile during a charge-discharge-cycle test for AOP-PWM method with initial imbalance of 5.5 V, and (**b**) battery-module current profile for two modules with maximum and minimum OCV.

Table 6. Comparative summary for different amplitude-based modulation strategies.

Modulation-Technique Feature	*EP PWM* [105,106]	*OP PWM* [105,106]	*AOP PWM* [105,106]	*PSC* [105,106]
MLC voltage THD at low power	12.6%	12.72%	16.4%	10.6%
MLC current THD at low power	5.6%	5.66%	5.3%	2.6%
MLC voltage THD at rated power	10.6%	12.26%	19.6%	10.6%
MLC current THD at rated power	2.6%	2.3%	1.7%	2.6%
Balancing potential	Yes	Yes	Yes	Partially
ΔV for discharge cycle	2.5 V	2.5 V	2.5 V	NA
ΔV for charge cycle	0 V	0 V	0.3 V	NA

Compared to the EP and OP based PWM methods, AOP−PWM was less effective at reducing the imbalance factor to zero for the reference charge−discharge profile.

7. Conclusions

MLCs are increasingly applied as BESS interfaces due to their improved voltage qualities over conventional two-level voltage-source inverters. In this paper, several MLC topologies are explored for grid-connected and off-grid applications. A critical overview of traditional and recently proposed multiport topologies is presented to offer a better understanding of MLC operation and limitation in grid-connected and off-grid modes. The

principle of active balancing is explained to show the implementation of the configurations in grid-connected and off-grid modes. The key findings can be summarized as follows:

(1) The state-of-the-art reduced-switch MLC topologies reported in the literature [35,36,38,66–76] are good candidates for only standalone applications and cannot inject power in the grid-connected mode. Two such topologies are reduced-switch cascaded half-bridge [73] and modified cascaded configurations [35,38].
(2) There is no universal topology that can be attributed as the best candidate for a dual (grid-connected and standalone) mode of operation. However, except for a relatively higher footprint, the symmetric cascaded H-bridge can be an optimal topology for a dual mode of operation.
(3) Many modulation strategies that are used for multiport MLCs maintain energy balance only among the battery modules. Therefore, these PWM strategies lack effectiveness when combined with the role of active balancing among unbalanced modules with different capacities/chemistries. These include all phase-shifted PWM methods and fundamental-frequency PWM methods with offline-angle calculations [108].
(4) Amplitude-based carrier PWM methods are inherently unbalanced, and the carrier signals need to be readjusted every few cycles even if the modules have the same initial OCV/SOC.
(5) At low power, the phase-shifted PWM strategy offers the lowest voltage and current THD (10% and 2.6%, respectively) compared to level-shifted carrier-based techniques. At rated power, AOP-PWM offers the lowest current THD of 1.7%.
(6) The balancing potential of the AOP-PWM strategy is 33% lower than the EP and OP-PWM methods.

To summarize, the diversity in cascaded MLC modulation, control, and switching strategies can allow for further improvement in the AC-side transient response and reduction in the losses. For future studies, a loss analysis can be conducted for state-of-the-art modulation strategies. In addition, during the idle state, either for grid-connected or standalone mode, the self-balancing feature of CHB-MLC can be further explored. To allow for faster balancing, it is critical to allow for a simultaneous charging/discharging feature, which means that high-capacity modules can discharge into low-capacity modules. A hybrid modulation, control, and switching strategy can be developed to allow such a feature to expedite the integration of battery modules with different capacities in stationary applications.

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