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High-Performance Power Electronic Battery Pack Based on a Back-to-Back Converter

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Abstract: This work studies a full-power, module-integrated back-to-back converter for battery energy storage applications. The proposed solution optimizes bank usage across a wide range of individual battery capacities. The converter design and control are examined, as well as the use of a loss reduction method when operating under a partial load. The suggested architectural work allows the bank to have a regulated voltage output, simulating a passive bank, while controlling the charge and discharge of individual batteries to their maximum capacities. Those capabilities are also evaluated using linear programming optimization, in order the quantify the advantage. The suggested system is used in a typical use-case examined experimentally. The energy provided by an experimental lead acid bank rose 38 times after a few charge/discharge cycles.

Keywords: battery storage plants; DC–DC power conversion; equalizers

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1. Introduction

A battery energy storage system (BESS) is composed of series and parallel batteries. These arrangements are necessary to reach the required energy and voltage output [1]. However, there is a challenge when batteries are associated in series. The elements have different charge amounts due to electrochemical mismatches. Moreover, after some time of use, multiple recharge cycles tend to increase those differences [2]. For instance, Lehner et al. [3] measured 700 new automotive cells and found a deviation from the mean capacity of ±7%.

One of the major factors causing this capacity divergence is temperature gradients inside the *BESS* [4]. Those differences can happen due to different cooling or loading conditions. As an example, an evaluation of Li-ion storage installed in Germany shows that the state-of-health (SoH, the level of degradation, and remaining capacity of the battery) at lower temperatures decrease by 1%/year, while the *SoH* at higher temperatures falls by 2%/year. Other factors associated with these differences are time and usage. Over time, Li-ion batteries tend to drift (regarding their capacities) since the electrochemical degradations behave differently for each cell [5].

The main problem with a series of battery arrangements is that the total 'storable' energy is dependent on the weakest battery. During discharge, the low-capacity battery empties first, forcing the entire storage (*BESS*) to shut down. During the charge, due to its incapacity of the absorbing charge, it quickly reaches its maximum voltage and must also stop charging the entire bank. Hence, an energy equalization system [6] is necessary at the cell and battery levels, which can be classified as passive or active balancing structures, as Figure 1 illustrates. The first type dissipates the excess energy in the form of heat, while the second type transfers the energy to the adjacent element.

This paper presents the technological evaluation of a series module-integrated converter for battery/cell equalization. The proposed design contribution shows the possibility of fully controlling the output voltage, which can speed up the balancing time and increase the balancing performance. The flexibility introduced is crucial to fully utilize the storage energy, even with a widely distributed charge range between the modules.

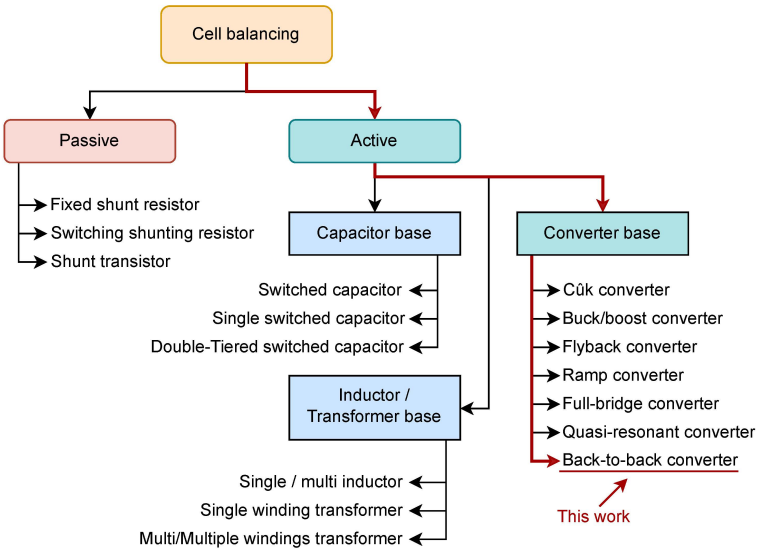


Figure 1. Classification of battery/cell equalization technologies [6].

The system can also promote battery replacement since it can adjust individual capacities independently, which is not possible in equalization systems available on the market. With the proposed solution, only the weak battery is replaced, such that the maintenance costs drastically reduce and the batteries are fully used. In a similar manner, the presented technology can also operate with batteries from different manufacturers or technologies. In order to demonstrate those advantages quantitatively, an analysis based on linear programming is presented to compare the energy outputs of the available architectures.

The converter topology selected to introduce this new feature is a multi-leg back-to-back converter. The system integrates the converter at the battery level, as seen in Figure 2, which is different from the alternatives at the cell level [7]. This brings benefits in terms of volume and efficiency, while still keeping high capacity utilization and high utilization under fault [8]. There are several other advantages to the presented modularization technique, such as its easy assembly and customization, the possibility of heterogeneous banks; system reliability improvement (due to lower stresses on the degraded batteries); the bypass of the defective batteries; and the ability to downgrade the performance while waiting for maintenance [5].

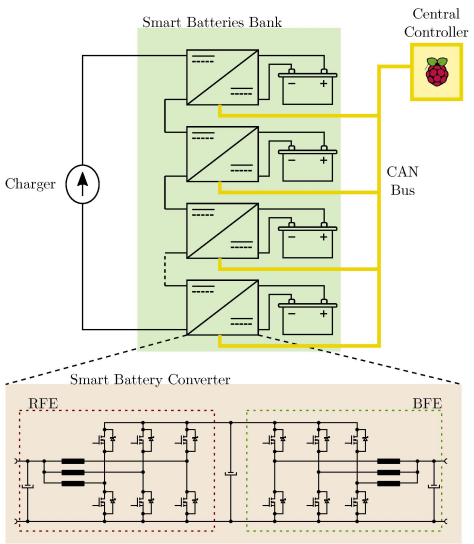


Figure 2. Proposed series cell-to-pack module-integrated bank based on back-to-back converters.

In this research, since the system enhances the battery behavior, the joint (battery plus electronic) is named a smart battery (*SB*) [9–11]. The combination of *SB* modules in series and parallel builds a smart battery bank that interacts with a charger, Figure 2. A central controller (*CC*) is responsible for managing the *SB* bank and commands the individual SBs via a CAN bus. It receives the converter measurements, such as the battery voltage and current as well as the DC link and terminal voltages, and calculates the terminal voltage setpoint of each module, taking care to keep the voltage sum constant. The CC is also responsible for turning the modules on and off, ordering them to enter the bypass mode, or resetting any error condition.

This paper's organization is as follows: Section 2 elaborates on the model employed to access the performance of the parallel and series architectures; Section 3 details the converter design and shows the importance of restricting the number of switching legs under partial load; Section 4 explains the converter's control strategy, modeling, tuning, and implementation of the partial load strategy; Section 5 presents the experimental setup and results; and Section 6 presents the conclusions of this work.

2. Architecture Performance Comparison

There are some topologies for the active equalization proposition. The use of a converter base is the most suitable since it enables more degrees of freedom to adjust the power flow between elements [12]. In order to compare those differences, a summary comparison is presented in Table 1.

Table 1. Comparison between different active equalization systems [12].

Equalization Technology	Advantage	Disadvantage
Multiple transformers	Fast equalization	Large size and cost
Multi-winding transformer	Fast equalization	Large size and cost
Buck–boost converter	Intermediate equalization	Complex control
Switched matrix with a dc–dc converter	Fast equalization	Complex control
Quasi-resonant converter	Simple control	Slow equalization for high power
Two-stage bidirectional interleaved dc–dc converter	Simple control Fast equalization	Suitable for high power

Among the active balancing circuits, the most common one used in the literature is energy redistribution balancing, which can be classified based on the architecture, such as adjacent cell-to-cell (*C2C*), direct cell-to-cell, and cell-to-pack (*C2P*) [13]. The latter architecture can be further divided into parallel or series. Figure 3 illustrates each strategy.

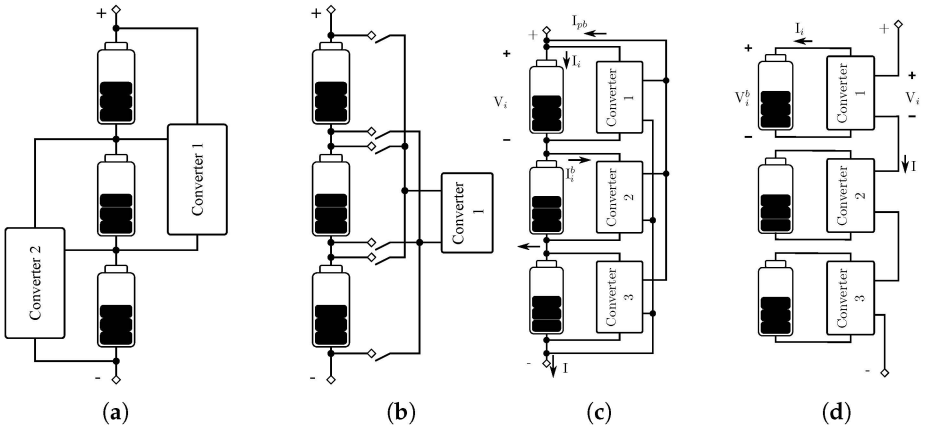


Figure 3. Equalization architectures based on energy redistribution balancing: (**a**) adjacent cell-to-cell, (**b**) direct cell-to-cell, (**c**) parallel cell-to-pack, and (**d**) series cell-to-pack.

In the adjacent cell-to-cell architecture, Figure 3a, energy is only transferred between adjacent cells. This is a simple and often adopted solution that has been the object of many works proposed for different converter topologies or balancing algorithms [14]. Its main drawbacks are its low efficiency, as the energy flows through many converters when cells with wide differences in capacity are far apart, and the low equalization speed that decreases as the number of cells increases [15].

In the direct cell-to-cell architecture, as seen in Figure 3b, energy can flow between any two cells of the pack. For example, authors from [16,17] propose an inductor as the storage element and an association of MOSFETs and diodes as switches. This architecture's main drawback is the low equalization speed since only a pair of cells are charged/discharged at a time. A hybrid adjacent/direct cell-to-cell architecture was proposed in [18].

In the parallel cell-to-pack architecture, as seen in Figure 3c, the energy transfer takes place between individual cells and the whole pack. Several authors have proposed different converter topologies for the realization of this architecture, e.g., [2,19–22]. An important drawback of this architecture is that the pack side of the converter must withstand a higher voltage and the converter has a high primary/secondary voltage ratio that compromises efficiency.

In the series cell-to-pack architecture, as seen in Figure 3d, energy transfer happens between the individual modules (cell plus converter) and the pack, but this process is more subtle since the modules are simply connected in series. The pack current flows through the string, but the converter controls the module terminal voltage. As a result, the energy supplied to or drawn from each module is proportional to the individual module terminal voltage. An example of the series cell-to-pack architecture involves the use of a cell-integrated bidirectional buck converter [7]. In a different approach [1,23,24], the modules operate in a bypass or inserted mode, in which the battery current is zero or equal to the pack current, respectively (the latter could also be classified as duty cycle balancing [13]).

The converter in the C2P series architecture has a 1:1 ratio and needs only low-voltage switches. It favors battery–converter integration, since the resulting module remains with two terminals, and the connections to the pack's positive and negative rails are avoided. However, the practical implementations proposed in the literature limit the module terminal voltage values, as they can only be higher or lower than the battery voltage since only step-up or step-down topologies have been proposed so far. This limited range compromises the ability to extract all of the stored energy from the bank when the battery capacities range widens, as will be shown in this work.

This section extends the work of Chatzinikolau and Rogers [13], who evaluated the performances of power electronic-enhanced battery packs through the use of linear programming optimization. Linear programming, in this work, is a tool to compare the performances of different architectures, but it has no influence on the system operation.

The performance of the parallel cell-to-pack (C2P) bank, as developed in [13], is repeated here, and compared with the performance of the C2P series. The modeling and development of the performance assessment of the C2P series bank is the contribution of this work, as [13] compared the architecture's parallel C2P, adjacent C2C, and direct C2C. Two implementations of the C2P series are considered: the bidirectional buck converter [7] and the proposed back-to-back converter.

2.1. Parallel Cell-to-Pack

In a parallel C2P topology, the average battery i current is (**??**),

$$I_i = I - I_i^b + I_{pb}, \tag{1}$$

where I is the pack current, I_i^b is the average balancing current extracted from the battery i, and I_{pb} is the total balancing current that is returned to the pack, as indicated in Figure 3c. The extracted power from the battery and delivered to the pack is (2),

$$\eta \sum_{i=1}^{N} V_i I_i^b = I_{pb} \sum_{i=1}^{N} V_i, \tag{2}$$

where η is the converter efficiency, considered constant, V_i is the module voltage, and N is the number of batteries. Considering equal battery voltages, I_{pb} will be (3). The average balancing current extracted from module i can be modeled as (4), where bI is the converter current capacity ($0 \leq b \leq 1$), T is the length of a full charge or discharge cycle, and t_i^b is the total time during which energy is transferred from module i to the pack.

$$I_{pb} = \frac{\eta}{N} \sum_{i=1}^{N} I_i^b \tag{3}$$

$$I_i^b = bI \cdot \frac{t_i^b}{T} \tag{4}$$

Therefore, replacing (3) and (4) in (1) leads to an average battery current described by (5). The first term corresponds to the pack current, the second term to the balancing current extracted by the converter, and the third term to the sum of the currents injected by all modules back in the pack.

$$I_i = I - \frac{bIt_i^b}{T} + \frac{\eta bI}{NT} \sum_{i=1}^{N} t_i^b. \tag{5}$$

If the capacity of each battery, Q_i, $n_i Q_i$ is the usable charge of module i in a complete discharge cycle, where $0 \leq n_i \leq 1$. With the pack current held constant (6),

$$I_i T = n_i Q_i. \tag{6}$$

The combination of (5) and (6) makes the operation length equal to (7). From (1), (5) and (7), we can derive (8).

$$T = \frac{\Sigma_{i=1}^{N} n_i Q_i + bI(1-\eta)\left(\Sigma_{i=1}^{N}\right) t_i^b}{NI} \tag{7}$$

$$n_i Q_i = \frac{\Sigma_{i=1}^{N} n_i Q_i}{N} - bIt_i^b + \frac{bI\left(\Sigma_{i=1}^{N}\right) t_i^b}{I} \tag{8}$$

The length of operation T will always be less than or equal to the maximum possible time, which corresponds to the full utilization of batteries energy, i.e., $T \leq \frac{1}{NI}\Sigma_{i=1}^{N} Q_i$. Hence, the inequality (9) holds.

$$\sum_{i=1}^{n} (1 - n_i) Q_i - bI(1-\eta) \left(\sum_{i=1}^{n} t_i^b \right) \geq 0 \tag{9}$$

2.2. Series Cell-to-Pack

In the C2P series architecture, the current flowing through the module terminals (secondary of the converter) is equal to the pack current I and, from the power balance, the battery current I_i is (10),

$$I_i = I \cdot \frac{\eta V_i}{V_i^b} = I + I_i^b, \tag{10}$$

where V_i^b is the battery voltage and V_i is the module voltage, as indicated in Figure 3d. The balancing current, I_i^b, is modeled proportionally to an equivalent balancing time t_i^b (11), which is a function of the module and converter voltages (12).

$$I_i^b = I\frac{t_i^b}{T}, \tag{11}$$

$$\frac{t_i}{T} = \frac{\eta V_i - V_i^b}{V_i^b}. \tag{12}$$

The operation length (13) is obtained from (6), (10), and (11), and combining (1), (10) and (13) leads to (14).

$$T = \frac{\Sigma n_i Q_i - I\Sigma t_i^b}{NI} \tag{13}$$

$$0 = \frac{\Sigma n_i Q_i}{N} - \frac{I\Sigma t_i}{N} + It_i - n_i Q_i. \tag{14}$$

Finally, the length of operation T is less than or equal to the maximum possible time, just as in (9), which results in (15).

$$\sum_{i=1}^{n}(1-n_i)Q_i + I\sum_{i=1}^{n} t_i^b \geq 0 \tag{15}$$

2.3. Additional Bidirectional Buck Constraints

At first look, the bidirectional buck converter of [7] is simpler and cheaper than the proposed topology. However, it has important operational restrictions that limit the pack's extractable energy. The first one (16) is on the module terminal voltage V_i, which must be higher than in the battery voltage V_i^b and lower than an upper limit $V_i^{\max}$. A second restriction (17) must be considered when the bank is connected to a commercial charger to feed energy to the grid, because the bank voltage, ΣV_i, is also constrained to $NV_i^{b\max}$, where $V_i^{b\max}$ is the maximum battery voltage.

$$V_i^b \leq V_i \leq V_i^{\max} \tag{16}$$

$$\Sigma V_i \leq NV_i^{b\max} \tag{17}$$

Using (12), (16) and (17) are translated into the decision variable t_i^b constraints (18) and (19).

$$(\eta - 1)T \leq t_i \leq \left(\frac{V_i^{\max}}{V_i^b}\eta - 1\right)T \tag{18}$$

$$\Sigma t_i \leq TN\left(\frac{V_i^{b\max}}{V_i^b}\eta - 1\right) \tag{19}$$

2.4. Additional Back-to-Back Constraints

The proposed converter also has constraints on its terminal voltage, but they are less strict than the previous case. The output voltage can be as low as $0V$ and as high as the DC link voltage V_{dc} (20). The maximum bank voltage restriction also applies and it is necessary to consider a lower limit proportional to the battery minimum voltage, $V_i^{b\min}$; hence, (21).

$$0 \leq V_i \leq V_{dc} \tag{20}$$

$$NV_i^{b\min} \leq \Sigma V_i \leq NV_i^{b\max} \tag{21}$$

Using (12), (20) and (21) are translated into the decision variable t_i^b constraints (22) and (23).

$$-T \leq t_i \leq \left(\frac{V_{\mathrm{dc}}}{V_i^b}\eta - 1\right)T \tag{22}$$

$$TN\left(\frac{V_i^{b\min}}{V_i^b}\eta - 1\right) \leq \Sigma t_i \leq TN\left(\frac{V_i^{b\max}}{V_i^b}\eta - 1\right) \tag{23}$$

2.5. Linear Programming Optimization

The linear programming optimizations seek the decision variable vector **x** that minimizes $\boldsymbol{f}^T\mathbf{x}$, where **A** and $\mathbf{A_{eq}}$ are matrices, **B**, $\mathbf{B_{eq}}$, **lb**, and **ub** are vectors that define inequality, equality, and range constraints (24).

$$\min_{\mathbf{x}} \boldsymbol{f}^T\mathbf{x}, \text{such that} \begin{cases} \mathbf{A}\cdot\mathbf{x} \leq \mathbf{B} \\ \mathbf{A_{eq}}\cdot\mathbf{x} = \mathbf{B_{eq}} \\ \mathbf{lb} \leq \mathbf{x} \leq \mathbf{ub} \end{cases} \tag{24}$$

In this work, the decision variable is $\mathbf{x} = \left[t_1^b \cdots t_N^b\ n_1 \cdots n_N\right]^T$. Following the development of the previous sub-sections, **A** and **B** are derived from (9) and (15), $\mathbf{A_{eq}}$, and $\mathbf{B_{eq}}$ are derived from (8) and (14) for the parallel and C2P series architectures, respectively. The range $0 \leq n_i \leq 1$ applies to all architectures, while for the parallel C2P, $0 \leq t_i^b \leq T$ is valid, and for the C2P series, (18) and (19) must be considered for the bidirectional buck topology and (22), and (23) for the proposed back-to-back topology.

Once all matrices and vectors are defined, the *linprog*() MATLAB function processes the parameters to find the t_i^b and n_i, for $i \in [1, 2, \ldots N]$, which maximize the energy output $\Sigma n_i Q_i$, given a certain Q_i set, battery voltage, and charge/discharge current.

To assess the performance differences between the implementations, Figure 4 shows the evaluation of a 20-module bank in which the battery capacity is uniformly distributed in a range from 0.2 to 1.8 Ah, always with a mean capacity of 1 Ah and a discharge current of 1 A. For example, if the pack has three batteries and the capacity distribution is 0.4 Ah, the battery capacity will be 0.8 Ah, 1.0 Ah, and 1.2 Ah. Table 2 shows the remaining parameters employed.

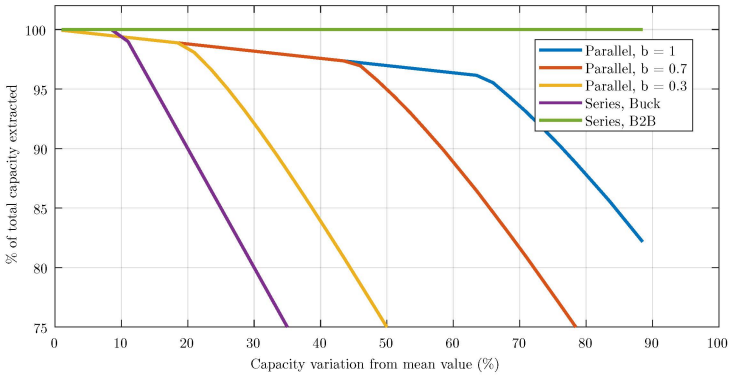


Figure 4. Bank extractable energy depending on the charge distribution and the implementation strategy.

The evaluation shows that the bidirectional buck converter is unable to extract full energy when the capacity distribution is 10%; when the distribution is 30%, it can only use 80% of the full capacity. The parallel C2P architecture performance has the influence of the converter current capacity modeled through the *b* parameter. For current capacities of $0.3I$, $0.7I$, and $1I$, the energy extracted starts to fall fast when the capacity distributions are 20%, 0.45%, and 0.65%, respectively. On the other hand, the proposed C2P series implementation can extract all of the bank energy for the capacity distribution evaluated. The tests with

different numbers of modules, capacities, and discharge currents returned similar results and are omitted.

Table 2. System parameters employed in linear programming.

Parameter	Value
Number of modules (N)	20
Battery-rated capacity (Q_i)	1.0 Ah
Battery-rated voltage ($V_i^{b\max}$)	12.0 V
Battery's maximum voltage ($V_i^{b\max}$)	14.0 V
Battery's minimum voltage ($V_i^{b\min}$)	9.0 V
Converter efficiency	90%
Discharge current (I)	1.0 A

This result shows that the proposed solutions are only able to extract the entire energy available in a battery bank, independent of the capacity and state of health of each module. This is important, as the batteries degrade differently over time, which tend to cause their capacities to drift apart, as already discussed. Another typical application is the second life of a battery bank since its elements naturally have heterogeneous capacities and *SoH*.

Another benefit is the opportunity to replace the batteries individually as they reach their end of life, as the other solutions are unable to cope with the large capacity differences that will appear as new batteries are introduced in banks with old ones. To evaluate this latter case of a bank with old batteries (that has a few replaced by new ones), the results of the linear programming are presented in Figure 5. A bank with 20 batteries is considered and the old batteries have a mean capacity of 0.7 Ah with a uniform distribution of ±0.10 Ah. To this bank, x new batteries replace the old ones, each with a mean capacity of 1.0 Ah with a uniform distribution of ±0.02 Ah. The graph shows the percentage of the total stored energy that the system can extract depending on the architecture adopted. Again, the proposed architecture using the back-to-back converter is the only one that can fully utilize the bank in all conditions. The parallel architecture also reaches high utilization, as long as the converter rating is high enough (in the simulated case, with a b > 0.35). The series architecture with a step-up converter has the worst performance when 12% of energy is not reachable when the bank is half old–half new.

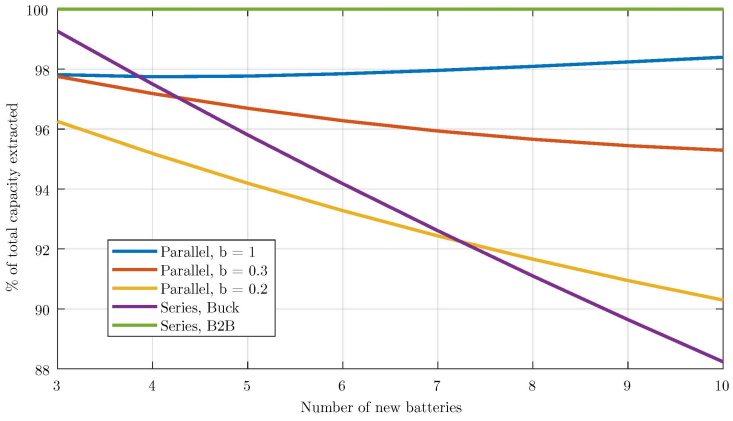


Figure 5. Percentage of energy extracted from a bank with 20 batteries depending on the system architecture, when the new batteries change (x-axis).

The results obtained with the linear programming optimization show that the proposed solution performs better if compared with the other architectures proposed so far and brings high flexibility to the systems, opening up possibilities, such as replacing EoL batteries, which are often ignored.

3. Converter Design

The topology proposed for the converter is a back-to-back interleaved H-bridge converter. The battery's front end (*BFE*) is the converter at the battery side, and the rectifier's front end (*RFE*) is the converter at the rectifier side (Figure 2). The following sub-sections address the relevant converter design and performance issues. Table 3 summarizes the main converter parameters.

Table 3. BFE and RFE converter parameters.

Parameter	Value
MOSFET part number	BSC007N04LS6
Rated terminal voltage	12 V
Leg inductor	10 µH
BFE/RFE capacitor	12 mF
DC capacitors	24 mF
Switching frequency	75 kHz
Sampling frequency	18.8 kHz

3.1. Power Losses

The converter operates with complementary pulses to the half-bridge switches, causing the inductor current to be in a continuous mode and to always flow through the *MOSFET*s (active rectification).

3.1.1. Semiconductor Losses

The total losses of *MOSFET* (25) are the sum of conduction and switching losses, calculated with (26) and (27)–(29), respectively, and the diode switching losses, due to reverse recovery, from (30), where R_{on} is the *MOSFET* on resistance, f_{sw} is the switching frequency, V_{dc} is the DC link voltage, I_{on} and I_{off} are the *MOSFET* switching currents at turn on and turn off, respectively, Q_{rr} is the reverse recovery charge, tri, tru, tfu, and tfi are the rise and fall times calculated according to [25]. The diode conduction losses are irrelevant due to the active rectification.

$$P_{loss} = P^{Q}_{cond} + P^{Q}_{sw} + P^{D}_{sw}, \tag{25}$$

$$P^{Q}_{cond} = D \cdot R_{on} \cdot I^{2}_{rms}, \tag{26}$$

$$P^{Q}_{sw} = \left(E^{Q}_{on} + E^{Q}_{off}\right) \cdot f_{sw}, \tag{27}$$

$$E^{Q}_{on} = V_{dc} \cdot I_{on} \cdot \frac{tri + tfu}{2} + Q_{rr} \cdot V_{dc}, \tag{28}$$

$$E^{Q}_{off} = V_{dc} \cdot I_{off} \cdot \frac{tru + tfi}{2}, \tag{29}$$

$$P^{D}_{sw} = \frac{1}{4} \cdot Q_{rr} \cdot V_{dc} \cdot f_{sw}. \tag{30}$$

The semiconductor's power losses were calculated for different Infineon *MOSFET*s assuming a switching frequency in the range of 50–100 kHz and a converter with up to five legs. The results, presented in Figure 6, show that a single-leg converter would result in junction temperatures higher than 150 °C and, consequently, failure. Among the devices considered, the BSC007N04LS6 consistently leads to the lowest losses. This device, a member of the Infineon OptiMOS 6 family, has 40 V of blocking voltage, drain-source resistance of 0.7 mΩ, and a gate charge of 94 nC. The DC link is set at half of the rated blocking voltage, i.e., 20 V. If one considers natural cooling and only the PCB pads as heatsinks, the estimated thermal resistance junction ambient is 50 °C/W.

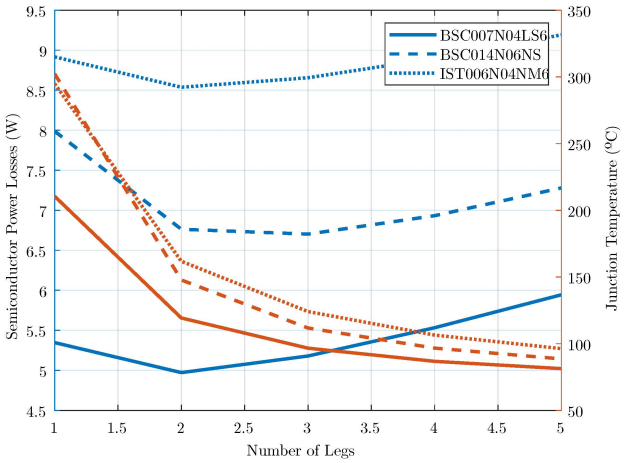


Figure 6. Semiconductor power losses (blue lines) and the estimated junction temperature (red lines).

3.1.2. Inductor Selection and Losses

The inductor specification is derived from the DC link voltage, switching frequency, and current ripple (31). The worst-case ripple happens when the leg's duty cycle is 0.5, but at the converter output, it will depend on the number of legs. The maximum current ripple at the capacitor is $\Delta I_C = \frac{\Delta I}{n}$, where n is the number of legs.

$$\Delta I_{\mathrm{L}} = \frac{D \cdot (1 - D)}{L \cdot f_{\mathrm{sw}}} \cdot V_{\mathrm{dc}}. \tag{31}$$

The selected off-the-shelf inductor is type PQ2614BLA from Bourns. This is a family of shielded power inductors that has low DC resistance, flat wirewound construction, and the lowest costs among the considered components. These inductors can carry up to 30 A_{RMS} and have saturation currents above the requirement of $\frac{50}{n} + \Delta I$ Amps for inductances between 1 μH and 10 μH (a ripple between 200% and 20%). All inductors have a DCR of 1.29 mΩ. The core losses can be neglected [7], and the current ripple has minor effects on the converter's total losses. Hence, the selected component was the PQ2614BLA-100K with 10 μH of inductance, allowing the lowest ripple at no extra cost.

3.1.3. Partial Load Efficiency Improvement

A multi-leg interleaved converter has several advantages over the conventional ones, such as an equivalent higher switching frequency, increased load handling capacity, and smaller passive components. Another benefit is higher efficiency under a partial load, achieved by reducing the number of switching legs depending on the load's current level. Figure 7 shows the efficiency of the converter when one, two, and all three legs are switching, where the benefit of reducing the number of switching legs becomes evident (the efficiency with a lower number of switching legs is higher, independent of the load current).

The efficiency of the converter with a single switching leg is the highest (up to a load current of 33 A). Temperature restrictions imply the switching of a second leg at loads higher than 18 A, keeping T_j under 100 °C. As a drawback, the overall converter efficiency falls from 97.8% to 96.8%. From the power losses and temperature rise estimations, the switching of the third leg is unnecessary; in fact, it decreases the converter efficiency even more. However, the selected inductor saturates at load currents higher than 40 A. Despite the lower efficiency, the third leg is switched beyond this current level and the efficiency falls from 97.5% to 96.8%. On the other hand, the power semiconductors work at lower temperatures, with a positive impact on the converter's reliability. Hence, the activations of the second and third legs happen when the load currents are 18 and 40 A, respectively, but the deactivation occurs at lower levels to implement a hysteresis (see Table 4) and prevent frequent changes in the number of active legs.

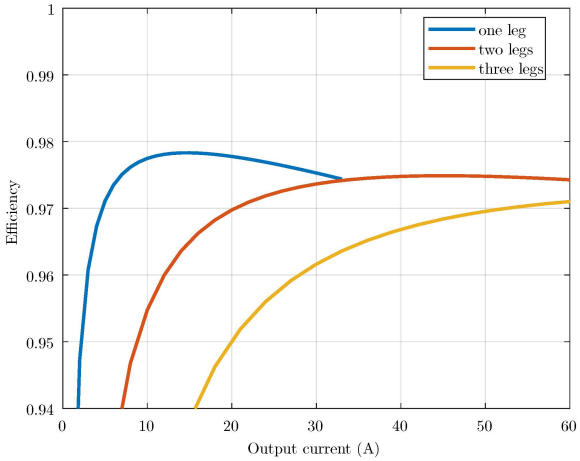


Figure 7. Full converter efficiency with one, two, or three switching legs.

Table 4. Current level threshold to activate or deactivate a leg.

Leg	Activate	Deactivate
1	>0 A	
2	>18 A	<15 A
3	>40 A	<35 A

4. Control

The smart battery system has a hierarchical control, with a local controller at each smart battery module and a central controller. During operation, the central controller (*CC*) receives values of the voltage, current, and temperature from each battery through the communication bus. It then calculates *SoC* and, based on historical data, it estimates *SoH*. Because the load demand is known, the *CC* calculates the RFE voltage references to reach optimum battery throughput and maximum bank capacity.

The local controller (on both the *BFE* and *RFE*) implements an inner loop to regulate the inductor currents, i_{L}. In the *BFE*, an outer loop controls the DC link voltage, v_{DC}. As a consequence, the battery current follows the power balance, i.e., $P_{\mathrm{RFE}} \approx P_{\mathrm{BFE}}$. The *RFE* seeks to emulate the voltage source behavior of a battery by controlling the terminal voltage v_{RFE}.

By modeling the converter as an equivalent single-leg circuit, Figure 8, the inductor current (32), DC link (33), and RFE terminal voltage dynamics (34) can be extracted,

$$i_{\mathrm{L}} = \frac{v_{\mathrm{t}} - v_{\{\mathrm{BFE,RFE}\}}}{sL_{\mathrm{eq}}}, \tag{32}$$

$$v_{\mathrm{dc}} = \frac{i_{\mathrm{in}} - D_1 i_L}{sC_{\mathrm{dc}}}, \text{and} \tag{33}$$

$$v_{\mathrm{RFE}} = \frac{i_L + i_r}{sC_1}, \tag{34}$$

where L_{eq} is the equivalent inductor equal to the leg inductor divided by the number of legs; v_{t} is the half-bridge synthesized voltage; $v_{\{\mathrm{BFE,RFE}\}}$ is either the battery or the RFE voltage; i_{in} and i_r are disturbance currents flowing to the DC link and the filter capacitor C_1, respectively; D_1 is the converter's duty cycle at the analyzed point of operation; and C_1 and C_{DC} are the RFE and DC link capacitors, respectively. Figure 9a–c show the block diagram of the inductor current, DC link voltage, and RFE voltage control loops, respectively.

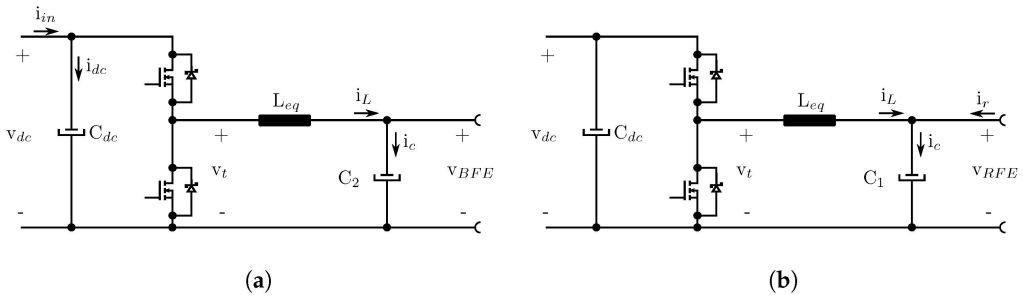


Figure 8. (**a**) Equivalent converter circuit diagram: (**a**) *BFE* and (**b**) *RFE*.

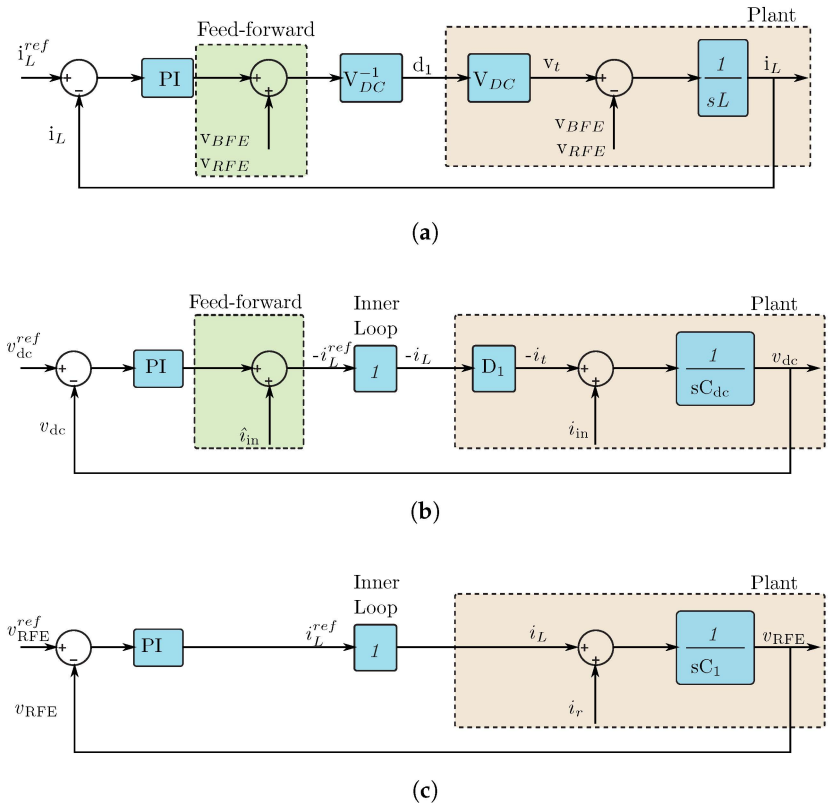


Figure 9. Control loops: (**a**) inductor current, (**b**) DC link voltage control loop, and (**c**) RFE terminal voltage control loop.

The control loops use proportional–integral controllers with feed-forward terms, one at the current loops and another at the DC link voltage loop. The first term is the measured battery or RFE voltage (Figure 9a) and the second term is the calculated input current reflected at the low side, $\hat{\imath}_{in}$, calculated assuming the power balance between BFE and RFE (Figure 9b). The control loop tuning employed pole placement using the parameters listed in Table 5.

Table 5. Controller-tuning parameters.

Parameter	Value
Inductor current bandwidth	930 Hz
DC link voltage bandwidth	62 Hz
RFE voltage bandwidth	75 Hz
Inductor current phase margin	40°
DC link voltage phase margin	84.4°
RFE voltage phase margin	84.4°

Current Equalization

In addition to the main converter controller, it is necessary to include a loop to equalize the converter leg currents. The selected approach uses the current from one leg as the reference and calculates the differences between the currents in each of the remaining legs and the reference one. The error is multiplied by a constant that produces a ΔD to modify the leg's duty cycle (35).

$$\Delta D_i = K_{eq} \cdot \left(i_{Lref} - i_{Li} \right). \tag{35}$$

This approach has some interesting advantages. First, it reduces the microcontroller load, since the number of control loops is constant and independent of the number of legs; second, under a partial load, it simply enables or disables the leg-switching pulses. Once a leg starts switching, the equalization control loop takes care of the current sharing.

5. Experimental Results

A prototype was built, which comprises two boards: a control board, *SB_CTRL*, and a power board, *SB_POWER*. The module prototype is connected to a lead acid 240 Ah battery (Figure 10) and the main system characteristics and converter parameters are summarized in Tables 3 and 6.

Figure 10. Test set-up with three smart battery modules in the series.

Table 6. System characteristics.

Parameter	Value
Rated terminal voltage	12 V
DC link voltage	20 V
Rated input/output current	50 A

A series of experiments were conducted in order to evaluate the electronic boards and the proposed control. The *SB_CTRL* was first tested using a hardware-in-the-loop (*HiL*) platform and the results are presented in Figure 11. The adopted equipment is a Typhoon HiL model 604. This step was used to develop the firmware of the system. Moreover, the HiL was used for the long-term discharge and charge operation and validation. The *HiL* simulations included a complete SB bank, such that the *CC* software was also validated prior to the tests in the power bank [12]. As an example, the *HiL* simulation validates the control response to a load transient that causes the second leg to start switching. Figure 11 shows the regulation of the RFE and DC link voltage, where I_{L4} and I_{L5} are the leg currents

of the BFE converter and I_{L1} and I_{L2} of the RFE converter. It also demonstrates that the second leg enters the switching mode seamlessly, as seen by the external quantities.

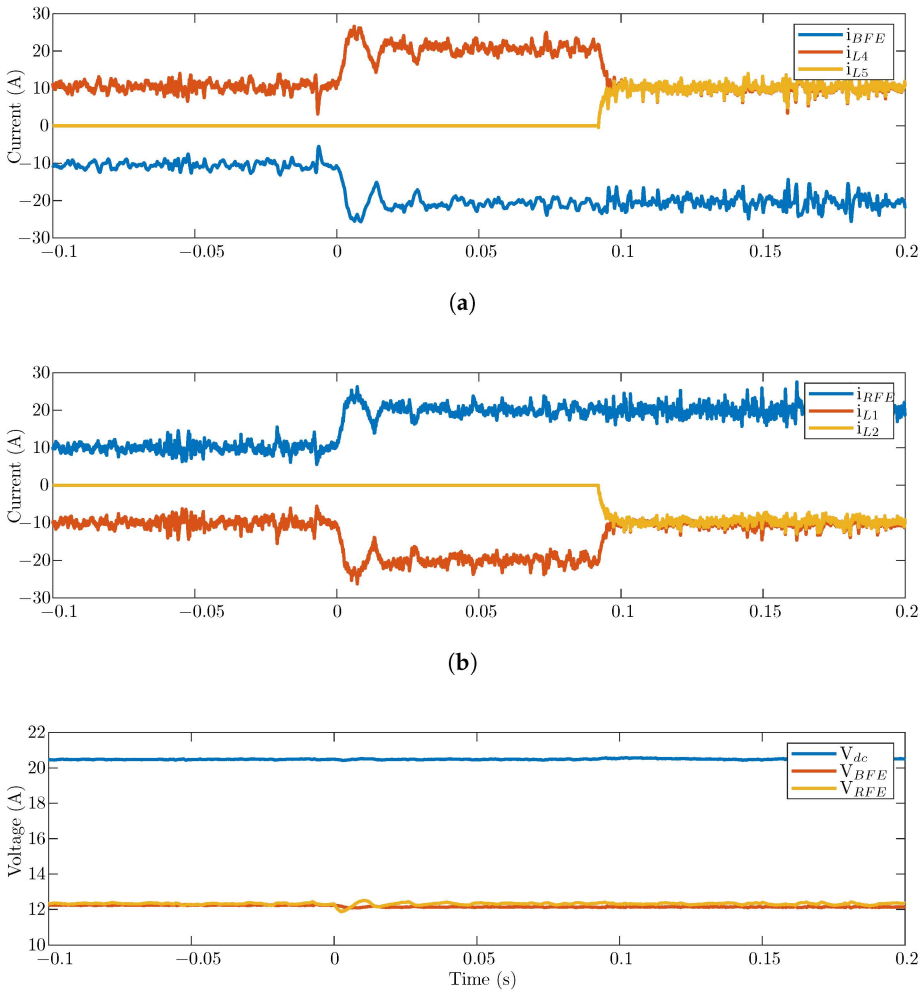
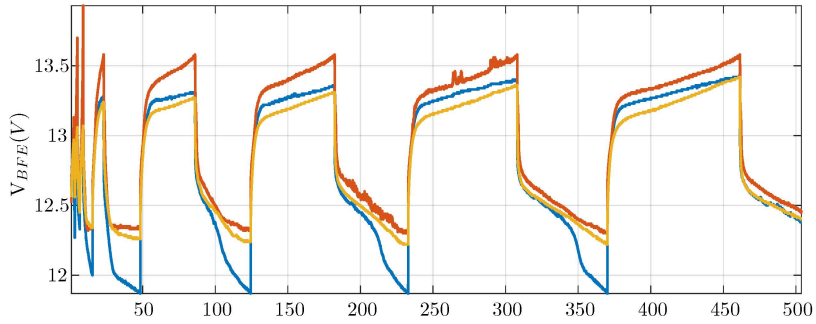


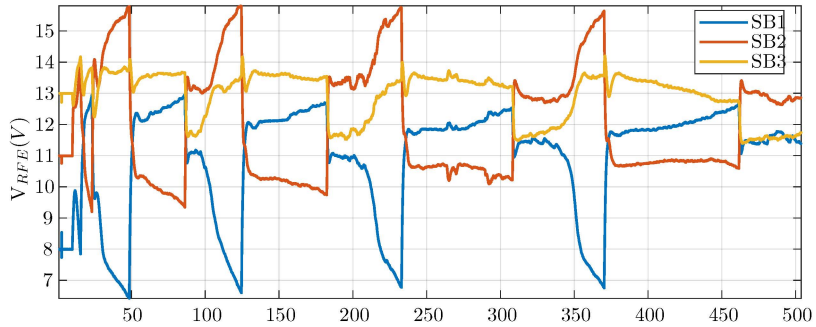
Figure 11. Converter response to a load step from 10 to 20 A. As the controller updates the RMS current value, it turns the second leg on and handles the current sharing, disturbing the terminal voltages. (**a**) BFE currents; (**b**) RFE currents; (**c**) BFE, DC, and RFE voltages.

After the HiL validation, the firmware and control implementation were tested through an experimental setup consisting of a power bank with three series-connected SB modules and the central controller. Figure 12 presents the results of a long-term experiment using lead acid batteries with a capacity of 240 Ah (C20), model 12MS234, manufactured by Moura. The initial conditions of the experiment were set, such that the battery of SB2 was near full charge, SB1 was only half-charged, and the SB3 charge was between the other two.

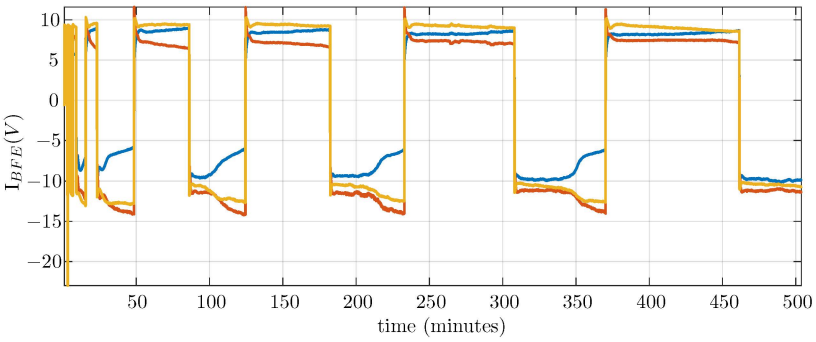
The experiment consisted of the power bank subjected to 10 A constant current charge/discharge cycles imposed by a DC controllable power source. Initially, for up to 10 min (see the expanded view of the battery currents in Figure 12d), the control balance was disabled. Watching the battery terminal voltage (V_{BFE}), it was noticeable that capacities were uneven between elements. When an element reached its maximum voltage, the entire system stopped charging and started to discharge. Likewise, when an element reached its minimum voltage, it started to recharge.



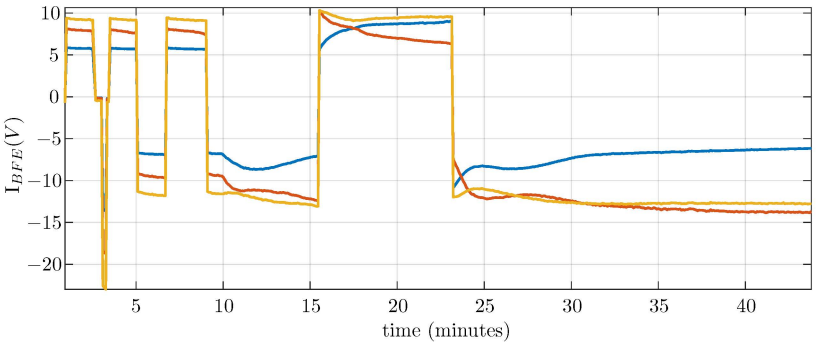
(**a**)



(**b**)



(**c**)



(**d**)

Figure 12. Experimental results with three SB modules in series being charged and discharged: (**a**) BFE voltages; (**b**) RFE voltage; (**c**) BFE current; (**d**) BFE currents during the initial cycles with the active balancing disabled (t < 10 min).

During the first cycles, SB2 quickly hit its full charge (*SoC* 95%). This behavior is shown by the red line of V_{BFE}. During discharging, SB1, presented by the blue line of V_{BFE}, quickly reached the limit of discharge (*SoC* 50%).

After those initial cycles, the active balancing was enabled and it started to modify the V_{RFE} voltage references, such that during discharge, the battery with higher *SoC* delivered the larger current and, during charge, the battery with lower *SoC* obtained a larger current. Notice that the control actions on the RFE voltages set the proper charges supplied/drawn from each battery.

The cycle after the system managed to balance the charge in the batteries. The discharge time of the bank significantly increased from 25.2 min at the first cycle ($23.2 < t < 48.45$) to 62.1 min ($308.1 < t < 370.2$). Since the discharge current and the power bank voltage were held constant (10 A and 36 V), the total energy delivered was directly proportional to the discharge time. After several cycles, the bank discharge time exceeded 100 min. This experiment demonstrates that the proposed strategy allows extracting 38.8 times more energy from the same battery bank when compared to the operational equivalent in a passive bank.

6. Conclusions

Power electronics can increase a battery energy storage system's lifespan, performance, and efficiency, as well as reduce investment costs. This paper proposes the use of a back-to-back converter in a series of cell-to-pack architectures. A quantitative evaluation using linear programming proved that this implementation can extract full energy from the bank even when the battery capacities are spread over a wide range—a feature that is absent in other proposed solutions found in the literature.

The proposed solution simplifies the module's integration and has several other benefits, such as easy assembly and customization, higher system reliability, and the possibility to downgrade the power bank performance while waiting for maintenance. Furthermore, the ability to operate the BESS with heterogeneous storage elements, i.e., batteries of different technologies or ages (new batteries together with old ones), from several manufacturers, reduces operational costs, since only elements that reach end-of-life have to be replaced, and the bank owner can select the battery with the best cost–benefit ratio at the time of the replacement.

This work presents the technological perspectives of the converter and control design. Moreover, a prototype was built and validated through experimental results. A three-series module power bank was built, showing how the battery's energy storage capacity utilization is greatly improved with the proposed solution. The strategy of reducing the number of switching legs improves the efficiency under a partial load and reduces the impacts of losses regarding the module's overall performance. It is important to highlight that the SB bank can deliver much more energy than a passive one.

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Conflicts of Interest: The authors declare no conflict of interest.

References

1. Chatzinikolaou, E.; Rogers, D.J. A Comparison of Grid-Connected Battery Energy Storage System Designs. *IEEE Trans. Power Electron.* **2017**, *32*, 6913–6923. [CrossRef]
2. Szalai, T.; Schwalbe, U.; Schilling, M.; Endert, F.; Heidrich, T.; Ivanov, S.D. Design of an active battery management system for electric vehicles. In Proceedings of the PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 20–22 May 2014; pp. 1–8.
3. Lehner, S.; Baumhöfer, T.; Sauer, D.U. Disparity in initial and lifetime parameters of lithium-ion cells. *IET Electr. Syst. Transp.* **2016**, *6*, 34–40. [CrossRef]
4. Gräf, D.; Marschewski, J.; Ibing, L.; Huckebrink, D.; Fiebrandt, M.; Hanau, G.; Bertsch, V. What drives capacity degradation in utility-scale battery energy storage systems? The impact of operating strategy and temperature in different grid applications. *J. Energy Storage* **2022**, *47*, 103533. [CrossRef]
5. Rogers, D.J.; Aslett, L.J.; Troffaes, M.C. Modelling of modular battery systems under cell capacity variation and degradation. *Appl. Energy* **2021**, *283*, 116360. [CrossRef]
6. Ci, S.; Lin, N.; Wu, D. Reconfigurable battery techniques and systems: A survey. *IEEE Access* **2016**, *4*, 1175–1189. [CrossRef]
7. Li, Y.; Han, Y. A Module-Integrated Distributed Battery Energy Storage and Management System. *IEEE Trans. Power Electron.* **2016**, *31*, 8260–8270. [CrossRef]
8. Fares, A.M.; Klumpner, C.; Sumner, M. Optimising the structure of a cascaded modular battery system for enhancing the performance of battery packs. *J. Eng.* **2019**, *2019*, 3862–3866. [CrossRef]
9. Hu, X.; Zou, C.; Zhang, C.; Li, Y. Technological developments in batteries: A survey of principal roles, types, and management needs. *IEEE Power Energy Mag.* **2017**, *15*, 20–31. [CrossRef]
10. Puviwatnangkurn, W.; Tanboonjit, B.; Fuengwarodsakul, N.H. Overcurrent protection scheme of BMS for Li-Ion battery used in electric bicycles. In Proceedings of the 2013 10th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology, Krabi, Thailand, 15–17 May 2013; pp. 1–5.
11. Buccolini, L.; Ricci, A.; Scavongelli, C.; DeMaso-Gentile, G.; Orcioni, S.; Conti, M. Battery Management System (BMS) simulation environment for electric vehicles. In Proceedings of the 2016 IEEE 16th International Conference on Environment and Electrical Engineering (EEEIC), Florence, Italy, 7–10 June 2016; pp. 1–6.
12. Alexandre Carvalho Maia, T.; Berrehil El Kattel, M.; Perpetuo Corrêa, T.; Rocha, A.V.; Filho, B.J.C. Battery energy management proposition for energy storage using active dc–dc converter. *Int. J. Circuit Theory Appl.* **2022**, *50*, 4325–4341. [CrossRef]
13. Chatzinikolaou, E.; Rogers, D.J. Performance Evaluation of Duty Cycle Balancing in Power Electronics Enhanced Battery Packs Compared to Conventional Energy Redistribution Balancing. *IEEE Trans. Pow. Electr.* **2018**, *33*, 9142–9153. [CrossRef]
14. Ghaeminezhad, N.; Ouyang, Q.; Hu, X.; Xu, G.; Wang, Z. Active Cell Equalization Topologies Analysis for Battery Packs: A Systematic Review. *IEEE Trans. Power Electron.* **2021**, *36*, 9119–9135. [CrossRef]
15. Li, Y.; Jones, E.A.; Wang, F. The Impact of Voltage-Balancing Control on Switching Frequency of the Modular Multilevel Converter. *IEEE Trans. Power Electron.* **2016**, *31*, 2829–2839. [CrossRef]
16. Yarlagadda, S.; Hartley, T.T.; Husain, I. A Battery Management System Using an Active Charge Equalization Technique Based on a DC/DC Converter Topology. *IEEE Trans. Ind. Appl.* **2013**, *49*, 2720–2729. [CrossRef]
17. Chen, Y.; Liu, X.; Shen, T.; Cheng, L.; Wang, X.; Yang, R.; Yang, S. An any-cell(s)-to-cell(s) equalization method with a single magnetic component for Lithium-ion battery pack. *J. Energy Storage* **2021**, *33*, 102071. [CrossRef]
18. Liao, L.; Chen, H. Research on two-stage equalization strategy based on fuzzy logic control for lithium-ion battery packs. *J. Energy Storage* **2022**, *50*, 104321. [CrossRef]
19. Uno, M.; Kukita, A. Bidirectional PWM converter integrating cell voltage equalizer using series-resonant voltage multiplier for series-connected energy storage cells. *IEEE Trans. Power Electron.* **2014**, *30*, 3077–3090. [CrossRef]
20. Kim, C.H.; Kim, M.Y.; Moon, G.W. A modularized charge equalizer using a battery monitoring IC for series-connected Li-ion battery strings in electric vehicles. *IEEE Trans. Power Electron.* **2012**, *28*, 3779–3787. [CrossRef]
21. Lim, C.S.; Lee, K.J.; Ku, N.J.; Hyun, D.S.; Kim, R.Y. A modularized equalization method based on magnetizing energy for a series-connected lithium-ion battery string. *IEEE Trans. Power Electron.* **2013**, *29*, 1791–1799. [CrossRef]
22. Mestrallet, F.; Kerachev, L.; Crebier, J.C.; Collet, A. Multiphase interleaved converter for lithium battery active balancing. *IEEE Trans. Power Electron.* **2013**, *29*, 2874–2881. [CrossRef]
23. Majmunovic, B.; Sarda, R.; Teodorescu, R.; Lascu, C.; Ricco, M. Highly efficient smart battery pack for EV drivetrains. In Proceedings of the Vehicle Power and Propulsion Conference (VPPC), Belfort, France, 14–17 December 2017; pp. 1–5.
24. Ji, F.; Liao, L.; Wu, T.; Chang, C.; Wang, M. Self-reconfiguration batteries with stable voltage during the full cycle without the DC-DC converter. *J. Energy Storage* **2020**, *28*, 101213. [CrossRef]
25. Graovac, D.; Purschel, M.; Kiep, A. MOSFET power losses calculation using the data-sheet parameters. *Infineon Appl. Note* **2006**, *1*, 1–23.