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Review

Topology Review of Three-Phase Two-Level Transformerless Photovoltaic Inverters for Common-Mode Voltage Reduction

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Abstract: In grid-connected photovoltaic (PV) systems, a transformer is needed to achieve the galvanic isolation and voltage ratio transformations. Nevertheless, these traditional configurations of transformers increase the weight, size, and cost of the inverter while decreasing the efficiency and power density. The transformerless topologies have become a good solution. However, the problem is that commode-mode voltage and leakage current can occur via the stray capacitors between the PV array and the ground of the inverter. Various transformerless inverters have been introduced with different techniques, such as reducing the common-mode voltage or eliminating the leakage current. Furthermore, to introduce the development of transformerless PV inverters, especially in three-phase two-level inverter systems, this paper provides a comprehensive review of various common-mode voltage reduction three-phase two-level inverters.

Keywords: common-mode voltage; transformerless topology; three-phase two-level inverter; leakage current; review

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1. Introduction

Nowadays, renewable energy sources play a key role in supporting the power system to adapt the ever-increasing load demand. Among the renewable energy sources, the PV source is considered as one of the most effective solutions due to its relatively small size, clean energy, noiseless operation, and simple installation [1–4]. To connect the PV array with a utility grid, grid-connected inverters are widely used for the PV systems and are divided into the transformer-based and transformerless topologies [4–9]. The use of a high-frequency transformer on the DC side or a low-frequency, bulky transformer in the AC side can be employed to ensure the safety issue with the galvanic isolation between the output and input sides [10–12]. Nevertheless, transformer-based topologies are heavy, high-cost, and high-loss. The efficiency of the transformerless inverter can improve by up to 2%. Therefore, transformerless topologies have been developed in both academic and industrial fields [13–18]. Voltage source inverters (VSIs), especially three-phase two-level transformerless topologies, are the most common solution to convert the DC voltage to AC voltage in any power system, with their merits of being low-cost, easy to implement, and mature technology. However, the disadvantage of transformerless topologies is the connection of the PV array to the grid without galvanic isolation. So, international agencies have regulated some broadly approved standards for PV inverters, which should be considered to avoid safety concerns. The main reason for these safety concerns is the presence of large stray capacitance (C_{PV}) between the PV panel and the

ground of the grid. As highlighted in Figure 1, a direct ground–current path may form between the grid and the PV panel. Due to the presence of large stray capacitance between the PV panel and grid grounds, the common-mode voltage (CMV) can appear, and the leakage current is originated from CMV fluctuations. Then, the leakage current flows through the ground and PV array, which leads to increased radiated electromagnetic emissions, higher current harmonics, and losses and low reliability of the transformerless, grid-connected PV transformerless inverter topologies [19–21]. Considering these issues, the leakage current should be carefully managed. The leakage current must be less than the VDE standard of 300 mA to prevent the unfavorable effects in VDE 0126-1-1. The leakage current can be suppressed by reducing the amplitude and frequency of the CMV or breaking the PV array from the grid on the DC side of the inverter system. In recent years, many approaches have been made to overcome the CMV and leakage current in transformerless PV inverters [21–38].

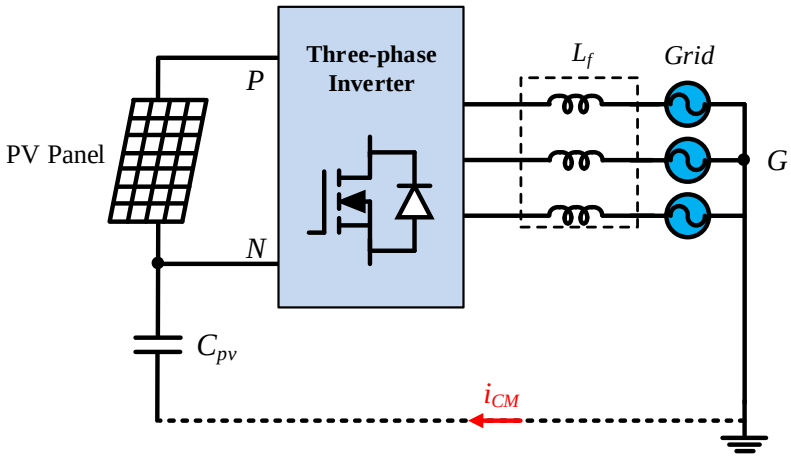


Figure 1. Typical three-phase transformerless VSI configuration using an *L*-filter.

The SVM control method is generally implemented to control the traditional three-phase two-level H6 VSI. Figure 2 shows the circuit and SVM diagram of the traditional three-phase two-level H6 VSI. It can be seen that eight possible combinations are synthesized of six active and two zero voltage vectors, as depicted in Table 1. Moreover, the CMV can be defined as the average of the voltages between the three-phase voltages, A-N, B-N, and C-N, and (1) and the CMV in each state are calculated in Table 1.

$$V_{CM} = V_{GN} = \frac{V_{AN} + V_{BN} + V_{CN}}{3} \tag{1}$$

There are several review papers reported in the literature which cover the topology modifications and PWM methods for CMV reduction in three-phase VSIs [27,37–40]. In the review study [27], the CMV in an electric drive fed by a conventional three-phase two-level inverter is described and a review of CMV reduction methods is presented. The PWM methods for CMV reduction in three-phase two-level transformerless inverters are discussed in [37–40] to demonstrate the effectiveness of the compared solutions. Generally, these review papers only focused on the traditional three-phase two-level transformerless inverters with a buck-type topology. Moreover, the prior-art solutions for traditional VSIs are not suitable for the impedance-source-based inverters system. Hence, the review solutions for CMV reduction in the impedance-source-based in VSIs are presented in [41]. However, not many different comparisons have been conducted in this review paper. Investigating the latest research in both traditional VSIs and impedance-source-based VSIs, the review and classification of three-phase two-level transformerless inverters have been studied in this paper to present a clear picture of the investigation of the three-phase two-level transformerless PV inverters for CMV reduction. For each category of three-

phase two-level transformerless inverters, several general inverter topologies of them are illustrated, and each inverter has been examined from different perspectives, such as the number of components, modulation index operating range, CMV reduction, boosting voltage capability, etc. The rest of this paper is organized as follows. Section 2 presents the classification of three-phase two-level transformerless topologies. A broad classification and discussion of different traditional three-phase two-level transformerless inverter topologies are given in Section 3. Section 4 provides the structure of major impedance-source-networks-based topologies with the comparison between them based on the merits and demerits. Finally, Section 5 gives the concluding remarks.

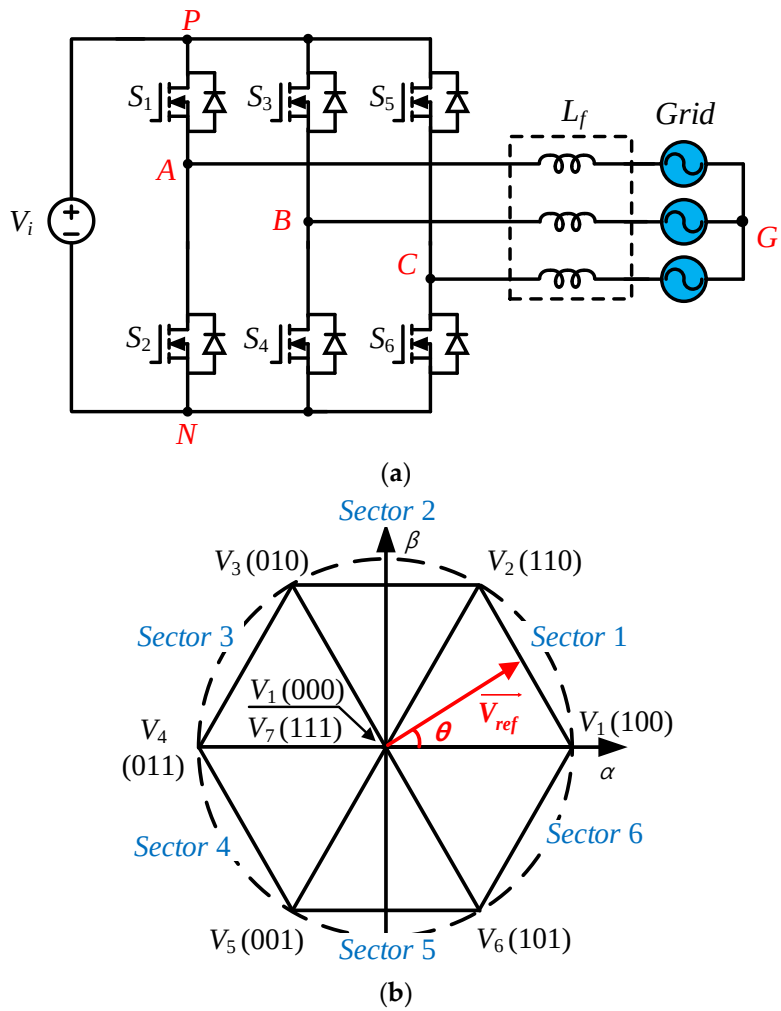


Figure 2. Traditional three-phase two-level voltage-source H6 inverter: (**a**) H6 inverter topology; (**b**) space vector modulation (SVM) diagram.

Table 1. Common-mode voltage of traditional H6 topology.

Switching State	Bridge States	*CMV* Value
M0	000	0
M1	100	$V_{PN}/3$
M2	110	$2V_{PN}/3$
M3	010	$V_{PN}/3$
M4	011	$2V_{PN}/3$
M5	001	$V_{PN}/3$
M6	101	$2V_{PN}/3$
M7	111	V_{PN}

2. Classification of Three-Phase Two-Level Transformerless Topologies for CMV Reduction

Compared with CSIs, the VSIs will be more dominant in the PV-grid-connected inverter systems because of their advantages of easy control, cost-effectiveness, and being a mature technology [42–52]. However, the traditional three-phase two-level voltage-source H6 inverter cannot provide the boost capability. Thus, an additional boost from a DC–DC converter or new topologies with added extra components can be used to boost the low input DC voltage to high DC-link voltage [53–57]. Moreover, a deadtime should be inserted in the H-bridge switches to avoid the short-circuiting of the DC-link bus. This leads to an increase in the THD value at the AC output voltage [58,59]. These days, single-stage, impedance-source inverter topologies [60–70] have been introduced and developed with buck-boost ability and improve reliability. In a transformerless PV inverter, the common mode voltage will be produced while the inverter is being worked and results in the high-leakage current on the capacitor C_{PV} [71,72]. In order to suppress the leakage current, the common mode voltage should be reduced or kept constant. To reduce the CMV for the traditional three-phase two-level H6 VSIs, both the PWM control methods [30–38] and system topology reconfiguration [42–57] are introduced. In addition, the solutions for the CMV reduction of the impedance-source inverter topologies were also developed. Moreover, by considering the number of active switches in the impedance-source network, these inverters can be classified into passive types [71–79] and active types in [80–83]. As a result, the transformerless three-phase two-level VSIs with CMV reduction can be classified into the traditional VSI group and impedance-source-based group. The overview of the several existed topologies is summarized and presented in Figure 3. The comprehensive comparison and discussion will be presented in the following sections.

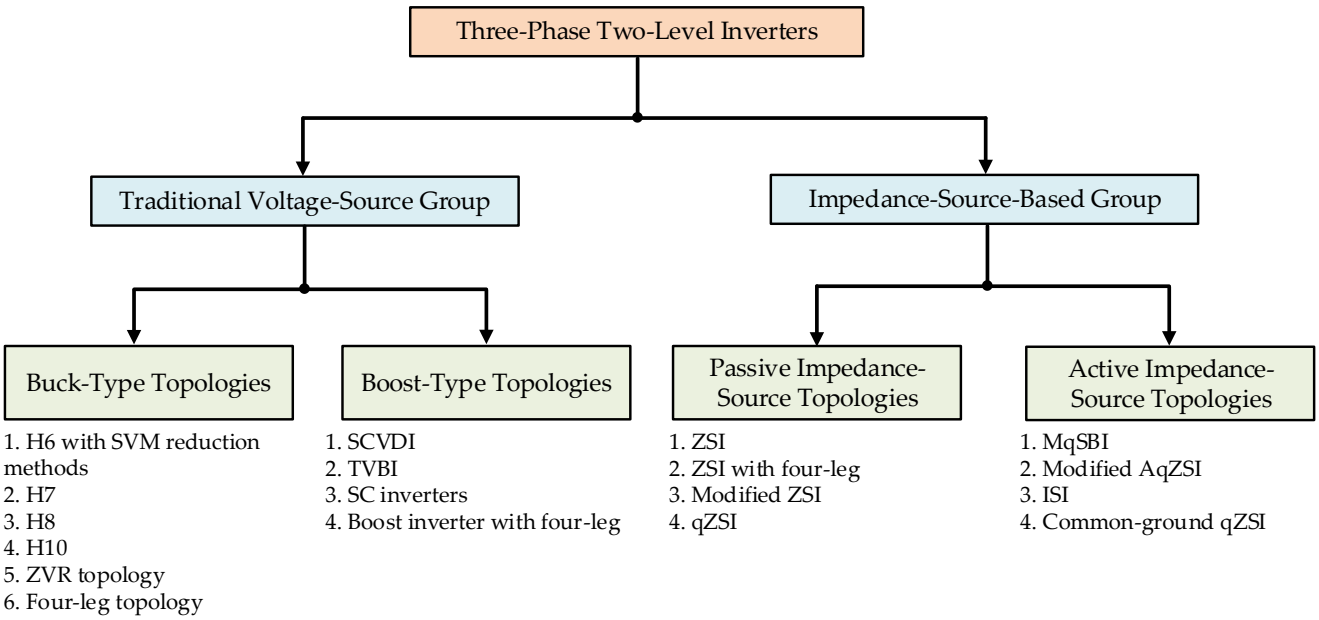


Figure 3. Classification of three-phase, two-level inverter topologies.

3. Traditional Voltage Source Topologies

3.1. Buck-Type Topologies

From the CMV values listed in Table 1, the CMV of the traditional three-phase two-level H6 VSI can be reduced to one high CMV level by only applying six active states. Various PWM technique modifications for CMV reduction have been presented. This section will briefly present some SVM methods, such as the traditional modulation-based CMV reduction methods. In the active zero-state SVM method introduced in [30,31], the zero states can be replaced by two opposite active states. The near-state SVM method is

implemented with three adjoining states [32]. The traditional three-phase two-level H6 VSI with these SVM methods can effectively decreases the CMV amplitude to 33% of DC-link voltage. The active zero-state PWM and near-state PWM methods, and the remote-state SVM method in [33], can offer the constant CMV by using only the three active states in the odd active or even vectors. Moreover, the combination of other states can be applied to reduce the amplitude value of CMV, introduced in [34–36]. However, this solution limits modulation index range and output voltage quality, which reduces the output quality of the inverter. The overview of these control methods is also discussed in [37–41].

Moreover, the inverter structure can be changed and introduced by modifying some components for the CMV reduction, as shown in Figure 4. For example, the H7 topology was introduced in [42,43] to limit the CMV of $V_{PN}/3$. An extra switch was added to positive DC input voltage to disconnect the inverter side and PV source during one zero vector when the inverter operated with the discontinuous SVM method. In addition, to eliminate two CMV levels in two zero vectors, a H8 topology with two additional switches was proposed in [44,45]. Two additional switches were controlled to float the inverter in zero states; the variation of CMV is $V_{PN}/3$. In [46], H8 topology with a voltage-clamping network was proposed. The CMV did not change with the zero vectors by turning off two additional switches. Thus, the CMV can vary from $V_{PN}/3$ to $2V_{PN}/3$. In addition, an improved H8 topology was also proposed in [47]. In the improved H8 topology, the CMV during zero states is kept constant at $2V_{PN}/5$, while it varies from $V_{PN}/3$ to $2V_{PN}/3$ in the active states. In [48,49], the H10 topologies and corresponding modulation scheme with omitting zero vectors were introduced to keep the constant CMV. Moreover, a constant CMV can be given by adding a zero-voltage-state rectifier module to the H6 inverter [50]. In [51], the modulation strategy for a three-phase four-leg PV inverter was discussed to achieve the constant CMV. Therefore, the leakage current can be eliminated remarkably.

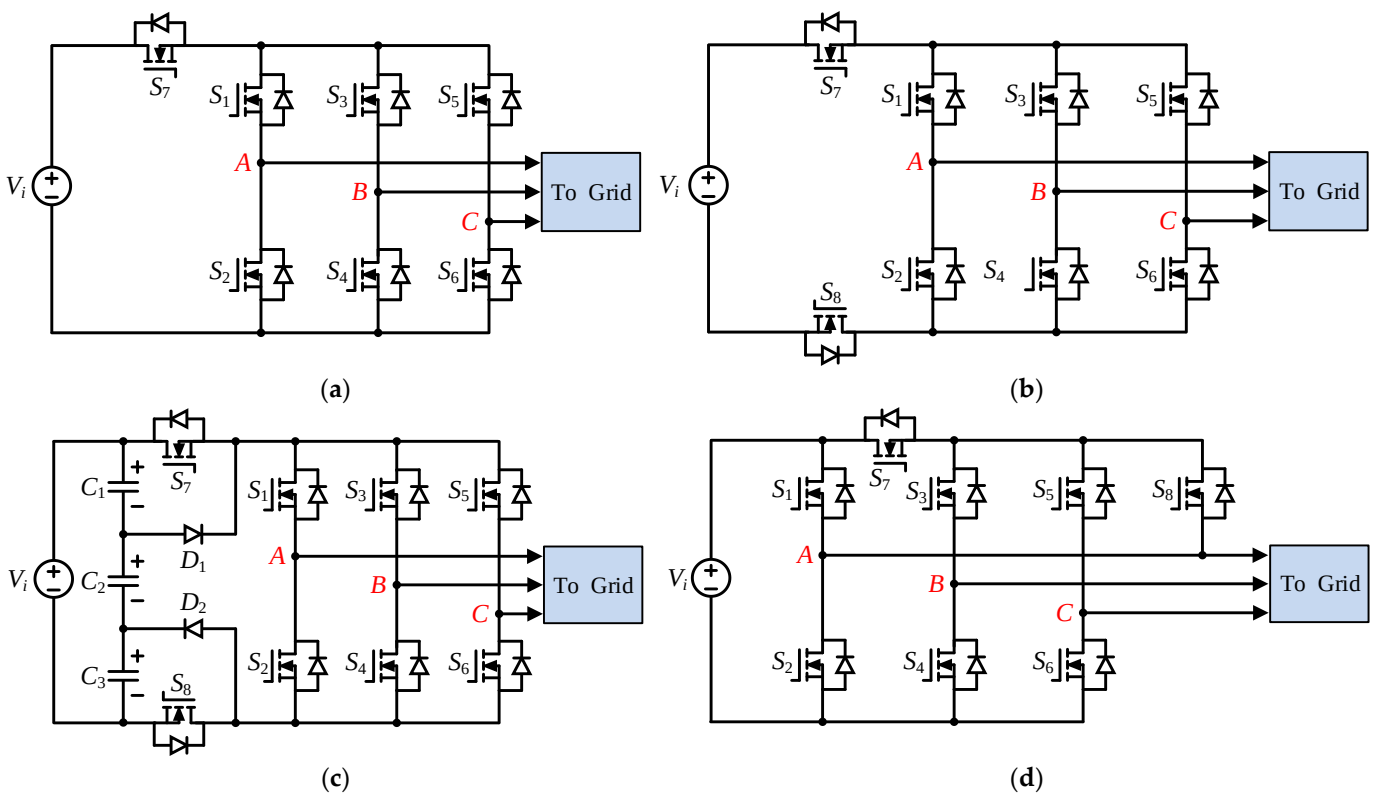


Figure 4. *Cont.*

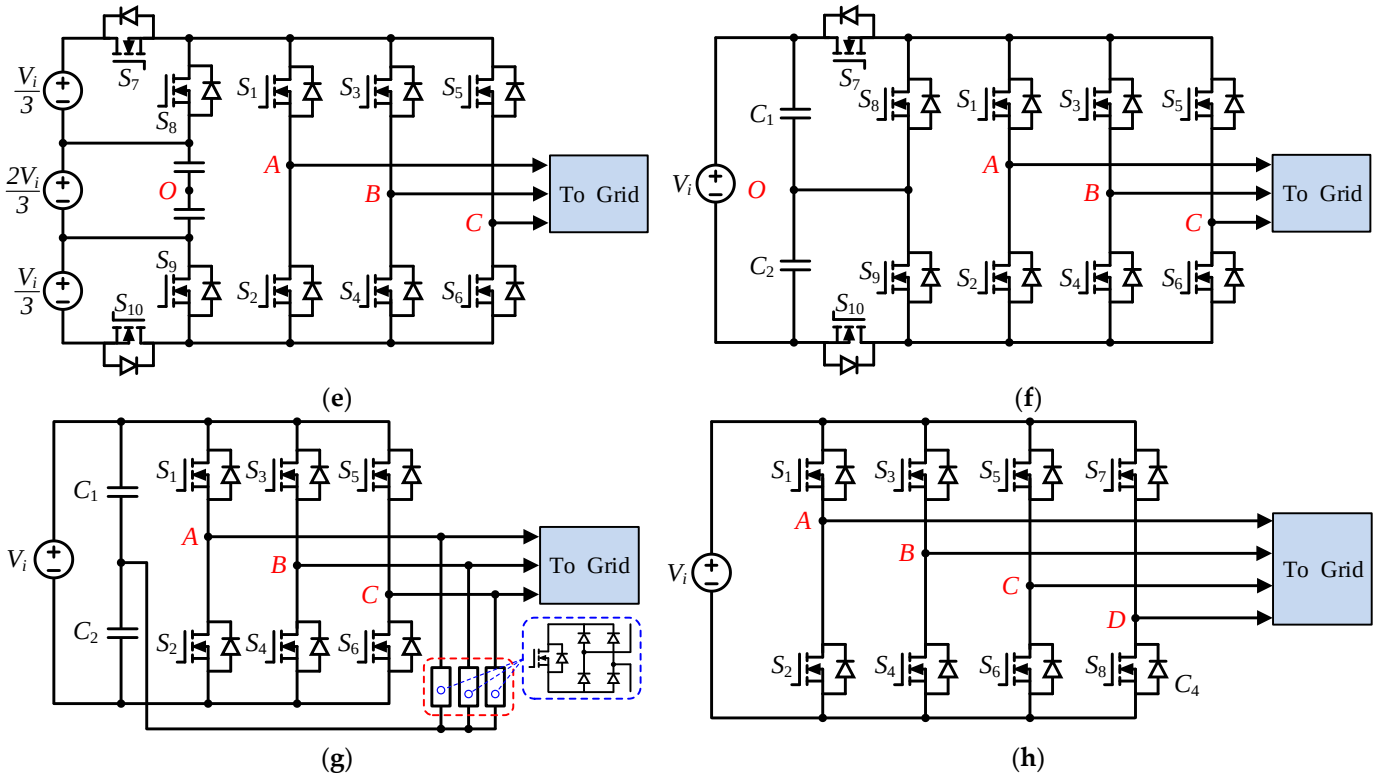


Figure 4. CMV reduction topologies. (**a**) H7 topology [42,43], (**b**–**d**) H8 topologies [44–47], (**e**,**f**) H10 topology [48,49], (**g**) ZVR topology [50], and (**h**) four-leg topology [51].

3.2. Boost-Type Topologies

Unlike the previous solutions, many three-phase two-level inverters are shown in Figure 5. They are based on a combination of different types of boost modules, and each has its unique characteristics. In [53], the H6 topology with a switched-capacitor voltage doubler and the novel SVM methods were proposed to limit the variation of CMV and offer the boosting ability, where the DC-link voltage of the inverter is always two times the input voltage. However, the topology in [53] produces bipolar output line-to-line voltage, and the linear modulation range is also limited. In addition, the proposed triple voltage boost inverter in [54] uses a voltage multiplier network to give the triple boosting voltage and keep the constant CMV. In [55,56], the three-phase H6 based-switched-capacitor inverters were presented to reduce the variation of CMV with one-third of DC-link voltage and also provided the boosting voltage. In the case of the introduced inverter in [55], the DC-link of the inverter can be one or two times of the input voltage depending on the state of the switched-capacitor circuit. On the contrary, the inverter in [56] is always given two times the input voltage. Like conventional four-leg topology, the four-leg inverter with adding boosting module in [57] can also achieve the constant CMV, and the DC-link of the proposed inverter is always two times the input voltage.

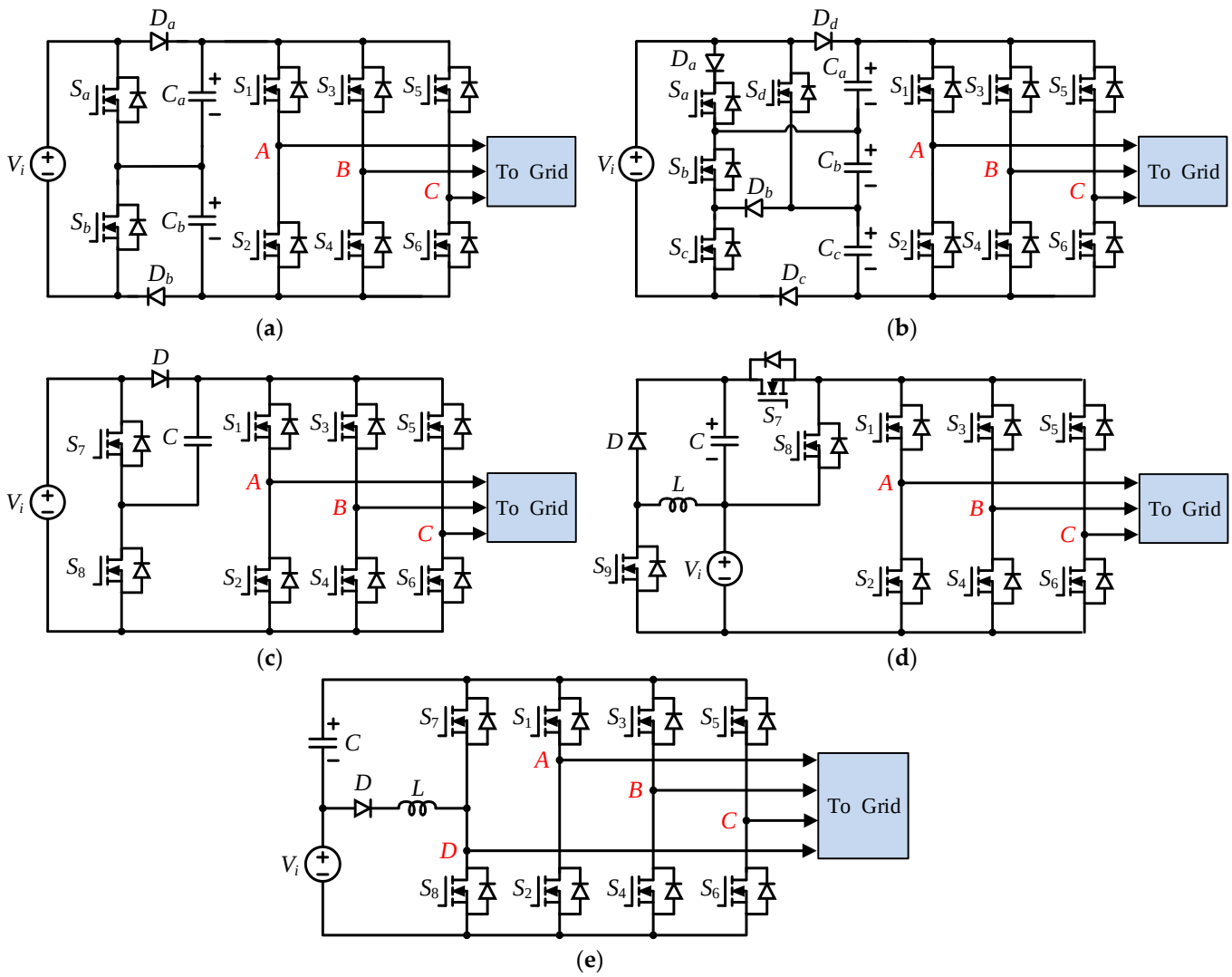


Figure 5. CMV reduction topologies with boosting capability. (**a**) Switched-capacitor voltage-doubler inverter [53], (**b**) triple-voltage boost inverter [54], (**c**,**d**) switched-capacitor-based inverters [55,56], (**e**) boost inverter with four-leg [57].

Table 2 presents the comparison of both buck-type and boost-type traditional three-phase two-level transformerless inverter topologies in terms of component count, modulation index range, boosting capability, and variation of CMV. Figure 6 highlights the comparison of the detailed component count with the number of switches, diodes, capacitors, and inductors. It can be seen that the boost-type topologies require more components when compared with other buck-type topologies. In terms of modulation index operating range, the majority of inverters can operate in the modulation index in full range. It is clear that some of the proposed new structures reviewed in this study are provided by the boosting voltage and very low or constant CMV. However, to overcome some of the limitations, other components should be added, which, in most cases, will increase the size and weight of the inverter package. It can be seen that all the mentioned inverters have their own advantages and disadvantages, as presented in Table 2. Thus, it is difficult to evaluate which inverter is more effective than the other. Nevertheless, there are several key points that should be kept in mind while choosing an inverter for grid-connected three-phase two-level transformerless PV applications.

Table 2. Comparison of different CMV reduction traditional VSIs topologies.

Topology	Component Count				Modulation Index	Boost Factor	CMV	Characteristic	
	S	*D*	*C*	*L*				Advantage	Disadvantage
Figure 4a [42]	7	0	0	7	0 to 1	1	$V_{PN}/3$	– Minimum components – Full range of modulation index	– Low CMV – No boosting capability
Figure 4b [45]	8	0	0	0	0 to 1	1	$V_{PN}/3$	– Simple structure – Full range of modulation index	– Low CMV – No boosting capability
Figure 4c [46]	8	2	3	0	0 to 1	1	$V_{PN}/3$	– Full range of modulation index	– Low CMV – No boosting capability – Requires more components
Figure 4d [47]	8	0	0	0	0 to 1	1	$V_{PN}/3$	– Simple structure – Full range of modulation index	– Low CMV – No boosting capability
Figure 4e [48]	10	0	2	0	0 to 1	1	0	– Constant CMV – Full range of modulation index	– Requires ten switches – No boosting capability
Figure 4f [49]	10	0	0	0	0 to 1	1	0	– Constant CMV – Full range of modulation index	– Requires ten switches – No boosting capability
Figure 4g [50]	9	12	2	0	0 to 1	1	0	– Constant CMV	– No boosting capability – High number of components – Limits modulation index
Figure 4h [51]	8	0	1	1	0.66 to 1	1	0	– Simple structure – Constant CMV	– No boosting capability – Limits modulation index
Figure 5a with DSVM [53]	8	2	2	0	0 to 1	2	$V_{PN}/3$	– Double of input voltage – Full range of modulation index	– Requires more components – Low CMV
Figure 5a with NSSVM [53]	8	2	2	0	0.66 to 1	2	$V_{PN}/6$	– Double of input voltage – Very low CMV	– Requires more components – Limits modulation index
Figure 5a with RSSVM [53]	8	2	2	0	0 to 0.57	2	0	– Double of input voltage – Constant CMV	– Requires more components – Limits modulation index
Figure 5b [54]	10	4	3	0	0 to 1	3	0	– Triple of input voltage – Constant CMV – Full range of modulation index	– High number of components
Figure 5c [55]	8	1	1	0	0 to 1	1 or 2	$V_{PN}/3$	– Double of input voltage – Full range of modulation index	– Requires more components – Low CMV

Table 2. *Cont.*

Topology	Component Count				Modulation Index	Boost Factor	CMV	Characteristic	
	S	*D*	*C*	*L*				Advantage	Disadvantage
Figure 5d [56]	9	1	1	1	0 to 1	2	$V_{PN}/3$	– Double of input voltage – Full range of modulation index	– Requires more components – Low CMV
Figure 5e [57]	8	1	2	2	0 to 1	2	0	– Double of input voltage – Constant CMV – Full range of modulation index	– Requires more components

S, *D*, *L*, and *C* are the number of switches, diodes, inductors, and capacitors, respectively.

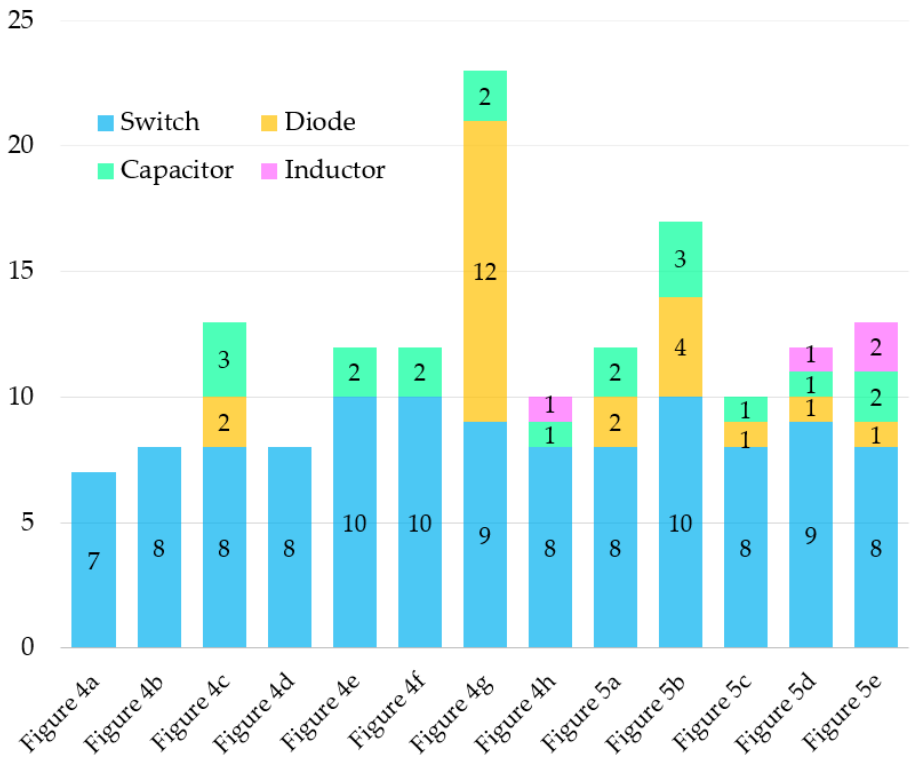


Figure 6. The components for topologies enlisted in Table 2.

4. Impedance-Source-Networks-Based Topologies

4.1. Passive-Type Topologies

Figure 7 presents the general structure of an impedance-source network three-phase, two-level VSI with possible switching devices depending on application requirements. The basic impedance-source network can be established as a combination of inductors, capacitors, diodes, and switches to improve the performance of the circuit. In the control method of the impedance-source-networks-based inverter topologies, the shoot-through states are used to create shoot-through immunity and reduce the deadtime in H-bridge legs. On the contrary with the traditional VSI topologies, the shoot-through states insertion causes very high peak-to-peak CMV in the impedance-source-networks-based inverter topologies [71–83]. To reduce the CMV of the impedance-source-networks-based inverter topologies, various topologies and modulation techniques will be reviewed in this section. In the shoot-through states, during which each switching cycle is added to the H-bridge,

none of the CMV reduction SVM control methods are ideal for impedance-source inverter topologies. In [71], an NSSVM strategy was proposed for a three-phase Z-source inverter, as shown in Figure 8a. In this work, the diode in the positive terminal is reversed-bias while the shoot-through states are implemented. Then, the input voltage source and an inverter are isolated. Similar to the NSSVM in the traditional H6 VSI, the magnitude CMV of three-phase Z-source inverters can be decreased to $V_{PN}/3$. Nevertheless, the modulation index operating range is narrow and followed the conventional NSSVM; in this case, it is operated within 0.66 and 1. In order to provide the constant CMV in the Z-source inverter topology, the Z-source inverter with four-leg was found and presented in [72,73], as shown in Figure 8b. By switching the fourth leg, the CMV variation is significantly limited. Nevertheless, this method will result in a high cost of the three-phase system. In the same way, the three-phase Z-source inverter was proposed in [74,75], with an additional diode in the negative terminal of the input voltage source, as shown in Figure 8c. An additional diode has a function to seperate the inverter and the PV array during shoot-through states. In this case, the CMV is kept constant by using odd vectors. The modulation index is operated up to 0.57.

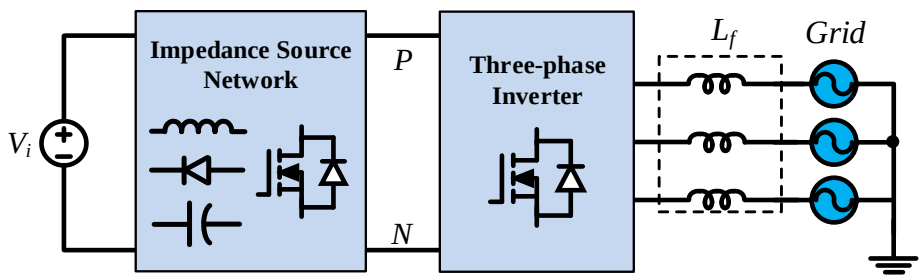
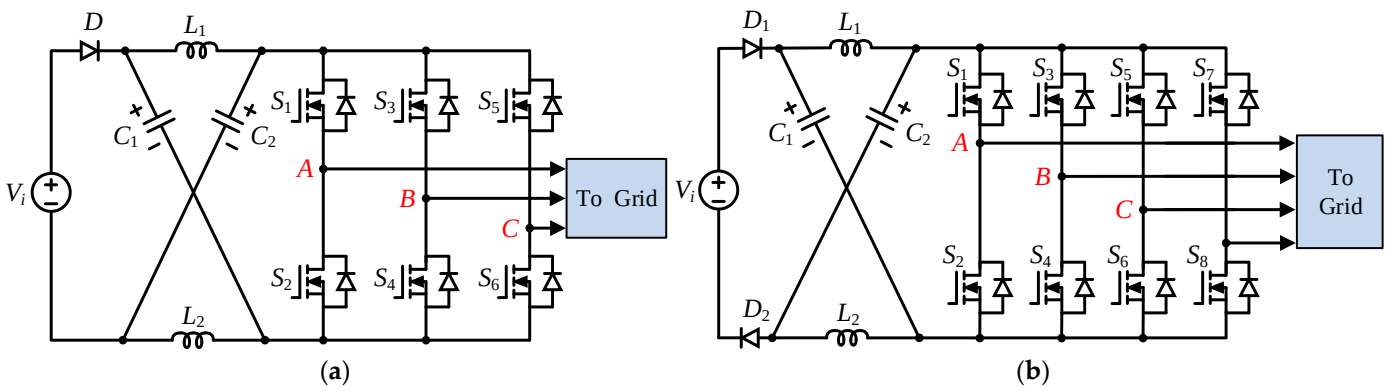


Figure 7. General structure of impedance-source-networks-based three-phase transformerless VSI.

Moreover, to improve the input current profile, the quasi-Z-source inverter and modified quasi-Z-source inverter based on SVM were proposed in [76–79]. In the case of references [76–78], by adding an inductor in the negative terminal of the PV panel, only three odd or even vectors were implemented to keep the constant CMV. However, similar to the RSSVM in the traditional H6 VSI, the linear modulation range is limited to a modulation index of 0.57 in these methods. In addition, a notch filter is considered in [79] to add to the inverter system as an output filter. The CMV waveform is reduced when compared with the conventional SVM method. However, the leakage current can be eliminated in this case.



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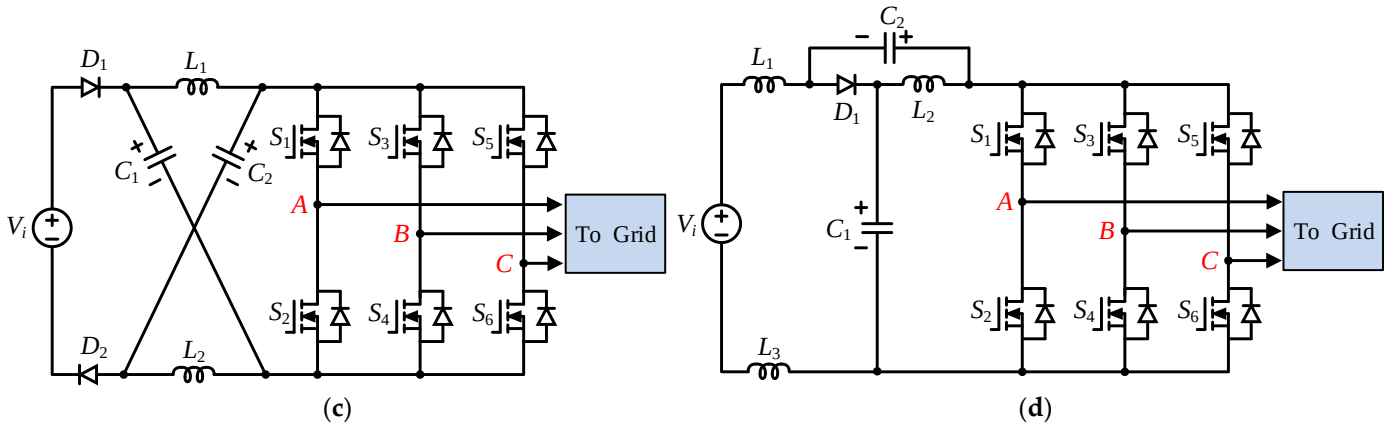

Figure 8. Passive impedance-source topologies for CMV reduction. (**a**) ZSI [71], (**b**) four-leg ZSI [72,73], (**c**) modified-ZSI [74,75], (**d**) qZSI [76,77].

4.2. Active-Type Topologies

There are close similarities in the topologies of the passive and active impedance-source inverters which show that with the high reliability with shoot-through immunity, the deadtime issues can be avoided. However, the size and weight of inverter systems in passive impedance-source inverters are still large because of using inductor and capacitor elements in the Z-source network [63–70]. In recent years, in order to decrease the size and weight of the impedance-source inverter system, research on active impedance-source inverter has been paying attention to fewer numbers of passive elements. However, the disadvantage of these inverters is required to use more numbers of switch and gate drivers. With the shoot-through states insertion, the CMV problem of these two types is quite similar. For instance, the modified quasi-switched boost inverter with an additional inductor was proposed in [80] and shown in Figure 9a. In this solution, an inductor is inserted between the negative input and Z-network. That provides to reduce one level of the CMV waveform. In addition, the novel AZSVM was modified with one more shoot-through vector to reduce the variation in CMV to $V_{PN}/3$, and the modulation index can operate up to 1. In the same way, the modified active quasi-Z-source inverter in Figure 9b was proposed to achieve the CMV of $V_{PN}/3$. In this solution, the zero vectors are not implemented with the NSSVM method. Nevertheless, the modulation index of this SVM method is limited, within [0.66, 1]. Moreover, the magnitude of CMV in these solutions is not very low and only equal to $V_{PN}/3$. In order to reduce the high CMV levels of the shoot-through vectors and provide smaller magnitude CMV voltage, the new impedance-source inverter with two switched-boost networks has been introduced in [82] and depicted in Figure 9c. In this solution, two additional switches in the Z-network are controlled to reduce the magnitude of CMV to $V_{PN}/6$ and improve the boost factor. However, a large number of components were used in the Z-network. Similar to the AZSVM in the method in [80], the modulation index operating of this inverter can be full range, from 0 to 1. Moreover, another method to suppress the leakage current is directly connecting the neutral of the grid to the negative input of the PV panel. The CMV will be zero and also immune to any high-frequency components. As a result, there is no leakage current in the inverter system. To provide the boosting voltage and achieve the common-ground between PV panel and the grid, the common-ground quasi-Z-source inverter is reported in [83], as shown in Figure 9d.

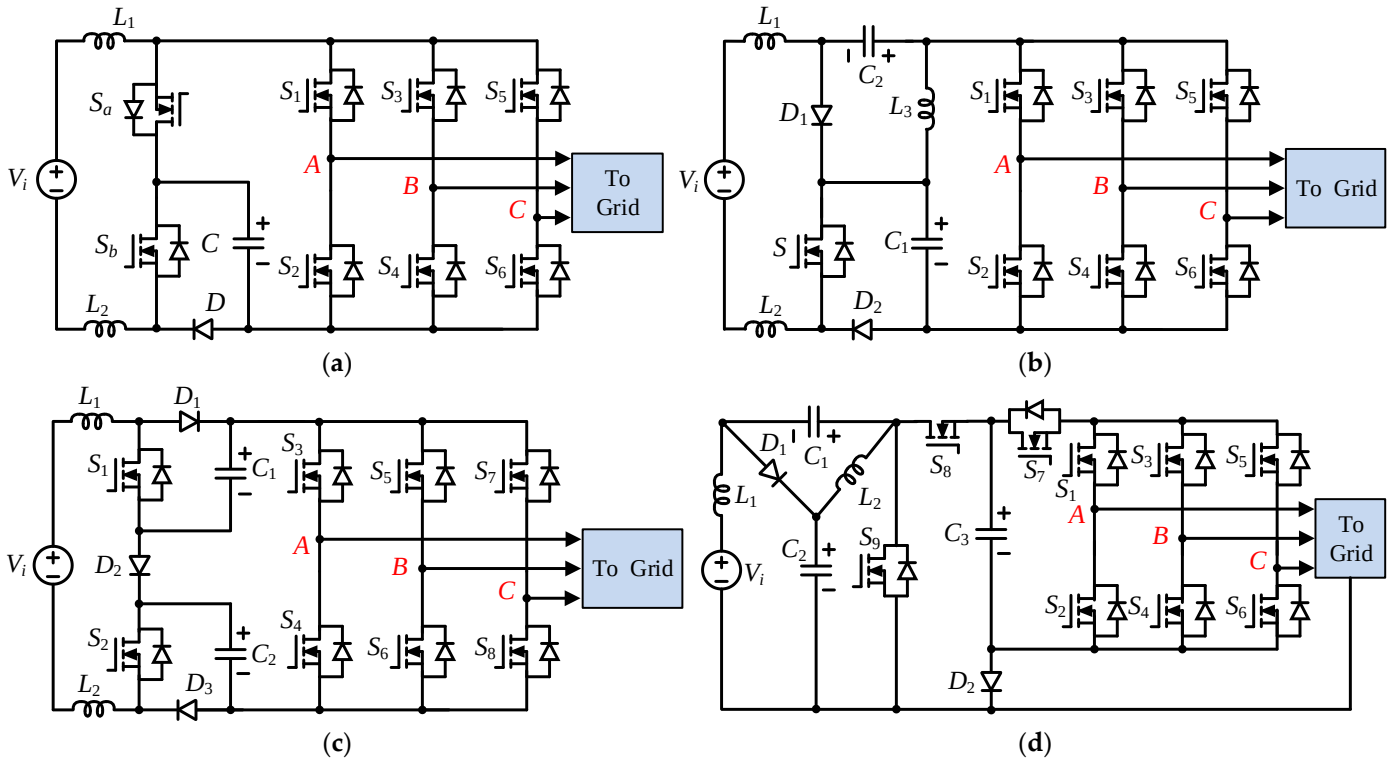

Figure 9. Active impedance-source topologies for CMV reduction. (**a**) MqSBI [80], (**b**) modified-AqZSI [81], (**c**) ISI [82], (**d**) and common-ground AqZSI [83].

The comparison of both passive and active three-phase, two-level transformerless impedance-source-networks-based inverters, in terms of component count, input current profile, modulation index range, boost factor, and variation of CMV, has been given in Table 3.

Table 3. Comparison of different CMV reduction impedance-source-networks-based topologies.

Topology	Component Count				Modulation Index	Boost Factor	CMV	Characteristic	
	S	*D*	*C*	*L*				Advantage	Disadvantage
Figure 8a [71]	6	1	2	2	0.66 to 1	$1/(1-2D)$	$V_{PN}/3$	– Low number of components and not require additional switch	– Discontinuous input current – Limits modulation index – Not high voltage gain – Low CMV
Figure 8b [73]	8	2	3	3	0 to 1	$1/(1-2D)$	0	– Full range of modulation index – Constant CMV	– High number of components – Discontinuous input current – Not high voltage gain
Figure 8c [74]	6	2	2	2	0 to 0.57	$1/(1-2D)$	0	– Low number of components and not require additional switch – Constant CMV	– Discontinuous input current – Limits modulation index – Not high gain

Table 3. *Cont.*

Topology	Component Count				Modulation Index	Boost Factor	CMV	Characteristic	
	S	*D*	*C*	*L*				Advantage	Disadvantage
Figure 8d [76]	6	1	2	3	0 to 0.57	$1/(1-2D)$	0	– Low number of components and not require additional switch – Continuous input current – Constant CMV	– Limits modulation index – Not high voltage gain
Figure 9a [80]	8	1	1	2	0 to 1	$1/(1-2D)$	$V_{PN}/3$	– Low number of components – Continuous input current – Full range of modulation index	– Require additional switch – Not high voltage gain – Low CMV
Figure 9b [81]	8	2	2	2	0 to 1	$2/(1-3D)$	$V_{PN}/6$	– Continuous input current – Full range of modulation index – High voltage gain	– High number of components and require additional switch – Low CMV
Figure 9c [82]	7	2	2	3	0.66 to 1	$1/(1-3D+D^2)$	$V_{PN}/3$	– Continuous input current – Full range of modulation index – High voltage gain – Very low CMV	– High number of components and require additional switch
Figure 9d [83]	9	2	3	2	0 to 1	$1/(1-2D)$	0	– Continuous input current – Full range of modulation index – Constant CMV	– High number of components and require additional switch – Not high voltage gain

S, *D*, *L*, and *C* are the number of switches, diodes, inductors, and capacitors, respectively.

Figure 10 depicts the comparison of the component count in detail. It can be observed that the active-type impedance-source topologies and four-leg ZSI require more components than other passive-type impedance-source topologies. The boost factor is also presented in Figure 11. The active-type impedance-source inverters in [81,82] can offer a higher boost voltage ability than the other inverters. From the CMV comparison in Table 3, which achieved the constant CMV, the majority of inverter topologies cannot utilize the full range of the modulation index, and the zero vectors have not been implemented in the SVM method. In addition, the number of components should be large. To solve the high CMV level caused by the shoot-through vectors, various solutions, such as reconfiguring by adding a component or modified SVM methods, are introduced. However, these topologies require a large number of components to provide the boosting voltage, and very low or constant CMV. The advantages and disadvantages of the different CMV reduction impedance-source-networks-based topologies are also highlighted in Table 3. It is also difficult to determine which solution is better than the other. Nevertheless, if compared with the traditional inverter, the impedance-source inverters can give a higher voltage gain and provide the shoot-through immunity. These inverters can be considered with competitive solutions in PV applications.

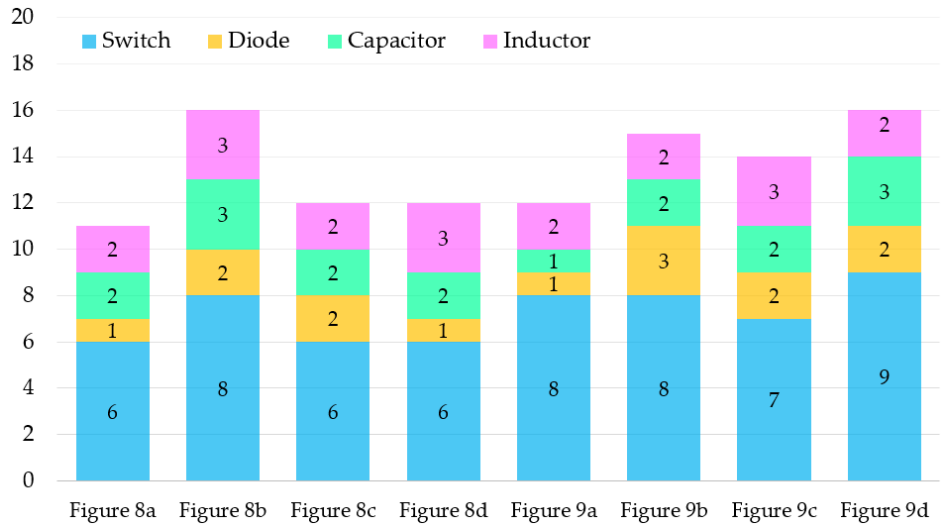

Figure 10. The components for topologies enlisted in Table 3.

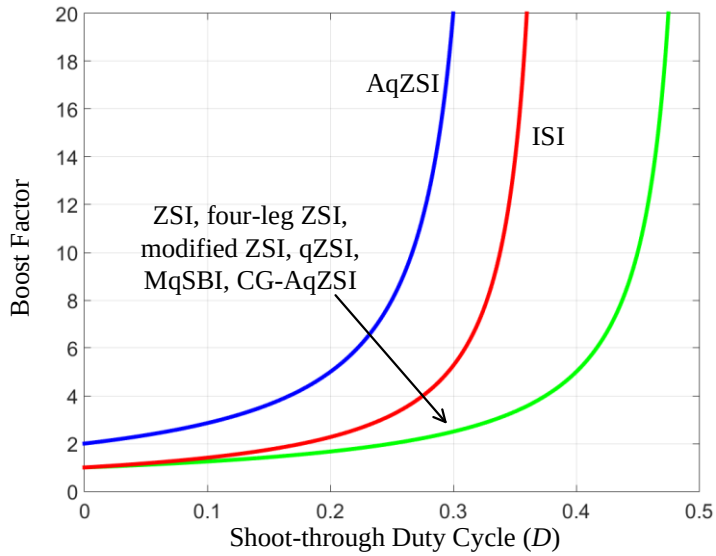

Figure 11. Comparison of boost factor.

5. Conclusions

To present the investigation of the three-phase two-level transformerless PV inverters for CMV reduction, the major three-phase two-level transformerless topologies have been surveyed based on conversion functionality. In detail, these topologies were classified into two different categories: traditional VSIs and impedance-source-based VSIs. For a general comparison, the features of both traditional buck-type and boost-type three-phase two-level transformerless topologies for CMV reduction were summarized. In addition, to have a further overview of common-mode voltage reduction in three-phase two-level inverters single-stage impedance-source-based inverters are also discussed in this paper. Different topologies were examined, in terms of the number of devices, modulation index operating range, boost factor, and CMV reduction. This survey and classification will help researchers to comprehend all these three-phase two-level transformerless photovoltaic inverters for CMV reduction and to identify their pros and cons. From this point, it can be observed that the transformerless photovoltaic inverters have been a certain mature technology and successfully employed in the distributed photovoltaic grid-connected systems. A comprehensive review of control and modulation techniques for CMV reduction of three-phase two-level transformerless PV inverters will be presented in future research.

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Abbreviations

PV	Photovoltaic
DC	Direct current
AC	Alternating current
VSIs	Voltage source inverters
CSIs	Current source inverters
CMV	Common-mode voltage
SVM	Space vector modulation
PWM	Pulse width modulation
THD	Total harmonic distortion
ZSI	Z-source inverter
DSVM	Discontinuous space vector modulation
NSSVM	Near-state space vector modulation
AZSVM	Active zero-state space vector modulation
RSSVM	Remote-state space vector modulation

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