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A Cost-Effective Passive/Active Hybrid Equalizer Circuit Design

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Abstract: This paper proposes a novel hybrid equalizer circuit (HEC) for a battery management system (BMS) to implement the passive HEC (P-HEC), active HEC (A-HEC), or active/passive (AP-HEC) with the same equalizer circuit architecture. The advantages of an HEC are that it is simple, cost-effective, highly energy efficient, and fail safe. The P-HEC can further use a cooling fan or heater instead of a conventional resistor as a power dissipation element to convert the energy of the waste heat generated by the resistor to adjust the battery temperature. Even if the P-HEC uses the resistor to consume energy as in conventional methods, the P-HEC still dramatically improves the component lifetime and reliability of the BMS because the waste heat generated by the equalizer resistor is outside of the BMS board. Three significant advantages of an A-HEC are its (1) low cost, (2) small volume, and (3) higher energy efficiency than the conventional active equalizer circuits (AECs). In the HEC design, the MOSFETs of the switch array do not need high-speed switching to transfer energy as conventional AECs with DC/DC converter architecture because the A-HEC uses an isolated battery charger to charge the string cell. Therefore, the switch array is equal to a cell selector with a simple ON/OFF function. In summary, the HEC provides a small volume, cost-effective, high efficiency, and fail-safe equalizer circuit design to satisfy cell balancing demands for all kinds of electric vehicles (EVs) and energy storage systems (ESSs).

Keywords: battery management system (BMS); hybrid equalizer circuit (HEC); passive equalizer circuit (PEC); active equalizer circuit (AEC)

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1. Introduction

Due to growing concerns about the environmental impact of fossil fuels, policymakers are increasingly turning their attention to clean energy and electric vehicles [1–5]. Therefore, the energy storage system (ESS) plays a critical role, and the lithium-ion battery (LIB) shares more than 90% of the ESS market. For these ESSs, they need to consist of many LIBs grouped in series and in parallel to assemble a battery pack to provide sufficient power and the desired energy. In practice, the difference in each cell's characteristics (e.g., internal capacity, impedance, self-discharge rate, etc.) will influence the voltage difference of all the series-connected cells of the battery pack. Therefore, a battery management system (BMS) [6–21] was designed to protect, monitor, and control the state of all cells of the battery pack. A good BMS can ensure safe operation, maximize the available capacity, and provide a real-time estimate of the remaining discharge capacity of the battery pack [19].

However, much effort and resources are required to test a BMS with a real ESS. Furthermore, by pushing the ESS operation under extreme operating conditions, it is almost impossible to verify that the BMS functions are safe and reliable. Therefore, some

research uses a hardware-in-the-loop (HIL) simulation tool to test BMS. The HIL can be used to simulate string cells of a battery pack [20] to test BMS functions for cells, e.g., test passive equalizer function [21]. Briefly, HIL is a good auxiliary tool in the development stage of a BMS, which can significantly reduce the development time and testing risk of the BMS. In many practical experiences, most battery pack failures are caused by the cell voltage imbalance issue, which means the voltage difference is enormous, drastically reducing the battery pack's available power, capacity, lifespan, and safety. Therefore, most BMS designs have an equalization unit to solve the imbalance issue [22–35].

In general, the BMS is composed of measurement, communication, calculation, memory, equalization units, etc. The equalization unit is also called the cell balancing unit. The equalization unit is composed of two parts: an equalization control strategy [23–29] and an equalization circuit (EC) [28,29,31–34]. Its purpose is to reduce the maximum and minimum cell voltage differences of the battery pack to avoid battery overcharge and overdischarge, which can improve the safety and lifespan. Besides, the low cell voltage difference also increases the available capacity of the battery pack. Therefore, the equalization unit is the most crucial part of all BMS units. Retired vehicle lithium battery packs with good cell balance can be reused in energy storage systems for secondary use to produce huge economic and environmental benefits. Various ECs have been proposed in the past, which can be divided into two types: (1) the passive equalizer circuit (PEC) [28], also called dissipative balance, discharges the energy with a power resistor to the series-connected cell with the highest voltage, and (2) the active equalizer circuit (AEC) [27–34,36–38], also called non-dissipative balance, charges the energy to the cell with the lowest voltage. Many review articles have provided a detailed summary or comparison for the equalization design [17,26,28,30,32,33,36]. Therefore, the following summary is more focused on commercialization.

The commonly used PEC architecture [28] is shown in Figure 1. The advantages of PEC are that it is very simple, easy to apply and low cost, and all switches (S_i) and discharge resistors (R_i) are placed on the BMS circuit board (where i = 1, 2, . . . , n). Therefore, the temperature of BMS board will increase a great deal when performing the cell balancing. In most commercial products, the typically balancing resistor is 33 Ω [39], and the current of each channel is around 100~127 mA which maps to 3.3~4.2 V and the waste heat of the PEC is around 0.3~0.5 W per channel in the BMS board. To avoid overheating the BMS board, the BMS also limits the number of balanced channels.

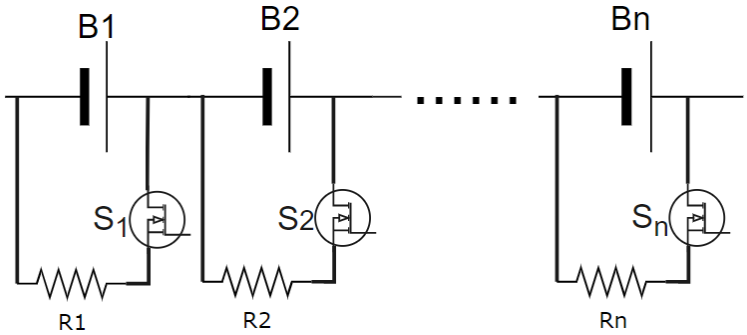


Figure 1. The circuit of PEC [28].

Briefly, the AEC uses the switch array, capacitors, inductors, or transformers to absorb the energy from the cell with the highest voltage and release the energy to the cell with the lowest voltage. Many kinds of AECs are shown in Figure 2, but most are based on the DC/DC converter principle.

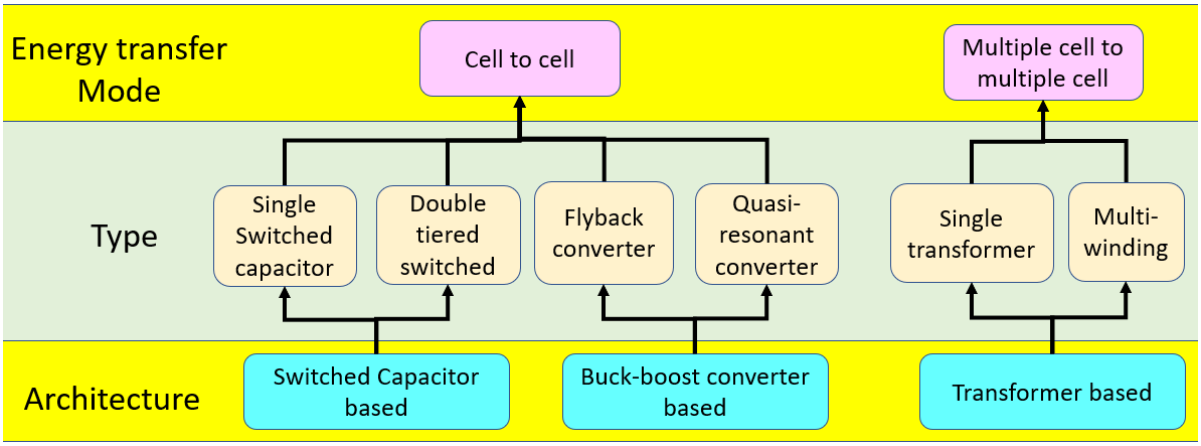


Figure 2. Classification of AEC [33].

Figure 3 shows the fundamental topology of an AEC with the DC/DC converter working principle, and all switches are the bidirectional switch (BS) which consists of a back-to-back MOSFET string, called BS-MOSFET. Obviously, all switches in Figure 3 need high-speed switching to transfer energy between the string cell and the transformer.

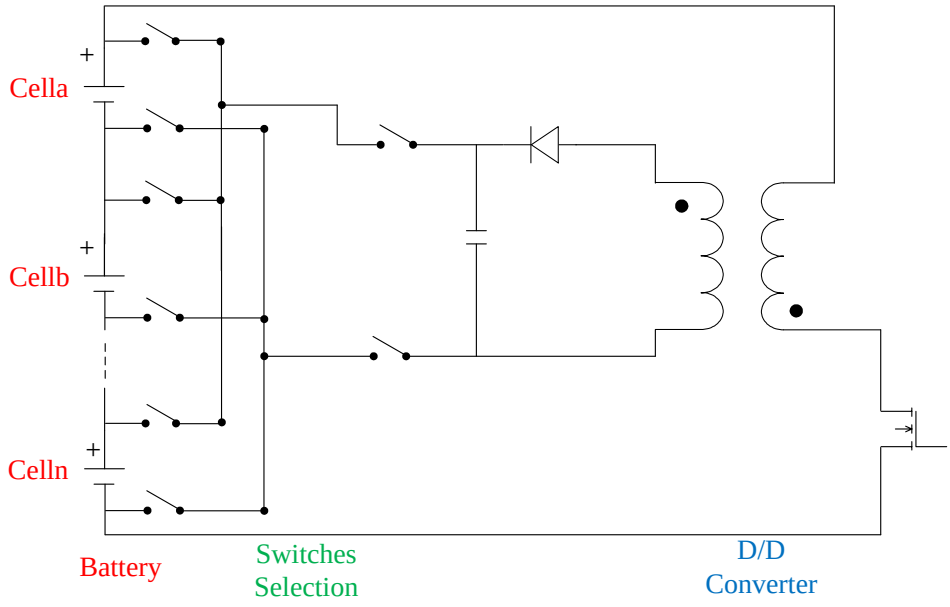


Figure 3. Unidirectional flyback-based balancing topology for AEC [36].

Based on the topology of Figure 3, the chipmaker analog device had commercialized the active balancing control IC LT8584 [40]. The AFE IC (LTC680x family) can drive the active balancing IC LT8584 and the transformer NA5743-AL to generate 2.5 A balancing current from the cell to the module. Moreover, the standalone balancing IC (LT3300 family) enables a bidirectional balancing current between cell and module up to 10 A.

Figure 4 shows another implementation of the AEC with a single switched capacitor (SSC) with DC/DC converter principle, and the switches in Figure 4 also need high-speed switching to transfer energy between the auxiliary battery, capacitor, and string cells.

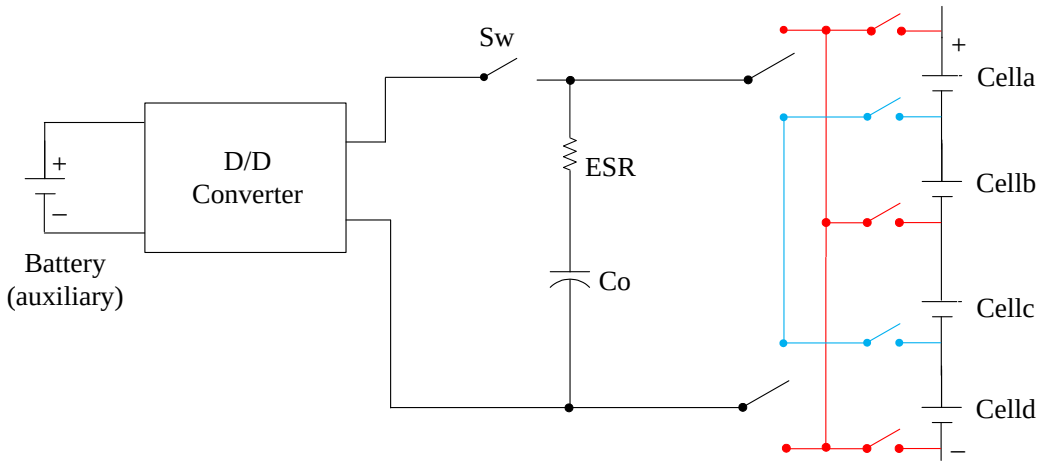


Figure 4. Implementation of modularized SSC and BC balancing system [34,35].

In fact, the working principle of most AECs is based on a DC/DC converter architecture to transfer energy between string cells or the module, and the energy storage components (e.g., capacitor or inductor) can be regarded as an energy transfer buffer. Therefore, the switches of the switch array of the AECs are not only used to select the string cell for sinking/draining energy but also needed high-speed switching for transferring energy through the energy buffer (e.g., inductor or capacitor). Due to high-speed switching requirements, most of the switching arrays composed of BS-MOSFETs in AEC circuits are mostly driven by gate drivers. Based on the above descriptions, it is easy to find the cost of AECs is related to the component's specification and the number of power resistors, inductors, capacitors, transformers, and BSs.

Thus, the low-cost or the low-series cell string pack prefers the PEC. The AEC is more applicable to high-end or high-series cell string packs. Therefore, this paper proposes the HEC architecture, which can be both PEC and AEC or either PEC or AEC. The advantages of the proposed HEC are its (1) cost-effective, (2) high efficiency, and (3) fail-safe features.

2. Operation Principle of Hybrid Equalizer

In Figure 5, the HEC corresponds to a PEC by replacing the discharge unit with a power resistor, which is called a P-HEC. All the switches in Figure 5 are replaced with BS-MOSFET, as shown in Figure 6.

Figure 7 is an example to illustrate the principle of P-HEC. To discharge the B_2 cell through the EQ-Bus, the BMS controls the $S_{2,n}$ and $S_{2,p}$ switches to be conducting. A discharge unit R_{EQ} can be a fan or a heater to regulate the battery temperature or be a power resistor to dissipate the cell energy as conventional ones. The R_{EQ} is installed out of the BMS board with proper cooling to prevent the BMS board temperature rising quickly when executing the balance operation. The cell balancing current (I_b) is related to the resistance of R_{EQ}, conducting resistance of $S_{2,n}$ and $S_{2,p}$, and the resistance of all connected parts from B_{2+} to B_{2-}. For example, the R_{EQ} is 1 Ω and the resistance of the BSs and wires is 0.5 Ω so that the total resistance is 1.5 Ω. The balancing current is 2.27 A (V_{B2} = 3.4 V) to 2.8 A (V_{B2} = 4.2 V) within cell operation voltage range. The fuse and switch specification will be calculated after given R_{EQ}. When the HEC is only used as PEC, it allows the opposite electrode of EQ-Bus. Therefore, the switches $S_{i,n}$ and $S_{i,p}$ can be replaced with a single switch S_i to save costs.

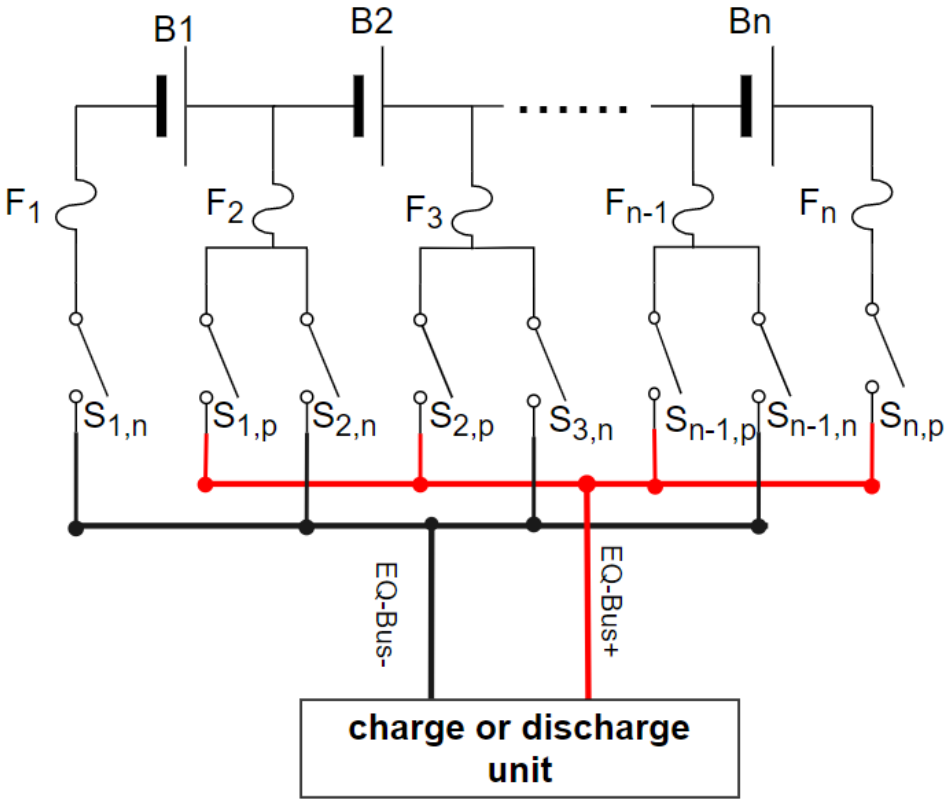


Figure 5. Hardware architecture of the HEC.

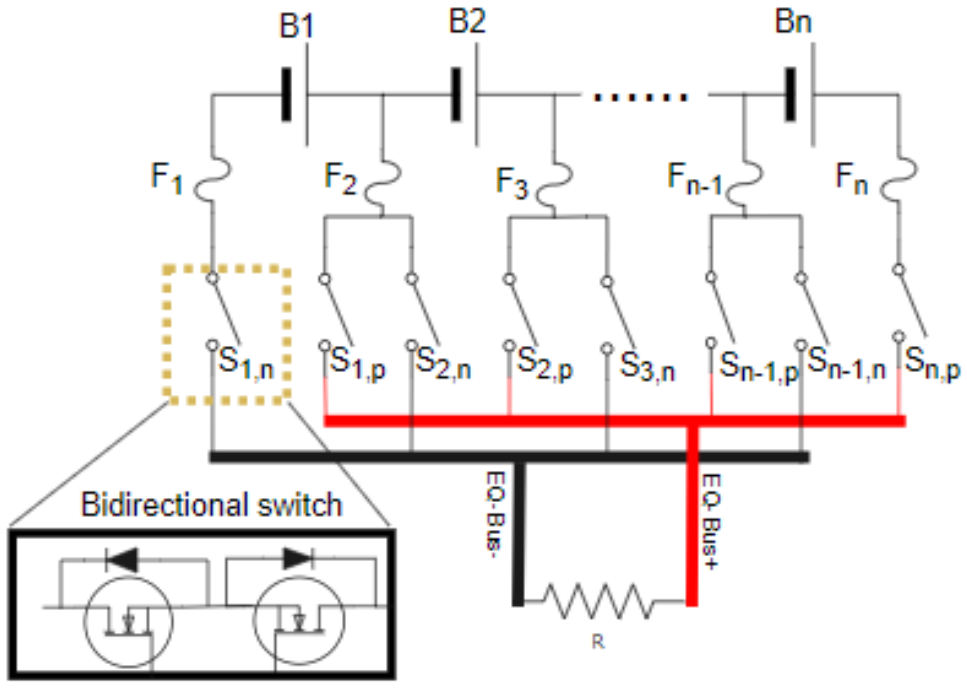


Figure 6. Implementation of the PEC with HEC architecture.

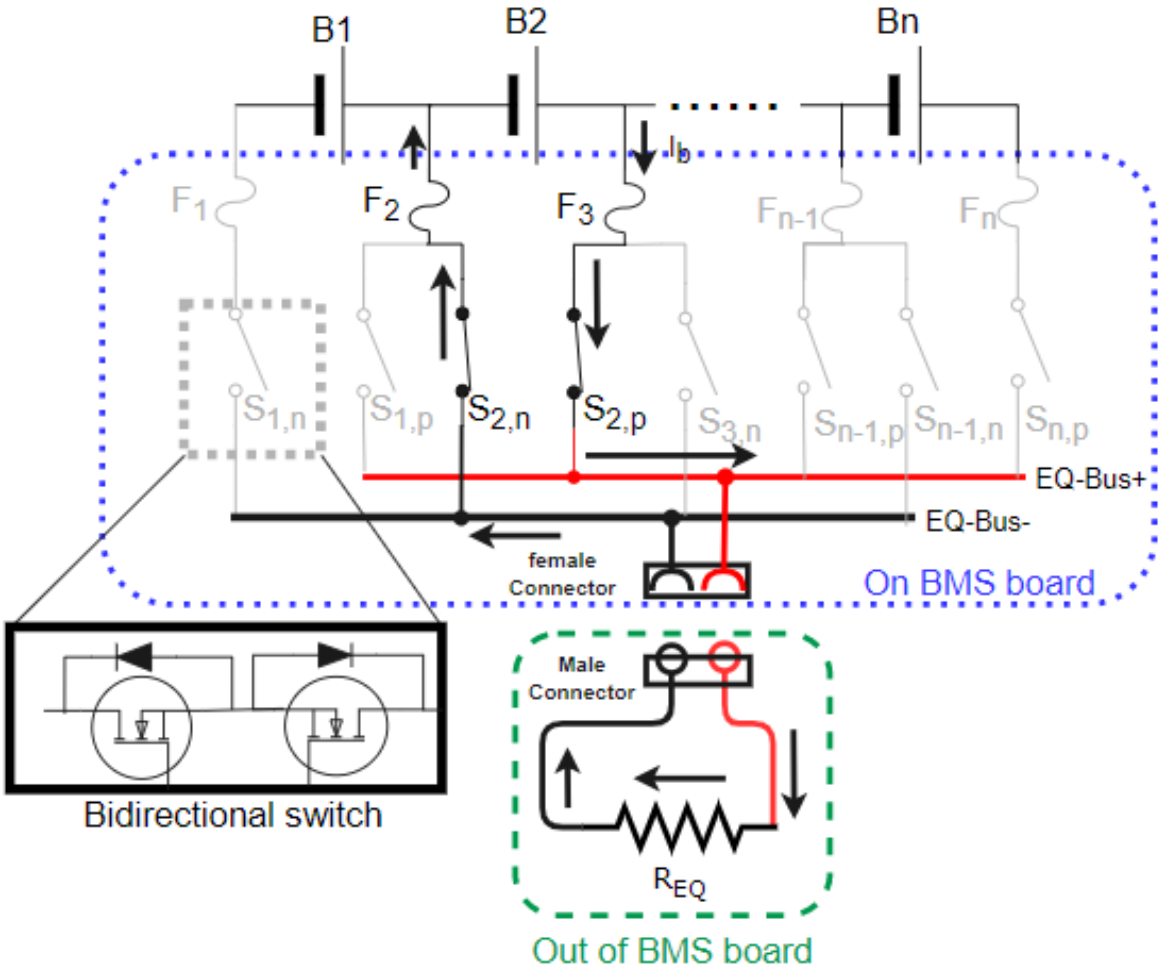


Figure 7. Discharge the energy of B_2 cell with the power resistor out of BMS board.

Figure 8 shows how the proposed HEC design can satisfy the fail-safe function when any switch of the switch array fails in short-circuit. Figure 8 assumes the $S_{1,p}$ incurs a short-circuit failure, and a short current (I_s) blows the fuse F_2 or F_3 when discharging the B_2 cell by conducting $S_{2,n}$ and $S_{2,p}$. The current path of the short current (I_s) goes through $F_3 \rightarrow S_{2,p} \rightarrow EQ-Bus+ \rightarrow S_{1,p} \rightarrow F_2$. Therefore, the HEC can avoid the cell being continuously discharged when the failed switch keeps conducting. In addition, it is easy to identify the failure switch path by detecting the balancing current or voltage change.

Figure 9 shows an HEC implement AEC architecture by replacing the charge unit of Figure 5 to an isolated CC-CV battery charger, which is called an A-HEC. The isolated CC-CV battery charger is composed of an isolated DC/DC converter and a CC-CV battery charger circuit. The switch S_B controls the input power, and the S_A controls the charger output power to the EQ-Bus.

Figure 10 shows the HEC architecture can be either PEC or AEC, but only one mode can be used at one time. It can be P-HEC by conducting the switch S_C and be A-HEC by conducting the switch S_A and S_B. The switches $S_A - S_C$ must be isolated switches because of the different ground levels.

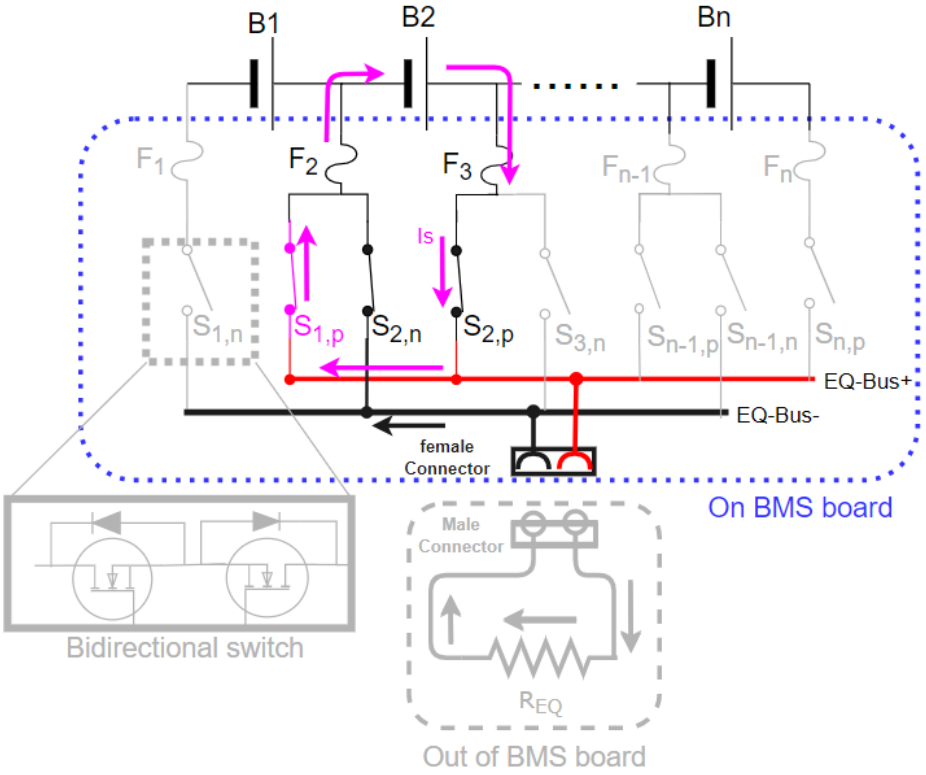


Figure 8. Switch fail-safe demonstration to blow fuse when $S_{1,p}$ fails and keeps conducting.

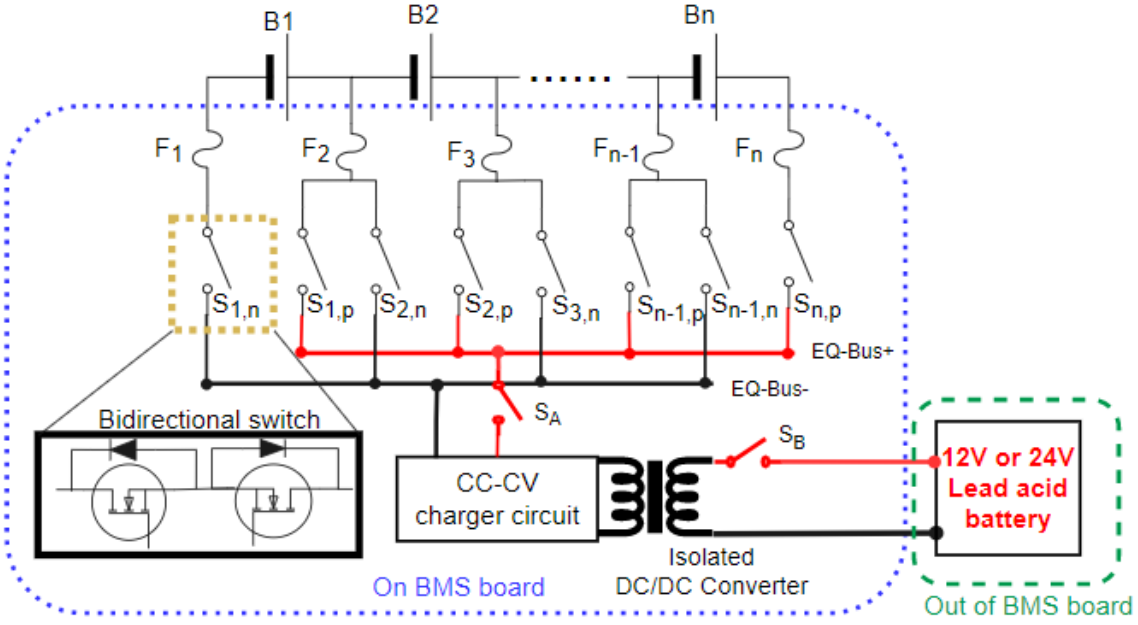


Figure 9. Implementing the AEC with HEC architecture.

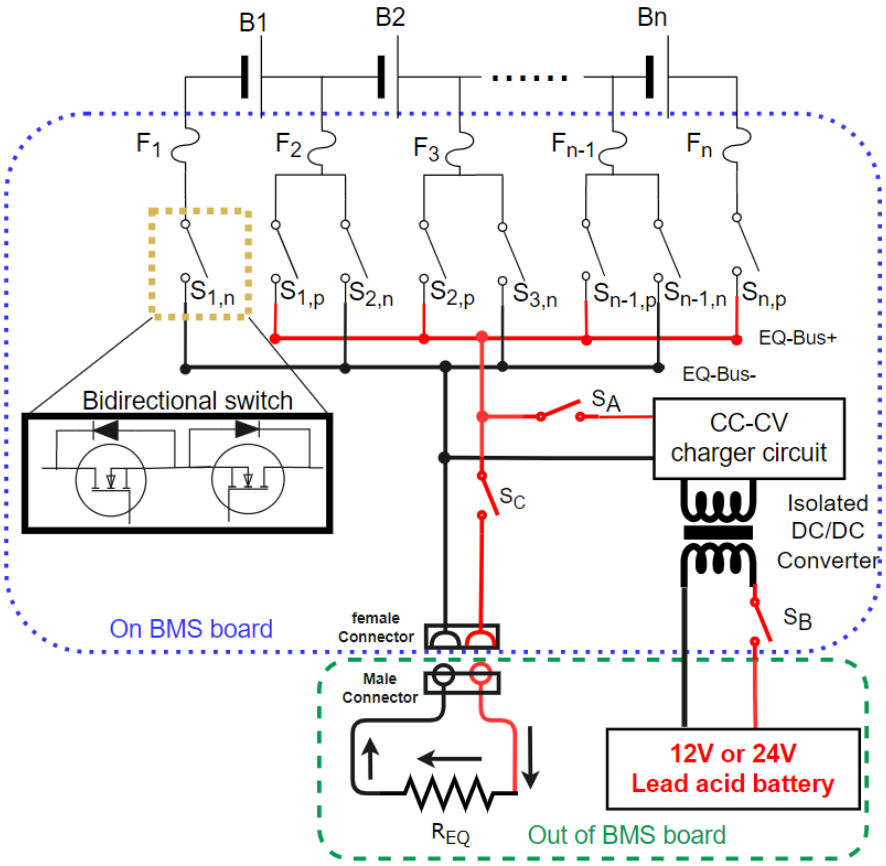


Figure 10. Implementing AEC and PEC with HEC architecture.

In summary, the proposed HEC combines three essential parts: (1) a switch array, (2) fuses, (3) the charging unit, or the discharging unit. The proposed HEC uses the switch array architecture of conventional AECs to implement the PEC and AEC. The P-HEC can solve the thermal issue of conventional PECs by placing the discharge unit out of the BMS board. The discharge unit might not only be a power resistor for dissipating the energy but also could be a fan or heater to reuse the energy to regulate the battery temperature. Furthermore, the balancing current (>2 A) of the P-HEC is more than 20 times that of the conventional PEC (10–127 mA) with a power resistor on the BMS board. The proposed HEC also adopts the auxiliary lead–acid battery of the EV to provide energy to the isolated DC/DC charger to charge the cell with the lowest voltage in the battery pack. The isolated charger is composed of an isolated DC/DC converter and a CC-CV charger circuit. The significant advantages are shown below: (1) simple and easy to implement with low-cost components, (2) its volume is much smaller. Whether the proposed HEC is a P-HEC or an A-HEC, the proposed HEC also satisfies the fail-safe requirement of functional safety because the balancing current will be cut off by blowing a fuse when any switch of the switch array fails in short-circuit state. The BMS also can detect the cell voltage or balancing current to identify the failed switch.

3. Cost-Effective Bidirectional Switch Circuit Design for HEC

The switch array of the HEC is very similar to the traditional AEC, but the basic control concept is entirely different even though the BSs of the switch array use the same BS-MOSFET structure. In conventional AECs based on the DC/DC converter principle, the BS-MOSFET in many AEC articles needs a gate driver [29] or an isolation optocoupler (TLP250) [34] to high-speed switch the BS-MOSFET to transfer the energy between the cell and the energy storage components. The disadvantage is the number of gate drivers dramatically increases the cost of the switch array. However, the BS-MOSFETs of the HEC

only use an ON/OFF switch, which is equal to a string cell selector for performing cell balancing. Therefore, Section 3 proposes a low-cost control circuit to replace the gate driver to control the BS-MOSFETs.

3.1. Low-Cost BS-MOSFET Drive Circuit

Based on the working principle of Figure 7, we further explain how to design the low-cost BS-MOSFET switch circuit. Therefore, the BS-MOSFET control circuit and the working principle are shown in Figure 11.

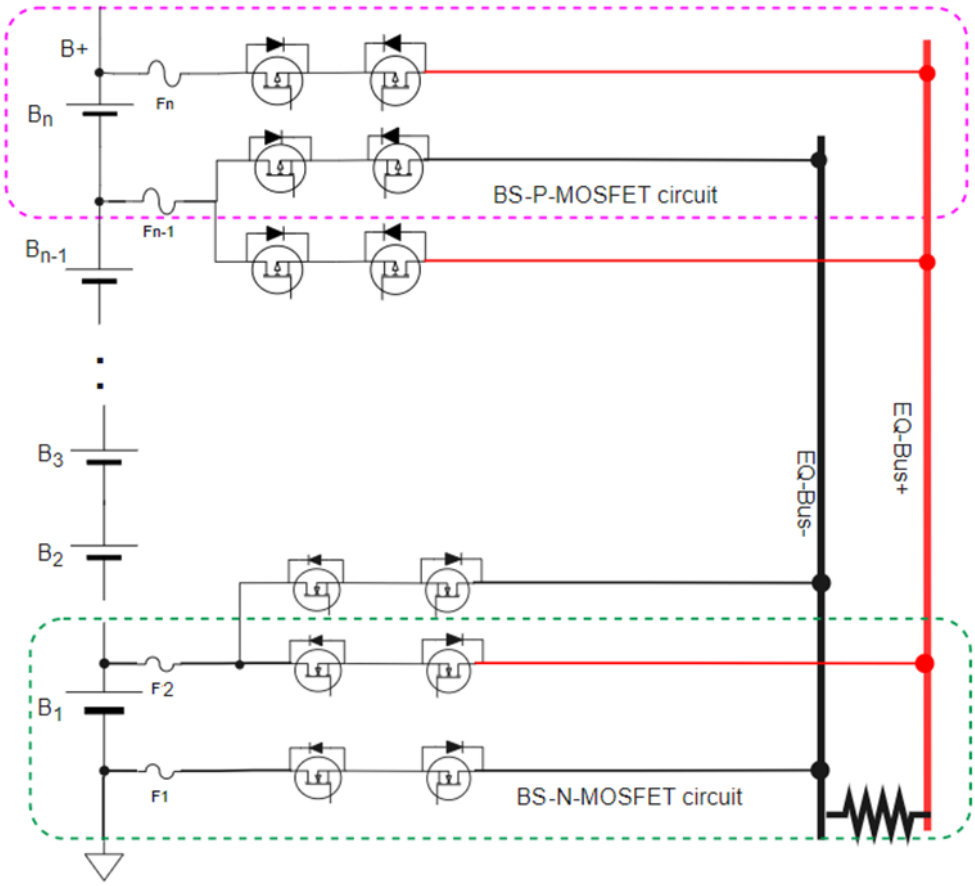


Figure 11. The BS-MOSFET switch and control circuit design.

In Figure 11, we use two back-to-back P-MOSFETs to be the BS-P-MOSFET drive circuit if the minimum voltage of the node is $\geq$8 V. Otherwise, we use two back-to-back N-MOSFETs to be the BS-N-MOSFET drive circuit for the maximum voltage of the node is <8 V and the battery pack voltage B_+ is $\geq$8 V.

3.2. BS-P-MOSFET Drive Circuit

Figure 11 can be simplified as Figure 12, where only two cells are series connected. The B_1 in Figure 12 corresponds to the battery consisting of B_1 to B_{n-1} of Figure 11. The B_2 in Figure 12 corresponds to the B_n of Figure 11. We use Figure 12 to demonstrate the principle of a BS-P-MOSFET driving circuit with a B_{2+} path to the EQ-Bus+ because the circuit of the B_{2-} path to the EQ-Bus- is the same structure. Therefore, we only use B_{2+} to demonstrate the operation principle.

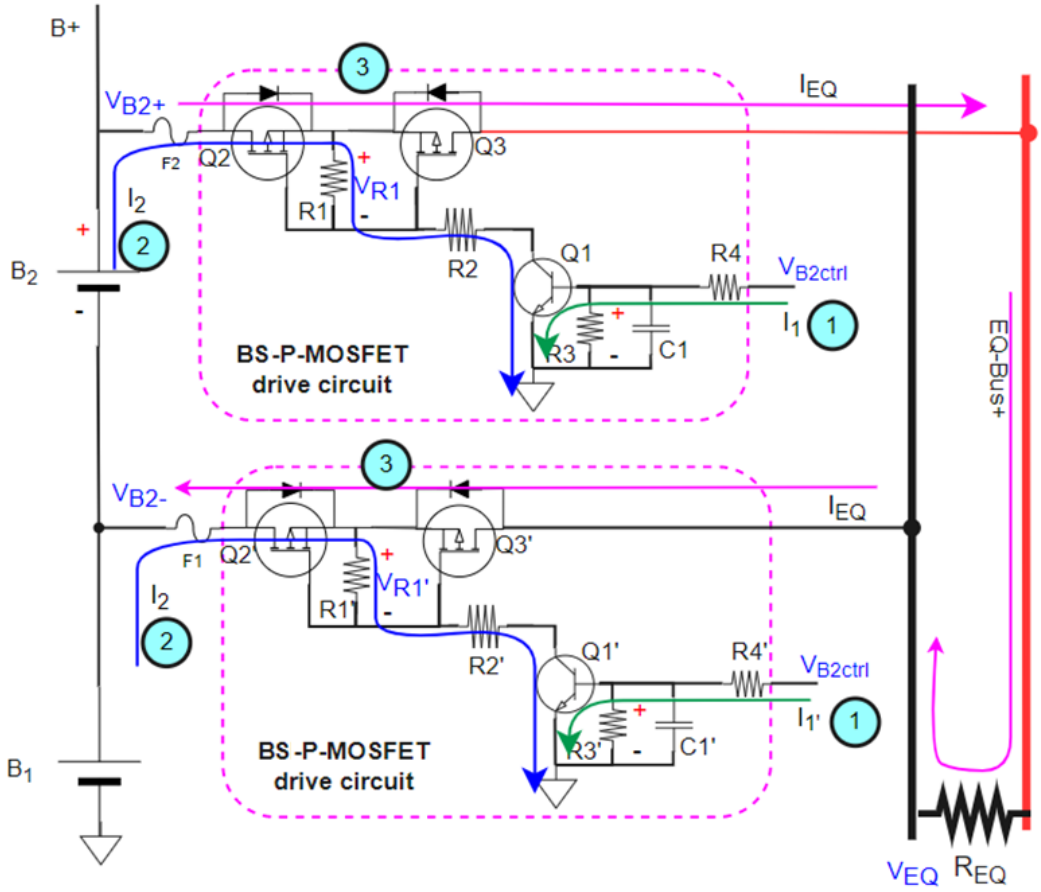


Figure 12. Simplified Figure 11 as a battery pack with 2S configuration for demonstrating BS-P-MOSFET drive circuit.

3.2.1. Schematic and Calculation for BS-P-MOSFET Circuit

In Figure 12, the principle of step 1 to step 3 to switch on the BS-P-MOSFET path is shown below.

Step 1: Switch on the transistor Q_1 by giving control voltage V_{B2ctrl}.

$$V_{R3} = V_{B2ctrl} \times (R3/(R3 + R4)), \quad (1)$$

$$I_1 = \left(V_{B2ctrl} - V_{BE(Q1)}\right)/R4, \quad (2)$$

where $V_{R3} > 1.2 \times V_{BE(ON)}$ is recommended before switch on Q_1 and the current of R_3 can be ignored after conducting Q_1; 50 µA $< I_1 <$ 100 µA is recommended and C_1 is parallel with R_3 to avoid malfunction.

Step 2: Switch on the P-MOSFETs Q_2 and Q_3 after Q_1 is switched on and the current I_1 drives I_2 and V_{R1}.

$$I_2 = \left(V_{B2+} - V_{CE(Q1)} - V_{DS(Q2)}\right)/(R1 + R2), \quad (3)$$

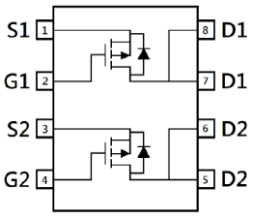
$$V_{R1} = I_2 \times R1, \quad (4)$$

where $V_{R1} > V_{gs(th)}$, 8 V $< V_{R1} <$ 12 V is recommended for switch on, and $V_{R1} <$ 0.2 V for switch off.

Step 3: Finish to conduct BS-P-MOSFET path to EQ-BUS.

3.2.2. Implementation and Test Results for BS-P-MOSFET Circuit

The transistor Q_1 uses the BC846, and the Q_2 and Q_3 use a dual P-MOSFET (MTB60B06Q8) in SOP8 package for size reduction, whose basic specification is shown in Figures 13 and 14 shows the implementation of the BS-P-MOSFET drive circuit.



BV_{DSS}	-60V
I_D@V_{GS}=-10V, T_C=25°C	-6A
I_D@V_{GS}=-10V, T_A=25°C	-3A
$R_{DS(ON)}$ typ. @V_{GS}=-10V, I_D=-3A	62mΩ
$R_{DS(ON)}$ typ. @V_{GS}=-4.5V, I_D=-2A	70mΩ

Figure 13. Dual p-channel power MOSFET (MTB60B06Q8).

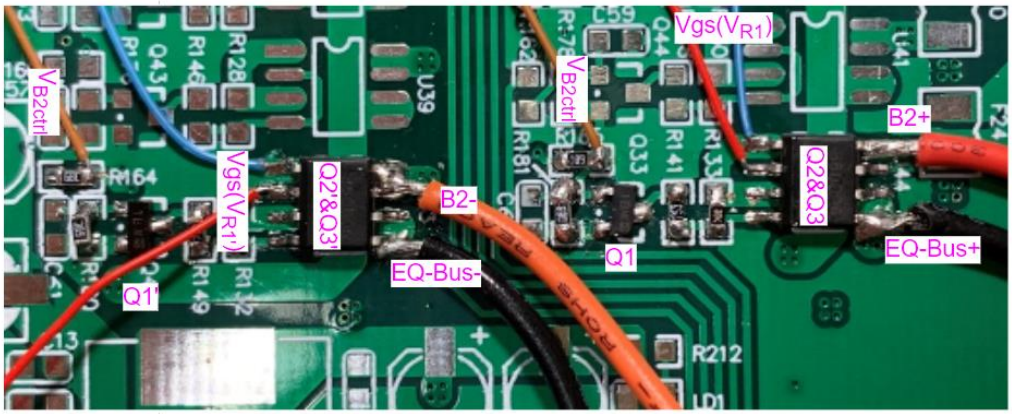


Figure 14. The implementation of BS-P-MOSFET drive circuit.

Based on the operation principle of Figure 12, the settings are defined as B_1 = 42 V (corresponding to the B_1~B_{n-1} string of the battery pack) and B_2 = 4 V (corresponding to the B_n). Other settings are R_1 = 20 kΩ, C_1 = 10 nF, R_2 = 75 kΩ, R_3 = 50 kΩ, and R_4 = 50 kΩ. We use the constant resistor mode of electrical load to simulate R_{EQ} for obtaining $I_{EQ} \cong 1$ A. Therefore, the calculated result is $V_{R3} = 1.65$ V ($V_{B2ctrl} = 3.3$ V), $I_1 \cong 52$ μA, and the voltage range of V_{R1} and $V_{R1'}$ is 9.2 V (B+ = 46 V) and 8.4 V (B+ = 42 V), respectively. Figures 15 and 16 show the signal of V_{B2ctrl}, V_{R1}, and V_{EQ} to exhibit the transient state of the switch on and off.

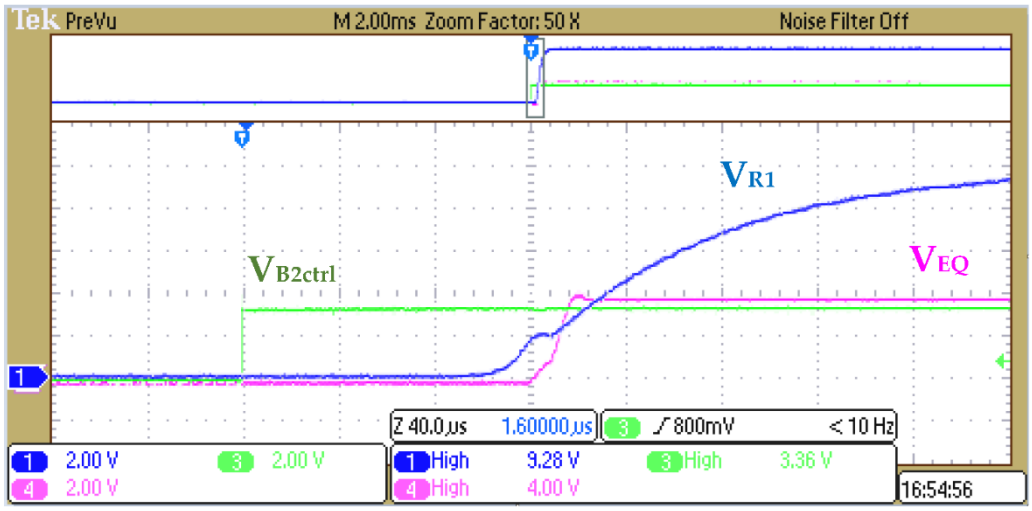


Figure 15. Transient state of turn on Q_2 and Q_3 with $I_{EQ} = 1$ A.

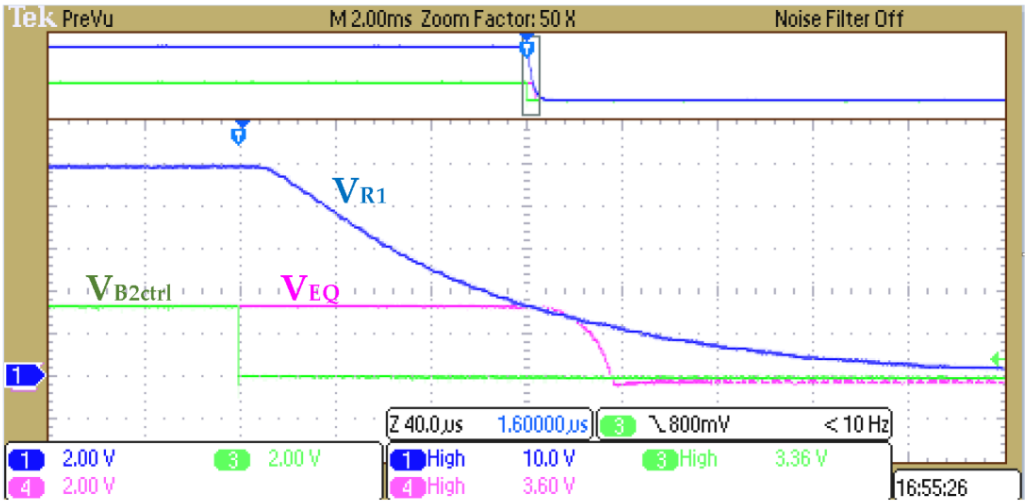


Figure 16. Transient state of turn off Q_2 and Q_3 with $I_{EQ} = 1$ A.

3.3. BS-N-MOSFET Drive Circuit

Figure 11 can be simplified as Figure 17, where only two cells are series connected. The B_1 in Figure 12 corresponds to the B_1 cell of Figure 11. The B_2 in Figure 17 corresponds of B_2 to B_n of Figure 11. We use Figure 17 to demonstrate the principle of BS-N-MOSFET driving circuit with B_{1+} path to EQ-Bus+ because the circuit of B_{1-} path to EQ-Bus- is the same structure. Therefore, we only use B_{1+} to demonstrate the operation principle.

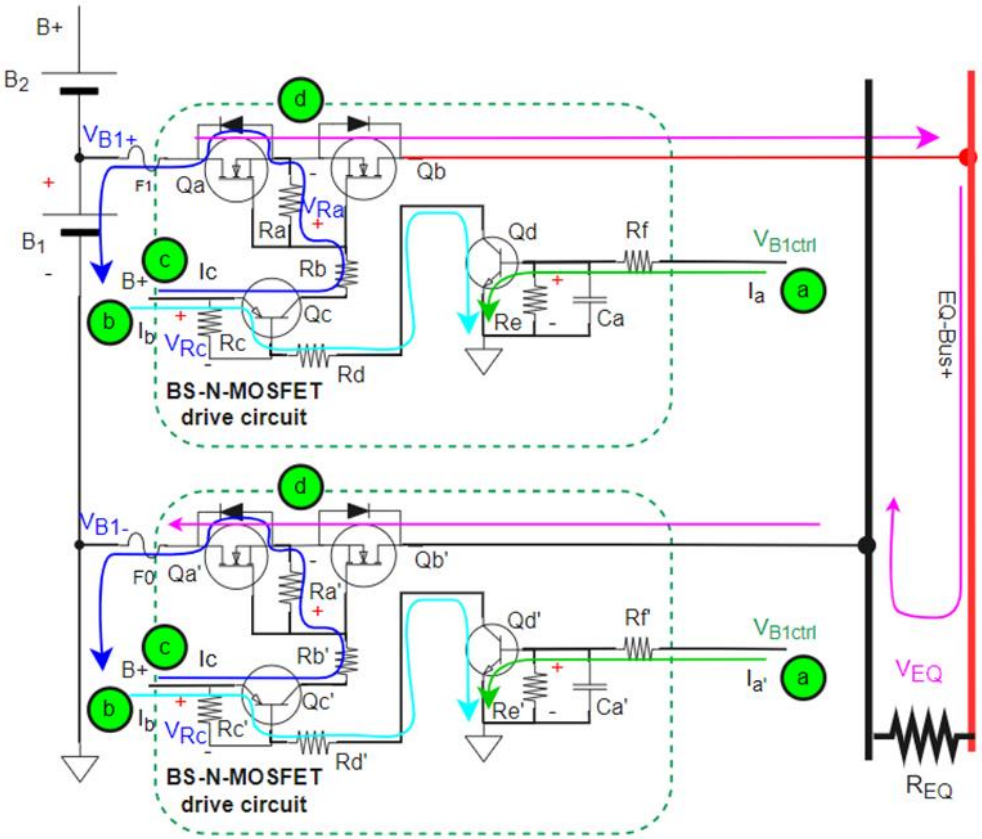


Figure 17. Simplified Figure 11 as a battery pack with 2S configuration for demonstrating BS-N-MOSFET drive circuit.

3.3.1. Schematic and Calculation for BS-N-MOSFET Circuit

In Figure 17, the principle of step 1 to step 4 for conducting the BS-N-MOSFET path is shown below:

Step 1: Conduct the transistor Q_d by giving control voltage V_{B1ctrl}.

$$V_{Re} = V_{B1ctrl} \times (Re/(Re + Rf)), \tag{5}$$

$$I_a = \left(V_{B1ctrl} - V_{BE(Qd)}\right)/Rf, \tag{6}$$

where $V_{Re} > 1.2 \times V_{BE(ON)}$ is recommended before conducting Q_d and the current of R_e can be ignored after conducting Q_d; 50 μA $< I_a <$ 100 μA is recommended and C_a is parallel with R_e to avoid malfunction.

Step 2: Conduct the transistor Q_c after Q_d is conducted and the current I_a drives;

$$V_{Rc} = \left(V_{B+} - V_{EB(Qc)}\right) \times (Rc/(Rc + Rd)), \tag{7}$$

$$I_b = \left(V_{B+} - V_{EB(Qc)} - V_{CE(Qd)}\right)/Rd, \tag{8}$$

where $V_{Rc} > 1.2 \times V_{BE(ON)}$ is recommended before conducting Q_c and the current of R_c can be ignored after conducting Q_c; 50 μA $< I_b <$ 100 μA is recommended to avoid malfunction.

Step 3: Conduct the N-MOSFETs Q_a and Q_b after Q_c is conducted and the current I_b drives;

$$I_c = \left(V_{B+} - V_{B1} - V_{EC(Qc)} - V_{SD(Qa)}\right)/(Ra + Rb), \tag{9}$$

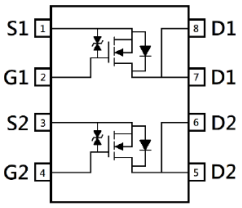
$$V_{Ra} = I_c \times R_a, \tag{10}$$

where $V_{Ra} > V_{gs(th)}$, and 8 V $< V_{Ra} <$ 12 V is recommended.

Step 4: Finish to conduct BS-N-MOSFET path to EQ-BUS.

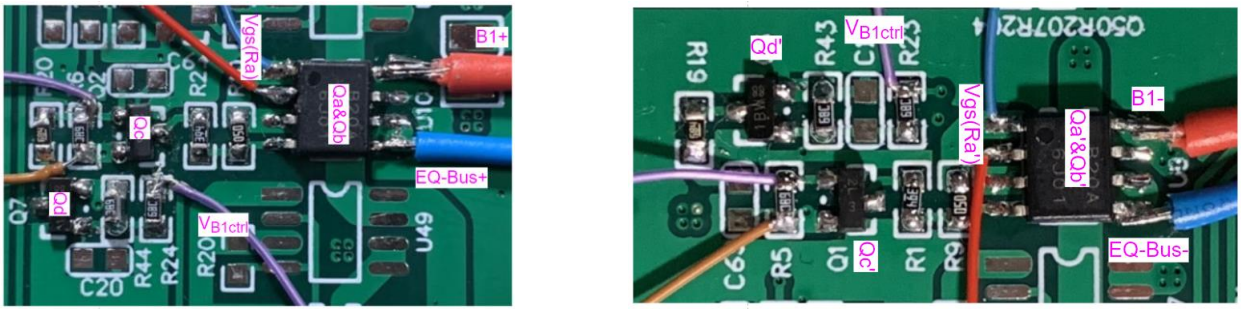
3.3.2. Implementation and Test Results for BS-N-MOSFET Circuit

The transistor Q_d uses the BC846 and Qc uses the MMBT5401, and the Q_a and Q_b use a dual N-MOSFET (MTB20A06KQ8) in SOP8 package for size reduction, whose basic specification is shown in Figures 18 and 19 shows the implementation of the BS-N-MOSFET drive circuit.



BV_{DSS}	60V
I_D@V_{GS}=10V, T_C=25°C	13A
I_D@V_{GS}=10V, T_A=25°C	6A
$R_{DS(ON)}$ typ.@V_{GS}=10V, I_D=6A	17mΩ
$R_{DS(ON)}$ typ.@V_{GS}=4.5V, I_D=6A	20mΩ

Figure 18. Dual n-channel power MOSFET(MTB20A06KQ8).



(**a**) (**b**)

Figure 19. The implementation for BS-N-MOSFET drive circuit verification: (**a**) BS-N-MOSFET path for B1+ in front of PCB; (**b**) BS-N-MOSFET path for B1—at the rear of PCB.

Based on the operation principle of Figure 17, the settings are defined as B_1 = 4 V (assumed the first string of the battery pack) and B_2 = 42 V (assumed the B_2~B_n string of the battery pack). Other settings are R_a = 110 kΩ, R_b = 390 kΩ, R_c = 50 kΩ, R_d = 680 kΩ, R_e = 50 kΩ, R_f = 50 kΩ, and C_a = 10 nF. We use the constant resistor mode of electrical load to simulate R_{EQ} for obtaining $I_{EQ} \cong 1$ A. Therefore, the calculated result is $V_{Re} = 1.65$ V ($V_{B1ctrl} = 3.3$ V), $I_a \cong 52$ μA, and the voltage range of V_{Ra} and $V_{Ra'}$ are 9.38 V and 9.24 V, respectively. Figures 20 and 21 show the signal of V_{B1ctrl}, V_{Ra}, and V_{EQ} to exhibit the transient state of the switch on and off.

The above experimental results have verified the transient characteristics of the BS-MOSFET circuit design of the highest string cell and the lowest string cell in the battery pack, respectively. Briefly, the time of the ON/OFF transient state is around 80–100 us. Therefore, the following section will demonstrate the A-HEC design to the BMS board and test the balancing current for the actual battery pack.

Table 1 shows the comparison results between the P-HEC and conventional PECs. P-HEC is suitable for a battery pack with many cells connected in series (>8S configuration), such as electric bicycles, electric scooters, or electric vehicles. The conventional PEC is suitable for the battery pack (2S or 3S configuration) of the notebook, power tool, or tablet computer.

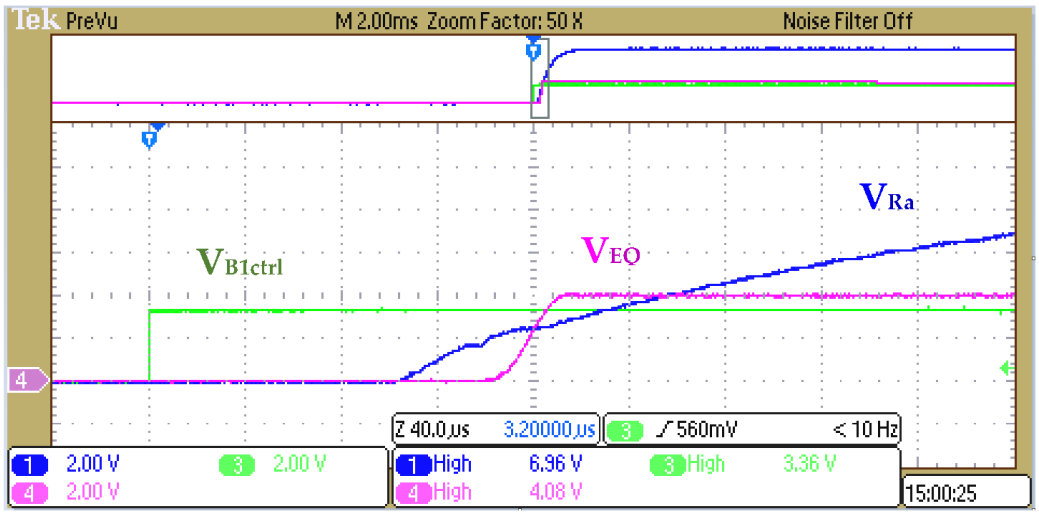


Figure 20. Transient state of turn on Qa and Qb with $I_{EQ} = 1$ A.

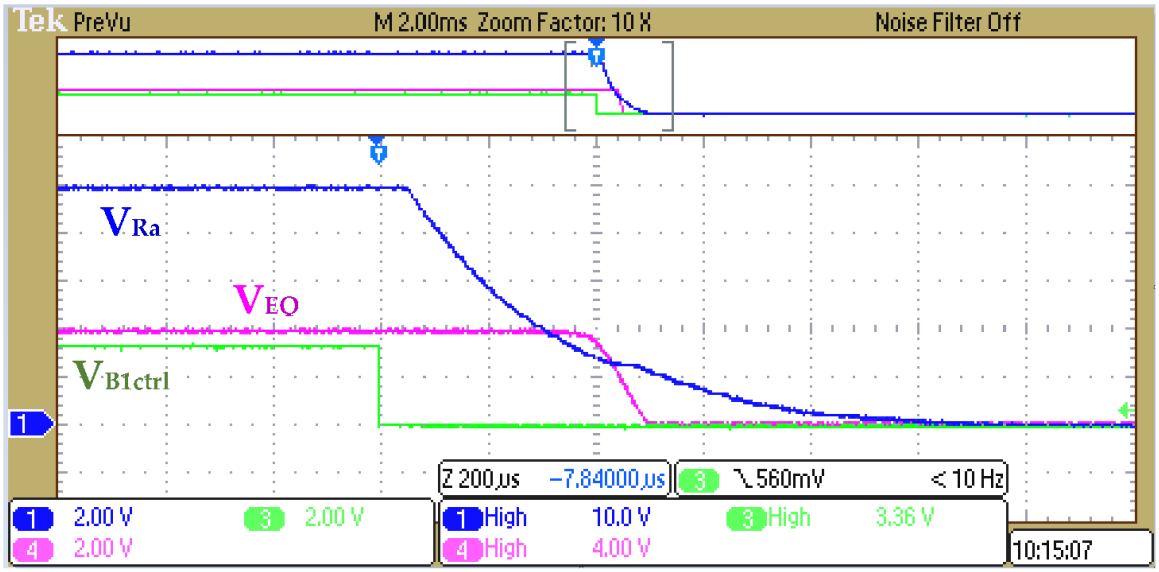


Figure 21. Transient state of turn off Qa and Qb with $I_{EQ} = 1$ A.

Table 1. Comparison of the proposed P-HEC with conventional PECs (series cells = N).

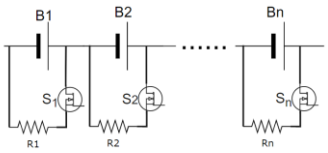
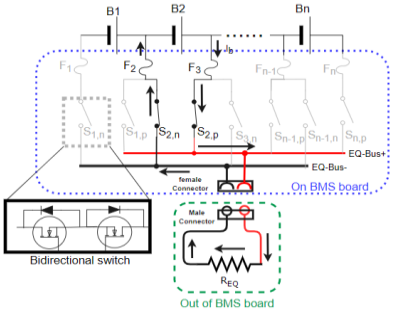
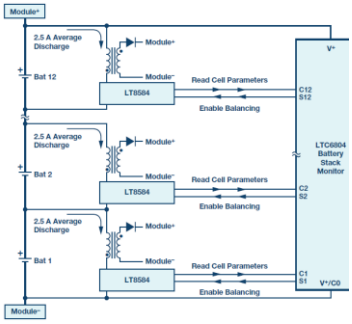
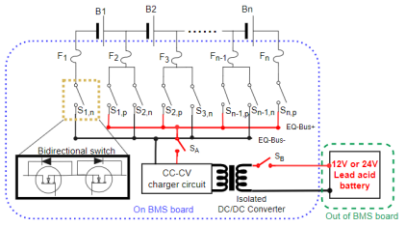
Item	PEC (Conventional)	P-HEC (Proposed)
Topology		
Limitation	—	Pack voltage > 8 V
Architecture	Switch + resistor	Cell selector + Discharge unit
MOSFET numbers/cost	N (Number of series cell) ~0.15 USD/MOSFET	(N + 1) × 2(Dual package) ~0.25 USD/Dual MOSFET
Channel cost	~0.2 USD/channel	~0.35 USD/channel
Max. ON channel	≤2 (Limited by heat)	1
Fail-safe	—	Yes (fuse)
Discharge unit	Power resistor × N (Typical: 33 Ω)	Power resistor × 1 (Typical:2 Ω), Fan or heater
Max. current	~0.127 A@4.2 V	~2.1 A@4.2 V
Waste heat	0.3–0.5 W/channel	4.5~8 W
Power cost	~0.4 USD/W (0.2 USD/0.5 W)	~0.04 USD/W (0.35 USD/8 W)
Location	On BMS board	Out of BMS board
Occupied area	1× (Including N resistors)	1.5–2× (Only fuse and switch arrays are placed on BMS)

Table 2 shows the comparison results between the A-HEC and the commercial active equalizer control IC (LT8584) evolved from Figure 3. The A-HEC is a more cost-effective solution than the LT8584 for the high voltage battery pack (>3S configuration) when the

total balancing current of the battery pack/module is less than 3 A. Not only is the channel cost of the HEC low, but also the occupied circuit board area of the equalizer circuit is only 2~3 times of the passive equalizer.

Table 2. Comparison of the proposed A-HEC with the conventional AEC (series cells = N).

Item	AEC (Commercial LT8584)	A-HEC (Proposed)
Topology		
Architecture	DC/DC converter	Cell selector + isolated charger
Channel cost	N × 6 USD LT8584 (~4) +Transformer (~2) Transformer: COILCRAFT NA5743-AL	(N × 0.25 × 2) + 15 USD Switch array(N × 0.25 × 2 paths) +Charger (~3) +Isolated DC/DC converter (~12) Iso. DC/DC: MEANWELL SCW12B-05
Max. ON channel	Multi-channel	1 channel
Fail-safe	—	Yes (fuse)
Max. current	N × 2.5 A	~2.1 A@4.2 V

4. Implementation of the A-HEC to the Battery Monitoring Unit of a Battery Pack

Figure 22 shows the implementation of the proposed A-HEC circuit of Figure 9 to the battery monitoring unit (BMU) board, and the maximum balancing charging current can reach 2.2 A. The battery pack has a 22S1P configuration with 25 Ah LTO cells, the cell operating voltage is 1.8~2.7 V and the pack operating voltage is 39.6~59.4 V. The battery packs can be series connected to form a high-voltage battery system in which the system voltage can be up to 600 V.

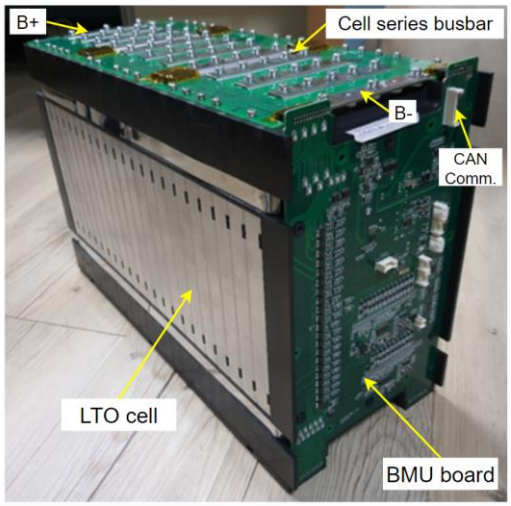
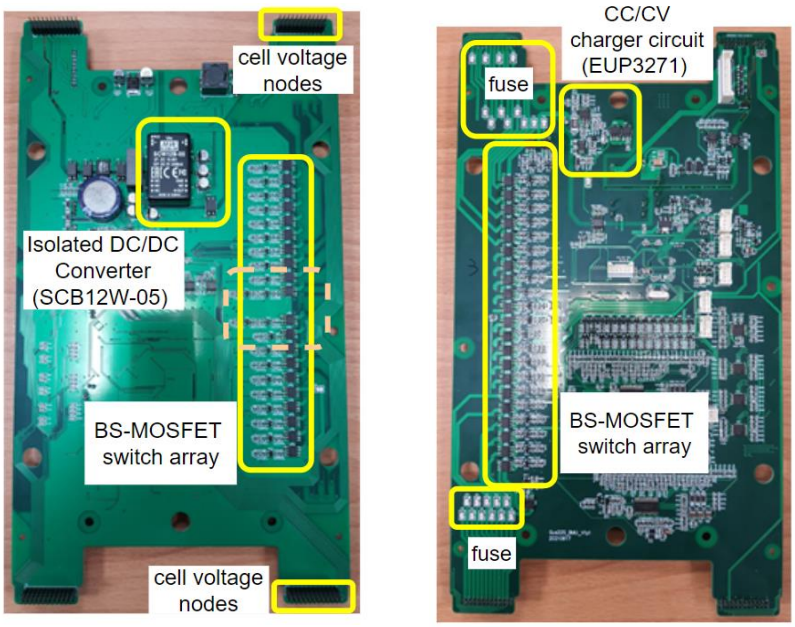


Figure 22. LTO battery pack with proposed A-HEC circuit on BMU board.

The circuit placement of the A-HEC circuit of the BMU board of Figure 22 is shown in Figure 23. The BS-MOSFET could be BS-N-MOSFET or BS-P-MOSFET, the BS-N-MOSFET and BS-P-MOSFET circuit are used to B_1–B_3 and B_4–B_{22}, respectively. We used a commercial product SCW12B-05 (12 W, η = 83%) as the isolated DC/DC converter of Figure 9 to transfer auxiliary input 18–36 V to isolated output 5 V. In Figure 9, the CC/CV charger circuit is implemented by the LIB charger IC (EUP3271) of which the maximum charge current is 4 A.



(**a**) (**b**)

Figure 23. The BMU board with A-HEC circuit: (**a**) back; (**b**) front.

An enlarged view of the BS-MOSFET switch array of Figure 23 is shown in Figure 24, which includes BS-N-MOSFET drive circuit for the B_1~B_2 cells and BS-P-MOSFET for the B_3~B_{22} cells, respectively.

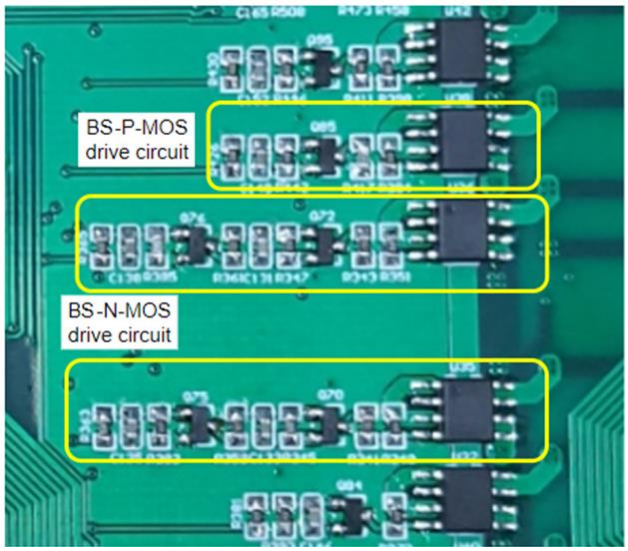


Figure 24. Enlarged view of the BS-N-MOSFET and BS-P-MOSFET drive circuit.

The balance current experiment results for the proposed A-PEC circuit design of Figure 23 are summarized in Table 3. The balancing current for each node of the battery string is around 1.95–2.25 A.

Table 3. The balancing current result for each node of the battery string.

Voltage Node	Balancing Charge Current (mA)	Voltage Node	Balancing Charge Current (mA)
B_{1+}	2265	B_{12+}	2265
B_{2+}	2270	B_{13+}	2270
B_{3+}	2255	B_{14+}	2265
B_{4+}	2260	B_{15+}	2220
B_{5+}	2265	B_{16+}	2270
B_{6+}	2265	B_{17+}	2245
B_{7+}	2270	B_{18+}	2270
B_{8+}	2270	B_{19+}	1960
B_{9+}	2265	B_{20+}	1955
B_{10+}	2260	B_{21+}	1975
B_{11+}	2260	B_{22+}	2260

5. Conclusions

This paper proposed the cost-effective and simple passive/active HEC design for a BMS. The key idea of the HEC is to let the switch array as a string cell selector for selecting the string cell to charge (A-HEC) or discharge (P-HEC) for cell balancing purposes. Therefore, the BS-MOSFETs of the switch array are equal to an ON/OFF switch and do not need high-speed switching to move energy. Furthermore, we proposed a low-cost and simple control circuit to drive these BS-MOSFET paths of HEC, which had been verified with a 48 V LTO battery pack. The comparison of the proposed HEC with conventional PEC and AEC are shown in Tables 1 and 2, respectively. The power cost per channel, low-temperature rise on the BMS by placing the discharge unit outside the BMS circuit board, and fail-safe function are the competitive advantages of P-HEC. Similarly, the low cost of the BS-MOSFET driving circuit, fail-safe and small size on BMS are the significant features of the A-HEC. The limitation of the HEC is the minimum pack voltage should be higher than 8 V (>3S~4S configuration) for driving the MOSFET and control circuit. Based on the above features, the equalizer circuit design with the HEC topology is a cost-effective solution for various EVs and ESSs with high voltage battery packs.

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Abbreviations

BMS	Battery management system
AFE	Analog front end
BMU	Battery monitoring unit
EV	Electric vehicle
ESS	Energy storage system
LIB	Lithium-ion battery
EC	Equalizer circuit
M-AEC	Modularized equalizer circuit
PEC	Passive equalizer circuit
AEC	Active equalizer circuit
HEC	Hybrid equalizer circuit
P-HEC	Passive hybrid equalizer circuit
A-HEC	Active hybrid equalizer circuit
AP-HEC	Active/passive hybrid equalizer circuit
BS	bidirectional switch
BS-MOSFET	bidirectional switch with back-to-back MOSFET
BS-P-MOSFET	bidirectional switch with back-to-back P-MOSFET
BS-N-MOSFET	bidirectional switch with back-to-back N-MOSFET

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