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Review

Review, Classification and Loss Comparison of Modular Multilevel Converter Submodules for HVDC Applications

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Abstract: The circuit topology of a submodule (SM) in an modular multilevel converter (MMC) defines many of the functionalities of the complete power electronics conversion system and the specific applications that a specific MMC configuration can support. Most prominent among all applications for the MMC is its use in high-voltage direct current (HVDC) transmission systems and multiterminal dc grids. The aim of the paper is to provide a comprehensive review and classification of the many different SM circuit topologies that have been proposed for the MMC up to date. Using an 800-MVA, point-to-point MMC-based HVDC transmission system as a benchmark, the presented analysis identifies the limitations and drawbacks of certain SM configurations that limit their broader adoption as MMC SMs. A hybrid model of an MMC arm and appropriate implementations of voltage-balancing algorithms are used for detailed loss comparison of all SMs and to quantify differences among multiple SMs. The review also provides a comprehensive benchmark among all SM configurations, broad recommendations for the benefits and limitations of different SM topologies which can be further expanded based on the requirements of a specific application, and identifies future opportunities.

Keywords: high-voltage direct current (HVDC); modular multilevel converter; multilevel converters; submodules/cells

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1. Introduction

Large-scale integration of renewable energy systems, predominantly through larger wind and solar farms, combined with the need for greater flexibility in operating electricity networks are among the key drivers of global growth in high-voltage direct current (HVDC) transmission systems [1]. Voltage-source converter (VSC) HVDC systems based on modular multilevel converters (MMCs) combine the *system advantages* of fast and independent active and reactive power control, passive network supply, black start capabilities, frequency support and power oscillation damping [2] with *power electronics benefits* such as scalable design [3], increased reliability, lower conversion losses and reduced filtering requirements, thus offering a commercially competitive solution. There are multiple reviews of the MMC topology in the current literature and interested readers can consult some of the following references [3–10].

From the perspective of power electronics conversion technology, the advantages of the modular design introduced by the MMC [11] have facilitated its use in other applications such as Static Synchronous Compensators (STATCOMs) [12], dc–dc conversion [4], battery energy storage systems (BESS) [13] and traction power supply systems [14]. In

HVDC transmission systems, MMC defines the current state-of-the-art converter topology with power transmission capacities of single MMC-based HVDC converter stations exceeding 2 GW, back-to-back solutions [15], multiterminal HVDC systems [16], hybrid line-commutated converter (LCC)-VSC HVDC configurations [17] and, most recently, the use of overhead lines in HVDC systems [9]. The early control system of MMC mainly focuses on the arm voltages generation [5]. To improve the system, the dynamic model is introduced to make the AC/DC current approach the reference value [10], and the average capacitance voltage control and capacitance voltage balance strategy are added [4].

In a modular multilevel converter (Figure 1), the submodules (SMs) are the major building block and also the key enabler of modularity in the topology. An MMC arm, which is formed by the series connection of multiple SMs, acts as a controllable voltage source [6]. The voltage (v_{arm}) depends on the number of SMs which are bypassed or connected within the arm, and the number of voltage levels in the output of each SM [7]. Beyond the high-level operation of the MMC (i.e., control of output voltages and currents), the specific topology of each individual SM further defines multiple features in the converter [8], for instance its fault blocking capability, reliability and redundancy aspects [18], internal voltage balancing requirements, etc. Several basic internal MMC variables such as its capacitor voltages, switching frequency, conduction and switching losses are also set by the choice of a SM structure [19].

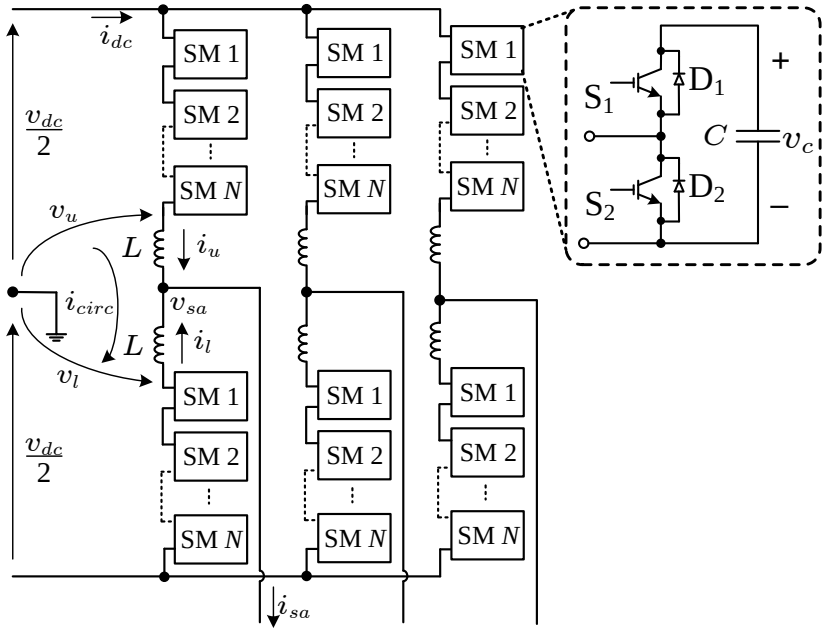


Figure 1. Circuit structure of a three-phase Modular Multilevel Converter based on half-bridge SMs.

Dealing with dc-side faults is particularly important in VSC-HVDC systems, especially as HVDC systems expand to large dc grids. In terms of the pole-to-ground fault in bipolar MMC systems, the faulty converter should be blocked to ensure the other converters can still operate normally while the dc component of the current is reduced [20]. Aiming to protect the MMC from damage due to dc-side faults, a virtual load configuration connected in parallel with a hybrid dc circuit breaker (DCCB) was proposed in [21], which can limit the dc-fault currents and improve the dc-fault tolerance of the converter. As the dc-fault current flows through the converter, the SMs need to have the ability to withstand this rising current for the period before any dc protection is activated [22]. This is further affected by whether a dc-fault is handled internally by the converter or through external dc protection. The dc fault-clearing capabilities of SMs define not only the design of the MMC, but also the overall system losses, cost and the design and footprint of the dc substation and specifications of any local DCCBs [23].

The structure of the SM is an important element of the MMC and multiple SM circuit topologies and configurations have been proposed in the existing literature. This has been the case, especially in recent years, where substantial SM topologies have been presented, specifically aimed at extending the functionalities of the MMC, in many cases aligned with niche applications of the converter rather than generic use as a VSC converter. Motivated by the above, the objective of this paper is to provide a comprehensive review of the existing SM topology literature, especially on those SMs that are well-suited to HVDC applications.

Instead of providing a repetitive description of SMs and switching states, which are already available in the literature and can be found in the corresponding references for each SM, the work of this paper aims to:

- Provide a current and detailed update on the existing status of MMC SMs. This is deemed necessary due to the considerable work presented in the literature that contributes to the development of novel SM topologies while also considering their suitability for HVDC applications;
- Provide multiple classifications of the SMs based on their characteristics and functionalities;
- Offer a comprehensive loss evaluation and comparison of SMs suited to HVDC applications, also considering practical operation aspects, such as voltage balancing and circulating current control and illustrate performance-related aspects of the different SM topologies.

The paper is structured as follows: Section 2 provides an overview and broad categorisation of the more than 50 SMs different SM topologies currently proposed in the literature. Detailed classifications based on an array of characteristics are provided in Section 3. The benchmark 800 MVA HVDC system and the modelling of the SMs with associated results are provided in Section 4. Comprehensive loss calculations and comparisons are provided in Section 5 and conclusions from this work are summarized in Section 7.

2. SM Configurations

2.1. Half and Full-Bridge Sub-Modules

Despite the large number of SM topologies and different configurations that have been proposed in the literature, the main differentiating feature between SMs is whether an SM can generate voltages of single polarity (positive) or both polarities (positive and negative) at its output terminals. This characteristic allows a general classification of SMs as either unipolar or bipolar. The unipolar and bipolar SMs most commonly applied in the converter are derived from basic power electronics topologies, i.e., the half-bridge and the full-bridge configurations. Some of the key characteristics of these two SMs are explained in the following sections to form the basis of the analysis for the remaining unipolar and bipolar SM configurations.

2.1.1. The Half-Bridge Submodule (HB-SM)

The HB-SM represents the simplest and most common SM topology utilized in MMCs. It is composed of a single capacitor and two insulated-gate bipolar transistors (IGBTs) that operate in a complementary mode. The output voltage of the SM is in a simple binary relation to the switching state of device S_1, with the output voltage being equal to V_c when S_1 is on (Figure 2a) and 0 when S_1 is off (Figure 2b). The direction of the current within the converter arm defines whether the capacitor is charging or discharging, as shown in Table 1.

For protection reasons, semiconductor devices in the SM should be blocked under dc-side faults. In the case of the HB-SM and all other unipolar SMs, diodes form a conduction path from the ac to the dc side that continues to feed the fault current. Therefore, in order to isolate the converter from dc-side faults, an additional device (e.g., DCCB) is usually necessary [24]. The blocking state for the HB-SM is shown in Figure 2c. Under all operating conditions, the current flows through only one of the SM devices which are uniformly rated based on the SM capacitor voltage V_c, as shown in Table 2.

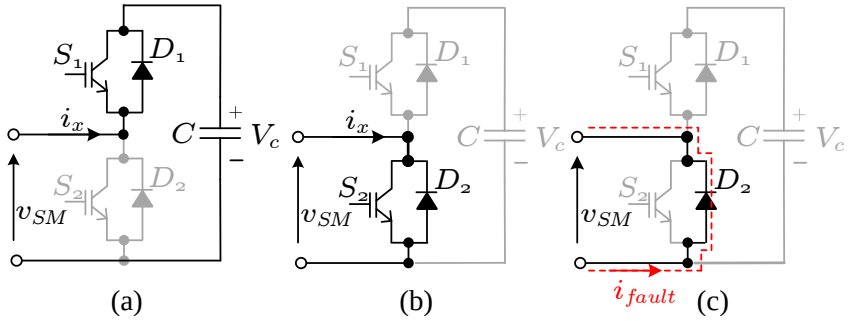


Figure 2. Half-bridge SM: (**a**) connected state, (**b**) bypassed state, and (**c**) blocking state.

Table 1. HB-SM switching states table.

States	S_1	S_2	V_{out}	$I_x > 0$	$I_x < 0$
State 1	1	0	V_C	C charging	C discharging
State 2	0	1	0	/	/

Table 2. HB-SM device blocking voltage.

States	V_{S1}	V_{S2}	Number of Devices Conducting Current
State 1	0	V_C	1
State 2	V_C	0	1

2.1.2. The Full-Bridge Submodule (FB-SM)

The full-bridge SM (FB-SM) is widely used as a bipolar SM, as shown in Figure 3. Similarly to the HB-SM, it provides a positive and a zero voltage level (Figure 3a,b, respectively), which give the FB-SM all the functionalities of the HB-SM. Additionally, the negative state of Figure 3c can be used [25] for improving the voltage/energy balancing and current control performance of the MMC [26], enabling multiple harmonic injections in the MMC arm [27]. FB-SMs can also be used in other converters such as the Alternate Arm Converter (AAC) [28]. The complete switching states for the FB-SM can be seen in Table 3.

Revisiting the dc-fault scenario, the fault current path through the FB-SM includes the SM capacitor (Figure 3d) effectively providing the FB-MMC with dc-fault clearing capabilities, as described by State 6 of Tables 3 and 4. This is the most prominent feature of the FB-SM and all other bipolar SMs, as it allows the converter to operate in a dc-grid without requiring additional DCCBs. The total blocking voltage required for dc-fault is equal to the total dc-link voltage, which can be provided by half the SMs in an FB-MMC. This means that an MMC built exclusively with FB-SMs is over-designed, a conclusion which gives rise to a whole family of SMs (as discussed in the following sections) as well as many hybrid configurations for the MMC [29].

Table 3. FB-SM switching states table.

States	S_1	S_2	S_3	S_4	V_{out}	$I_x > 0$	$I_x < 0$
State 1	1	0	0	1	V_C	C charging	C discharging
State 2	0	1	0	1	0	/	/
State 3	1	0	1	0	0	/	/
State 4	0	1	1	0	$-V_C$	C discharging	C charging
State 5	0	0	0	0	V_C	C charging	/
State 6	0	0	0	0	$-V_C$	/	C charging

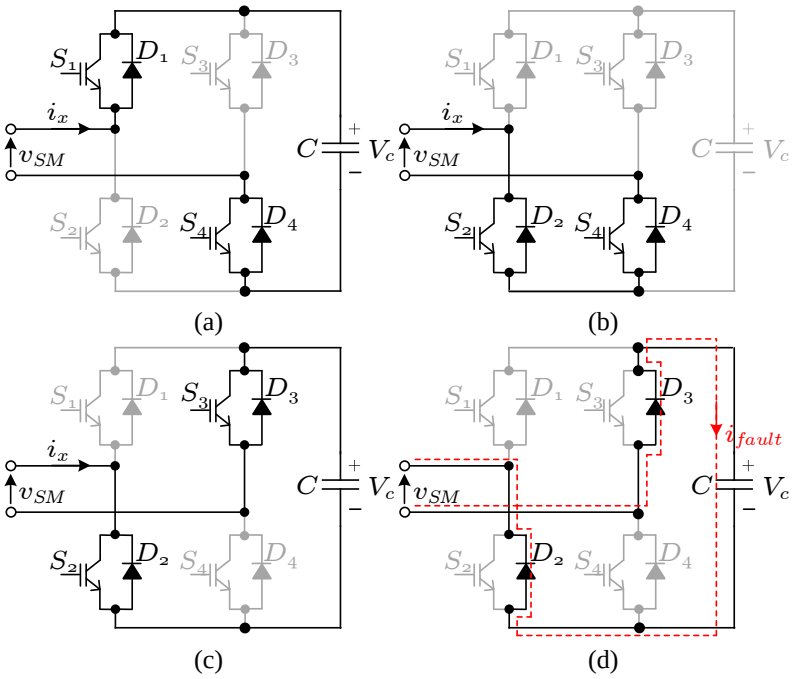


Figure 3. Full-bridge SM: (**a**) positive state, (**b**) zero state, (**c**) negative state, and (**d**) blocking state.

Table 4. FB-SM device blocking voltage.

States	V_{S1}	V_{S2}	V_{S3}	V_{S4}	Number of Devices Conducting Current
State 1	0	V_C	V_C	0	2
State 2	V_C	0	V_C	0	2
State 3	0	V_C	0	V_C	2
State 4	V_C	0	0	V_C	2
State 5	0	V_C	V_C	0	2
State 6	V_C	0	0	V_C	2

2.2. Unipolar SMs

From the perspective of arm voltage generation, unipolar SMs provide identical functionalities to the HB-SM as they can only generate voltages of positive polarity. This means that any high-level controllers remain identical to the ones used in the HB-MMC and only internal (typically voltage balancing) requirements need to be considered for each SM. The unipolar SMs are shown in Figure 4. Unipolar SMs are generally simpler in structure and some topologies can reduce the losses of the converter. However, unipolar SMs normally can offer only a subset of functions in the operation of the MMC. Furthermore, a bypass thyristor may be required for each SM or for groups of SMs to guarantee the fault tolerant operation of the converter [30].

Unipolar SMs structures can be based on well-known multilevel converter topologies such as the flying capacitor (FC—Figure 4a [31]) or the active neutral-point clamped converter (M-ANPC—Figure 4b, [32]) providing additional voltage levels from a single SM. Similar structures have been proposed based on NPC and T-type converters, however there are challenges with balancing of the capacitor voltages at unity power factor, as will be discussed in Section 2.5. This lack of capacitor voltage balancing makes these SMs unsuitable for HVDC applications. Addition (SS-SM, Figure 4c [33]) or substitution of devices with bidirectional switches (BBSM1 and BBSM2, Figure 4d,e [34]) result in unipolar SMs with identical behavior to the HB-SM. Such structures may provide a fault current blocking state to the converter; however, the interruption of the fault current in the main

path and the lack of fault current dissipation paths can lead to substantial over-voltages and potential destruction of the SMs during a dc-fault.

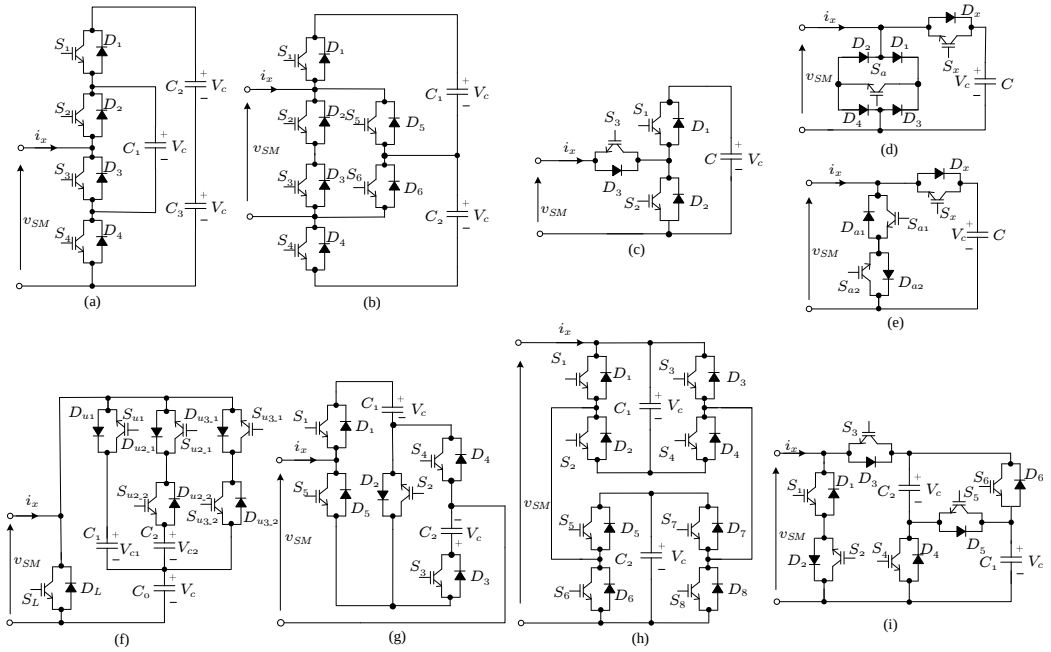


Figure 4. Unipolar SMs: (**a**) FC-SM—Flying capacitor SM; (**b**) M-ANPC-SM—Modified active neutral-point clamped unipolar SM; (**c**) SS-SM—Series switch SM; (**d**) BBSM1—Bidirectional blocking SM 1; (**e**) BBSM2—Bidirectional blocking SM 2; (**f**) SSwC-SM—Stacked switched capacitor SM; (**g**) 3L-SwCSM—Three-level switched-capacitor SM; (**h**) 3L-DSM—Three-level double SM; and (**i**) FTSM—Fault tolerant SM.

Other unipolar structures include the stacked switched capacitor SM [35,36] and the three-level switch capacitor SM [37], shown in Figure 4f,g respectively. The switched capacitor structure allows for one or more capacitors to be inserted in series to the main SM capacitor, effectively reducing the required capacitance (and energy stored in the MMC arms) for the same voltage ripple but at the cost of additional devices. The three-level double SM [38] of Figure 4h can replace two HB-SMs for the same number of devices as the FB-SM. The main advantage of this topology is that it allows for parallel connection of devices allowing for higher currents and parallel connection of the capacitors reducing the voltage ripple in capacitors, peculiarly at lower output frequencies. In the fault-tolerant SM [39] shown in Figure 4i, the S_4 and S_6 can be controlled either independently or together and the capacitors in the topology can be connected in parallel when both of the switches are on. Due to the possibility of high circulating current, the capacitor voltage balancing should be considered when the capacitors are connected in parallel. Besides, since the fault tolerance is inherent to the MMC structure by bypassing the faulty SMs, the advantages of a fault tolerant SM are not as major.

2.3. Bipolar SMs

Bipolar SMs have the ability to generate both positive and negative output voltages, meaning that the total arm voltage can have two polarities. This feature provides two key functionalities to the MMC: (i) the capability of blocking and clearing dc-side faults (something that unipolar SMs cannot do and which requires a bypass structure to eliminate extreme stress on semiconductor devices in the SM) and (ii) operation in the overmodulation range by generating output voltages larger than the maximum voltage of the dc-link. These additional functionalities expand the operational envelope of the MMC, the ways it can be designed, sized and controlled as well as further extending its areas of application.

Due to the number of combinations that can be used for generating bipolar SMs, the amount of bipolar circuit topologies proposed in the literature is substantially greater than unipolar ones.

The simplest implementation of a bipolar structure is the combination of a single FB-SM with one HB-SM, in what has been called as a Mix-SM or as a hybrid HB-FB converter, shown in Figure 5a [40]. Based on the analysis of Sections 2.1.1 and 2.1.2, this implementation is straightforward and will not be analysed further.

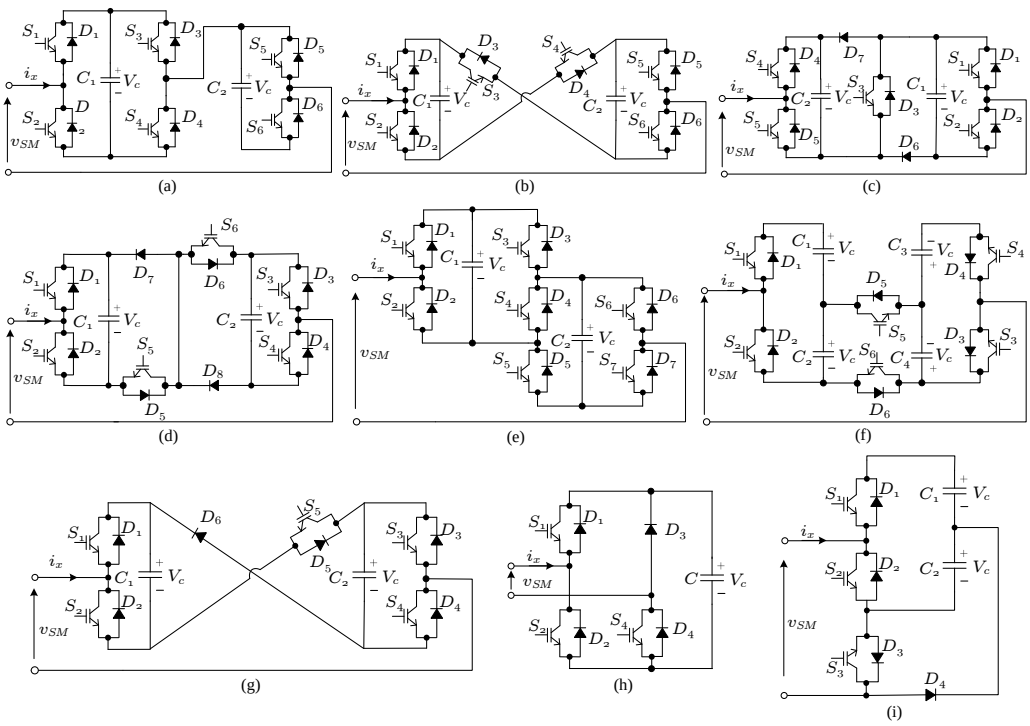


Figure 5. Bipolar SMs: (**a**) Mix-SM—Mix-connected SM; (**b**) CCSM—Cross-connected SM; (**c**) CD-SM—Clamped-double SM; (**d**) 3L-CDSM—Three-level clamped-double SM; (**e**) SFB-SM—Semi-full-bridge SM; (**f**) AFB-CCDSM—Cross-Connected Asymmetrical Full Bridge SM; (**g**) 3L-CCSM—Three-level cross-connected SM; (**h**) UFBSM—"Unipolar-voltage" full-bridge SM; and (**i**) SC-SM—Single-clamped SM.

A common way of implementing a bipolar SM is by combining HB-SMs through a dc-side structure that allows for positive and negative voltages to be generated. These SMs can also be seen as derivatives or simplifications of two or more FB-SMs. Examples in this category of bipolar SMs include the cross-connected SM (CC-SM) [40], the clamped-double SM (CD-SM) [41] and the three-level CD-SM (3L-CDSM), shown in Figure 5b–d, respectively. For CD-SM, under the blocking state, the two capacitors in the topology are connected in parallel. The 3L-CDSM adds two additional switches (S_5, S_6), so the two capacitors can be fully used to clear the dc-side fault. Similar functionalities are provided by the Semi-full-bridge SM (SFB-SM, [42]) and the Cross-Connected Asymmetrical Full Bridge SM (AFB-CCDSM [43]). The SFB-SM is a similar structure to CD-SM, but using IGBTs in the whole topology. On the other hand, the complicated topology of the AFB-CCDSM requires additional balancing. Substitution of switches with diodes create equivalent simplified SMs such as the three-level cross-connected SM (3L-CCSM, [44]).

Substitution of switches to diodes reduces the controllability of a specific SM as not all voltage levels can be generated for both current directions. The UFBSM or "Unipolar-voltage" full-bridge SM [44] and the SC-SM or Single-clamped SM [45] of Figure 5h,i are examples of such SMs, where the negative voltage (either as V_c or $V_c/2$) can only be generated in their blocking state when the arm current direction is negative (i.e., during a dc-fault).

A variety of other bipolar SMs are shown in Figure 6 and include: (i) the CSM or self-blocking composite multilevel SM which is modified by two HB-SM [46] and improves the voltage-balancing capability of the SM capacitors so that negative voltages are only generated during blocking states (Figure 6a); (ii) the 4LT^{2}C is 4-Level T-Type Neutral Point-Clamped SM which addresses the voltage-balancing issues of the three-level T-type SM with the inclusion of S_4 and S_5 [47]. These devices provide an additional path to control the voltage of capacitor C_1 (Figure 6b); (iii) the T^{2}HBSM or T-type half-bridge based SM ([48], Figure 6c); and (iv) ACTSM or Active clamped T-type SM ([49], Figure 6d) which also address voltage-balancing issues of the T-type SM with alternative current paths while providing controllable negative voltages; (v) the switched-capacitor SM [50] expanding unipolar switched capacitor SMs to enable bipolar voltages; (vi) the ASM or Asymmetrical SM ([40], Figure 6i); and (vii) the AUFBSM or Asymmetrical unipolar full-bridge SM [51] which, despite its name, provides bipolar functionalities through an additional capacitor, albeit reducing the scalability of the SM structure due to the unequal voltage blocking of each device; (viii) the DCBSSM or Diode-Clamped Bidirectional Switch SM [52], which uses two clamping diodes (D_7 and D_8) to create a current path which also includes the SM capacitor for the purpose of dc-fault blocking under a negative current.

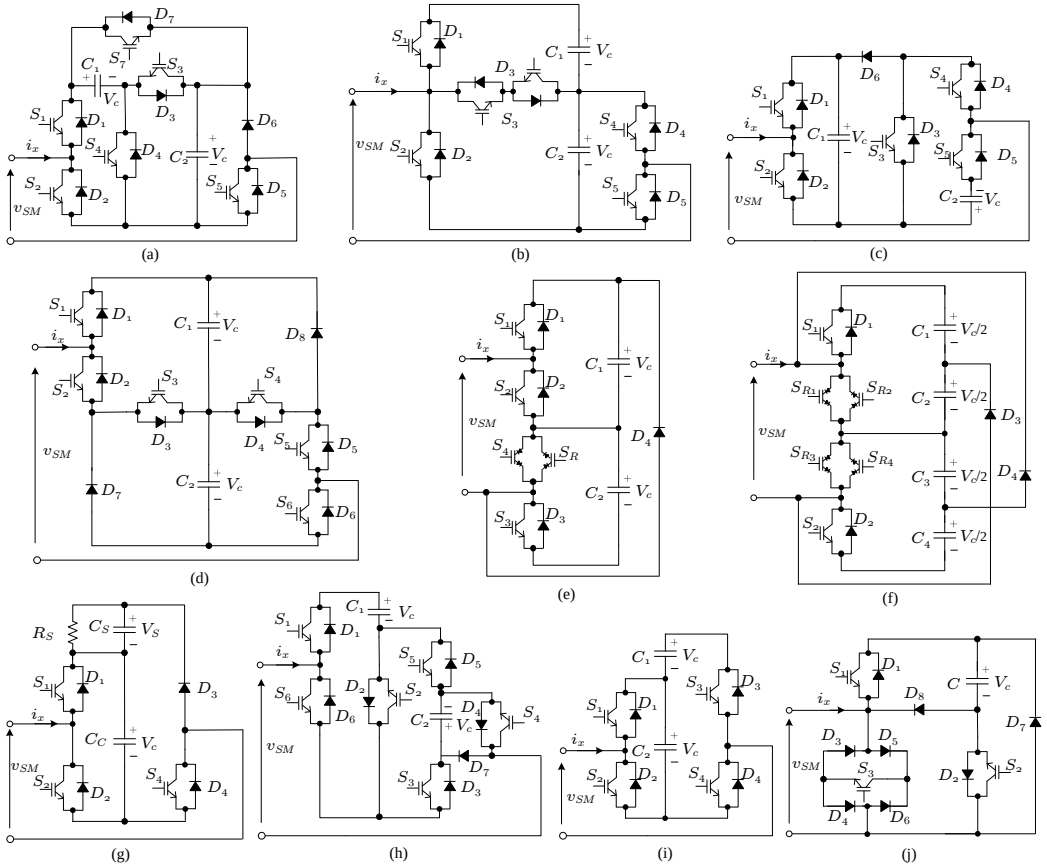


Figure 6. Bipolar SMs (cntd.): (**a**) CSM—Self-blocking composite multilevel SM; (**b**) 4LT^{2}C— 4-Level T-Type Neutral Point-Clamped SM; (**c**) T^{2}HBSM—T-type half-bridge based SM; (**d**) ACTSM—Active clamped T-type SM; (**e**) HDDBSM—Hybrid Double Direction Blocking SM; (**f**) M-HDDBSM—Modified Hybrid Double Direction Blocking SM; (**g**) AUFBSM—Asymmetrical unipolar full-bridge SM; (**h**) SwCSM—Switched-capacitor SM; (**i**) ASM—Asymmetrical SM; and (**j**) DCBSSM—Diode clamp with bidirectional switch SM.

In an effort to reduce losses in the SMs, the concept of the SC-SM (Figure 5i) was extended to double HB-SMs; an extension that leads to two different possible configurations. The HDDBSM (Hybrid Double Direction Blocking SM) of [53] uses a single diode in the

blocking state to provide a current path through one of the two capacitors in the SM [54]. Blocking of the current through the main circuit is provided by means of a bidirectional switch which substitutes one of the unidirectional switches of the SM. The same concept is seen in the modified HDDBSM [55] of Figure 6f which uses substitutes two devices with bidirectional switches and offers a path for the dc-side fault current via splitting capacitors and two additional diodes.

In most configurations, dc-fault blocking is provided by the main devices and particularly capacitors of the SMs. An alternative approach is that of the BBSM/RBSM (Bidirectional blocking SM/Reverse blocking SM) [56] and the RBDSM (Reverse blocking Double SM) [57]. Both of these SMs operate as a regular SM in normal operation but block the current conduction through the main devices of the SM during a dc-fault. Instead, dc-fault clearing capabilities are provided through the inclusion of a bypass circuit using a diode D_x and an additional capacitor C_S which operate (and charge) during the dc-fault blocking state. These two SMs are shown in Figure 7a,b, respectively. The main issues with such an approach are the need for an additional capacitor, which results in a substantial increase in the size of the SM, particularly in high-power applications, as well as pre-charging of the capacitors and the transient response, immediately after a fault if the auxiliary capacitor is not fully charged.

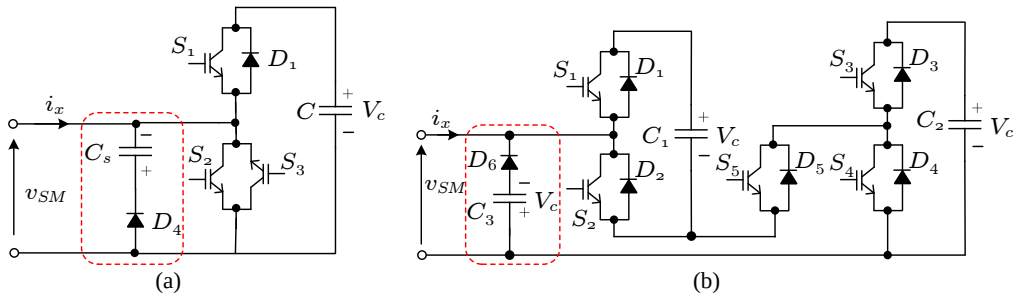


Figure 7. Bipolar SMs with bypass circuits: (**a**) BBSM/RBSM—Bidirectional blocking SM/Reverse blocking SM; and (**b**) RBDSM—Reverse blocking Double SM.

As it will be discussed later, bipolar SMs typically introduce additional semiconductor devices which leads to an increase in the overall power losses of the converter, but this increase in losses should be evaluated together with their fault clearing capacity.

2.4. Multilevel SMs

The combination of FB-SMs and other multilevel topologies or the hybridization of multilevel converters with HB-SMs results in a category of multilevel SMs which, although have extended SM structure, can be treated similar to unipolar or bipolar SMs. These SMs include the dual FB parallel-connected SM and the dual FB (identical to the CCSM of Figure 5b) as 5-level fully controllable SMs [58] which can be seen as alternative connections of two FB-SMs [59].

The 5-LCFCSM (Figure 8c) and 5-LFCSM (Figure 8e) are two FC-SMs [60] connected on the dc-side [61] either through a CD-SM structure or as a multilevel H-bridge [62], while, similarly, the 5-LCNPCSM (Figure 8d) and 5-NPCSM (Figure 8f) are based on the NPC-SMs [63]. The additional switching states and current paths can be used to address the voltage-balancing issue of the NPC-SM through an increase in the switching frequency. A hybrid combination of a FC-SM and one HB-SM [64] creates the SC-FCHBSM (Figure 8g) and demonstrates a method of generating, at least in theory, additional multilevel SMs.

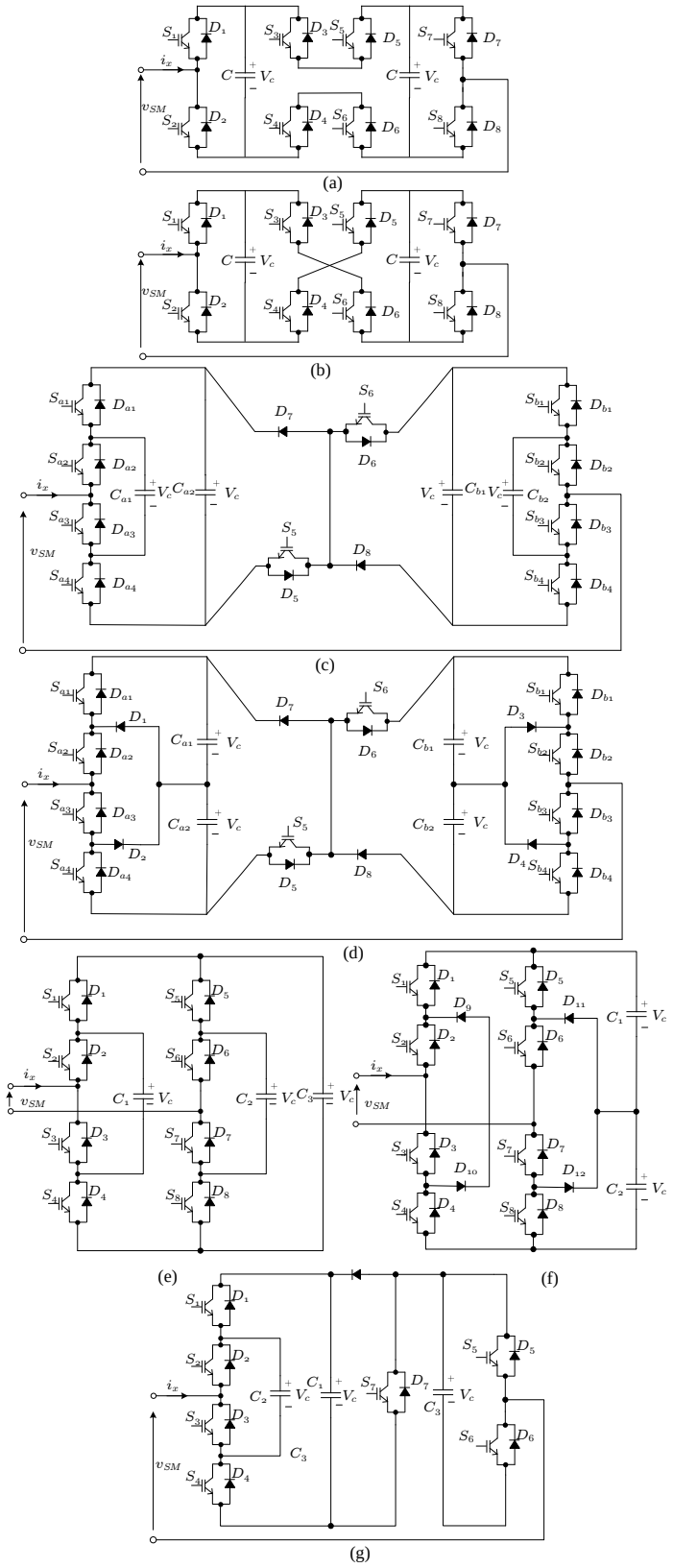


Figure 8. Multilevel SMs: (**a**) Dual FB Parallel-Connected SM; (**b**) Dual FB Cross-Connected SM; (**c**) 5-LCFCSM—Five-level cross-connected flying capacitor SM; (**d**) 5-LCNPCSM—Five-level cross-connected neutral point clamped SM; (**e**) 5-LFCSM—Five-level flying capacitor SM; (**f**) 5-LNPCSM—Five-level neutral point clamped SM; and (**g**) SC-FCHBSM—Series-connected flying capacitor with half-bridge SM.

2.5. SMs with Voltage Balancing Limitations

For the steady operation of the MMC, the capacitor voltage balancing is one of the basic requirements in HVDC applications. Although capacitor voltage balancing is generally considered possible under all operating conditions, this is not always the case for certain SMs. This category includes, most prominently, SMs with neutral-point voltages such as the NPC-SM [31], the T-type SM [65] (both TSM1 and TSM2 [47]) and the ANPC-SM [32]. The main reason for the reduced voltage-balancing capability is the inability to charge or discharge the two capacitors (C_1 and C_2) for the same time under the operation of unity power factor. Another topology with limited voltage balancing capabilities is the DCMSM (Figure 9g), which is a modified version of the NPC-SM to provide dc-fault-blocking capability but again with limited control options over C_1 [66]. The Asymmetrical Mixed SM (AMSM [67]) and the self-blocking composite multilevel SM (CSM-1 [46]) also exhibit similar limitations and will not be further considered in this work.

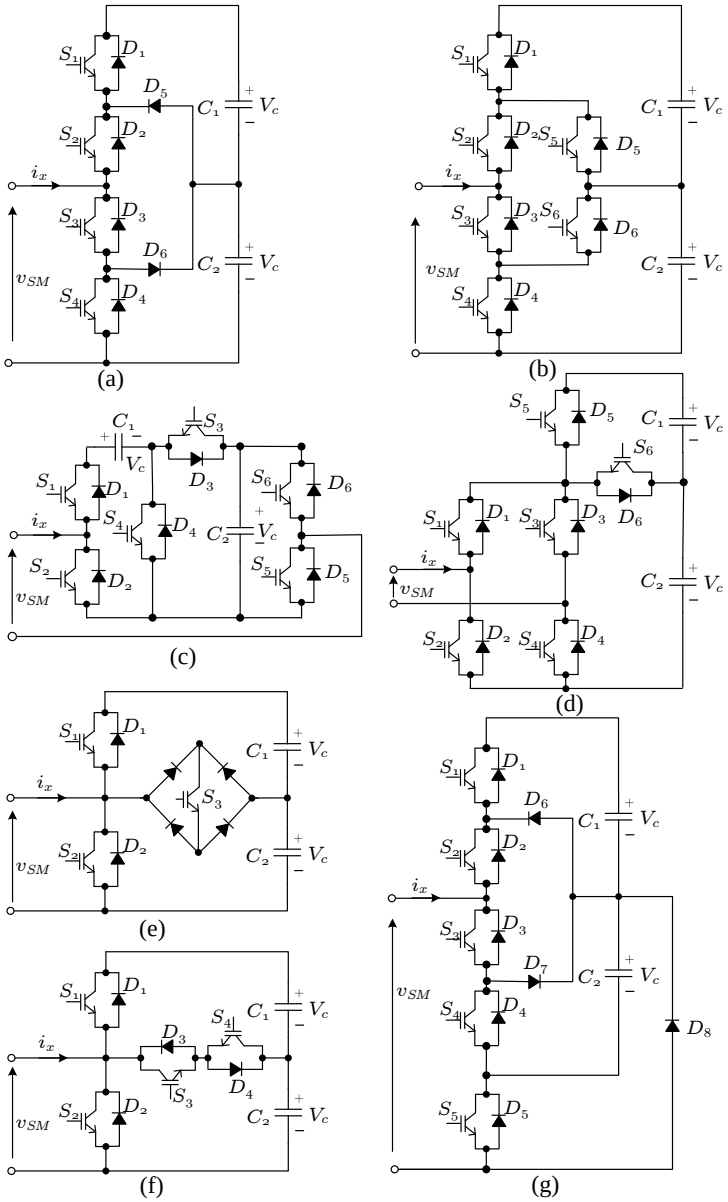


Figure 9. SMs with voltage balancing issues: (**a**) NPC-SM/DC-SM—Neutral point clamped SM/Diode clamped SM; (**b**) ANPC-SM—Active neutral-point clamped unipolar SM; (**c**) CSM-1—Self-blocking composite multilevel SM 1; (**d**) AMSM—Asymmetrical Mixed SM; (**e**) TSM1—T-connected NPC SM 1; (**f**) TSM2—T-connected NPC SM 2; and (**g**) DCMSM—Double clamped diode SM.

2.6. Unidirectional SMs

The assumption that a converter does not need to operate at all four quadrants allows for further simplifications in the SM structure, mainly through the substitution of bidirectional switches with diodes. For example, the unidirectional SM (version 1 and 2 in Figure 10) [68] have a similar topology; both of them substitute one IGBT of the HB-SM with a diode. The same approach is used in the RD-SM, removing all components that are not used in unidirectional current flow [69]. The combined half-bridge full-bridge SM [70] has a diode instead of a switch in the terminal, which is unique and does not exist in any other SMs. As these SMs cannot meet all of the requirements for HVDC applications, they are also not considered in the analysis of the following sections.

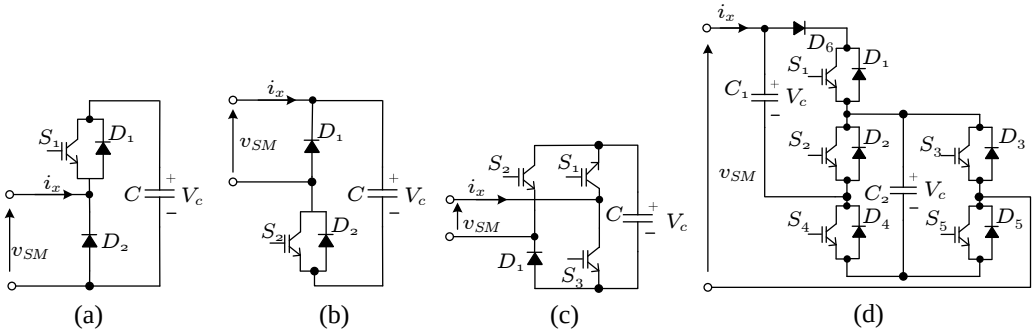


Figure 10. Unidirectional SMs: (**a**) Unidirectional SM1; (**b**) Unidirectional SM2; (**c**) RD-SM—Reduced device SM; and (**d**) CHBFBSM—Combined half-bridge full-bridge SM.

2.7. Other VSC SMs

Some SMs that could not be included in the previous sections are briefly summarised here. The "improved" hybrid SM or IHSM [71] consists of a UFBSM and a HB-SM and can be considered as a reduced functionality Mix-SM with identical switching states and functionality except the reduced control for negative voltage levels. The virtual infinite capacitor (VIC) configuration has been added in an HB-SM as VIC-SM (Figure 11b) to provide adjustable voltage and reduced capacitance [72]. The two switches on the left side work similar to the traditional HB-SM, while the required switching frequency of S_1 and S_2 in the VIC section is much higher than the frequency in HVDC applications. As for the three-level clamp full-bridge SM (TL-CFBSM [73]), two inductors are added in 3L-DSM to protect capacitors from damage due to unequal voltages. However, the switching states and blocking states do not change and can be functionally considered identical.

Ref. [74] introduces the Modified switched capacitor SM (MSCSM) of Figure 11d as a dc-fault-tolerant topology, but the blocking state limits the current flow paths through the SM. Higher voltage levels from a single SM can be generated by the lattice SM (LSM [75]) that can also be viewed as equivalent to four HBSMs connected in series. However, the requirement for six RB-IGBTs and the lack of an easily scalable structure reduces the benefits, considering that a fault-clearing path is also not available.

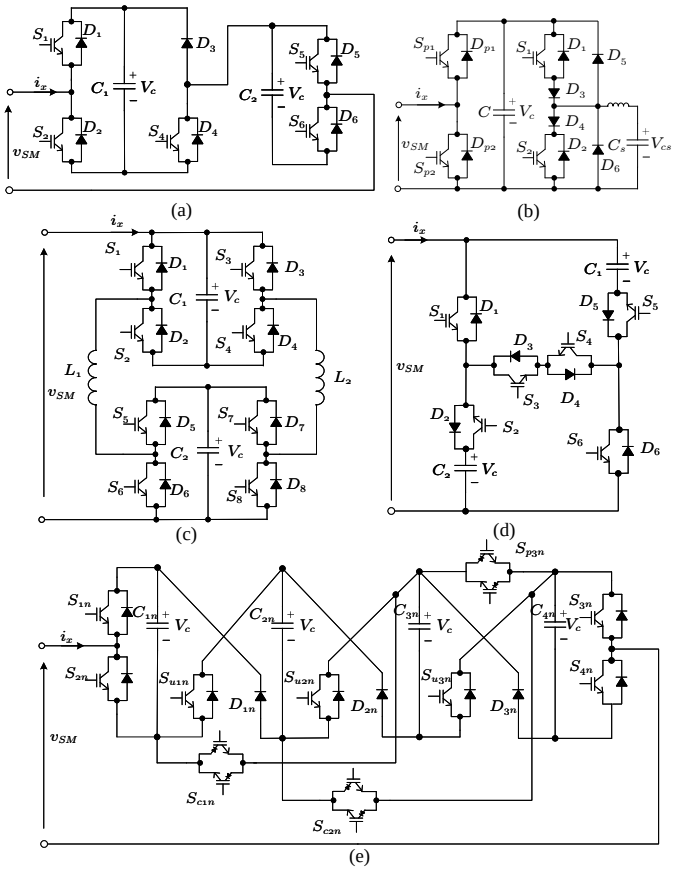


Figure 11. Others: (**a**) IHSM—Improved hybrid SM; (**b**) VIC-SM—Virtual infinite capacitor SM; (**c**) TL-CFBSM—Three-level clamp full-bridge SM; (**d**) MSCSM—Modified switched capacitor SM; and (**e**) LSM—Lattice SM.

2.8. Csc and AC-AC Submodules

For completeness of the review, this section includes VSC-based SMs that have been developed for other applications. The DBSMs of Figure 12a,b are designed as HB-SM alternatives for current-source converters [76], while the Packed U-Cell SM (7L-PUC [77]) uses hybrid voltage levels and unequal device ratings in a structure mostly suitable, but with many design and operation limitations, to ac–ac conversion. These three SMs will also not be further considered for the loss analysis in the rest of this article.

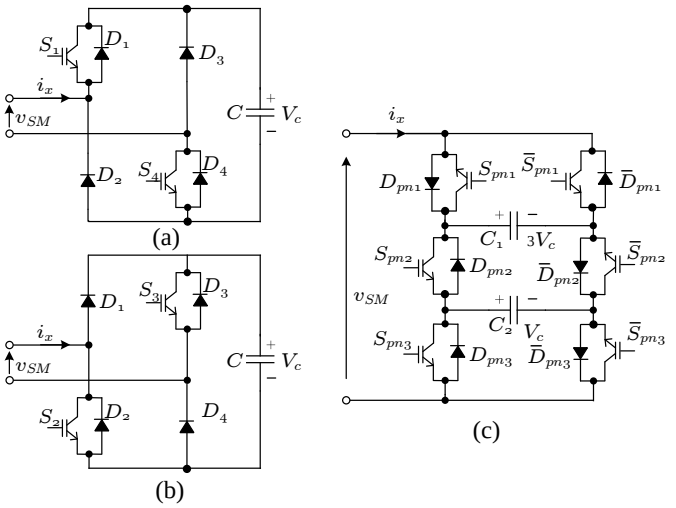


Figure 12. CSC and AC-AC SMs: (**a**) DBSM-1—Diagonal bridge SM 1; (**b**) DBSM-2—Diagonal bridge SM 2; and (**c**) 7L-PUC—7-Level Packed U-Cells.

3. SMs Categorization

Figure 13 shows the evolution of the literature in MMC SMs. It can be seen that the early literature focused on the operation of the MMC using HB-SMs and FB-SMs. The development and proposal of new SM structures since 2012 can also be appreciated.

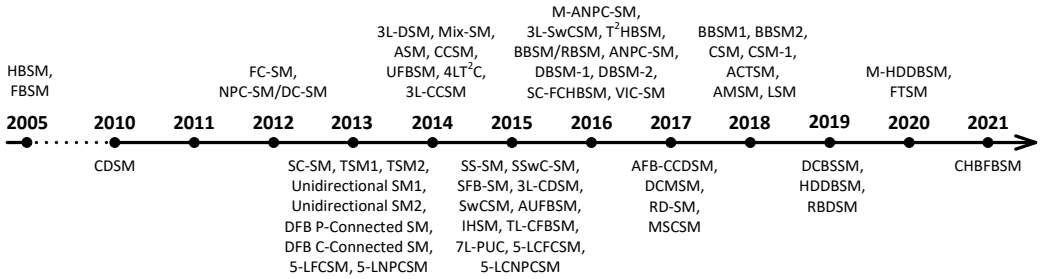


Figure 13. Timeline of SM introduction in the literature.

Although the literature on MMC SMs covers different aspects and introduces many traits of a certain SM structure, the characteristics of a single SM topology are better defined when it is compared directly to other SMs. Therefore, it is necessary to make appropriate categorizations including a variety of SM features, meanwhile, considering the feasibility of SMs in HVDC applications.

Based on the above, and the reasoning provided in each of the categories, the following SM classifications are introduced in this section: (i) output voltage levels, (ii) dc-fault blocking, (iii) negative voltage controllability, (iv) number of components in SMs, and (v) number of capacitors.

3.1. Output Voltage Levels

According to the different SM topologies, the output voltage levels of SMs are not the same. For an MMC with a given dc-link voltage, the difference in the positive output voltage levels per SM results in different numbers of SMs in each arm. All SMs have been categorized based on the number of positive output levels in Figure 14. In summary, we identify 12 two-level SMs and 20 three-level SMs. The SMs are further classified based on their negative output voltage levels. Only two SMs have two distinct negative voltage levels in their output while the rest of the bipolar SMs simply provide one negative voltage level.

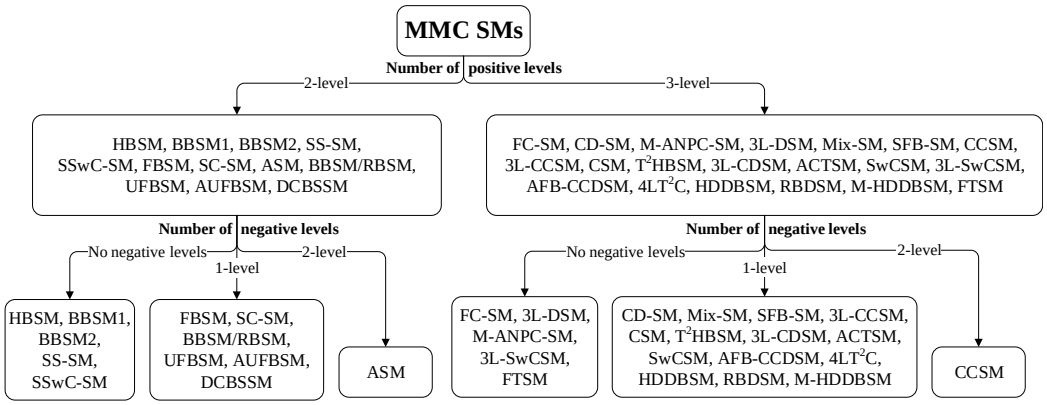


Figure 14. Classification of SMs based on number of positive and negative levels in their output voltage.

The classifications of SMs based on the number of positive levels provides information to define the required number of SMs per arm either considering one SM type or combinations of SM types. Operation of the MMC in the overmodulation region and other modular VSCs, for example, the alternate arm converter (AAC) that operate in overmodulation region under normal operation, require SMs to generate negative voltage levels. This

classification also helps with determining the suitability of different SMs with negative voltage levels for such cases. However, the controllability of negative levels has to be considered and is discussed in following sections.

3.2. DC Fault Blocking

Bipolar SMs have the ability to generate negative voltage levels, providing an effective way to block dc-faults [78]. The lack of dc-fault tolerance of the typical HBSM-based MMC can be overcome by introducing various bipolar SMs that have dc-fault blocking capability within the arms [79]. When the fault occurs and after the blocking of the converter, the IGBTs in SMs are turned off and the capacitors as well as diodes (typically) provide a path to current. Since the current is charging the capacitors, the capacitor of the SMs effectively generates a reverse voltage that blocks the dc-fault current [80].

According to dc-fault blocking capabilities, the 32 SMs are classified into two distinct categories in Table 5. None of the unipolar SMs can block and clear the dc-side faults due to the absence of negative voltage levels. Some SMs have more than one capacitor, but not all capacitors are utilized in the blocking state. The numbers within brackets indicate the number of capacitors in the blocking path and the number of overall capacitors in a single SM.

Table 5. Classification of SMs based on DC fault blocking.

DCFB (#/#) *	**Non-DCFB**
FBSM (1/1)	HBSM
SC-SM (1/2)	FC-SM
CD-SM (2/2)	SS-SM
Mix-SM (1/2)	SSwC-SM
ASM (2/2)	M-ANPC-SM
CCSM (2/2)	3L-DSM
UFBSM (1/1)	BBSM1
3L-CCSM (2/2)	BBSM2
CSM (1/2)	3L-SwCSM
SFB-SM (2/2)	FTSM
BBSM/RBSM (1/2)	
T^2HBSM (1/2)	
ACTSM (2/2)	
3L-CDSM (2/2)	
SwCSM (1/2)	
AUFBSM (1/2)	
AFB-CCDSM (2/4)	
4LT^2C (1/2)	
DCBSSM (1/1)	
HDDBSM (1/2)	
RBDSM (1/2)	
M-HDDBSM (2/4)	

* (# Capacitors in blocking path/# Total capacitors).

If the blocking voltage provided by the series-connected SM capacitors is above the ac peak voltage, dc-faults can be fully blocked. Therefore, the required number of dc-fault blocking SMs, depending on the intended level of dc-fault tolerance in each arm, can be determined based on the information of Table 5. Moreover, depending on the number of capacitors of each SM that contribute to block dc-faults, the SMs can be combined in hybrid MMC configurations using combinations of unipolar and bipolar SMs.

3.3. Negative Voltage Controllability

The maximum number of negative voltage levels generated by bipolar SMs is defined by the number of capacitors that can be connected in series in each SM. However, not all negative levels of a bipolar SM may be controllable. The definition of "negative voltage

level controllability" of a bipolar SM can be expressed as the ability to generate each possible negative voltage level at the output while allowing bidirectional current flow without having to change the switching state of the SM under normal operation.

Based on the previous definition, Table 6 provides a categorization of bipolar SMs on account of their negative voltage controllability. The SMs in the controllable category can all produce negative output levels regardless of the direction of the current; noncontrollable SMs produce negative voltages during the blocking state and for negative arm current direction. Therefore, noncontrollable SMs cannot be utilized under normal operation for applications that require negative voltage levels. Negative voltage controllability should be considered together with the number of negative voltage levels in order to appropriately select SMs for modular VSC topologies depending on different applications (e.g., dc-fault tolerant operation, motor drives etc).

Table 6. Classification of SMs based on negative voltage controllability.

Controllable (#/#) *	Non-Controllable (#/#) *
FB-SM (1/1)	SC-SM (0/1)
Mix-SM (1/1)	CD-SM (0/1)
ASM (2/2)	UFBSM (0/1)
CCSM (2/2)	3L-CCSM (0/1)
SFB-SM (1/1)	CSM (0/1)
AFB-CCDSM (1/1)	BBSM/RBSM (0/1)
4LT^{2}C (1/1)	T^{2}HBSM (0/1)
	ACTSM (0/1)
	3L-CDSM (0/1)
	SwCSM (0/1)
	AUFBSM (0/1)
	DCBSSM (0/1)
	RBDSM (0/1)
	HDDBSM (0/1)
	M-HDDBSM (0/1)

* (# Controllable negative levels/# Total negative levels).

3.4. SM Component Count

The types and number of components in SMs define the complexity of SM structure. Moreover, the amount of components and voltage ratings concerning the number of voltage levels provides an overview of losses, efficiency, converter footprint, and cost. Table 7 categorizes the SMs based on number of output levels and lists the number of switches (IGBT modules), discrete diodes and capacitors that are used in each SM.

Some SMs contain switches with different voltage ratings which reduces their modular nature (these SMs are marked with a '*' in Table 7). The number of switches are stated regardless of their voltage rating. Hence in practice, the equivalent number of switches that has a similar voltage rating can be more than the stated number in marked ('*') SMs of Table 7. An equivalent analysis for the SMs can also be performed based on either their total blocking voltage (TBV) or total semiconductor area (TSA) used in each SM and in the total arm of the MMC, however, such analysis is not considered within the scope of this work.

Table 7. Number of components in SMs.

Level	SM	Switch	Discrete Diode	Capacitor
2-level	HBSM	2	0	1
	BBSM1	2	4	1
	BBSM2	3	0	1
	SS-SM	3	0	1
	SSwC-SM *	6	0	3
	FB-SM	4	0	1
	ASM *	4	0	2
	SC-SM *	3	1	2
	UFBSM	3	1	1
	BBSM/RBSM	3	1	2
	AUFBSM *	3	1	2
	DCBSSM	3	6	1
3-level	FC-SM	4	0	3
	CD-SM	5	2	2
	M-ANPC-SM	6	0	2
	3L-DSM	8	0	2
	Mix-SM	6	0	2
	CCSM *	6	0	2
	SFB-SM	7	0	2
	CSM *	6	1	2
	3L-CCSM *	5	1	2
	T^2HBSM	5	1	2
	3L-CDSM	6	2	2
	ACTSM	6	2	2
	SwCSM	6	1	2
	3L-SwCSM	5	0	2
	AFB-CCDSM	6	0	4
	4LT^2C	6	0	2
	HDDBSM	5	1	2
	RBDSM	5	1	2
	M-HDDBSM	6	2	4
	FTSM *	6	0	2

* SMs that have switches with unequal voltage ratings.

3.5. Number of Capacitors

The number of capacitors in each SM is a primary defining factor for the dimensions of SMs, as the capacitors occupy the majority of size and weight in an SM. It also reflects the internal capacitor voltage balancing characteristics and requirements. Table 8 shows the number of capacitors in each SM. Considering the same number of voltage levels, the size of a SM become larger as the number of capacitors increase, as an example, SSwC-SM has the highest number of switches and capacitors among the 2-level SMs which can lead to a significantly larger converter footprint.

Remark: In this analysis, "capacitors" refer to a capacitor stack in a given SM which maybe be assembled from multiple individual capacitors in order to meet the capacitance and voltage requirements.

SMs with larger number of capacitors introduce further challenges as internal voltage balancing may be required among the capacitors within the SM in addition to the overall arm energy control. When there are multiple states generating the same voltage level, dedicated internal capacitor voltage-balancing techniques are required for appropriate selection of the states to maintain the internal voltage balance. Capacitor voltage balancing becomes further challenging when the SM has a more asymmetrical structure due to uneven current flows and conduction duration for each of the SM capacitors.

Table 8. Classification of SMs based on Number of Capacitors in SMs.

Number	SMs
1	HBSM, SS-SM, BBSM1, BBSM2 FB-SM, UFBSM, DCBSSM
2	M-ANPC-SM, 3L-DSM, 3L-SwCSM, SC-SM, CD-SM, Mix-SM, ASM, CCSM, 3L-CCSM, CSM, SFB-SM, BBSM/RBSM, T^2HBSM, ACTSM, 3L-CDSM, SwCSM, AUFBSM, 4LT^2C, HDDBSM, FTSM
3	FC-SM, SSwC-SM, RBDSM
4	AFB-CCDSM, M-HDDBSM

4. HVDC System Description and SM Modeling

Detailed loss evaluation of all HVDC suitable SMs is performed based on an 800 MVA, ±200 kV MMC-HVDC system. The base model is developed using 400 HB-SMs in each arm; equivalent numbers that yield identical performance are considered for the multilevel SMs. The MMC arms are simulated using an hybrid switching/average model where 8 HBSMs (or equivalent) in each arm are modeled using a detailed switching model and the other SMs are included in a detailed equivalent average model. Such a hybrid approach (shown in Figure 15) provides a computationally efficient representation for the converter so that control levels consisting of a sorting algorithm and capacitor voltage balancing can be implemented. The nominal voltage of SM capacitor is selected equal to 1 kV, the switching and thermal models are implemented based on the Infineon FZ1500R33HL3 IGBT due its use in HVDC projects [81] with a capacitance of 20mF per HBSM, which corresponds to stored energy of 30kJ/MVA. At the same time, as the focus of the article is on SM performance, losses of the arm inductors and the capacitors [82] have not been included. All model parameters are given in Table 9.

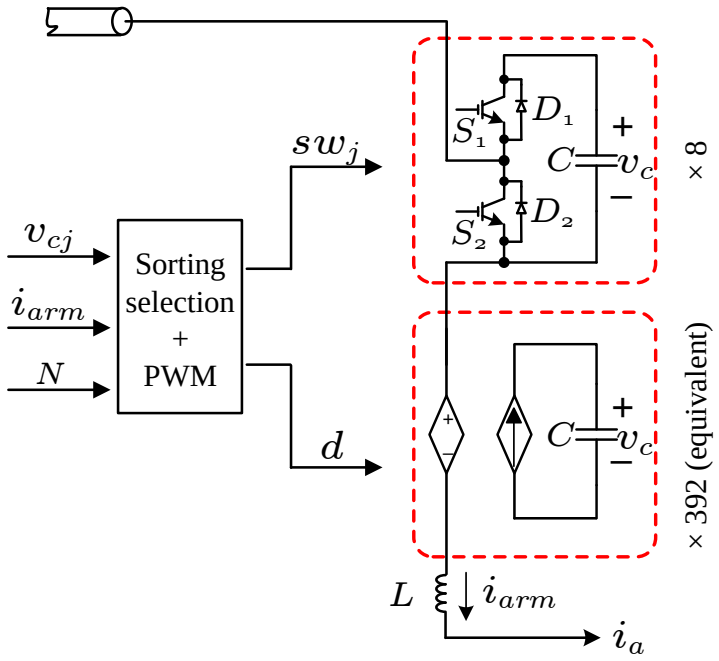


Figure 15. A hybrid approach of modeling an MMC arm by the combination of average and switching models.

Table 9. Parameters of the MMC-HVDC model.

Parameters	Value
Rated Power (MVA)	800
DC-Voltage (kV)	±200
Number of SMs per arm	400
SM Voltage (kV)	1
Stored Energy (kJ/MVA)	30
SM Capacitance (mF)	20
AC-Grid Voltage (kV)	380
Arm Inductance (p.u.)	0.15
Nominal Frequency (Hz)	50
Nominal Operating Point (p.u.)	0.9
T/F Resistance (p.u.)	0.006
T/F Leakage Inductance (p.u.)	0.18
Transformer Ratio	0.997
Short-circuit Power (GVA)	30
R/X Ratio	0.1

As shown in Figure 16, an isotherm environment in the thermal model is offered by a "virtual heat sink", which covers the diodes and IGBTs of each SM. Moreover, the thermal capacitor and resistor are also included in the model and is defined as the thermal chain. The total power losses are divided into switching losses and conduction losses, which are calculated separately and summed up further.

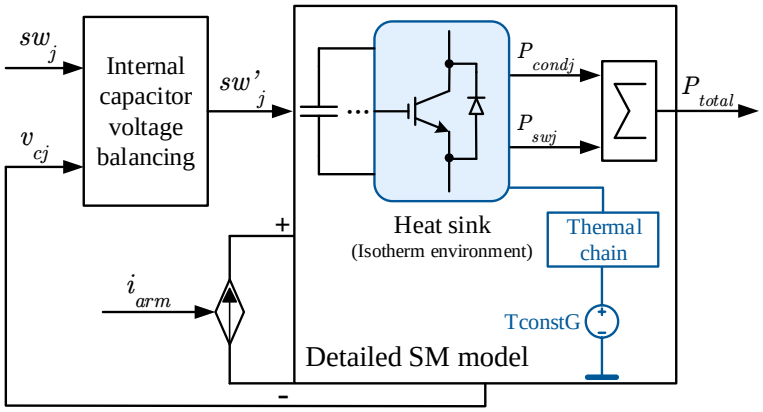


Figure 16. Thermal model of the IGBT module.

Since the system configuration is common across all cases, representative results for inverter operation under 1.0 p.u. power transfer are provided in Figure 17. The large number of the multilevel output voltage leads to low distortion and the output currents are sinusoidal (Figure 17b).The different levels of controllers that regulate the circulating current and balance the voltage of the SM capacitor eliminate the influence of higher order harmonics in the MMC arm currents (Figure 17c) and the average SM capacitor voltages (Figure 17d).

The implementation of switching SM models together with a restricted sorting algorithm [83] provides detailed voltages for the SMs, as shown for four different SMs in Figure 18 as well as an indication of internal voltage balancing in each SM. Here, the HBSM, CSM and ACTSM demonstrate appropriate voltage balancing, although the structure of the ACTSM limits its voltage-balancing capacity and leads to greater capacitor voltage ripple (Figure 18c). At the same time, the NPC-SM does not have voltage balancing capability at unity power factor leading to SM capacitor voltage deviations, as shown in Figure 18d. As explained in Section 2.5, such SMs have been excluded from further analysis. The voltage-balancing capabilities of all SMs have been verified with similar results generated; these have not been included here due to space limitations.

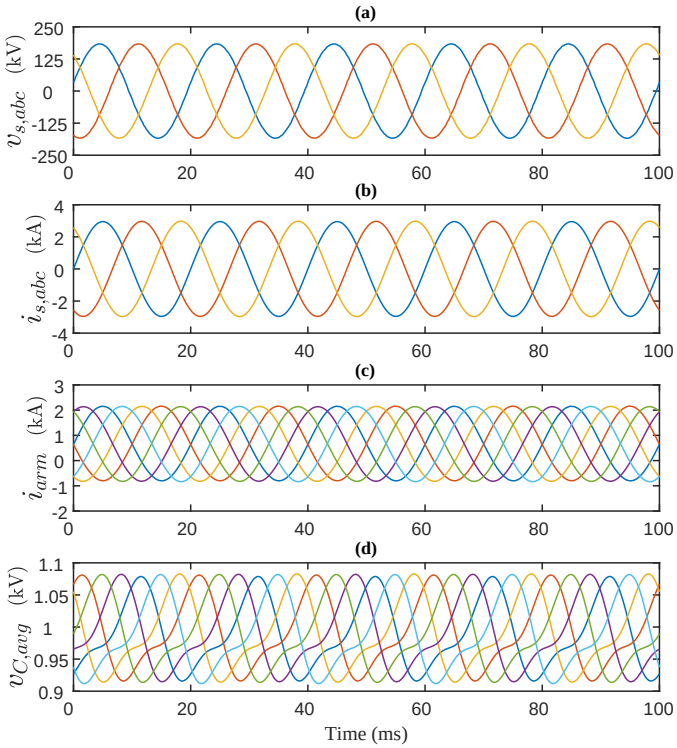


Figure 17. Steady–state waveforms of voltage and current in the MMC–HVDC system: (**a**) voltages in the output terminal ($v_{s,abc}$), (**b**) currents in the output terminal ($i_{s,abc}$), (**c**) arm currents of the MMC (i_{arm}), and (**d**) average voltages of SM capacitors ($v_{C,avg}$).

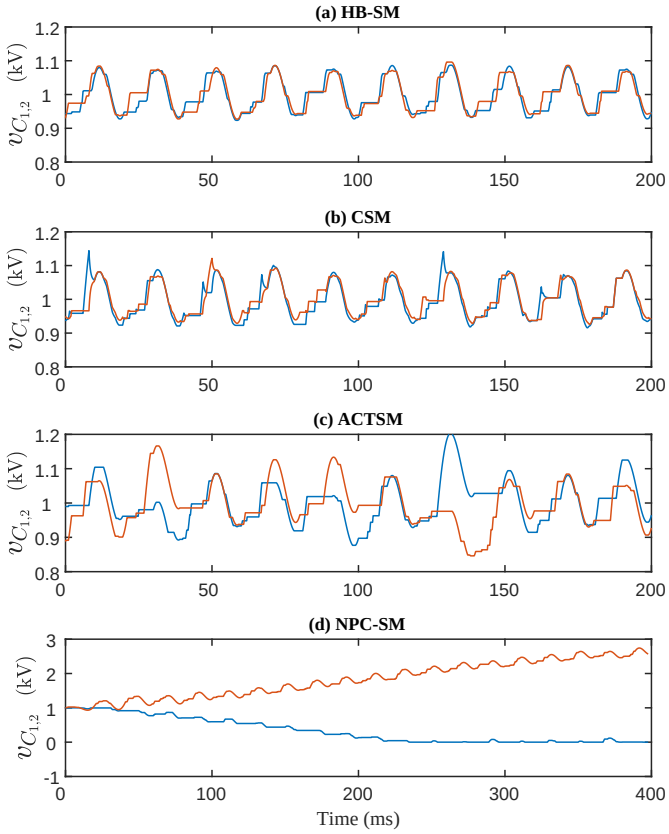


Figure 18. Capacitor voltages of selected SMs: (**a**) HB–SM, (**b**) CSM, (**c**) ACTSM, and (**d**) NPC–SM.

5. Results and Comparison

5.1. Calculation of SM Average Losses

Loss comparisons for MMC SMs typically consider average calculations of the switching and conduction losses as well as a combined loss value based on different operating points for the converter. The average loss calculations for the selected 29 SMs are shown in Figure 19 with the converter operating under inverter mode at full power and at a unity power factor. The losses have been normalised to the average losses of the HB-SM to allow for easier comparison between the different topologies, always accounting for the output voltage levels (i.e., comparing one three-level SM against two two-level SMs).

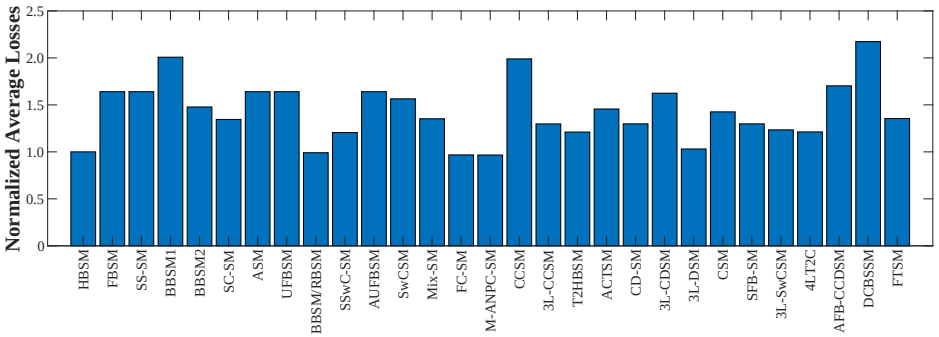


Figure 19. Average loss of SMs at unity power factor.

From Figure 19 we can derive some general conclusions about losses in SMs. The SMs with the lowest average losses (the M-ANPC-SM) takes advantage of the current sharing [32] in its inner devices (S_2, S_3, S_5 and S_6) at zero voltage level. However, minor differences between these devices (e.g., due to aging) can lead to unequal thermal loading, requiring additional monitoring of the SMs. Other configurations with low losses are the HBSM, as expected based on the analysis of [84], the FCSM albeit with a higher capacitor voltage ripple and the BBSM/RBSM.

On the other hand, complex structures that provide additional functionalities and require additional devices will naturally lead to higher losses. The DCBSSM and the BBSM1 have the highest average losses (double the losses of the HBSM) with a number of SMs generating 1.2 to 1.3 times the losses of the simpler structures (e.g., FBSM, SS-SM, ASM, UFBSM etc) for the same output voltage level.

A qualitative comparison of 5 SMs is illustrated in Figure 20, which is based on the number of output levels, the number of devices, efficiency, and dc-fault-blocking capability. The HB-SM and FB-SM are two conventional SMs, the M-ANPC-SM and CCSM represent SMs with relative low and high losses, respectively, while the CDSM is included as a bipolar SM with more functionalities and relatively high efficiency. According to the classifications and results provided in Sections 3 and 5, and based on the requirements of a given application, similar comparisons can be performed among two or more suitable SMs.

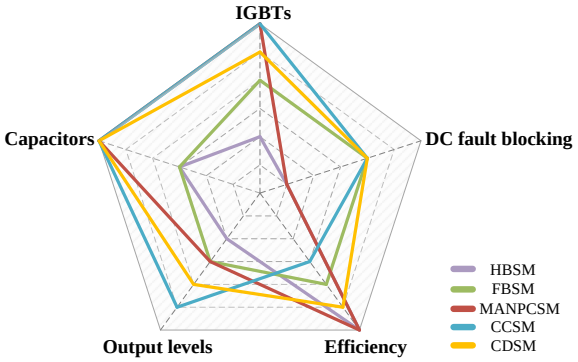


Figure 20. Qualitative comparison of selected submodules for the Modular Multilevel Converter.

5.2. Impact of Voltage Balancing

Although average losses provide a general indication of SM performance, they fail to explain the influence of the voltage-balancing algorithm that selects the switching instants of an SM based on the voltages of all other SMs within the arm. This means that losses (both conduction and switching) between consecutive periods are not generally equal due to (i) different conduction periods, (ii) different values for the arm current at the switching instances, (iii) variation in the SM capacitor voltage and (iv) for multilevel SMs, selection of different redundant states for voltage-balancing purposes.

Considering the above, it becomes apparent that a statistical approach to SM losses will provide further insights into the operation of each SM. Considering steady-state inverter operation at unity power factor, an analysis of SM losses over 1000 consecutive periods is provided in Figure 21. By considering not only the average or median value of the SM losses but also their distribution, we can reach additional conclusions:

- The losses of one period can vary up to 20% below or above the average loss. As explained above, this results from the implementation of the SM capacitor voltage-balancing algorithm directly and is observed across all SMs;
- Certain SMs (i.e., CCSM, AFB-CCDSM) exhibit even higher variation, up to 40% as certain transitions between redundant states require multiple devices to change their switching state;
- A tighter box, which illustrates a tighter interquartile range of the losses, is more common in SMs with fewer redundant states where the variation in the losses is mostly attributed to current and timing variations;
- Multiple redundant states lead to outliers in the losses. These outliers can be above the typical maximum (e.g., AFB-CCDSM) demonstrating excessive losses for multiple periods, or below the minimum (e.g., M-ANPC-SM, FC-SM) demonstrating lower losses for certain periods. Both of these instances of outliers can impact the thermal design of the SM;
- Excessive losses without substantial benefits in the operation or functionalities of the MMC effectively limit the SMs that can be considered as feasible topologies for practical implementations.

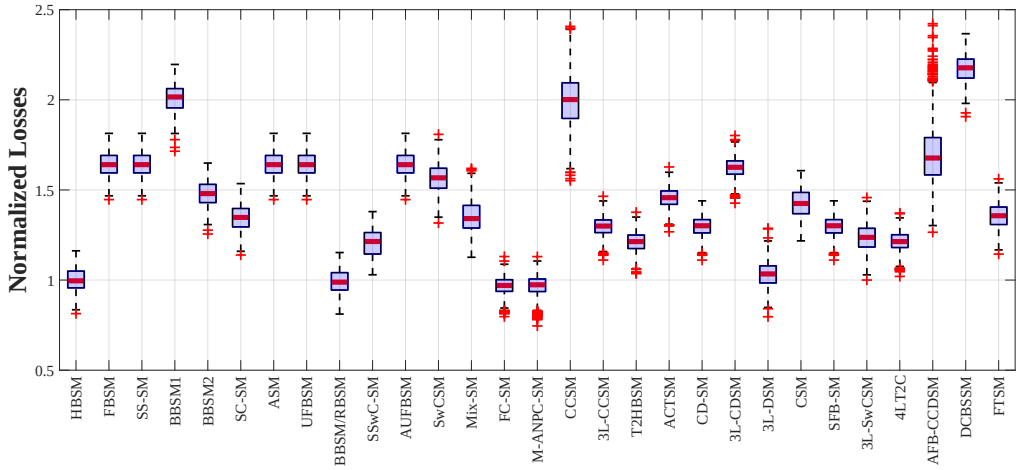


Figure 21. Losses of SMs over 1000 consecutive periods at unity power factor (inverter).

In the case of the converter operating in rectifier mode, a similar analysis for SM losses is shown in Figure 22. The different conduction paths within the SMs of the MMC tend to increase the losses compared to the HBSM for most configurations. However, SMs such as the M-ANPC-SM and the FC-SM can exhibit losses up to 10% lower than the HBSM which can be important in applications where converter efficiency is critical. Further to that, the losses of certain SMs increase substantially compared to their inverter operation

(e.g., BBSM1 10% higher) and a comprehensive loss study is necessary to identify worst case operation for each SM.

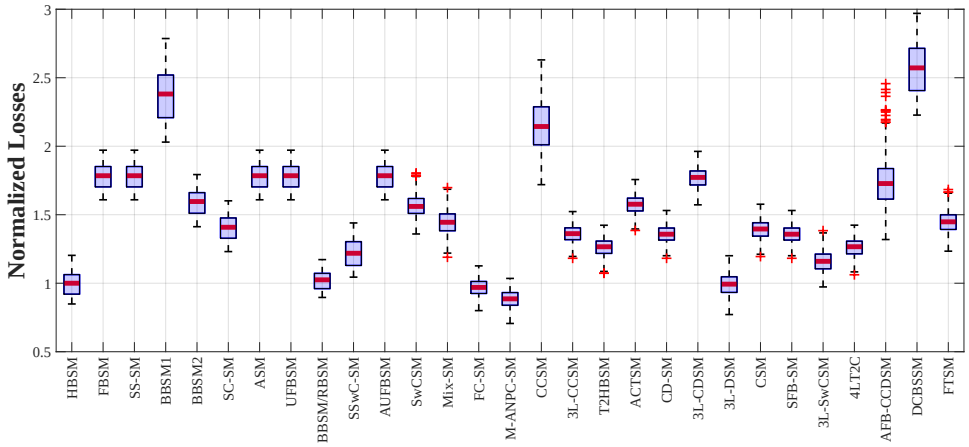
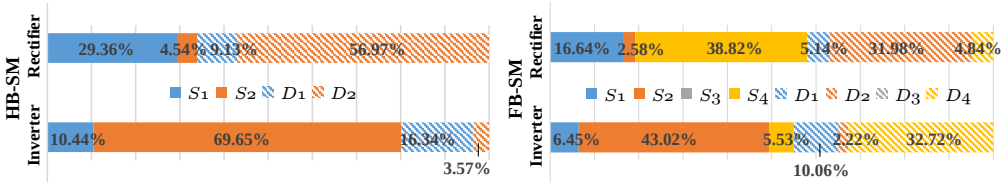


Figure 22. Losses of SMs over 1000 consecutive periods at unity power factor (rectifier).

5.3. Device Loss Distribution

Development of the hybrid simulation model for multiple SMs allows for further analysis and insights in the stress of individual devices within the SMs as each device (IGBT and diode) is modeled independently and the proportion of losses that corresponds to each device can be directly evaluated. This analysis has been performed for all 29 SMs and selected results are provided in this section as illustrative cases for loss distribution in inverter and rectifier operation of the MMC.

As shown in Figure 23a, the losses of the HB-SM are mostly on S_2 when the converter operates under inverter mode and on both S_1 and D_2 during rectifier operation. These results are similar to previous analysis in the literature with variations caused by the choice of device, switching frequency and the selected current control method. Similarly, the losses of the FB-SM (shown in Figure 23b) are mostly defined by the Pulse-Width Modulation (PWM) implementation and whether the second leg in the bridge is used or one device is always conducting. Again, the major losses in inverter mode occur on S_2, while D_4 is the diode that continuously conducts the arm current, while in rectifier mode, the losses of D_2 and S_1 increase, while S_4 which is constantly conducting is the component with the highest loss percentage. As S_3 is not used, there are no losses and this choice of modulation scheme can substantially impact the thermal balancing and the design of the active cooling and heat-sink in the SM.



(**a**) (**b**)

Figure 23. Loss distribution amongst SM devices: (**a**) HBSM and (**b**) FB-SM.

Considering the SMs with the lowest and highest losses, the loss distribution of different devices is illustrated in Figure 24. Based on the switching states of each SM, the distribution of losses in the devices remains relatively similar; however, multilevel states for the FC-SM and the sharing of the current in the M-ANPC-SM lead to lower losses, compared to the additional devices in the current path (due to the bidirectional switch also used in BBSM2) during the normal operation of a BBSM1 MMC converter which increases losses and required additional thermal management for the converter.

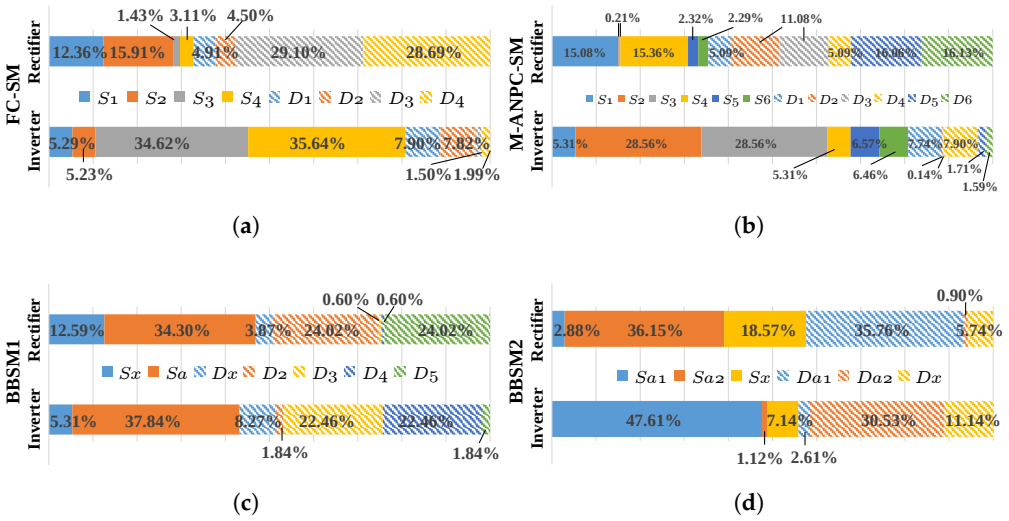


Figure 24. Loss distribution amongst SM devices: (**a**) FCSM, (**b**) M-ANPC-SM, (**c**) BBSM1, and (**d**) BBSM2.

Some other examples of loss distribution in SMs are provided in Figure 25 as indicative of the operation of the SMs. These include the BBSM/RBSM as a two-level bipolar SM with no controllable dc fault blocking state (Figure 25a), the CCSM and CD-SM as multilevel SMs with controllable and non-controllable dc fault blocking states (Figure 25b,c, respectively) and the ASM/UFBSM as examples of SMs with reduced components either due to the asymmetric structure or due to the simplification in the switching states as a result of substituting fully controllable devices with diodes.

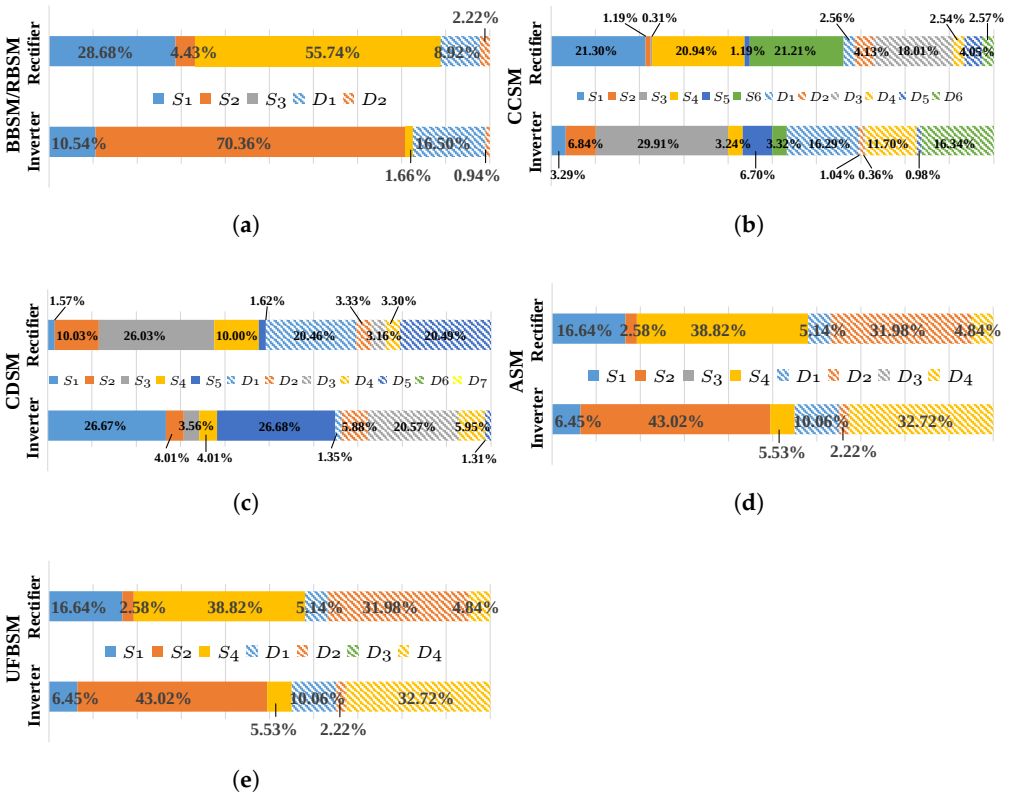


Figure 25. Loss distribution amongst SM devices: (**a**) BBSM/RBSM, (**b**) CCSM, (**c**) CDSM, (**d**) ASM, and (**e**) UFBSM.

It is generally observed that (i) the distribution of losses depends on the operation mode of the converter and the current flows in the SMs (e.g., S_2 for the BBSM and UFBSM in inverter operation and S_4 in rectifier operation), (ii) additional losses are generally attributed to devices that add to converter functionalities, (iii) substitution of switches with diodes in fault-tolerant topologies does not necessarily lead to improvement in the converter efficiency and system losses as these devices are generally not conducting in normal converter operation and (iv) active thermal management can be quite challenging when low switching frequencies in the SMs are considered.

6. Challenges and Future Opportunities

Despite the large volume of literature on SM configurations, there are many areas that require further development and challenges that need to be addressed. These create multiple opportunities for new SM designs and combinations of SMs, allowing for an even broader adoption of the MMC in power conversion applications. Specifically:

- *Power/Voltage Ratings:* Early designs of HVDC systems based on the MMC were commonly rated below 1 GW with voltage ratings around 1 kV per SM. As transmission capacity over HVDC corridors is increasing, power ratings have increased with an accompanying increase in SM voltage ratings (i.e., using 4.5 kV [85] or 6.5 kV IGBTs [86]). This design approach allows for higher dc voltages without increasing the number of SMs and the associated increase in control complexity or a reduction in the number of SMs leading to fewer dc-link capacitors, higher efficiency and improved reliability of the converter [87]. Such designs also consider compromises between fewer SMs and greater requirements of redundancy and potentially lower quality of the harmonic performance [88]. With higher rating devices, combinations of different SMs and development of hybrid MMC converters that combine two or more of the many SMs reviewed earlier [89] also become valid approaches to MMC design. Another solution to achieve even higher power capability is the parallel connection of SMs which should consider uneven current sharing and optimization of the capacitor voltage balancing capability. Such options open new directions for design of SMs, aiming towards greater MMC ratings.
- *New Applications:* The SM-based structure of the MMC makes it well-suited to HVDC power transmission as it elegantly addresses voltage sharing between devices connected in series and is the primary reason for the growth in MMC-based HVDC applications. With the structure and operation of the converter being better understood, its fitness to lower voltage and lower power applications can be re-evaluated. Such applications include converters for medium voltage dc (MVDC) systems for renewable and grid-connected applications [90], medium voltage motor drives, as well as transportation electrification (e.g., railway traction power supplies [14], battery chargers [91], marine vessels [92], etc.). The review and comparison we have presented in this article focuses on HVDC application to set the key requirements for the operation of the converter and SM specifications. As these new applications have different operating requirements and power/voltage design envelopes, further evaluation based on the principles introduced in this article would be required.
- *DC Circuit Breakers:* With the development of larger multiterminal dc systems (MTDCs) and dc grids, the design and utilization of DCCB becomes a key requirement [93]. Some of the recently proposed DCCB designs move away from the original hybrid DCCB, which was built as a combination of mechanical circuit breaker and solid-state circuit breaker [94], and towards an SM-based design which enables a reduced number of IGBTs, simpler voltage balancing and lower power losses in circuit breaker [95]. These designs can shorten the charging time of the capacitor and provide an extended period for the system to deal with faults [96]. Typical SM-based designs mostly utilise FBSMs but it has been shown that asymmetric SM structures can reduce the influence of electrical stress, reduced loop stray inductance can prevent the sharp voltage increase across IGBTs [97] or transition between current-limiting and the

normal operation modes quickly [98]. Use of alternative SM configurations in DCCB applications is still limited and newer designs may further improve the operation while reducing the cost of DCCB solutions.

- *DC–DC Conversion:* Dc–dc converters for high-power applications are lagging in terms of development and industrial application. Modular solutions based on the MMC are a promising path forward and one where the design of SMs can have a major impact in terms of efficiency, power rating and voltage levels. A critical element in dc–dc conversion is the location of the (typically medium- or high-frequency) transformer, which can be inserted either between two converters or between each basic cells in the two sides [99]. Here, if the two sides of the dc–dc converter are connected via a single transformer, the SMs are required to withstand high current stress, which can be accomplished by high power devices. On the other hand, individual transformer is used to connect each SM to a DAB module, leading to increased system complexity and cost. Options for SM designs can consider either approach as well as one or more of the many SMs summarised in this article for developing modular dc–dc solutions suitable to different power applications.
- *New Converter Designs:* The introduction of the MMC has sparked new research in topologies that take advantage of modular converter structures and has led to the proposal and development of multiple new converter designs [100]. For some of these converters, common SM configurations offer optimal performance; for instance in the alternate arm converter (AAC), the presence of director switches in the arms, means that the most suitable SM in AAC is the standard FB-SM [28]. However, the fitness of the many SMs reviewed in this article to new converter designs is an open area in the current literature.
- *New Semiconductor Devices:* Perhaps the most important development that can lead to the development of new SM configurations for MMCs and all other modular converters and applications is the introduction of new wide band-gap semiconductor devices and specifically high-power silicon carbide (*SiC*) devices [101]. Compared with conventional silicon (*Si*) devices, *SiC* semiconductor devices can operate with higher operating temperature, higher switching frequency [102], higher blocking voltage, while lower switching losses [103]. Possible options in SM designs include: (i) New SMs, such as the introduction of an SiC-FET in series with the SM capacitor to limit the internal fault currents and reduce the power losses [104] due the short-circuit withstand capability of SiC MOSFETs, (ii) Hybrid SMs that combine *Si* with *SiC* devices, or (iii) optimisation of current SM configurations based on SiC devices.

7. Conclusions

The popularity and commercial success of the modular multilevel converter and its flexible circuit topology using submodule (SM) structures has led to a substantial increase in the number of circuit topologies that have been proposed for use in the converter. This paper provides a comprehensive review as well as multiple classifications of available SMs based on their output voltage levels and multiple elements of functionality they provide to the MMC. By providing a detailed review of the literature, readers can evaluate available options for MMC submodules, avoid duplication of topologies and also demonstrate the range of available topologies that can be used in modular and multilevel topologies other than the MMC.

As MMCs are commonly used in high-power HVDC conversion, the article focuses on the performance of those SMs fitting to HVDC systems, excluding SMs that do not fit the requirements of full four-quadrant operation or complete voltage balancing across all operating points. The work in this article also quantifies and compares suitable SMs based on conversion losses. The work then provides, for the first time, an analysis of the sorting algorithm impact to the losses in each SM and also to loss distribution for inverter and rectifier operation. Here we demonstrate that the losses over a single period of operation can deviate by more than 30% in SMs with large number of devices and multiple capacitors

that require voltage balancing, while simpler structures tend to exhibit smaller overall loss deviations (≈10%).

The results identify different low-loss options for SM topologies, both with unipolar and bipolar voltage outputs which can lead to new approaches in the design of MMCs. The large number of SMs and a better understanding of their functions and how different SMs can work together within an MMC arm open up opportunities for future work on the topology including MMC arm hybridisation and pathways for implementing and optimising MMCs in other (i.e., non-HVDC) applications.

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Abbreviations

The following abbreviations are used in this manuscript:

d	Duty cycle
i_l	Current of lower arm
i_u	Current of upper arm
i_x	SM current
i_{arm}	Arm current
i_{circ}	Circulating current
i_{dc}	DC current
$i_{s,abc}$	Output phase currents
L	Inductor
N	Number of SMs per arm
P_{condj}	Conduction power losses
P_{swj}	Switching power losses
P_{total}	Total power losses
S	Switching device
s_{wj}	Switching signal
V_C	Capacitor voltage
v_l	Voltage of lower arm
v_u	Voltage of upper arm
v_{arm}	Arm voltage
$v_{C,avg}$	Average voltages of SM capacitor
v_{cj}	Voltages of SM capacitor
v_{dc}	DC voltage
V_{out}	Output voltage of SM
$v_{s,abc}$	Output phase voltages
v_{SM}	SM voltage
V_{Sn}	Voltage of switching device

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