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Reducing Circling Currents in a VHF Class Φ_2 Inverter Based on a Fully Analytical Loss Model

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Abstract: This paper proposes a fully analytical loss model to reduce circling currents and improve the power efficiency of a class Φ_2 inverter. Firstly, analytical expression of the switching node voltage is derived by analyzing its harmonic components. Based on the result, the power switch is modeled as a voltage source, where the circuit is simplified to a linear network and analytical expressions of branch currents are solved. Secondly, root mean square (RMS) values of branch currents and component losses are calculated to form the analytical loss model for a Φ_2 inverter. The influence of circuit parameters on the circling current and power efficiency are thoroughly analyzed, which derives optimal design constraints to reduce circling currents of a class Φ_2 inverter. Furthermore, detailed design guidance and equations are provided to calculate circuit parameters of a class Φ_2 inverter, which reduces its circling currents and improves overall power efficiency. Finally, a class Φ_2 inverter prototype is built, and experimental results demonstrate a 7% efficiency improvement compared to conventional empirical design methods.



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1. Introduction

Increasing the operation frequency can reduce the values of inductors and capacitors while maintaining the same voltage and current waveforms. Thus, the energy storage and volume of passive components (inductors and capacitors) are reduced, which provides great potential for a high power density and a fast dynamic response [1–4]. However, the switching losses increase greatly with the increase of switching frequency, which degrades the overall power efficiency. To maintain a high efficiency while increasing the operating frequency, it is essential to realize zero-voltage-switching (ZVS) and zero-current-switching (ZCS) for VHF power systems [5–7]. Owing to the easy realization of ZVS, low switch voltage stress and ground-referenced switch, class Φ_2 topology is widely used not only in DC–DC converters [8–11] and wireless power transfer systems [12–15], but also as power amplifiers in plasma generation [16,17] and medical imaging [18].

The topology of a class Φ_2 inverter is shown in Figure 1, which consists of a resonant tank, a power switch and an output network. Compared to class E topology, the class Φ_2 inverter adds a second harmonic resonant branch across the power switch, i.e., L_M – C_M in Figure 1. By absorbing the second harmonic voltage, the class Φ_2 inverter significantly reduces the switch voltage stress from $3.6\text{--}4\ v_{in}$ to $2\text{--}2.4\ v_{in}$. Parameters of the resonant tank directly affect the inverter performance, such as power efficiency and switch voltage stress. To improve its performance, extensive research has been carried out on the modeling and design of VHF class Φ_2 inverters [19–22]. The conventional empirical design method usually chooses the value of the resonant capacitor C_F based on the designers' experience [23], and values of other parameters are roughly calculated according to pole

and zero positions of the resonant tank. Then, further iterative simulations are required to improve the circuit performance. The conventional empirical design method highly relies on experience, and improper selections for C_F would result in high voltage stress or low power efficiency. The parameter scanning method can reduce power switch voltage with massive computer aided simulations [24]. However, circling losses are not considered, and it is hard to reduce switch voltage stress and improve power efficiency simultaneously.

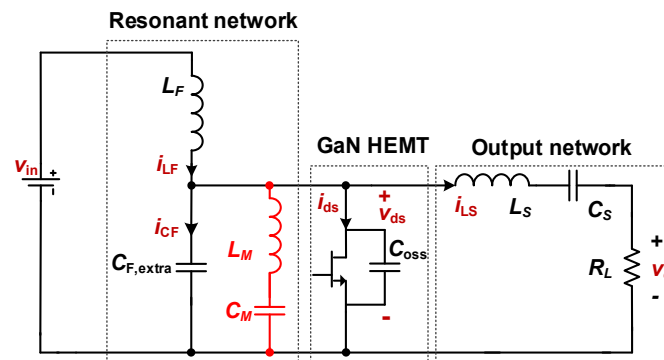


Figure 1. Topology of a VHF class Φ_2 inverter.

To provide detailed guidance for the resonant parameters design of class Φ_2 inverters, extensive research has been carried to explore modeling methods for class Φ_2 inverter. To minimize resonant current magnitude and conduction losses for resonant power converters, an analytical switching cell model is proposed based on the fundamental harmonic approximation (FHA) [25]. However, the third harmonic is neglected in [25], which induces a large error for class Φ_2 inverters. A study [26] established a mathematical model by solving differential equations of the class Φ_2 inverter, where the high-order resonant tank is approximated by a capacitor with an equivalent series resistor (ESR). The approximation simplifies the calculations but induces a larger error for the Φ_2 inverter. To improve the model accuracy and achieve maximum output capacity, a normalized full-order model is proposed which considers high-order voltage and current harmonics [27]. However, the above methods have not explored the relationship between resonant parameters and the power efficiency. To realize optimal parameter design and reduce circling losses of class Φ_2 inverters, an accurate model considering inductor ESR is required to perform fully quantitative calculations.

To achieve efficiency optimization for class Φ_2 inverters, this paper proposes an analytical loss model for class Φ_2 inverters based on harmonic analysis. Firstly, harmonic magnitudes of the switching node voltage are thoroughly analyzed based on operating principles of class Φ_2 inverters. With the results, the power switch is modeled as a voltage source, which simplifies the inverter as a linear network and derives analytical expressions of branch currents. Secondly, root mean square (RMS) values of branch currents and component losses are calculated to establish the analytical loss model. Furthermore, the relationship between the circuit parameters and the overall power efficiency are thoroughly explored. Detailed parameter design guidance and equations are provided to reduce circling losses and improve power efficiency of class Φ_2 inverters. Finally, a class Φ_2 inverter prototype is built to verify the effectiveness of the proposed design strategy.

The rest of this paper is organized as follows. Section 2 describes operating principles of class Φ_2 inverters. In Section 3, the analytical loss model for a class Φ_2 inverter is presented. Based on the model, detailed design guidance for resonant parameters is provided to reduce the circling loss of class Φ_2 inverters. Sections 4 and 7 presents simulation and experimental results, respectively. Section 8 concludes this paper.

2. Topology and Operating Principles of a Class Φ_2 Inverter

The topology of a class Φ_2 inverter consists of a resonant tank, a power switch and a load network, as shown in Figure 1. Compared to a class E inverter, a class Φ_2 inverter adds

a second harmonic resonant branch, i.e., L_M and C_M , to reduce the switch voltage stress. L_F , C_F , L_M and C_M form a high-order resonant tank, which shapes the switching node voltage. Voltage waveforms with different harmonics are shown in Figure 2. Figure 2a shows the switching node voltage consisting of fundamental and third harmonics, while Figure 2b shows the switching node voltage consisting of fundamental and second harmonics. It shows that the third harmonic can effectively reduce the peak value of the switching node voltage.

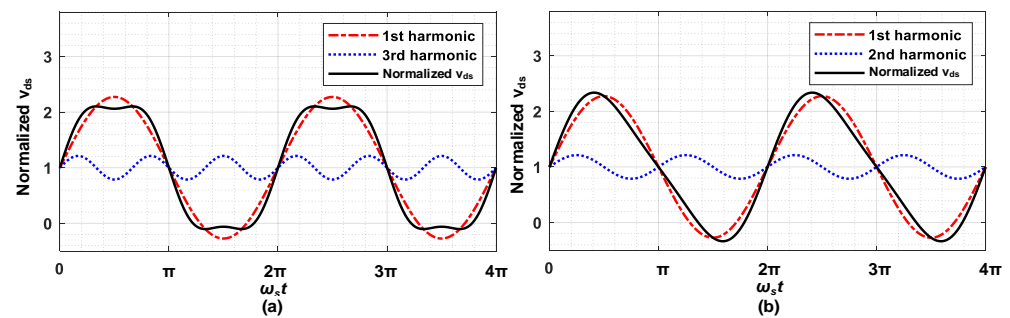


Figure 2. Switch voltage with different harmonics: (a) 1st and 3rd harmonics; (b) 1st and 2nd harmonics.

By properly designing pole and zero positions of the resonant tank, the switching node voltage is formed by the fundamental and third harmonics, which reduces its peak value. Specifically, the switching node impedance consists of two pairs of conjugation poles and a pair of conjugation zeros. Two conjugation poles of the resonant tank are placed at ω_s and $3\omega_s$, while the conjugation zeros are placed at $2\omega_s$, where $\omega_s = 2\pi f_s$ and f_s is the operating frequency of the class Φ_2 inverter. With the above settings, the switching node impedance is high at ω_s and $3\omega_s$, whereas the switching node impedance is low at $2\omega_s$. Therefore, the switching node voltage is formed by fundamental and third harmonics, where the second harmonic is absorbed owing to the zeros at $2\omega_s$.

Based on the above analysis, conventional design methods set the poles at ω_s and $3\omega_s$, and the zeros at $2\omega_s$. Thus, the resonant parameters should satisfy Equation (1) [23].

$$L_F = \frac{1}{9\pi^2 f_s^2 C_F}, L_M = \frac{1}{15\pi^2 f_s^2 C_F}, C_M = \frac{15}{16} C_F \quad (1)$$

There are four parameters L_F , C_F , L_M , C_M , but only three equations are provided. Thus, with conventional design methods, designers are required to choose the value of C_F according to the rated output power and the designers' experience. Then, values of other parameters are calculated by Equation (1). Furthermore, a time-consuming iterative parameter tuning procedure based on circuit simulations is required to adjust values of L_F and C_F , to achieve the desired switch voltage shape. Typically, C_F is increased to reduce switch voltage stress and L_F is reduced to ensure ZVS. The step-by-step design procedure can be found in [23].

Since conventional design methods do not perform fully quantitative calculations, it is hard to achieve an optimal design for a class Φ_2 inverter. Specifically, the selection of C_F highly relies on experience. A small value for C_F can reduce circling loss, but it will lead to an insufficient power transfer capacity and a large switch voltage stress. A large value for C_F can reduce the switch stress, but it increases circling losses which degrades the overall power efficiency. Without fully quantitative calculations, the power efficiency of the Φ_2 inverter is hard to optimize.

3. Analytical Loss Model for a Class Φ_2 Inverter

To provide a fully quantitative theoretical analysis and improve the power efficiency of class Φ_2 inverters, this paper proposes an analytical loss model based on voltage and current harmonic analysis. Firstly, based on basic principles of class Φ_2 inverters, harmonic

components and an analytical expression of switching node voltage are derived. With the results, the power switch is modeled as a voltage source to simplify the calculations. Then, analytical expressions and RMS values of branch currents are calculated based on the switching node voltage, which forms the analytical loss model of class Φ_2 inverters. Furthermore, the influence of resonant parameters on the total loss and power efficiency are thoroughly analyzed, and detailed design guidance and equations for class Φ_2 inverters are provided.

3.1. Switching Node Voltage and Branch Currents Analysis

Based on the principles of class Φ_2 inverters, the switching node voltage mainly consists of the fundamental and the third harmonic. To reduce the switch voltage stress, the fundamental and third harmonics should remain in phase. Additionally, the DC component of the switching node voltage (v_{ds}) equals the input voltage v_{in} , which is derived according to the voltage-second balance of L_F . Therefore, the analytical expression of v_{ds} is given by

$$v_{ds}(t) = v_{in} + v_1 \sin(\omega_s t) + v_3 \sin(3\omega_s t) \quad (2)$$

where v_1 and v_3 are the magnitudes of the fundamental and the third harmonic, respectively. To minimize the switch voltage stress, v_1 and v_3 are $4v_{in}/\pi$ and $2v_{in}/3\pi$, respectively. With the analytical expressions of $v_{ds}(t)$, the power switch is modeled as a voltage source to simplify the calculations. The equivalent circuit is shown in Figure 3.

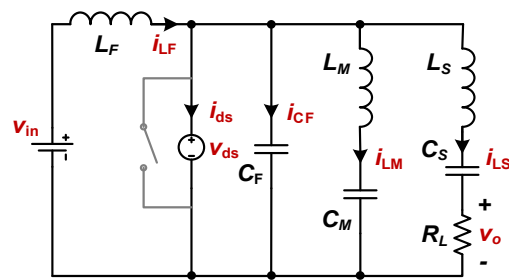


Figure 3. Voltage source equivalent model of a VHF class Φ_2 inverter.

Based on Figure 3, branch currents in a class Φ_2 inverter are calculated as follows. The current of L_F is calculated by integrating the voltage across it, i.e.,

$$\begin{aligned} i_{LF}(t) &= \frac{1}{L_F} \int_0^t v_{in} - v_{ds}(t) dt = \frac{v_1 \cos(\omega_s t)}{\omega_s L_F} + \frac{v_3 \cos(3\omega_s t)}{3\omega_s L_F} + \bar{i}_{ds} \\ &= \frac{4v_{in} \cos(\omega_s t)}{\pi\omega_s L_F} + \frac{2v_{in} \cos(3\omega_s t)}{9\pi\omega_s L_F} + \bar{i}_{ds} \end{aligned} \quad (3)$$

where \bar{i}_{ds} is the average value of the power switch current, calculated using the load power and input voltage. The current of C_F is calculated by differentiating the voltage across it, i.e.,

$$\begin{aligned} i_{CF}(t) &= C_F \frac{dv_{CF}(t)}{dt} = v_1 \omega_s C_F \cos(\omega_s t) + 3v_3 \omega_s C_F \cos(3\omega_s t) \\ &= \frac{4v_{in} \omega_s C_F \cos(\omega_s t)}{\pi} + \frac{2v_{in} \omega_s C_F \cos(3\omega_s t)}{\pi} \end{aligned} \quad (4)$$

Furthermore, by dividing the switching node voltage with the impedance of the load network, the current of L_S is calculated as

$$\begin{aligned} i_{LS}(t) &= \frac{v_1}{|Z_L(j\omega_s)|} \sin(\omega_s t - \angle Z_L(j\omega_s)) + \frac{v_3}{|Z_L(j3\omega_s)|} \sin(3\omega_s t - \angle Z_L(j3\omega_s)) \\ &= \frac{4v_{in}}{\pi|Z_L(j\omega_s)|} \sin(\omega_s t - \angle Z_L(j\omega_s)) + \frac{2v_{in}}{3\pi|Z_L(j3\omega_s)|} \sin(3\omega_s t - \angle Z_L(j3\omega_s)) \end{aligned} \quad (5)$$

$Z_L(j\omega_s)$ is impedance of the load network, which is given by

$$Z_L(j\omega_s) = R_L + j\omega_s L_S + \frac{1}{j\omega_s C_S} \approx R_L + j\omega_s L_S \quad (6)$$

where C_S is a DC-blocking capacitor and is near-short-circuited at the switching frequency. The value of L_S is calculated according to required output power.

Furthermore, the current of L_M is calculated as follows. When the power switch is on, the L_M - C_M branch satisfies the zero-input response equation, since it is a source-free resonant circuit during this period.

$$\begin{cases} L_M \frac{di_{LM}(t)}{dt} + v_{CM}(t) = 0 \\ i_{LM}(t) = C_M \frac{dv_{CM}(t)}{dt} \end{cases} \quad (7)$$

The analytical expression of $i_{LM}(t)$ is derived by solving (7), which is given by

$$i_{LM}(t) = I_2 \sin\left(\sqrt{\frac{1}{L_M C_M}} t\right) \quad (8)$$

where I_2 is the magnitude of the current in L_M - C_M and it is determined by the energy stored in L_M and C_M at the switching-off moment. When the power switch is off, the power switch current is zero. Thus, when the power switch is off, the current of L_M is calculated as

$$i_{LM}(t) = i_{LF}(t) - i_{CF}(t) - i_{LS}(t) \quad (9)$$

In this paper, I_2 is approximated as the maximum value of (9) which has been verified by the LTspice simulation. The SPICE netlist for the LTspice simulation is provided in Appendix A. In fact, with proper design to reduce losses of the class Φ_2 inverter, the resonant switching frequency of L_M - C_M is $2\omega_s$ and current of L_M - C_M only contain the second harmonic. Therefore, (8) can represent the current of L_M - C_M in a whole switching period, i.e.,

$$i_{LM}(t) = I_2 \sin(2\omega_s t) \quad (10)$$

Furthermore, the current of the power switch is calculated as

$$\begin{aligned} i_{ds}(t) &= i_{LF}(t) - i_{LM}(t) - i_{CF}(t) - i_{LS}(t) \\ &= \frac{4v_{in}}{\pi\omega_s L_F} \cos(\omega_s t) + \frac{2v_{in}}{9\pi\omega_s L_F} \cos(3\omega_s t) + \overline{i_{ds}} - I_2 \sin(2\omega_s t) \\ &\quad - \frac{4v_{in}C_F\omega_s}{\pi} \cos(\omega_s t) - \frac{2v_{in}C_F\omega_s}{\pi} \cos(3\omega_s t) \\ &\quad - \frac{4v_{in} \sin(\omega_s t - \angle Z_L(j\omega_s))}{\pi |Z_L(j\omega_s)|} - \frac{2v_{in} \sin(3\omega_s t - \angle Z_L(j3\omega_s))}{3\pi |Z_L(j3\omega_s)|} \\ &\approx \overline{i_{ds}} + I_1 \sin(\omega_s t + \theta_1) - I_2 \sin(2\omega_s t) - I_3 \sin(3\omega_s t + \theta_3) \end{aligned} \quad (11)$$

where I_1 , I_3 , θ_1 and θ_3 are given by

$$\begin{cases} I_1 = \frac{4v_{in}}{\pi} \sqrt{\frac{(\frac{1}{\omega_s L_F} - C_F\omega_s + \frac{1}{|Z_L(j\omega_s)|} \sin(\angle Z_L(j\omega_s)))^2}{+(\frac{\cos(\angle Z_L(j\omega_s))}{|Z_L(j\omega_s)|})^2}} \\ I_3 = \frac{2v_{in}}{3\pi} \sqrt{\frac{(\frac{1}{3\omega_s L_F} - 3C_F\omega_s + \frac{1}{|Z_L(j3\omega_s)|} \sin(\angle Z_L(j3\omega_s)))^2}{+(\frac{\cos(\angle Z_L(j3\omega_s))}{|Z_L(j3\omega_s)|})^2}} \\ \theta_1 = \text{asin}[\cos(\angle Z_L(j\omega_s))] = \frac{\pi}{2} - \angle Z_L(j\omega_s) \\ \theta_3 = \text{asin}[\cos(\angle Z_L(j3\omega_s))] = \frac{\pi}{2} - \angle Z_L(j3\omega_s) \end{cases} \quad (12)$$

With the above calculations, analytical expressions of branch currents are derived. Based on the results, component losses are calculated to establish the analytical loss model for a class Φ_2 inverter.

3.2. Analytical Loss Model for a Class Φ_2 Inverter

Losses of power converter mainly include conduction losses and switching losses. In class Φ_2 inverters, the turning-on loss of the power switch is eliminated owing to zero-voltage switching (ZVS). Additionally, the use of a gallium nitride high electronic mobility transistor (GaN HEMT) greatly reduces the turning-off loss of power switch. Therefore, in a class Φ_2 inverter, the losses are mainly caused by a parasitic resistance of inductors and the on-resistance of the GaN HEMT. A circuit model considering inductor parasitic resistance and power switch on-resistance is shown in Figure 4.

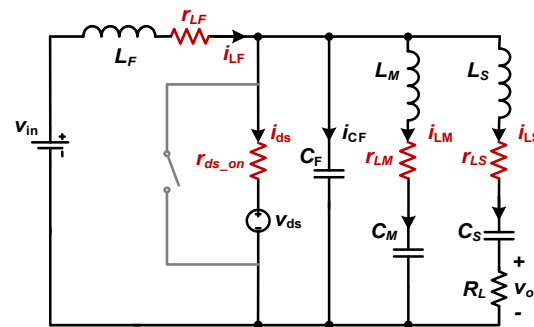


Figure 4. Circuit model for a class Φ_2 inverter considering inductor parasitic resistance and power switch on-resistance.

Based on the derived branch currents in Section 3.2, losses of the inductors and the power switch are calculated to establish the loss model for a class Φ_2 inverter.

Conduction loss of L_F is given by

$$P_{Loss_LF} = \frac{r_{LF}}{T} \int_0^T i_{LF}^2(t) dt \quad (13)$$

Substituting (3) to (13) yields

$$P_{Loss_LF} = r_{LF} \left(\bar{i}_{ds}^2 + \frac{1}{2} \left(\frac{4v_{in}}{\pi\omega_s L_F} \right)^2 + \frac{1}{2} \left(\frac{2v_{in}}{9\pi\omega_s L_F} \right)^2 \right) \quad (14)$$

Similarly, the conduction loss of L_M is calculated as

$$P_{Loss_LM} = \frac{r_{LM}}{T} \int_0^T i_{LM}^2(t) dt = \frac{r_{LM} I_2^2}{2} \quad (15)$$

The conduction loss of L_S is calculated as

$$P_{Loss_LS} = \frac{r_{LS}}{T} \int_0^T i_{LS}^2(t) dt = r_{LS} \left(\frac{1}{2} \left(\frac{4v_{in}}{\pi Z_L(j\omega_s)} \right)^2 + \frac{1}{2} \left(\frac{2v_{in}}{3\pi Z_L(j\omega_s)} \right)^2 \right) \quad (16)$$

The conduction loss of the power switch is calculated as

$$P_{Loss_SW} = \frac{r_{ds,on}}{T} \int_0^T i_{ds}^2(t) dt = r_{ds,on} \left(\bar{i}_{ds}^2 + \frac{I_1^2}{2} + \frac{I_2^2}{2} + \frac{I_3^2}{2} \right) \quad (17)$$

Therefore, the total loss of a class Φ_2 inverter is calculated as

$$P_{Loss} = P_{Loss_LF} + P_{Loss_LM} + P_{Loss_LS} + P_{Loss_SW} \quad (18)$$

Furthermore, the output power of a class Φ_2 inverter is calculated as

$$P_o = R_L \left(\frac{1}{2} \left(\frac{4v_{in}}{\pi Z_L(j\omega_s)} \right)^2 + \frac{1}{2} \left(\frac{2v_{in}}{3\pi Z_L(j\omega_s)} \right)^2 \right) \quad (19)$$

The overall power efficiency of a class Φ_2 inverter is calculated as

$$\eta = \frac{P_O}{P_O + P_{Loss}} \quad (20)$$

3.3. Design Guidance to Reduce Total Loss

In Section 3.2, an analytical loss model for a class Φ_2 inverter is established. To achieve efficiency optimization, this section thoroughly explores the influence of circuit parameters on the total loss of a class Φ_2 inverter. Detailed design guidance is provided to reduce circling losses and improve overall power efficiency.

Conventional design methods derive constraints on-resonance parameters from an empirical perspective. The impedance of the resonant tank is given by

$$Z_{MR}(j\omega) = \frac{j\omega L_F(1 - \omega^2 L_M C_M)}{1 - \omega^2(L_M C_M + L_F C_F + L_F C_M) + \omega^4 L_M C_M L_F C_F} \quad (21)$$

Observing (21), it is found that $Z_{MR}(j\omega)$ consists of two pairs of conjugation poles ($P_{1,2}, P_{3,4}$) and a pair of conjugation zeros ($Z_{1,2}$). Then, based on principles and physical intuition for class Φ_2 inverters, conventional design methods set $P_{1,2} = \omega_s$, $P_{3,4} = 3\omega_s$ and $Z_{1,2} = 2\omega_s$. However, there are four parameters, but only three equations are provided. Designers must select a value for the resonant element, which highly relies on experience. Moreover, the constraints $P_{1,2} = \omega_s$ and $P_{3,4} = 3\omega_s$ are derived by qualitatively analyzing operation principles of class Φ_2 inverters. Therefore, it is hard to realize optimal design, such as minimized voltage stress, minimized circling losses and maximum power efficiency. In this section, design constraints are reconsidered to realize efficiency optimization while minimizing switch voltage stress.

In fact, $Z_{1,2} = 2\omega_s$ is the optimal setting to absorb the second harmonic of the switching node voltage, to reduce the peak value of the switching node voltage. Furthermore, to minimize the switch voltage stress, the switching node impedance should satisfy

$$\frac{Z_{ds}(j\omega_s)}{Z_{ds}(j3\omega_s)} = \frac{6I_3}{I_1} \quad (22)$$

where $Z_{ds}(j\omega_s) = Z_{MR}(j\omega_s) \parallel Z_L(j\omega_s)$, and I_1 and I_3 are magnitudes of the switch current at ω_s and $3\omega_s$, respectively.

The above constraints can realize the optimal design of the power switch voltage stress. To reduce the circling losses, further analyses are carried out as follows. Firstly, the L_M - C_M branch is designed to absorb the second harmonic voltage. At ω_s and $3\omega_s$, the magnitude of the L_M - C_M series resonant branch should be large, to reduce the fundamental and third harmonic currents in L_M . The small capacitor and large inductor form a high characteristic impedance, which reduces unnecessary circling losses. Therefore, the ratio of C_M and C_F is selected as a design constraint to represent circling loss in the L_M - C_M branch, i.e.,

$$k_1 = \frac{C_F}{C_M} \quad (23)$$

where k_1 is larger than 1.

Additionally, to guarantee zero-voltage switching (ZVS) of the power switch, $Z_{ds}(j\omega_s)$ must be inductive at ω_s . Therefore, the lower poles ($P_{1,2}$) of $Z_{MR}(j\omega_s)$ need to be located

between ω_s and $2\omega_s$. The location of $P_{1,2}$ is selected as another design constraint for class Φ_2 inverters, i.e.,

$$P_{1,2} = k_2\omega_s \quad (24)$$

where k_2 is in range [1,2). The following explores the influence of k_1 and k_2 on waveforms and RMS values of branch currents. Constraints of the resonant parameters are summarized as

$$\begin{cases} k_1 = \frac{C_F}{C_M}, P_{1,2} = k_2\omega_s \\ Z_{1,2} = 2\omega_s, \frac{Z_{ds}(j\omega_s)}{Z_{ds}(j3\omega_s)} = \frac{6I_3}{I_1} \end{cases} \quad (25)$$

With (25), the four resonant parameters L_F , C_F , L_M , and C_M can be determined uniquely. The influence of k_1 and k_2 on branch current RMS values and component losses are thoroughly analyzed, to provide detailed design guidance and improve power efficiency of class Φ_2 inverters.

Substituting the main specifications of class Φ_2 inverters, the values of L_F , C_F , L_M , and C_M are calculated with different selection of k_1 and k_2 . The main specifications used in the following calculations are consistent with experiments, where $v_{in} = 40$ V, $f_s = 27.12$ MHz, $P_O = 25$ W and $R_L = 25 \Omega$.

Choosing $k_2 = 1.1$ and a scanning k_1 from 3 to 11, waveforms of $i_{LF}(t)$, $i_{LM}(t)$, $i_{ds}(t)$ and $i_{LS}(t)$ under different k_1 values are shown in Figure 5. As k_1 increases, current magnitudes of $i_{LF}(t)$, $i_{LM}(t)$ and $i_{ds}(t)$ are reduced, whereas the current waveform of $i_{LS}(t)$ remains unchanged. This indicates that increasing k_1 can effectively reduce unnecessary circling loss while maintaining the same output current. However, as k_1 increases, the reduction rate of the resonant current decreases.

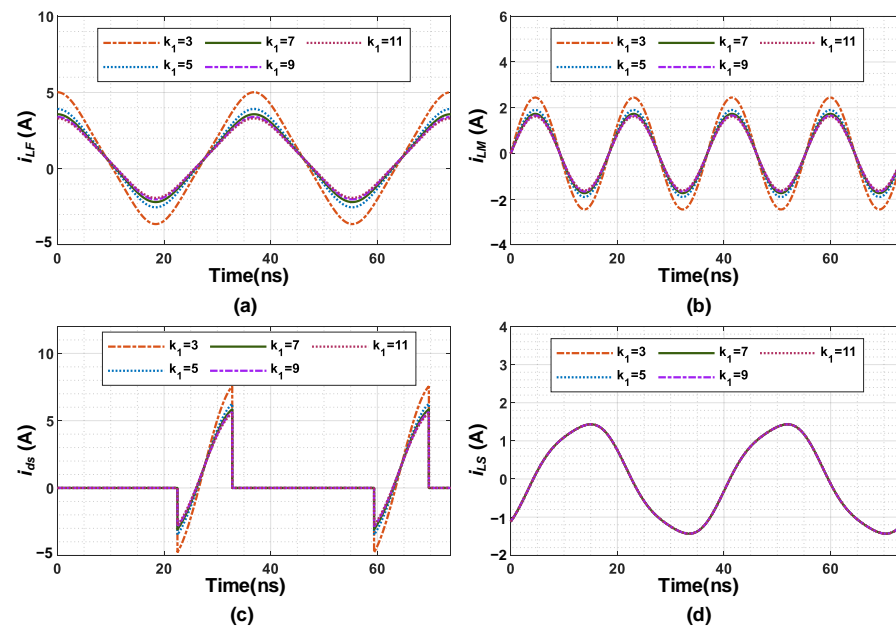


Figure 5. Current waveforms of branch currents under different k_1 values when selecting $k_2 = 1.1$. (a) waveforms of $i_{LF}(t)$; (b) waveforms of $i_{LM}(t)$; (c) waveforms of $i_{ds}(t)$; (d) waveforms of $i_{LS}(t)$.

To further explore the influence of k_1 on circling losses, RMS values of $i_{LF}(t)$, $i_{LM}(t)$, $i_{ds}(t)$ and $i_{LS}(t)$ with respect to k_1 were calculated and are shown in Figure 6. By increasing k_1 , the RMS values of $i_{LF}(t)$, $i_{LM}(t)$ and $i_{ds}(t)$ are effectively reduced, while the RMS current of the output branch, i.e., $i_{LS}(t)$, remains unchanged. This illustrates that the unnecessary circling losses are reduced, which improves power efficiency. However, the slope of the curve in Figure 6b decreases with the increase of k_1 . This indicates that as k_1 increases, the effect on reducing the RMS current of $i_{LF}(t)$ diminishes. From Figure 6b, k_1 is selected as 10.

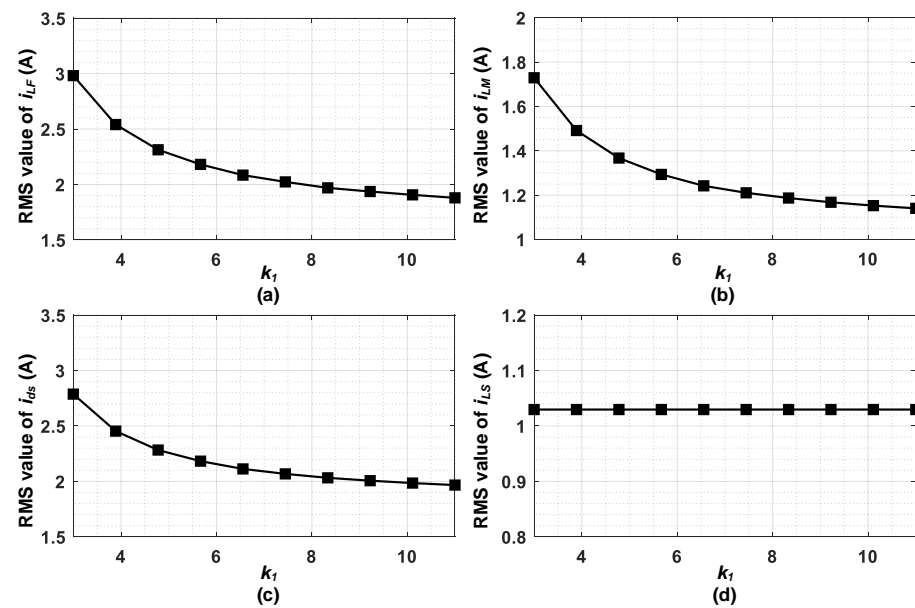


Figure 6. RMS values of branch currents under different k_1 values when selecting $k_2 = 1.1$. (a) RMS values of $i_{LF}(t)$; (b) RMS values of $i_{LM}(t)$; (c) RMS values of $i_{ds}(t)$; (d) RMS values of $i_{LS}(t)$.

Furthermore, at $k_1 = 10$ and a scanning k_2 from 1.05 to 1.25, waveforms of $i_{LF}(t)$, $i_{LM}(t)$, $i_{ds}(t)$ and $i_{LS}(t)$ under different k_2 values are shown in Figure 7. RMS values of branch currents are shown in Figure 8. According to the calculation results, setting k_2 close to 1 can reduce the circling current in class Φ_2 inverters. However, to guarantee zero voltage-switching of the power switch, the switching node impedance must be inductive at the switching frequency. Therefore, the lower poles $P_{1,2}$ should be located higher than ω_s , i.e., $k_2 > 1$. To leave a margin for ZVS, k_2 is selected as 1.1.

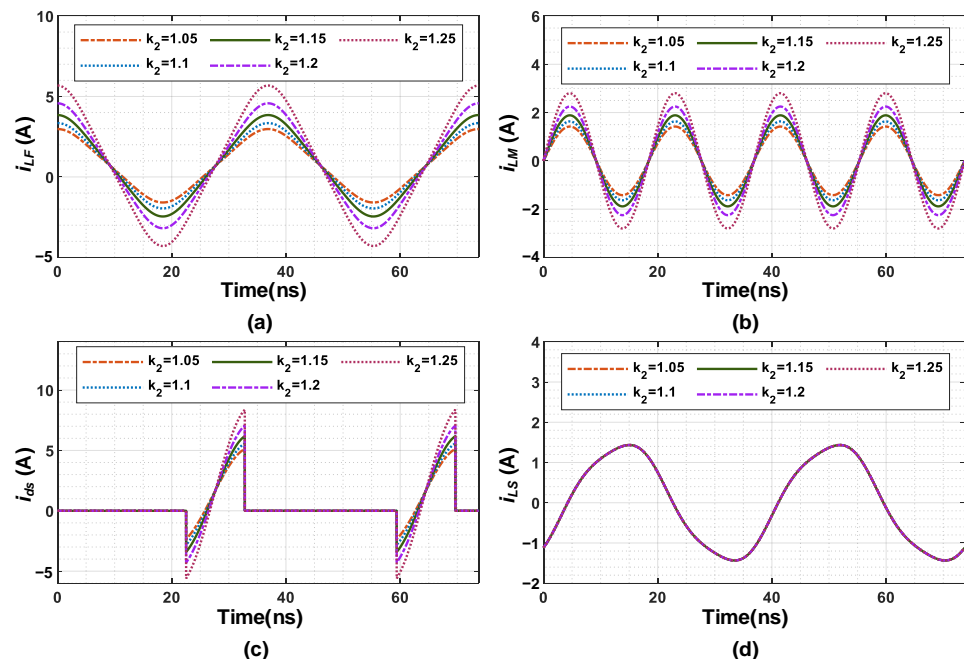


Figure 7. Current waveforms of branch currents under different k_2 values when selecting $k_1 = 10$. (a) waveforms of $i_{LF}(t)$; (b) waveforms of $i_{LM}(t)$; (c) waveforms of $i_{ds}(t)$; (d) waveforms of $i_{LS}(t)$.

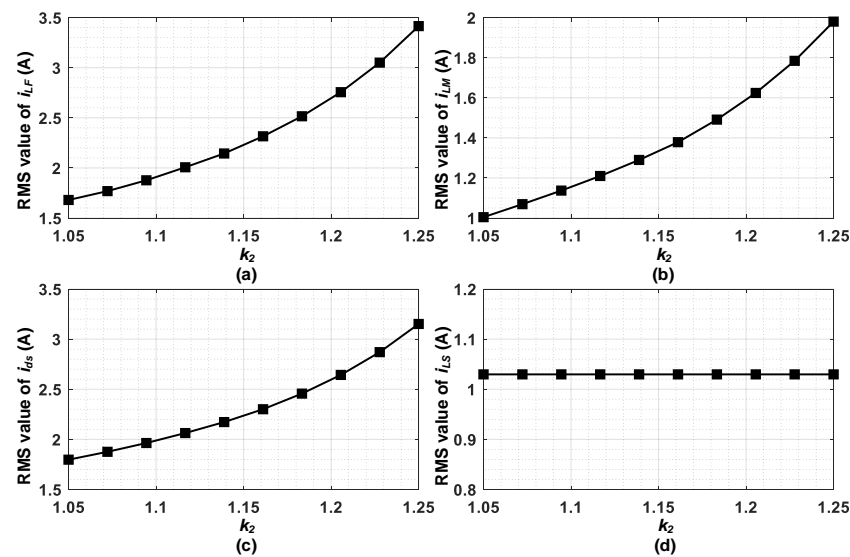


Figure 8. RMS values of branch currents under different k_2 values when selecting $k_1 = 10$. (a) RMS values of $i_{LF}(t)$; (b) RMS values of $i_{LM}(t)$; (c) RMS values of $i_{Ls}(t)$; (d) RMS values of $i_{LS}(t)$.

Furthermore, based on the following assumptions, inductor and power switch losses under different k_1 and k_2 values were calculated. (1) The equivalent series resistance of the inductor is proportional to the inductance. Specifically, $\omega_s L / R_{ESL} = 100$. (2) The on-resistance of the power switch is 100 m Ω . The calculated total loss and overall power efficiency are shown in Figure 9. As k_1 increases and k_2 decreases, the total loss is reduced and the power efficiency is increased.

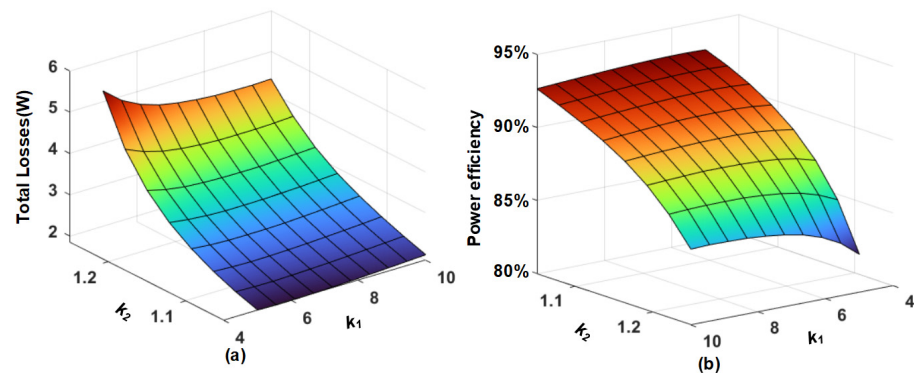


Figure 9. Total loss and overall power efficiency with respect to k_1 and k_2 : (a) total loss; (b) power efficiency.

Combining analyses of RMS branch currents and total loss, optimal values of k_1 and k_2 are derived as

$$\begin{cases} k_1 = 10 \\ k_2 = 1.1 \end{cases} \quad (26)$$

Finally, combining (26) and (25), the optimal circuit parameters L_F , C_F , L_M and C_M are calculated, which reduce circling losses and improve power efficiency. Furthermore, the proposed design method is still effective in a VHF DC–DC power converter by modeling the rectifier stage as a resistor. A VHF DC–DC power converter consists of an inverter stage and a rectifier stage. When designing a VHF class Φ_2 DC–DC power converter, the input impedance of the rectifier at fundamental frequency is tuned to be nearly resistive. Thus, the rectifier is modeled as a resistor in the design of the inverter stage. Therefore, the proposed design method can be easily adopted when designing the DC–DC power converter.

4. Simulation Results Comparisons

To verify the effectiveness of the above analysis and the proposed design constraints, circuit simulations were carried out with different design methods. The main specifications of the simulated class Φ_2 inverter are shown in Table 1, which are the same as those of experiments. Parameters of the proposed design are calculated with (25) and (26), and parameters of conventional design are calculated with the method in [23]. Resonant parameters with different design methods are shown in Table 2. The simulations are carried out in LTspice, and the SPICE netlist is provided in Appendix A. Branch current waveforms, RMS values of branch currents, and component power losses are compared as follows.

Table 1. Main specifications of the class Φ_2 inverter.

Parameters	Values
Switching frequency	27.12 MHz
Input voltage	40 V
Output power	25 W
Load resistance	2.5–25 Ω

Table 2. Circuit parameters with different design methods.

Parameters	Proposed Design Method	Conventional Design Method [23]
L_F	138 nH	65 nH
C_F	205 pF	262 pF
L_M	420 nH	56 nH
C_M	20.2 pF	150 pF
L_S	152 nH	152 nH
C_S	4 nF	4 nF
R_L	25 Ω	25 Ω

5. Branch Current Waveform Comparisons

Waveforms of $i_{LF}(t)$, $i_{LM}(t)$, $i_{ds}(t)$ and $i_{LS}(t)$ at $R_L = 25 \Omega$ are shown in Figure 10. RMS values of branch currents are marked on the figures. With the proposed efficiency optimization design method, the peak and RMS value of branch currents are reduced, thus reducing circling losses and improving the power efficiency of the class Φ_2 inverter.

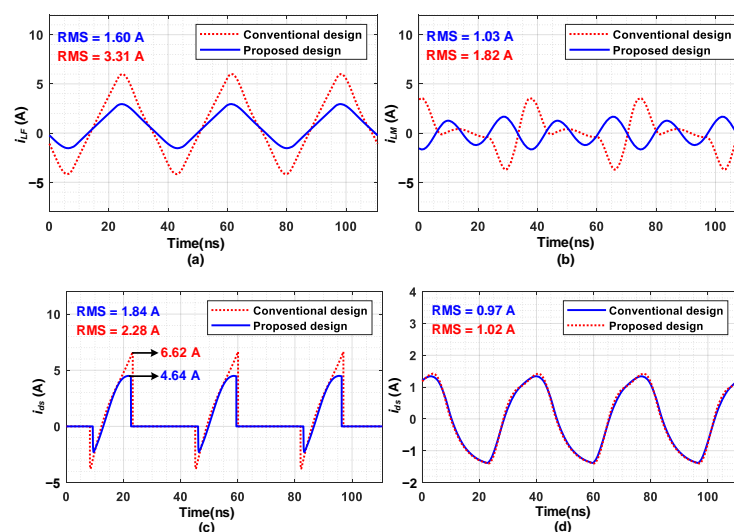


Figure 10. Waveforms of $i_{LF}(t)$, $i_{LM}(t)$, $i_{ds}(t)$ and $i_{LS}(t)$ with different design methods. (a) Waveforms of $i_{LF}(t)$; (b) waveforms of $i_{LM}(t)$; (c) waveforms of $i_{ds}(t)$; (d) waveforms of $i_{LS}(t)$.

6. Loss and Efficiency Comparisons

RMS values of branch currents under different load resistances are summarized in Table 3. Component losses are summarized in Table 4. Parasitic resistances of the proposed design are $r_{LF} = 0.21 \Omega$, $r_{LM} = 0.62 \Omega$, $r_{LS} = 0.33 \Omega$ and $r_{ds_on} = 0.10 \Omega$. Parasitic resistances of the conventional design are $r_{LF} = 0.15 \Omega$, $r_{LM} = 0.60 \Omega$, $r_{LS} = 0.33 \Omega$ and $r_{ds_on} = 0.10 \Omega$. Compared with the conventional design, the proposed design method significantly reduces the RMS value of $i_{LF}(t)$ from 3.31 A to 1.60 A at 25 W, while reducing the loss of L_F from 1.64 W to 0.54 W. The RMS value of L_M is reduced from 1.82 A to 1.03 A, while the loss of L_M is reduced from 1.98 W to 0.65 W. The RMS value of L_S under different designs are essentially the same, which indicates a similar output power. The RMS value of the power switch is reduced from 2.28 A to 1.84 A, while the loss of the power switch is reduced from 0.52 W to 0.34 W. The total loss is reduced from 4.49 W to 1.84 W. At 18 W and 8 W, the RMS values of branch currents and the total loss are also reduced.

Table 3. RMS values of branch currents.

Component	$R_L = 25 \Omega$		$R_L = 10 \Omega$		$R_L = 5 \Omega$	
	Proposed	Conventional	Proposed	Conventional	Proposed	Conventional
L_F	1.60 A	1.60 A	1.60 A	3.34 A	1.60 A	3.34 A
L_M	1.03 A	1.03 A	1.56 A	2.22 A	1.56 A	2.22 A
L_S	0.97 A	0.97 A	1.33 A	1.37 A	1.33 A	1.37 A
Power switch	1.84 A	1.84 A	2.34 A	2.76 A	2.34 A	2.76 A

Table 4. Component losses of the class Φ_2 inverter.

Component	$R_L = 25 \Omega$		$R_L = 10 \Omega$		$R_L = 5 \Omega$	
	Proposed	Conventional	Proposed	Conventional	Proposed	Conventional
L_F	0.54 W	1.64 W	0.54 W	1.67 W	0.51 W	1.66 W
L_M	0.65 W	1.98 W	1.51 W	2.96 W	1.83 W	3.31 W
L_S	0.31 W	0.34 W	0.58 W	0.61 W	0.67 W	0.70 W
Power switch	0.34 W	0.52 W	0.55 W	0.76 W	0.59 W	0.80 W
Total loss	1.84 W	4.49 W	3.18 W	6.01 W	3.60 W	6.48 W

7. Experimental Results

To verify effectiveness of the proposed efficiency optimization design method, two prototypes are built with the conventional and proposed design method, respectively. A block diagram of the prototype is shown in Figure 11, the prototypes are shown in Figure 12, and the main specifications of the prototypes are shown in Table 5. The power switch is EPC2019 from EPC, the gate driver is realized with high-speed buffer NC7WZ17.

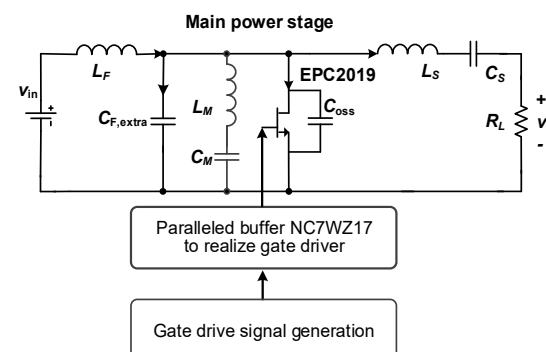


Figure 11. Block diagram of the prototype.

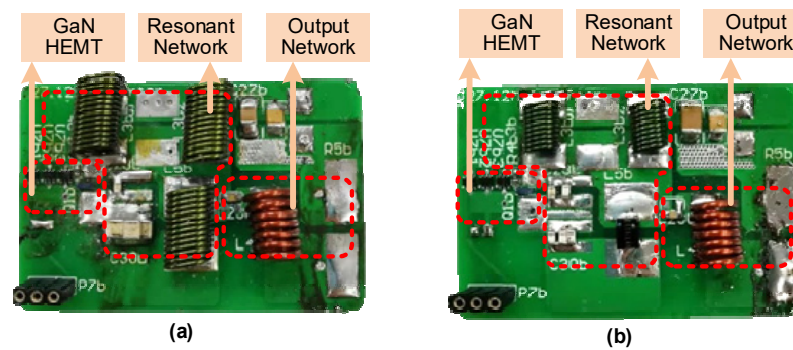


Figure 12. Class Φ_2 inverter prototypes with different design methods: (a) proposed method; (b) conventional design method.

Table 5. Circuit parameters with different design methods.

Parameters	Proposed Design Method	Conventional Design Method
L_F	140 nH	60 nH
C_F	200 pF	290 pF
L_M	430 nH	56 nH
C_M	20 pF	153 pF
L_S	150 nH	150 nH
C_S	4.7 nF	4.7 nF
R_L	25 Ω	25 Ω
Power switch	EPC2019	EPC2019
Gate driver	3 NC7WZ17	3 NC7WZ17

7.1. Waveform Comparisons

The voltage waveforms were measured with the oscilloscope MDO3054. Figure 13 shows the waveforms at $V_{in} = 40$ V and $R_L = 25$ Ω , Figure 14 shows the waveforms at $V_{in} = 40$ V and $R_L = 16$ Ω , and Figure 15 shows the waveforms at $V_{in} = 30$ V and $R_L = 16$ Ω . Output voltages of the proposed and conventional design are essentially the same at different working conditions, whereas the proposed design method reduces the harmonic components of the switching node voltage. This indicates smaller circling losses in the resonant network, which improves the overall power efficiency of the class Φ_2 inverter.

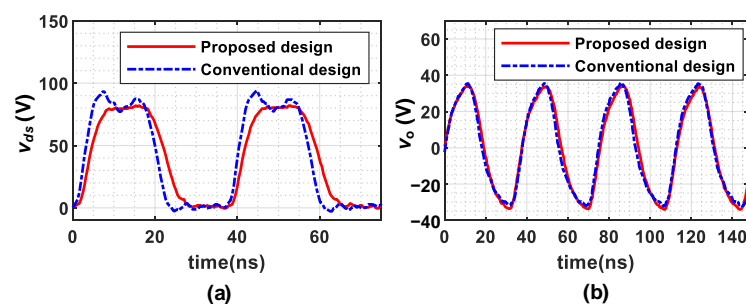


Figure 13. Voltage waveforms of the class Φ_2 inverter at $V_{in} = 40$ V, $R_L = 25$ Ω . (a) Switching node voltage; (b) output voltage.

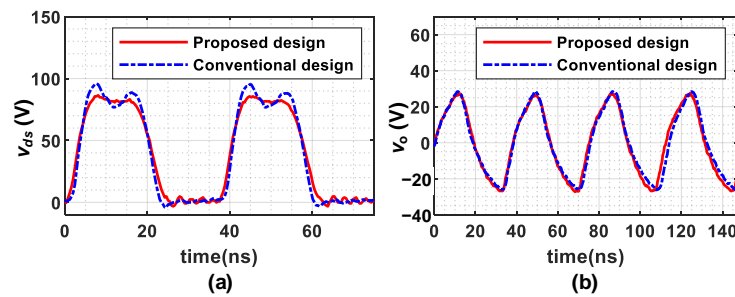


Figure 14. Voltage waveforms of the class Φ_2 inverter at $V_{in} = 40$ V, $R_L = 16$ Ω . (a) Switching node voltage; (b) output voltage.

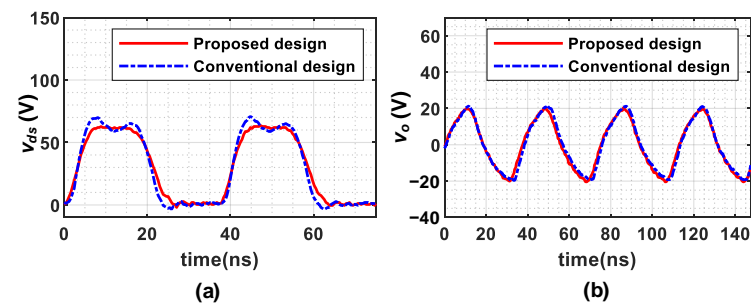


Figure 15. Voltage waveforms of the class Φ_2 inverter at $V_{in} = 30$ V, $R_L = 16$ Ω . (a) Switching node voltage; (b) output voltage.

7.2. Efficiency Comparisons

The input power is obtained by measuring the average input voltage and current with multimeters. The output power is obtained with the value of load resistance and the RMS value of the output voltage. Figure 16a shows the prototype efficiency with respect to load resistance, and Figure 16b shows the prototype efficiency with respect to input voltage. Compared with conventional design, the proposed efficiency optimization design significantly improves the power efficiency over the whole load range. At a rated output power, the proposed design achieves a peak efficiency of 93.6%. Compared with conventional design, an improvement of 9.6% is achieved. Over the whole load range, the power efficiency is improved by more than 7%. The experiments demonstrate that the proposed design method can effectively improve power efficiency of a class Φ_2 inverter by reducing the resonant current magnitude and unnecessary circling losses.

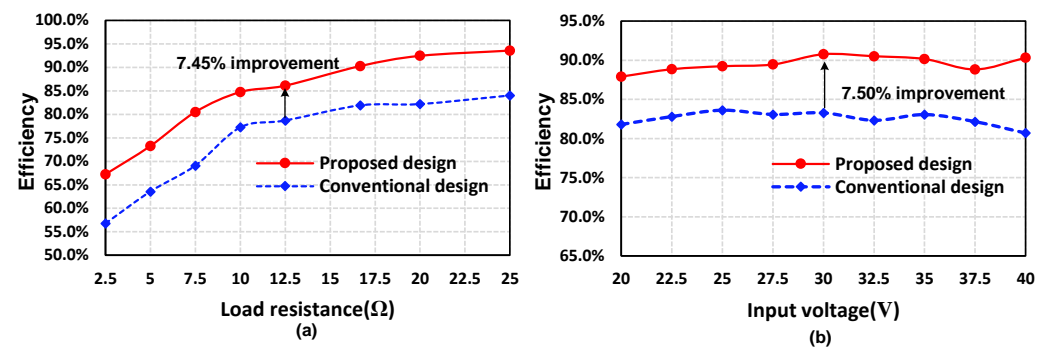


Figure 16. Prototype efficiency under different working conditions. (a) Efficiency with respect to load resistance when $V_{in} = 40$ V; (b) efficiency with respect to input voltage when $R_L = 16$ Ω .

8. Conclusions

This paper proposed an efficiency optimization design method for a very high frequency class Φ_2 inverter based on an analytical loss model. The analytical expression of

the switching node voltage was derived by analyzing its harmonic components. With the result, the circuit was simplified by modeling the power switch as a voltage source. Then, analytical expressions and the RMS value of branch currents were derived to calculate components losses, which form the analytical loss model. Furthermore, the influence of circuit parameters on the total loss and power efficiency were thoroughly analyzed, to derive the optimal design equations and minimize circling losses in the class Φ_2 inverter. Finally, the proposed design method was verified by experiments. The proposed harmonic analysis modeling method and analytical losses model can also be used in other resonant topologies to improve power efficiency.

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Data Availability Statement: The datasets used and/or analyzed during the current study are available from the corresponding author upon reasonable request.

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Conflicts of Interest: The authors declare that they have no conflict of interest.

Appendix A

This appendix provides the SPICE netlist used in LTSPICE simulations.

* SPICE netlist for the proposed design

```
V1 N005 0 PULSE(0 4 0 1p 1p 13.4n 36.87315n 10000)
L1 N001 N002 138n Rser=0.28
L2 N002 N003 152n Rser=0.1
L3 N002 N006 420n Rser=0.6
C1 N006 0 20.2p
C2 N004 N003 4n
R1 N004 0 25
V2 N001 0 40 Rser=0.1
C3 N001 0 1μ
C4 N002 0 205p Rser=0.2
S1 N002 0 N005 0 MySwitch
D1 0 N002 D
.model D D
.lib C:\Users\10652\Documents\LTspiceXVII\lib\cmp\standard.dio
.model MySwitch SW(Ron=.1 Roff=1Meg Vt=1)
.tran 5u
.backanno
.end
```

* SPICE netlist for the conventional design

```
V1 N005 0 PULSE(0 4 0 1p 1p 15N 36.87315n 10000)
L1 N001 N002 65n Rser=0.28
L2 N002 N003 152n Rser=0.1
L3 N006 N002 56n Rser=0.6
C1 N006 0 150p
C2 N004 N003 4n
```

```

R1 N004 0 25
V2 N001 0 40 Rser=0.1
C3 N001 0 1μ
C4 N002 0 262p Rser=0.2
S1 N002 0 N005 0 MySwitch
D1 0 N002 D
.model D D
.lib C:\Users\10652\Documents\LTspiceXVII\lib\cmp\standard.dio
.model MySwitch SW(Ron=.1 Roff=1Meg Vt=1)
.tran 10U
.backanno
.end

```

References

1. Perreault, D.J.; Hu, J.; Rivas, J.M.; Han, Y.; Leittermann, O.; Pilawa-Podgurski, R.C.N.; Sagneri, A.; Sullivan, C.R. Opportunities and Challenges in Very High Frequency Power Conversion. In Proceedings of the 2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition, Washington, DC, USA, 15–19 February 2009; pp. 1–14.
2. Xu, D.; Guan, Y.; Wang, Y.; Wang, W. Topologies and control strategies of very high frequency converters: A survey. *CPSS Trans. Power Electron. Appl.* **2017**, *2*, 28–38. [\[CrossRef\]](#)
3. Knott, A.; Andersen, T.M.; Kamby, P.; Pedersen, J.A.; Madsen, M.P.; Kovacevic, M.; Andersen, M.A.E. Evolution of Very High Frequency Power Supplies. *IEEE J. Emerg. Sel. Top. Power Electron.* **2014**, *3*, 386–394. [\[CrossRef\]](#)
4. Rigot, V.; Phulpin, T.; Sakly, J.; Sadarnac, D. A New 7 kW Air-Core Transformer at 1.5 MHz for Embedded Isolated DC/DC Application. *Energies* **2022**, *1*, 5211. [\[CrossRef\]](#)
5. Li, Y.; Ruan, X.; Zhang, L.; Lo, Y. Multipower-Level Hysteresis Control for the Class E DC–DC Converters. *IEEE Trans. Power Electron.* **2020**, *3*, 5279–5289. [\[CrossRef\]](#)
6. Zhang, Y.; Feng, Y.; Liu, S.; Wu, J.; He, X. Impedance Matching Method for 6.78 MHz Class-E2-Based WPT System. *Energies* **2021**, *1*, 4289. [\[CrossRef\]](#)
7. Liu, C.-Y.; Wang, G.-B.; Wu, C.-C.; Chang, E.Y.; Cheng, S.; Chieng, W.-H. Derivation of the Resonance Mechanism for Wireless Power Transfer Using Class-E Amplifier. *Energies* **2021**, *1*, 632. [\[CrossRef\]](#)
8. Zhang, Z.; Zou, X.; Dong, Z.; Zhou, Y.; Ren, X. A 10-MHz eGaN Isolated Class- Φ_2 DCX. *IEEE Trans. Power Electron.* **2017**, *3*, 2029–2040. [\[CrossRef\]](#)
9. Zou, X.; Zhang, Z.; Dong, Z.; Zhou, Y.; Ren, X.; Chen, Q. A 10-MHz eGaN FETs Based Isolated Class- Φ_2 DCX. In Proceedings of the 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 20–24 March 2016; pp. 2518–2524.
10. Si-Yuan, C.; Jun-Ping, H.; Zi-Fan, L. Resonant DC/DC Converter with Class Φ_2 Inverter and Class DE Rectifier based on GaN HEMT. Proceedings of the 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe), Online, 7–11 September 2020; pp. 1–6.
11. Guan, Y.; Wang, Y.; Wang, W.; Xu, D. A 20 MHz Low-Profile DC–DC Converter with Magnetic-Free Characteristics. *IEEE Trans. Ind. Electron.* **2020**, *6*, 1555–1567. [\[CrossRef\]](#)
12. Gu, L.; Zulauf, G.; Stein, A.; Kyaw, P.A.; Chen, T.; Davila, J.M.R. 6.78-MHz Wireless Power Transfer with Self-Resonant Coils at 95% DC–DC Efficiency. *IEEE Trans. Power Electron.* **2021**, *3*, 2456–2460. [\[CrossRef\]](#)
13. Choi, J.; Xu, J.; Makhoul, R.; Rivas, J. Design of a 13.56 MHz Dc-to-Dc Resonant Converter using an Impedance Compression Network to Mitigate Misalignments in a Wireless Power Transfer System. In Proceedings of 2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL), Padova, Italy, 25–28 June 2018; pp. 1–7.
14. Tang, X.; Zeng, J.; Pun, K.P.; Mai, S.; Zhang, C.; Wang, Z. Low-Cost Maximum Efficiency Tracking Method for Wireless Power Transfer Systems. *IEEE Trans. Power Electron.* **2018**, *3*, 5317–5329. [\[CrossRef\]](#)
15. Zhang, Y.; Ma, J.; Tang, X. A CMOS Active Rectifier with Efficiency-Improving and Digitally Adaptive Delay Compensation for Wireless Power Transfer Systems. *Energies* **2021**, *1*, 8089. [\[CrossRef\]](#)
16. Choi, J.; Ooue, Y.; Furukawa, N.; Rivas, J. Designing a 40.68 MHz Power-Combining Resonant Inverter with eGaN FETs for Plasma Generation. In Proceedings of 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, USA, 23–27 September 2018; pp. 1322–1327.
17. Liang, W.; Raymond, L.; Praglin, M.; Biggs, D.; Righetti, F.; Cappelli, M.; Holman, B.; Davila, J.R. Low-Mass RF Power Inverter for CubeSat Applications Using 3-D Printed Inductors. *IEEE J. Emerg. Sel. Top. Power Electron.* **2017**, *5*, 880–890. [\[CrossRef\]](#)
18. Stedman, Q.; Gu, L.; Pai, C.N.; Rasmussen, M.; Brenner, K.; Ma, B.; Ergun, A.S.; Davila, J.R.; Khuri-Yakub, B. Compact Fast-Switching DC and Resonant RF Drivers for a Dual-Mode Imaging and HIFU 2D CMUT Array. In Proceedings of the 2019 IEEE International Ultrasonics Symposium (IUS), Glasgow, UK, 6–9 October 2019; pp. 1951–1954.
19. Yanagisawa, Y.; Miura, Y.; Handa, H.; Ueda, T.; Ise, T. Characteristics of Isolated DC–DC Converter with Class Φ_2 Inverter Under Various Load Conditions. *IEEE Trans. Power Electron.* **2019**, *3*, 10887–10897. [\[CrossRef\]](#)

20. Guan, Y.; Wang, Y.; Wang, W.; Xu, D. A high-performance isolated high-frequency converter with optimal switch impedance. *IEEE Trans. Ind. Electron.* **2019**, *66*, 5165–5176. [[CrossRef](#)]
21. Kitazawa, K.; Wei, X.; Katsuki, A.; Hirokawa, M. Analysis and Design of the Class- Φ_2 Inverter. In Proceedings of the 44th Annual Conference of the IEEE Industrial Electronics Society, Washington, DC, USA, 21–23 October 2018; pp. 1023–1028.
22. Roslaniec, L.; Jurkov, A.S.; Bastami, A.A.; Perreault, D.J. Design of Single-Switch Inverters for Variable Resistance/Load Modulation Operation. *IEEE Trans. Power Electron.* **2015**, *3*, 3200–3214. [[CrossRef](#)]
23. Rivas, J.M.; Han, Y.; Leitermann, O.; Sagneri, A.D.; Perreault, D.J. A High-Frequency Resonant Inverter Topology with Low-Voltage Stress. *IEEE Trans. Power Electron.* **2008**, *2*, 1759–1771. [[CrossRef](#)]
24. Panov, Y.; Huber, L.; Jovanović, M.M. Design Optimization and Performance Evaluation of Class Φ_2 VHF DC/DC Converter. In Proceedings of 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, 15–19 March 2020; pp. 2170–2177.
25. Lee, K.; Ha, J. Resonant Switching Cell Model for High-Frequency Single-Ended Resonant Converters. *IEEE Trans. Power Electron.* **2019**, *3*, 11897–11911. [[CrossRef](#)]
26. Guan, Y.; Hu, X.; Zhang, S.; Wang, Y.; Xu, D.; Wang, W. A Novel Single Switch High-Frequency DC/DC Converter and Its Mathematical Model. *IEEE Trans. Ind. Appl.* **2019**, *5*, 3877–3888. [[CrossRef](#)]
27. Ma, J.; Asiya, Wei, X.; Nguyen, K.; Sekiya, H. Analysis and Design of Generalized Class-E/ F_2 and Class-E/ F_3 Inverters. *IEEE Access* **2020**, *8*, 61277–61288. [[CrossRef](#)]