

Article

Analysis of a Single-Phase Transformerless Bidirectional PFC

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Abstract: This paper presents a single-phase transformerless bidirectional power factor corrector (PFC). A capacitor is inserted into a conventional full-bridge PFC by connecting the ac line terminal and a terminal of DC voltage. The functions of this inserted capacitor have two roles: to bypass the common-mode leakage current from the stray capacitor; to form an LCL filter to reduce the inductor current ripple. A hybrid modulation method is employed in this PFC. The unipolar switching scheme is applied to modulate the PFC, which can achieve high efficiency. Meanwhile, an additional modulation is inserted into the blank time of low-frequency switches to decrease the changing speed of the voltage on the inserted capacitor, and to decrease the spike on the inductor current and leakage current. The performance of the PFC is experimentally verified using a 5 kW prototype.

Keywords: power factor corrector (PFC); common-mode (CM) leakage current; LCL filter; modulation

1. Introduction

Power factor correction (PFC) converters have rapidly developed during the last decade, such as motor drive, electronic ballast, EV charger, and power supply, which act as the grid-connected power stage [1–5]. Advanced PFC topology can acquire good performances, such as efficiency, power density, and common-mode leakage current [6–9]. Figure 1 shows one traditional configuration for a low-power servo motor, which includes a line transformer, single-phase diode rectifier, and drives. The traditional configuration exhibits three problems, which can be solved by advanced PFC topology, as follows:

- (1) The power flow in the diode rectifier is unidirectional, the regenerative power, generated when the motors decelerate, must be consumed on the bleed resistor, which is installed at the DC bus. Therefore, the total energy efficiency of traditional configuration is very low, and results in the high temperature of the bleed resistor.
- (2) The line transformer is always added to supplement the low grid voltage, due to the fact that the DC voltage converted by the diode rectifier is not high enough for the normal operation of the drive for the motor. One additional line transformer must be added to boost the voltage. However, the line transformer is heavy, bulky, and expensive.
- (3) The stray capacitor, existing in the long cables to connect the drive with the motor, passes the common-mode leakage current through the ground terminal in the absence of the line transformer. The common-mode leakage current needs to meet certain standards to protect the equipment and humans [10–12]; for example, the rms value of the leakage current should be limited to 300 mA. Therefore, a single-phase bidirectional and transformerless PFC with common-mode leakage current suppression technologies needs to be used for low-power servo motor application.

The conventional full-bridge PFC with the bipolar switching scheme has the advantage of a lower common-mode leakage current than with the unipolar switching scheme [13–18]. However, the bipolar switching scheme leads to high current ripple and large semiconductor losses. The unipolar switching scheme has good efficiency and current ripple, but the common-mode leakage current is high, which limits this scheme's employment. To achieve



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the unipolar switching scheme and low common-mode leakage current simultaneously, some PFC topologies, such as H5 [19,20], H6 [21,22], HERIC [23,24], and AVG [25,26], have been proposed. H5 topology, H6 topology, and HERIC topology add semiconductors to break the common-mode leakage current path. However, these topologies require more semiconductors, which increases the cost and losses, because added semiconductors are in the current path and switch with the main high-frequency switches in the PFC converter. AVG topology adds one capacitor and two bidirectional semiconductors to bypass the common-mode leakage current from the stray capacitor. The advantages of AVG topology are the additional bidirectional semiconductors at low frequency and LCL filter formed by inserting the extra capacitor to reduce the inductor current ripple. However, the drawbacks are still higher semiconductor cost and losses.

In this paper, a single-phase transformerless bidirectional PFC is studied, the configuration of which is shown in Figure 2. In Figure 2, it consists of a conventional full-bridge PFC and a capacitor C_f connecting the ac line terminal and a negative terminal of DC voltage, in which extra semiconductors are unnecessary. This PFC can mitigate the common-mode leakage current issue, since the inserted capacitor C_f provides a path to bypass the common-mode leakage current. In addition, the capacitor C_f combining the inductors in PFC converter can form LCL filter, which results a reduction in inductor current ripple. A hybrid modulation method is employed in this PFC. The unipolar switching scheme is applied to modulate the PFC converter; thus, two high-frequency switches and two low-frequency switches are required. Meanwhile, an additional modulation is inserted into the blank time of low-frequency switches when grid voltage is zero-crossing. This inserted modulation is to decrease the changing speed of the voltage on the capacitor C_f , which leads to a spike on the inductor current and leakage current. Therefore, this PFC can also achieve low cost and high efficiency.

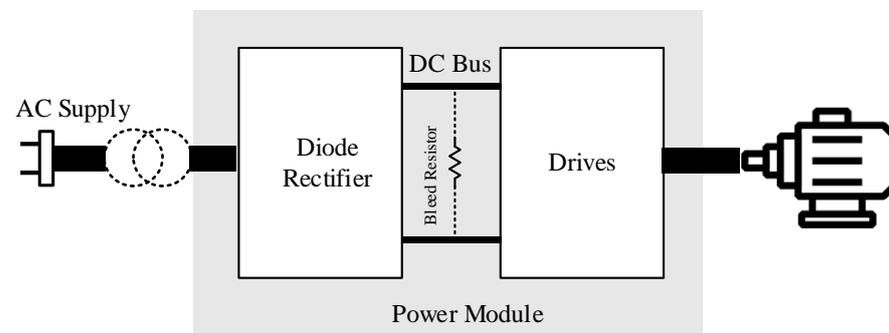


Figure 1. Traditional configuration for low-power servo motor drive application.

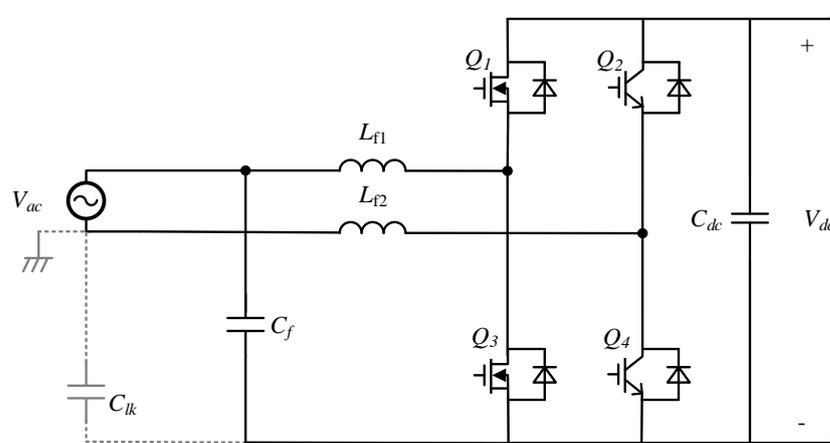


Figure 2. Configuration of PFC topology.

The rest of this paper is structured as follows. Section 2 presents a detailed description of operating principle. The characteristics analysis results are presented in Section 3. System implementations are presented in Section 4. Experimental verification is presented in Section 5. Finally, Section 6 presents the main conclusions.

2. Analysis of Operating Principle

In Figure 2, Q_1 and Q_3 are required high-frequency switches, such as SiC MOSFETs, and Q_2 and Q_4 are required low-frequency switches, such as IGBTs. Switches Q_1 , Q_2 , Q_3 , and Q_4 and inductors L_{f1} and L_{f2} form the conventional full-bridge PFC. Capacitor C_{lk} represents the stray capacitor existing in the long cables which connect drive with motor. An additional capacitor C_f connects the ac line terminal and a negative terminal of DC voltage. Figure 3 shows the steady-state waveforms of the PFC, which exhibits Pattern I, Pattern II, Pattern III, and Pattern IV. The current conducting paths of every pattern are presented in Figure 4. For the convenience of the analysis, assumption that all switches, diodes, inductors, and capacitors are ideal.

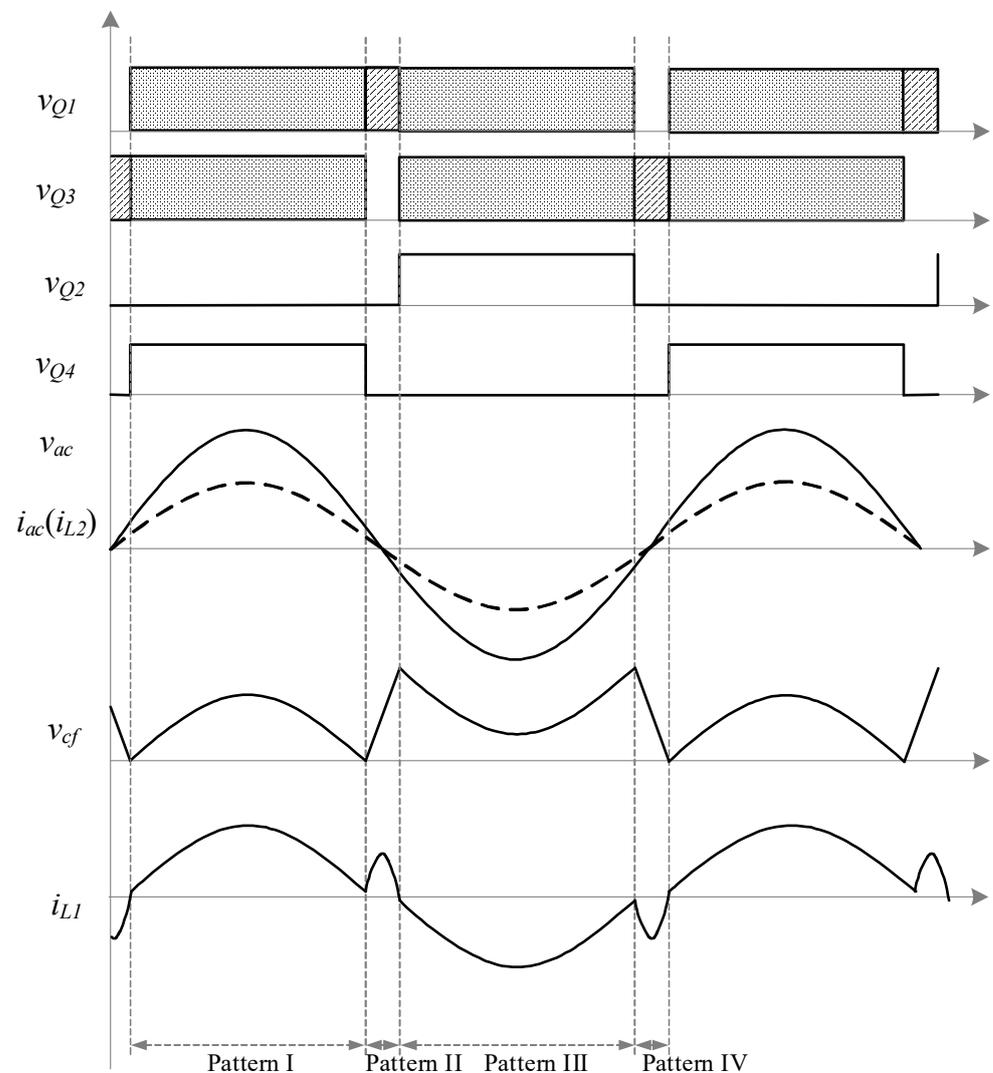


Figure 3. Steady-state waveforms of the PFC.

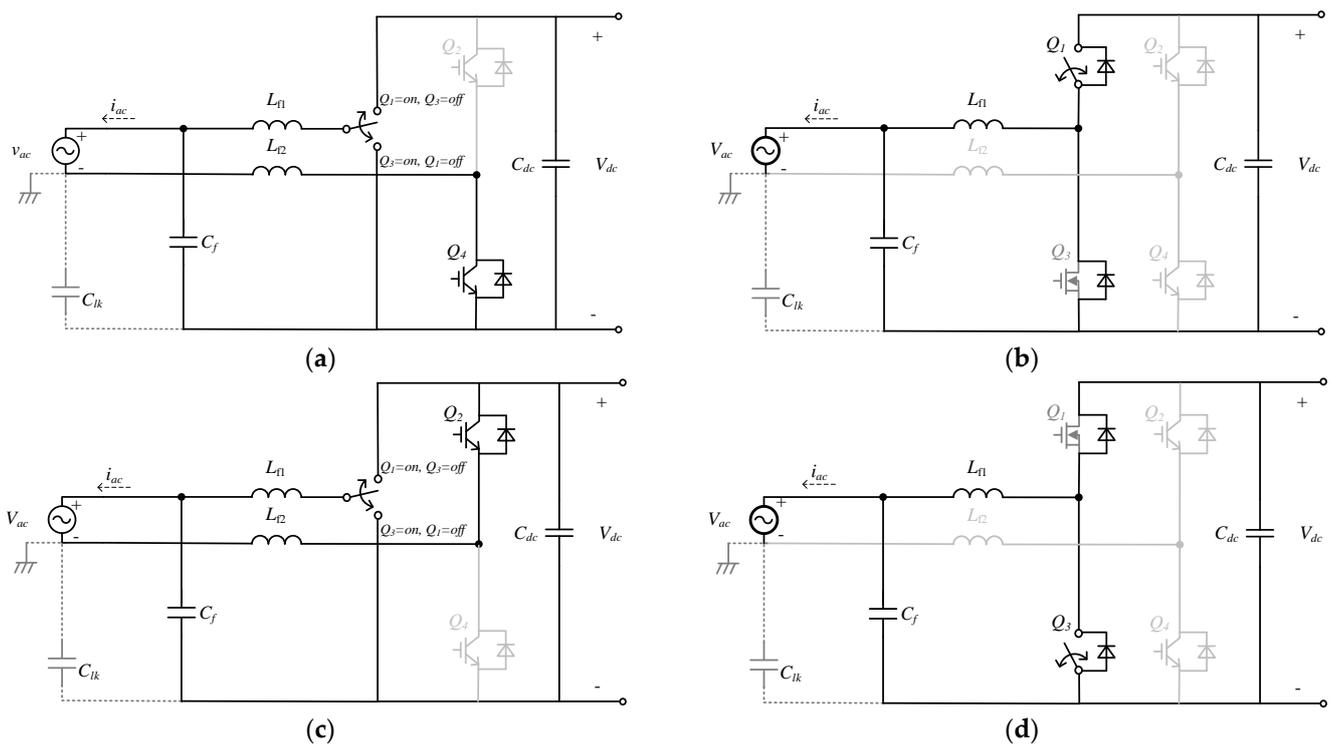


Figure 4. The current conducting path of every pattern. (a) Pattern I, (b) Pattern II, (c) Pattern III, and (d) Pattern IV.

2.1. Operation Pattern

- (1) Pattern I: Switches Q_1 and Q_3 are switching complementarily with high frequency, and switch Q_4 is constantly in the ON state when the grid voltage is in the positive half cycle. The switching state of Pattern I is shown in Figure 4a. It can be observed that the middle voltage of the high-frequency leg is high-frequency switching voltage with magnitude changing between V_{dc} and zero, which creates large high-frequency current ripple. Due to the capacitor C_f , connecting the ac line terminal and the negative terminal of the DC-side, the LCL filter is configured with the inductors L_{f1} and L_{f2} , which act as the converter-side inductor and the grid-side inductor, respectively. The equivalent circuit of this pattern is shown in Figure 5a. As a result, a significant reduction in the inductor current ripple will be realized. In addition, it can be observed that the stray C_{lk} is in parallel with the capacitor C_f when the grid is assumed to be short-circuit because it can be regarded as a constant voltage source in the high-frequency analysis. The impedance in the capacitor C_f path is lower. Capacitor C_f couples the voltage between the terminal of the grid-side and the negative terminal of the DC-side, which clamps the voltage difference, and the ripple voltage on the capacitor C_f is small. Therefore, the common-mode leakage current flow of the stray capacitor C_{lk} is minimized.
- (2) Pattern II: Switches Q_2 and Q_4 are in the OFF state, switch Q_1 switches ON or OFF with high frequency when the grid voltage zero-crossing point transitions from positive to negative. Switch Q_3 acts as the synchronous switch of D_3 . The switching state of Pattern II is shown in Figure 4b. The reason for this pattern is that the middle voltage of the low-frequency leg changes rapidly from zero to V_{dc} if switches Q_2 and Q_4 switchover fast, while the voltages on capacitor C_f and stray capacitor C_{lk} are approximately zero, the voltage difference on which will lead to a large spike on the inductor current and leakage current, which is unwanted. In this pattern, a similar buck converter is formed by DC voltage V_{dc} , switch Q_1 , diode D_3 (synchronous switch Q_3), inductor L_{f1} , capacitor C_f and stray capacitor C_{lk} . The equivalent circuit of this

pattern is shown in Figure 5b. The voltages on capacitor C_f and stray capacitor C_{lk} will be charged up slowly to suppress the appearance of the current spike.

- (3) Pattern III: Switches Q_1 and Q_3 are switching complementarily with high frequency, and switch Q_2 is constantly in the ON state when the grid voltage in the negative half cycle. The switching state of Pattern III is shown in Figure 4c. Although the inductor L_{f2} is changed to connect the positive terminal of the DC-side, the LCL filter is formed by capacitor C_f , inductors L_{f1} and L_{f2} , which achieves the low inductor current ripple. The equivalent circuit of this pattern is also shown in Figure 5a. Additionally, capacitor C_f and stray capacitor C_{lk} are in parallel, which achieves low common-mode leakage current.
- (4) Pattern IV: Switches Q_2 and Q_4 are in the OFF state, switch Q_3 switches ON or OFF with high frequency when the grid voltage zero-crossing point transitions from negative to positive. Switch Q_1 acts the synchronous switch of D_1 . The switching state of Pattern IV is shown in Figure 4d. If switches Q_2 and Q_4 switchover fast, the middle voltage of the low-frequency leg changes rapidly from V_{dc} to zero, while the voltages on capacitor C_f and stray capacitor C_{lk} are approximately V_{dc} , the voltage difference on which will also lead to a large spike on the inductor current and leakage current. In this pattern, a similar boost converter is formed by capacitor C_f and stray capacitor C_{lk} , inductor L_{f1} , switch Q_3 , diode D_1 (synchronous switch Q_1), and DC voltage V_{dc} . The equivalent circuit of this pattern is shown in Figure 5b. The voltages on capacitor C_f and stray capacitor C_{lk} will be discharged slowly to suppress the appearance of the current spike.

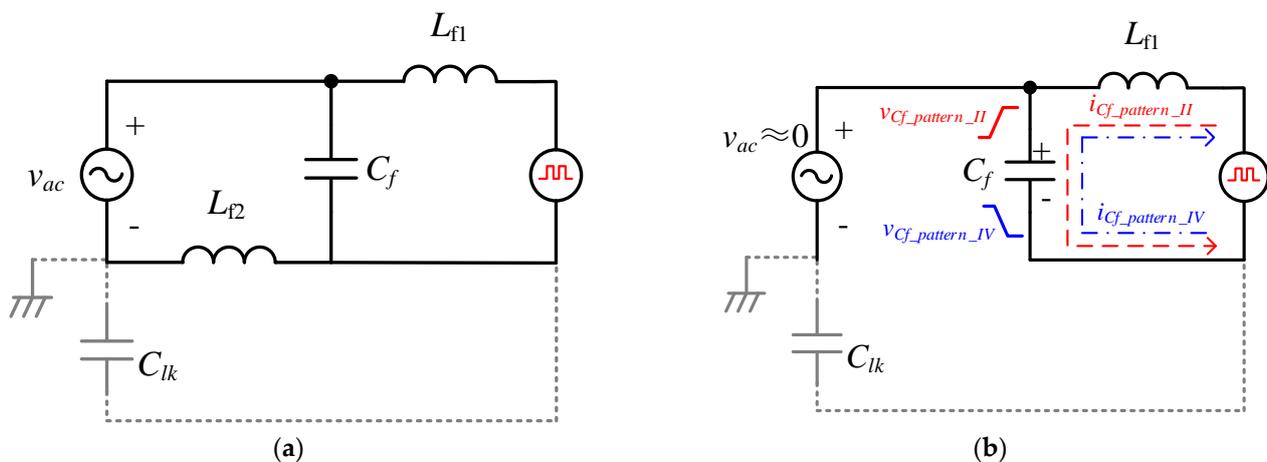


Figure 5. Equivalent circuit of every pattern. (a) Pattern I and Pattern III, (b) Pattern II and Pattern IV.

2.2. Control Scheme

Figure 6 presents the control block diagram of the PFC. The pattern selection is based on the polar and the trend of the grid voltage.

For Pattern I and Pattern III, a basic double-loop control methodology is applied. DC voltage V_{dc} is regulated by a proportional integral (PI) controller in the outer loop. The output of outer loop is the grid current reference i_{ac_ref} of the inner loop, which realizes to track the grid current i_{ac} in sinusoidal by PI controller. The output of inner loop is used to generate the PWM signals of switches Q_1 and Q_3 for Pattern I and Pattern III. The signals of switches Q_2 and Q_4 are controlled by the polar of grid voltage V_{ac} . Switch Q_4 remains in the ON state at the positive half grid cycle for Pattern I, and switch Q_2 remains in the ON state at the negative half grid cycle for Pattern III.

For Pattern II or Pattern IV, switches Q_1 or Q_3 operate at high-frequency ON or OFF, and are controlled by the open-loop control. The frequency Q_1 and Q_3 are same with Pattern I and Pattern III, and the duty ratio expands gradually to decrease the changing speed of voltage on the capacitor C_f and stray capacitor C_{lk} , which will lead to a spike

on the inductor current and leakage current. The zoomed-in waveforms in Pattern II or Pattern IV are shown in Figure 7. Note that switches Q_1 and Q_3 switch complementarily in Pattern II or Pattern IV to decrease the losses of diodes D_1 and D_3 .

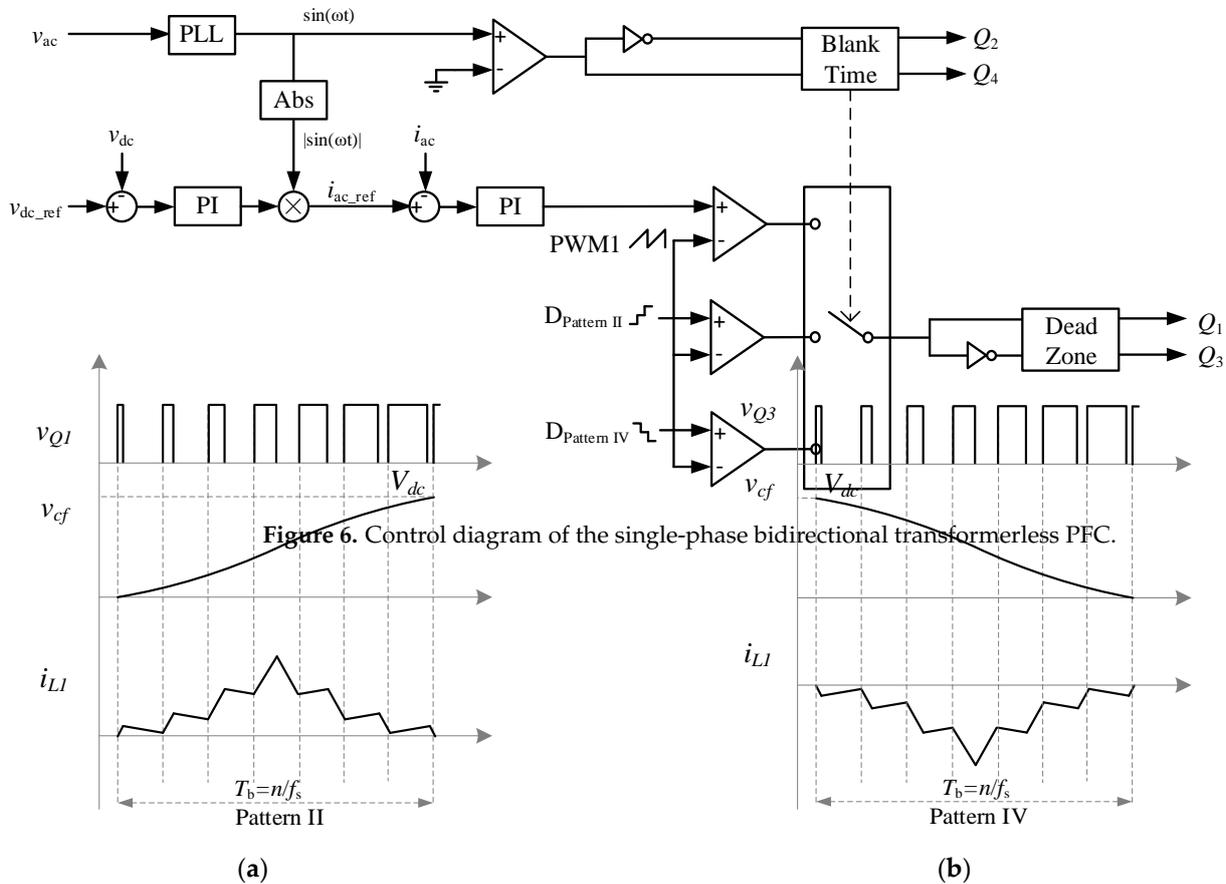


Figure 6. Control diagram of the single-phase bidirectional transformerless PFC.

Figure 7. The zoomed-in waveform during the grid voltage zero-crossing. (a) Pattern II and (b) Pattern IV.

3. Characteristics Analysis

The characteristics of this single-phase bidirectional transformerless PFC are analyzed based on Figure 5. The inductors L_{f1} and L_{f2} are identical and have the same values. The positive half grid cycle is used for the following analysis; the negative half grid cycle has the same characteristics, which are not present in this paper.

3.1. Duty Cycle

In Pattern I and Pattern III, the PFC works as a simple boost converter when neglecting the small voltage drop on the grid-side inductor L_{f2} . Thus, the duty ratio can be expressed by

$$D_{I, III} = 1 - \frac{v_{ac}(t)}{V_{dc}} \tag{1}$$

where v_{ac} is the instantaneous grid voltage, $v_{ac} = V_{ac}\sin(\omega t)$, V_{ac} is the peak amplitude of grid voltage, and ω is the angular grid frequency. The duty ratio can be obtained as

$$D_{I, III} = 1 - \frac{V_{ac}}{V_{dc}} \sin \omega t \tag{2}$$

At all times, the duty cycle is time varying and follows the change of grid voltage.

In Pattern II or Pattern IV, a similar buck or boost converter is formed to charge or discharge slowly the capacitor C_f and stray capacitor C_{lk} . The duty ratio of the switches Q_1 or Q_3 can be expressed as

$$D_{II, IV} = (n - 1)\Delta D \quad (3)$$

where ΔD is the incremental step of the duty ratio, and n is the number of switching periods in Pattern II or Pattern IV, $n = 1, 2, 3 \dots$, which are always set in the digital controller. When the duty ratio of the switches Q_1 or Q_3 expands gradually to 1, the Pattern II or Pattern IV finish the modulation.

3.2. Current Ripple and Voltage Ripple of LCL Filter in Pattern I and Pattern III

Under fixed switching frequency and continuous conduction mode operation, the converter-side inductor current ripple is developed from the ON-state characteristic as

$$\Delta i_{L1_I, III} = \frac{(V_{dc} - V_{ac} \sin \omega t) V_{ac} \sin \omega t}{V_{dc} L_1 f_s} \quad (4)$$

where f_s is the switching frequency of switches Q_1 and Q_3 .

The voltage ripple of the capacitor C_f is mainly contributed by the current ripple of the converter-side inductor, which is calculated as

$$\Delta v_{cf_I, III} = \frac{(V_{dc} - V_{ac} \sin \omega t) V_{ac} \sin \omega t}{8V_{dc} L_1 (C_{lk} + C_f) f_s^2} \quad (5)$$

The grid current ripple is basically contributed by the capacitor C_f and stray capacitor C_{lk} , thus, the grid current ripple is formed as

$$\Delta i_{L2_I, III} = \frac{(V_{dc} - V_{ac} \sin \omega t) V_{ac} \sin \omega t}{16\pi V_{dc} (C_{lk} + C_f) L_1^2 f_s^3} \quad (6)$$

3.3. Duty Cycle Fundamental Current of Inductor L_1 in Pattern II and Pattern IV

The current spike caused by charging or discharging the capacitor C_f and stray capacitor C_{lk} is suppressed by inserting a modulation of switches Q_1 or Q_3 at the blank time between Q_2 and Q_4 . The transition of the voltage on capacitor C_f and stray capacitor C_{lk} in Pattern II and Pattern IV can be approximately treated, as shown in the following formulas,

$$v_{cf_II} = \frac{1}{2} V_{dc} (1 - \cos \omega_b t) \quad (7)$$

$$v_{cf_IV} = \frac{1}{2} V_{dc} (1 + \cos \omega_b t) \quad (8)$$

where ω_b is the equivalent angular frequency of the blank time, $\omega_b = \pi f_s / n$. In Pattern II or Pattern IV, the current of inductor L_1 is the charging or discharging current for capacitor C_f and stray capacitor C_{lk} . The fundamental current of inductor L_1 can be approximately calculated as a derivation of v_{cf} , which are

$$i_{L1_II} = \frac{\omega_b (C_{lk} + C_f) V_{dc}}{2} \sin \omega_b t \quad (9)$$

$$i_{L1_IV} = -\frac{\omega_b (C_{lk} + C_f) V_{dc}}{2} \sin \omega_b t \quad (10)$$

3.4. Current Ripple and Voltage Ripple of LCL Filter in Pattern I and Pattern III

The common-mode leakage current is defined as the current passing through the stray capacitor on the cable and the ground. As shown in Figure 2, the stray capacitor C_{lk} is virtually parallel with the capacitor C_f . In Pattern I and Pattern III, the high-frequency part of i_{L1} passes through the capacitor C_f and the stray capacitor C_{lk} . In Pattern II and Pattern

IV, current i_{L1} charges or discharges the capacitor C_f and the stray capacitor C_{lk} together; thus, the common-mode leakage current can be expressed as

$$\Delta i_{C_{lk}} = \frac{C_{lk}}{C_f + C_{lk}} \Delta i_{L1} \tag{11}$$

Based on (11), the common-mode leakage current is directly proportional to the capacitance ratio between capacitor C_f and stray capacitor C_{lk} , and the converter-side inductor current ripple Δi_{L1} . In Pattern I and Pattern III, the common-mode leakage current can be adjusted by the value of capacitor C_f . However, in Pattern II and Pattern IV, capacitor C_f and blank time between Q_2 and Q_4 need to be traded off to suppress the spike on inductor current i_{L1} and THDi of the PFC.

4. System Implementation

4.1. Topology Variants

Figure 2 shows one of the possible single-phase bidirectional transformerless PFCs; the alternative configurations are shown in Figure 8, which have same electrical characteristics, except the DC voltage offset across capacitor C_f , because three variants connect the capacitor C_f to V_{dc} minus, half V_{dc} , or V_{dc} plus, respectively.

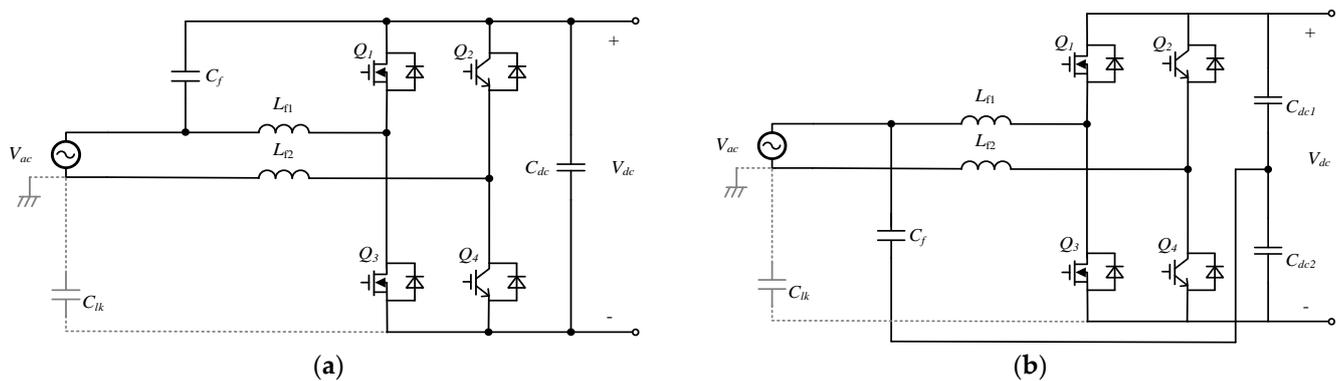


Figure 8. Possible configurations of the single-phase bidirectional transformerless PFC. (a) C_f connecting to V_{dc} plus and (b) C_f half V_{dc} minus.

4.2. System Implementation

A hardware setup to evaluate the PFC in the laboratory. Table 1 shows the key parameters of hardware setup. A 47nF capacitor is used to simulate the stray capacitor C_{lk} . This prototype is used to verify the performances of the PFC.

Table 1. Key parameters of hardware setup.

Parameters	Values
DC voltage	370 V
Grid voltage	230 V
Grid frequency	50 Hz
Power	5 kW
Switching frequency	60 kHz
Blank Time of Pattern II or IV	120 μ s
Stray Capacitor	47 nF

4.3. Selection of Filter Components

In the design, the inductor current ripple is set to 20% of peak current at full power. Based on (4), the minimum value of the required inductance is calculated as 0.12 mH. Considering both the inductance drop due to nanocrystalline material and experimental performance, inductor L_{f1} and L_{f2} are designed as 0.17 mH. The selection of C_f is based on

the following two criteria: one is the LCL filter resonance frequency, which should be a large ratio difference from the switching frequency, such as a tenfold difference; the other is the common-mode leakage current, which should meet some standards to limit the leakage current to a certain level. To fulfill both criteria, the value of capacitor C_f is selected as $6.8 \mu\text{F}$ based on the parameters in Table 1.

4.4. Simulation Verification

To verify the operating principle of the PFC, the simulation model is generated in PLECS. In addition, the comparisons between the prior PFCs in [18,26] and the PFC in this paper are presented in this section.

The PFC in [18] is the conventional full-bridge PFC with the bipolar switching scheme. The PFC with AVG in [26] is the conventional full-bridge PFC with one added capacitor and two bidirectional semiconductors, which uses the unipolar switching scheme. The compared simulation results are shown in Figure 9, in which the grid voltage v_{ac} , the grid current i_{ac} (i_{L2}), the common-mode leakage current i_{Clk} , and the capacitor voltage v_{Clk} are presented. The capacitor current i_{Clk} is used to represent the common-mode leakage current. The parameters of the PFCs in simulation models are same with Table 1. Based on the simulation results in Figure 9, the common-mode leakage current of the PFC in this paper is higher than others, but it meets the requirement of 300 mA [10–12]. Figure 10 presents the simulation semiconductor losses of the prior PFCs in [18,26] and the PFC in this paper. The high-frequency switches use C3M0065100K from Cree Inc., Durham, NC, USA, and the low-frequency switches use IKW75N65EL5 from Infineon Inc., Ilmenau, Germany. The simulation semiconductor losses include the conduction losses and the switching losses of switches of the full-bridge PFC, the losses of body diodes, and the losses of switches on AVG. From Figure 10, the simulation semiconductor losses of the PFC in this paper are much lower than those of the prior PFCs. What is more, the PFC in this paper has no additional semiconductors and only two high-frequency switches, which can be acquired at low cost.

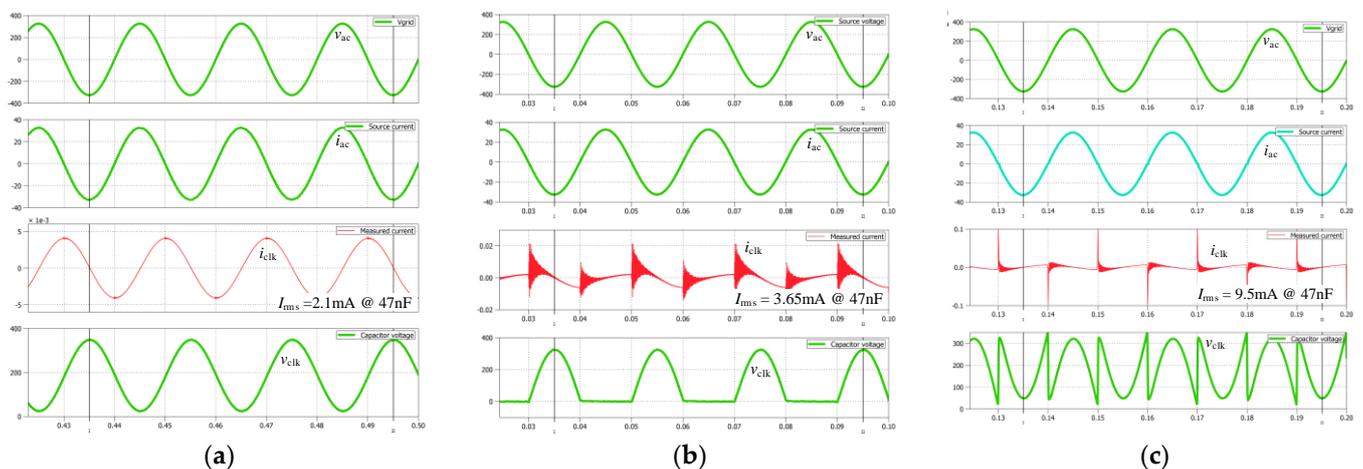


Figure 9. Simulation results of the prior PFCs in [18,26] and the PFC in this paper. (a) Conventional full-bridge PFC with bipolar switching scheme in [18], (b) conventional full-bridge PFC with AVG in [26], and (c) PFC in this paper.

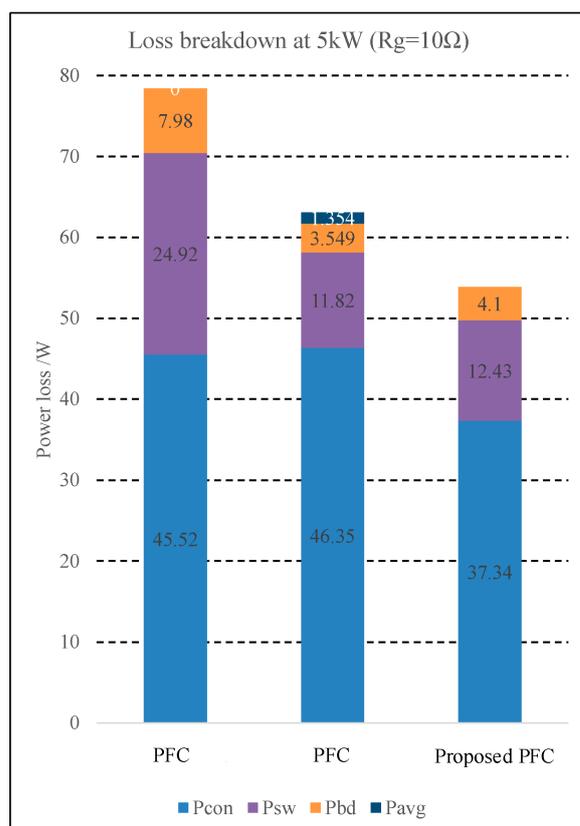


Figure 10. Simulation semiconductor losses of the prior PFCs in [18,26] and the PFC in this paper.

5. Experimental Verification

Experiments of the PFC are implemented on a 5 kW prototype to demonstrate the performance; the design guidelines are provided in Section 4.

Figures 11 and 12 presents the steady-state performances of the PFC under different conditions. Figure 11 presents the experimental results at PFC mode. Figure 12 presents the experimental results at inverter mode. The prototype is tested under grid voltage 230 V and DC voltage 370 V, with power levels of 0.5 kW, 1 kW, 2.5 kW, and 5 kW. In Figures 11 and 12, the grid voltage v_{ac} , the grid current i_{ac} (i_{L2}), the capacitor voltage v_{Cf} , and the inductor current i_{L1} are presented. As seen in Figures 11 and 12, the converter-side inductor current i_{L1} and the grid-side current i_{ac} (i_{L2}) varied under different power level conditions. The voltage on the capacitor C_f changed by V_{dc} when Q_2 and Q_4 switched complementarily according to the polarity of grid voltage. Due to the inserted modulation into the blank time of switches Q_2 and Q_4 , the changing speed of voltage on the capacitor C_f was low, and the spike on the current of inductor L_{f1} was also low. Because the LCL filter was configured at the grid-side, no spike is present on the grid-side current i_{ac} (i_{L2}).

Figure 13 presents the common-mode leakage current performance of the PFC. The prototype is tested under grid voltage 230 V and DC voltage 370 V, with power levels of 0.5 kW, 1 kW, 2.5 kW and 5 kW. In Figure 13, the grid voltage v_{ac} , the grid current i_{ac} (i_{L2}), the capacitor voltage $v_{C_{lk}}$, and the common-mode leakage current $i_{C_{lk}}$ are presented. A 47nF capacitor was used to simulate the stray capacitor [27–29]. The capacitor current $i_{C_{lk}}$ was used to represent the common-mode leakage current. During each half grid cycle, small spikes on the common-mode leakage current appeared during the blank time of low-frequency switches Q_2 and Q_4 . These results prove that the common-mode leakage current was able to be controlled into the mA range, which was accepted by standards.

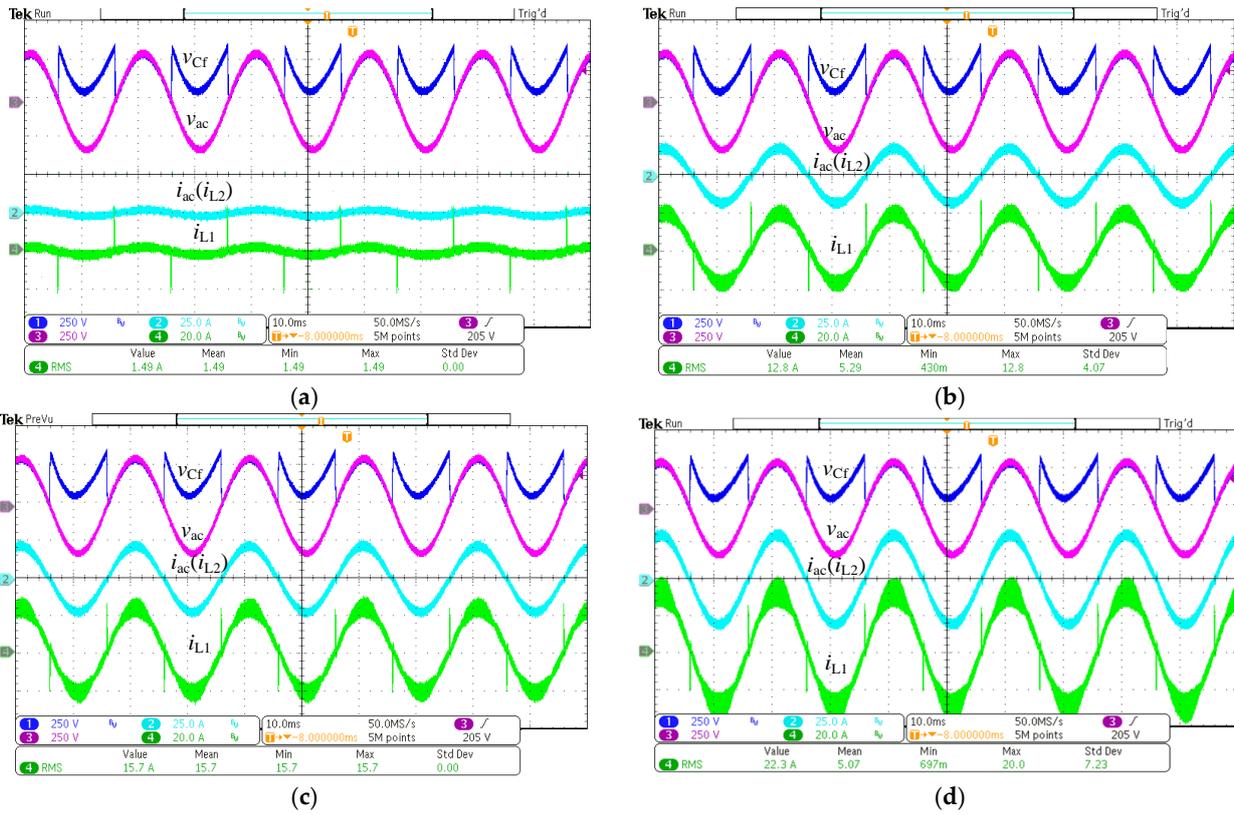


Figure 11. Steady-state waveforms of the PFC at PFC mode. (a) 0.5 kW, (b) 1 kW, (c) 2.5 kW, and (d) 5 kW.

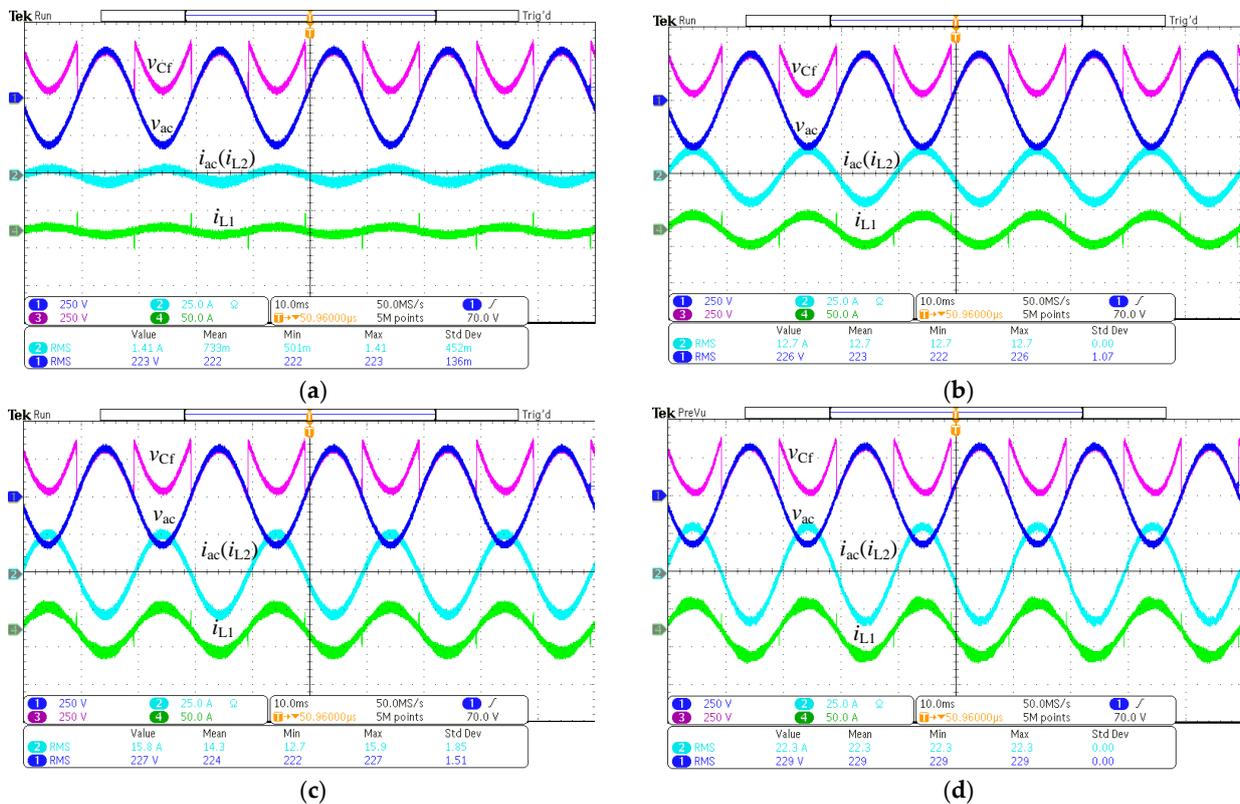


Figure 12. Steady-state waveforms of PFC at Inverter mode. (a) 0.5 kW, (b) 1 kW, (c) 2.5 kW, and (d) 5 kW.

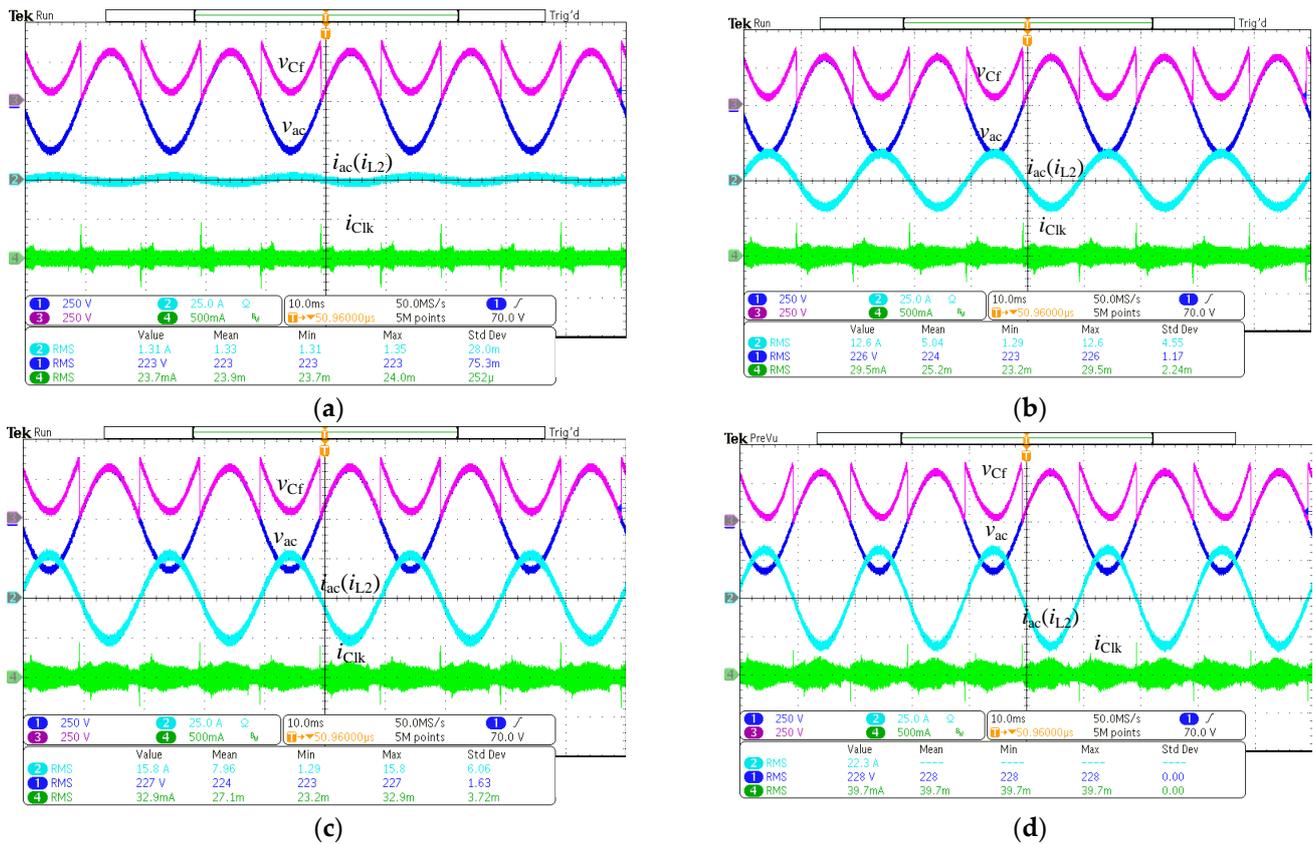


Figure 13. Common leakage current performance of the PFC. (a) 0.5 kW, (b) 1 kW, (c) 2.5 kW, and (d) 5 kW.

Figure 14 presents the experimental efficiency of the PFC. In Figure 14, the power is from 0.2 kW to 5 kW. The lowest efficiency is 94.12% when the power is 0.2 kW. The highest efficiency is 98% when the power is 2 kW. The efficiency of the full power is 97.22%. Additionally, the total harmonics distortion (THD) at different power levels are also attained, as shown in Figure 15, which demonstrates that the THD at 5 kW is less than 2%.

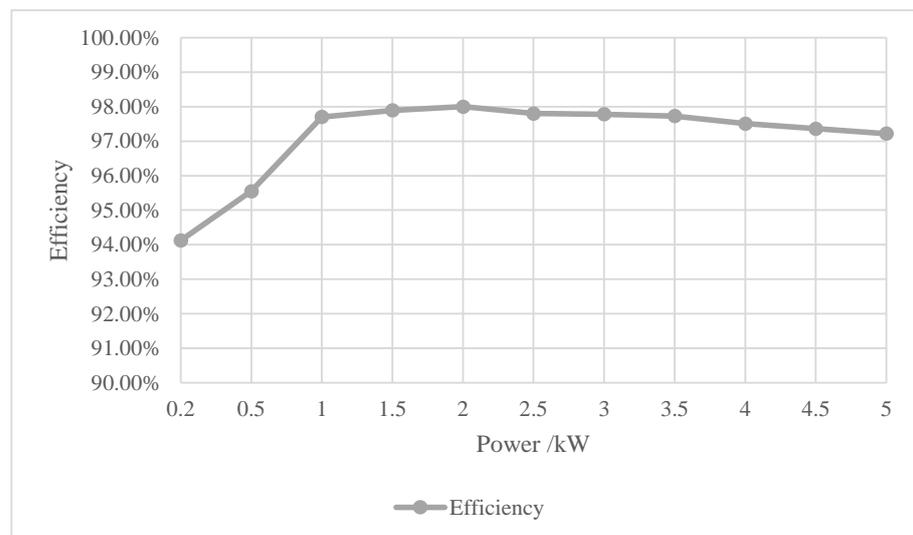


Figure 14. Efficiency of the PFC at different power levels.

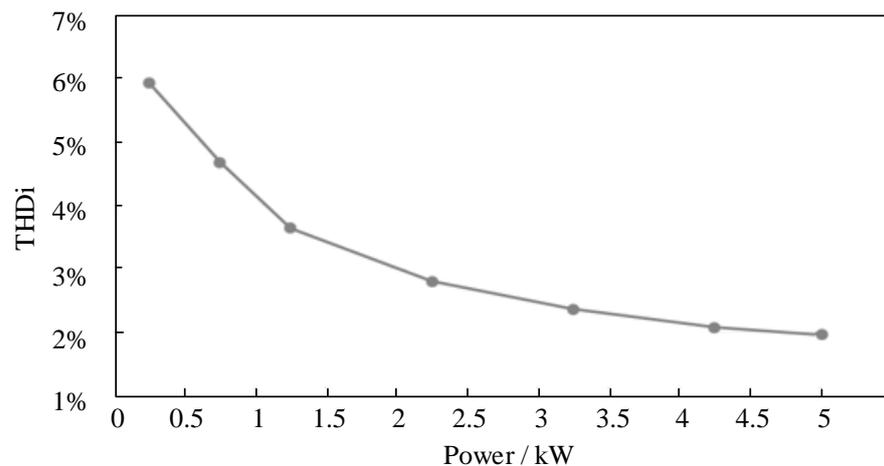


Figure 15. Total harmonics distortion (THD) at different power levels.

6. Conclusions

This paper evaluates a single-phase bidirectional and transformerless PFC associated with hybrid modulation method. This PFC not only mitigates the common-mode leakage current issue, but also builds an LCL filter to reduce the inductor current ripple. A hybrid modulation method is employed in this PFC. The unipolar switching scheme and the addition of another modulation inserted into the blank time of low-frequency switches are combined. This hybrid modulation method guarantees the high efficiency and the suppression effectiveness on the common-mode leakage current. The operating principles of the PFC are analyzed in detail. The performances of the PFC are verified by experiments.

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