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Modular SEPIC-Based Isolated dc–dc Converter with Reduced Voltage Stresses across the Semiconductors

Marcos Vinicius Mosconi Ewerling [1,*], Telles Brunelli Lazzarin [1] and Carlos Henrique Illa Font [2]

[1] Department of Electrical and Electronic Engineering, Federal University of Santa Catarina, Florianopolis 88040-900, Brazil
[2] Department of Electronics Engineering, Federal University of Technology—Parana, Ponta Grossa 84017-220, Brazil
* Correspondence: marcos.ewerling@posgrad.ufsc.br

Abstract: This paper presents the theoretical analysis, experimental results and generalized structure for N modules of an isolated dc–dc SEPIC converter. The structure comes from the integration of N conventional SEPIC converters based on the input-series and output-parallel connection. The main advantages provided by the proposed structure are reduced voltage stress across the semiconductors and division of the current stress in the output diodes. The proposed converter is presented in a generalized approach, varying the voltage stress across the semiconductors according to the number of modules used. As the converter uses more than one switch, the commands can be either equal or phase-shifted by $360°/N$ degrees. When operating with phase-shift modulation, a multilevel converter is obtained, which brings another advantage of the structure, since there is a reduction in the volume of the input inductors (L_{i1} and L_{i2}) and the output capacitor (C_o). In this paper, the steady-state analysis, a dynamic model, system control and experimental results are presented for phase-shift modulation and discontinuous conduction mode (DCM). The performance of the proposed converter was verified in a prototype with four modules and the following specifications: 500 W output power, 800 V input voltage, 120 V output voltage and 50 kHz switching frequency. The converter achieved 94.42% efficiency at rated power.

Keywords: dc–dc SEPIC converter; multilevel; isolated-converter; DCM

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1. Introduction

In recent years, the implementation of dc grids integrated with renewable sources and dc loads has been presented as a new configuration for the grids of the future [1–3]. The power processing in microgrids is managed by converters and, in the case of dc grids, by dc–dc converters, which has significantly increased the demand for new converters [1–3]. The bus voltage of the dc networks is an important parameter, as it determines factors such as losses, isolation, system safety, and, most notably, the voltage levels at which the converters will operate [4]. When a bus voltage of 800 V or more is used, the voltage stresses that the semiconductors will be submitted to must be analyzed carefully because, in some structures, these stresses can be relatively high [5–7]. Studies that relate the viability of a dc system and voltage levels have been reported in [8,9]. Among the various voltage and power levels of a microgrid, there are commercial and residential applications, which include low power loads [9–11].

In many applications, galvanic isolation between the input and output is desirable to isolate the power supply from the load [12]. The challenge of isolated structures is the overvoltage on the semiconductors due to the presence of the leakage inductance, which increases when the transformer turns ratio is different from unity. In order not to oversize the semiconductors, which could generate a decrease in the efficiency of the structure, it is necessary to use a snubber circuit to avoid failures in these semiconductors [13–15]. Thus,

for applications involving input voltage values from 600 to 2000 V, dc–dc converters able to provide reduced stress across the semiconductors are sought.

The literature has presented a significant number of studies for dc–dc step-down converters, mainly isolated buck converters, for a wide range of power and voltage levels [16–18]. The isolated topologies group, such as full-bridge, half-bridge, flyback and forward, can provide output voltages either lower or higher than the input voltage just using the transformers turns ratio. However, once designed as a step-up, the converter will always operate as such, or if it was designed as a step-down, it will just operate as a step-down. Thus, the conventional isolated converters are not suitable for design specifications with a wide input voltage range.

The dc–dc converters operating with high voltage levels (in input and/or output) present challenges in relation to voltage stress on the semiconductors. This challenge is higher for step-down/step-up converters (as SEPIC, Cuk, Zeta, flyback) due to the theoretical maximum voltage across the semiconductor being equal to the sum of input and output voltages. The series connection of components or modules is a method to overcome this challenge, for instance, as in the input-series-output-parallel (ISOP) [19–22], the input-series-output-series (ISOS) [23,24], and the input-parallel-output-series (IPOS) converters [25–27]. However, the literature is lacking solutions using module connection to increase the voltage range of dc–dc step-down/step-up converters, such as SEPIC, which is the focus of this research.

Two other methods that should also be noted are the stacking of a number of converters [28] and low-power multilevel topologies [29]. In the stacking converters, the stacked cells increase or decrease the voltage gain compared to the single converter cell [30]. In [28], a stacked flyback converter operating as a voltage step-down converter is presented. An interesting solution for low-power applications is proposed in [29], which is based on the isolated three-level SEPIC converter. However, the cited paper presents only a brief analysis of the structure and numerical simulation results; i.e., the subject needs to be further explored.

SEPIC converter-derived topologies feature dc current at the input with low ripple [31,32] and output with a voltage source characteristic, and they operate as a step-up/step-down voltage regulator without reversing the polarity of the output voltage. SEPIC structures are widely used in several applications including renewable energy [33,34], battery chargers [35] and LED lighting drivers [36,37], and also to perform power factor correction [38–41].

In the light of the current challenges, this paper presents a multilevel structure based on the isolated SEPIC converter. The structure results from the integration of N SEPIC converters with the output connected in parallel, reducing the voltage stress on the semiconductors. In addition, the reduction of the stresses on the semiconductors allows selecting lower drain-source breakdown voltage components, which are cheaper, present better performance in terms of efficiency, and provide fewer switching problems due to the lower dv/dt. With the characteristics presented, the converter can be used in LED lighting drivers and in dc microgrids with voltages above 400 V. In [42], the structure with two modules was briefly presented. However, the main features and contributions of the structure were not addressed. In this paper, the generalization of the structure, mathematics analysis, and experimental results are presented in detail.

The following sections report the principles of operation, modulation, generalization, design equations, control strategy, dynamic model, prototype, experimental results, comparisons, and conclusions.

2. Generalization of Proposed Converter

The proposed topology is based on the conventional dc–dc SEPIC converter, and it is generated from the inclusion of modules (N), as can be seen in Figure 1. Each module consists of a switch (S), a coupled inductor (L_o) and a diode (D). The input capacitors (C_i) alternate in different configurations, using N capacitors when N is even and $N + 1$ capacitors when N is odd. These capacitors have the function of exchanging energy with

the circuit and not shorting the switches; that is, they are input SEPIC capacitors. The input inductors (L_{i1} and L_{i2}) and the output capacitor (C_o) remain constant, regardless of the number of modules.

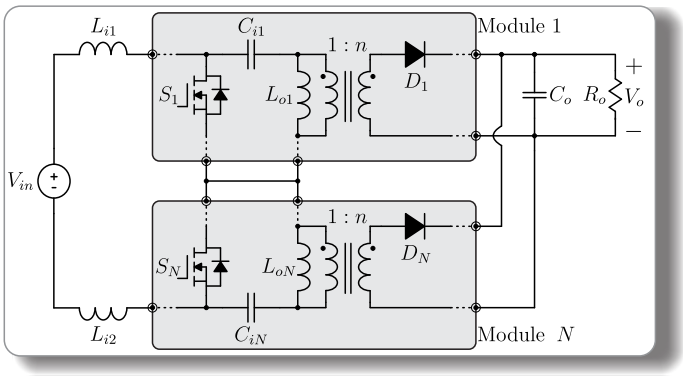


Figure 1. Generalization of the proposed structure.

The proposed integration reduces the voltage stress on the semiconductors, since the input voltage (V_{in}) is divided by the number of modules, as can be seen in

$$V_{Smax} = \frac{V_{in}}{N} + \frac{V_o}{n} \tag{1}$$

and

$$V_{Dmax} = -\left(\frac{V_{in}n}{N} + V_o\right). \tag{2}$$

It should be noted that for the same input and output (V_o) voltage level and a fixed turns ratio (n), the maximum voltage across the switches and diodes decreases with the addition of modules. On the other hand, for the same voltage stress across the switches and diodes, the input or output levels can be increased (mainly the input voltage).

The proposed converter characteristics solve the critical challenge of high-voltage stress on the switch present in conventional SEPIC converters. Thus, components with a lower drain-source breakdown voltage can be selected, reducing the cost of the structure, with better performance in terms of efficiency and less switching problems due to the lower level of operating voltage. In addition, the output of the N-based converters is parallel-connected, allowing division of the current stress in the output diodes.

On the other hand, when the number of modules increases, the number of components will also increase, which is the main drawback of the proposed solution (a typical disadvantage of modular connection). Figure 2a–c show the proposed topology with two (N = 2), three (N = 3) and four (N = 4) modules, respectively.

Table 1 gives the number of components as a function of the number of modules. Analyzing Table 1, it can be seen that regardless of the number of modules used, the number of input inductors and output capacitor remain constant (being equal to one). The switches, diodes and coupled inductors increase as the number of modules increases, as

$$N_S = N_D = N_{Lo} = N, \tag{3}$$

where N_S, N_D and N_{Lo} are the number of switches, diodes and coupled inductors, respectively.

The amount of input capacitors (C_i) increase in a particular way. For N = 1, the converter has one input capacitor (N_{Ci} = 1). When the converter operates with two modules (N = 2), it has two input capacitors (N_{Ci} = 2). In these two situations, the number of input capacitors can be represented by

$$N_{Ci} = N. \tag{4}$$

When the number of modules is greater than or equal to three, two cases must be analyzed: if N is even, the number of input capacitors is given by (4); if N is odd, the number of input capacitors is determined by

$$N_{Ci} = N + 1. \tag{5}$$

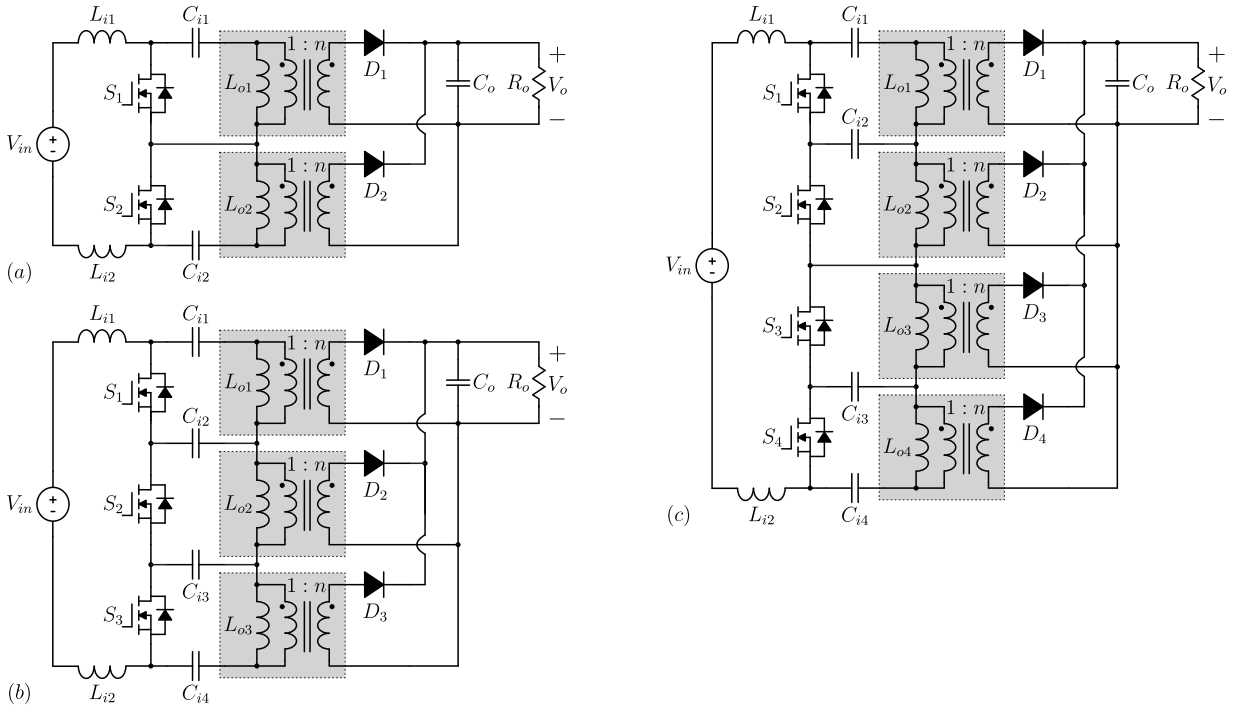


Figure 2. Proposed structure of the dc–dc converter with: (**a**) two modules, (**b**) three modules and (**c**) four modules.

Table 1. Number of components as a function of the number of modules.

Elements	**Number of Elements**					
	N = 1	**N = 2**	**N = 3**	**N = 4**	**N = 5**	**N = 6**
Switches (S)	1	2	3	4	5	6
Diodes (D)	1	2	3	4	5	6
Inductors (L_i)	1	1	1	1	1	1
Inductors (L_o)	1	2	3	4	5	6
Capacitors (C_i)	1	2	4	4	6	6
Capacitors (C_o)	1	1	1	1	1	1
Total	**6**	**10**	**15**	**18**	**23**	**26**

Figure 3 presents an analysis of the parameterized stress across the switches, diodes and capacitors C_{i1} and C_{i2}, as a function of the number of modules. The voltage stress values are given in pu (per-unit), normalized by the input voltage, considering constant output voltage and turns ratio. As the number of modules increases, the stress across the semiconductors will decrease. However, from $N = 4$, the rate of reduction decreases. Therefore, the use of the converter with five or more modules is not attractive, since the number of components increases significantly. The voltage stress on capacitor C_{i1} is equal to the input voltage for the conventional SEPIC converter ($N = 1$) and equal to half the input voltage for the converter operating from two modules. The lowest voltage stress on the capacitor C_{i2} occurs when $N = 3$.

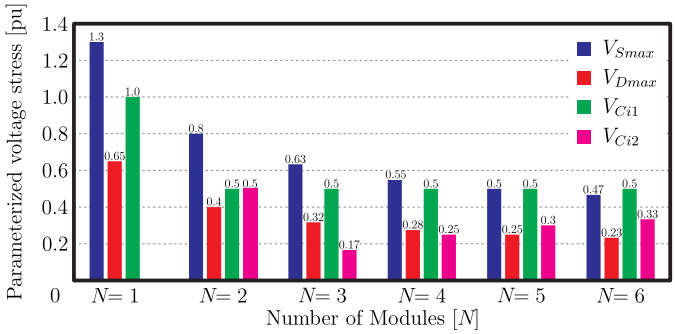


Figure 3. Parameterized voltage stresses across the semiconductors and capacitors C_{i1} and C_{i2}.

As an advantage, the structure is able to keep the voltage stress on the semiconductors inside a range of values when the input voltage increases just by regulating the number of modules. As can be seen in Figure 4, the four-module converter can operate at twice the input voltage compared to the two-module structure for the same values of output voltage and turns ratio.

Another parameter to be analyzed is the static gain. Figure 5 shows the variation of the static gain as a function of the number of modules. It should be noted that the static gain will decrease when the number of modules increases. Thus, the structure operates as a high step-down voltage regulator with less stresses regarding the duty-cycle, voltage and current.

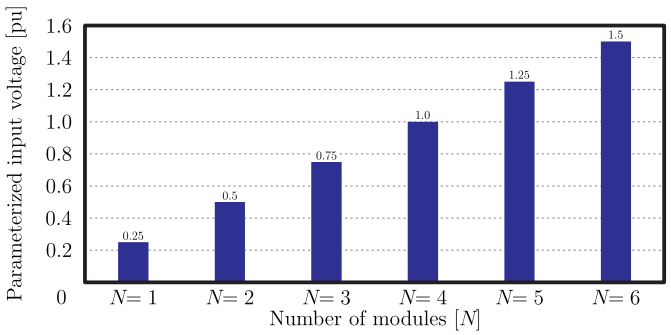


Figure 4. Parameterized input voltage as a function the number of modules.

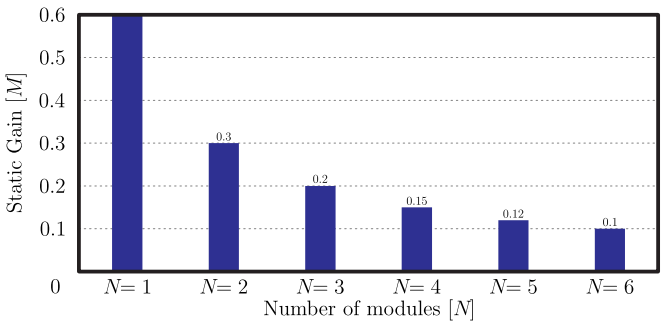


Figure 5. Static gain as a function the number of modules.

2.1. Modulation Strategy

The proposed converter employs two or more switches; thus, two modulation strategies can be used to generate the command signals. In the first modulation strategy, all switches are turned on at the same time, as seen in Figure 6a. The second modulation strategy is detailed in Figure 6b, and it consists of phase-shift modulation in which the number

of modules (N) defines an adequate phase between the carriers (Φ) and, consequently, between the gate signals. The phase-shift value is given by

$$\Phi = \frac{360^\circ}{N}. \tag{6}$$

When the first modulation strategy is used (Figure 6a), the proposed converter behaves similarly to the conventional dc–dc SEPIC converter, containing three operating stages in the discontinuous conduction mode (DCM) operation, regardless of the number of modules. The command signals profile of this modulation is called $M1$. It was briefly analyzed in [42], and the advantage of the converter using this command signal profile is a reduction in voltage stress across the semiconductors.

The second modulation strategy (Figure 6b) provides an isolated multilevel dc–dc SEPIC, which can operate in three different modes called $M2$, $M3$ and $M4$. The operating stages, ideal waveforms, and design equations change in each operation mode. In the DCM operation, the multilevel SEPIC contains $3{\cdot}N$ operating stages, according to the mode used. The advantages of the multilevel converter are reduced voltage stress across the semiconductors and the smaller volume of the inductors (L_{i1} and L_{i2}) and capacitor (C_o). The volume reduction is provided by increasing the operating frequency of these elements, which is proportional to the number of modules used; that is, the volume reduces as the number of modules increases.

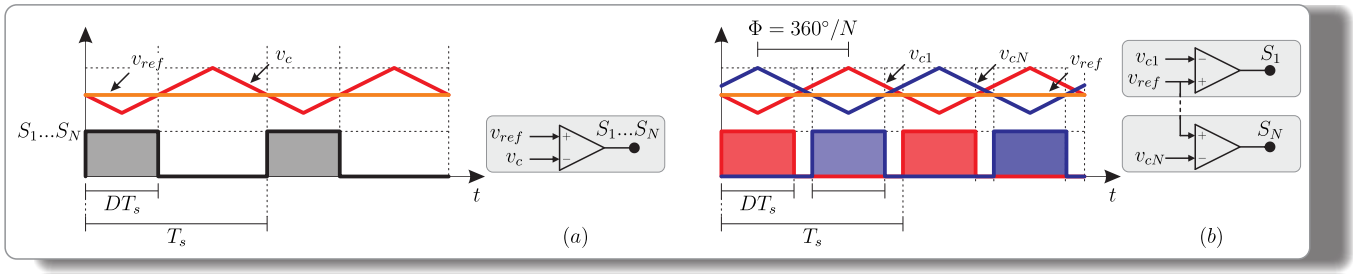


Figure 6. Gate signal profiles for each modulation strategy: (**a**) pulses with the same carrier signal; (**b**) pulses with phase-shifted carriers.

In the $M2$ command signal profile, the converter has an operating restriction related to the maximum duty cycle. In $M3$, the converter presents two operating restrictions in terms of duty cycle: one of them is a minimum value, which defines the border between $M3$ and $M2$ modes, and the other is a maximum value ($1/N$), which is the limit where the pulses do not overlap and is the border between modes $M3$ and $M4$. In $M4$, the converter also presents two operating restrictions in terms of duty cycle: one is the minimum value defined by $1/N$ and the other is the maximum value, which is the border between the DCM and continuous conduction mode (CCM) operation.

Depending on the design specifications selected, the $M2$ and $M4$ restrictions can make applications in these modes unfeasible. In $M2$, the duty cycle values can be very small and, consequently, the converter can operate with high-RMS-current values, increasing the losses (reducing the efficiency). For the $M4$ command signal profile, the range of the duty cycle can be very small, that is, the maximum value of the duty cycle is close to $1/N$ (minimum value).

Considering these factors, the $M1$ and $M3$ modes are more applicable in practical experimentation due to the duty cycle ranges. In $M3$ mode, the converter operates as a multilevel SEPIC, and thus, it was chosen for the study reported in this paper.

2.2. Operation Stages

Operating in DCM with four modules, the converter has twelve operating stages, as seen in Figure 7. However, only the first six operating stages will be described herein, since the next six stages are similar.

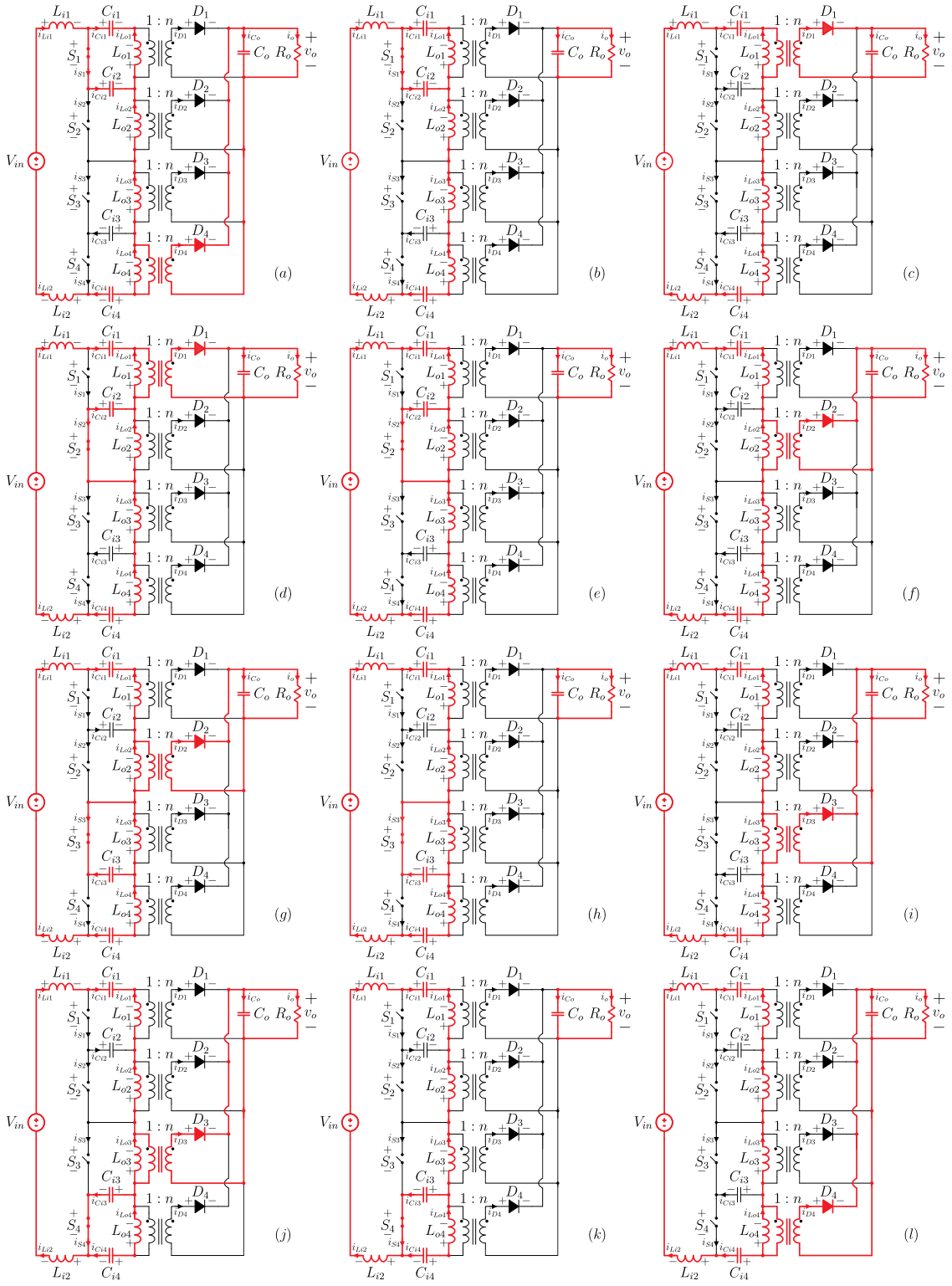


Figure 7. Operating stages for the *M*3 command signal profile with four modules: (**a**) first, (**b**) second, (**c**) third, (**d**) fourth, (**e**) fifth, (**f**) sixth, (**g**) seventh, (**h**) eighth, (**i**) ninth, (**j**) tenth, (**k**) eleventh, and (**l**) twelfth.

In the first operating stage (Figure 7a), S_1 and D_4 are conducting, while S_2, S_3 and S_4 are turned off. The currents in D_2 and D_3 are null, since the currents in L_{o2} and L_{o3} reach the same absolute value as the inductor currents in L_{i1} and L_{i2}. Diode D_1 is reverse-biased. During this stage, the voltage source V_{in}, capacitor C_{i1}, and inductors L_{i1}, L_{i2} and L_{o4} supply energy to the inductor L_{o1}, capacitors C_{i2}, C_{i4} and C_o and the load.

When the current in L_{o4} reaches the same absolute value as the inductor currents L_{i1} and L_{i2}, the forward current in D_4 is null, initializing the second operating stage (Figure 7b). During this stage, the voltage source V_{in} and the capacitor C_{i1} supply energy to L_{i1}, L_{i2}, L_{o1}, C_{i2} and C_{i4}, while the capacitor C_o supplies energy to the load.

The third operating stage (Figure 7c) starts when S_1 is turned off and, consequently, D_1 is forward-biased. In this stage, the voltage source V_{in} and the inductors L_{i1}, L_{i2} and L_{o1} supply energy to C_{i4}, C_o and the load.

In the fourth operating stage (Figure 7d), S_2 is turned on and it conducts together with D_1. Thus, D_2 is reverse-biased. The voltage source V_{in}, C_{i2}, L_{i1}, L_{i2} and L_{o1} supply energy to C_{i1}, C_{i4}, C_o, L_{o2} and the load.

When the current in L_{o1} reaches the same absolute value as the inductor currents of L_{i1} and L_{i2}, the forward current in D_1 is null, initializing the fifth operating stage (Figure 7e). During this stage, the voltage source V_{in} and C_{i2} supply energy to L_{i1}, L_{i2}, L_{o2}, C_{i1} and C_{i4}. The capacitor C_o supplies energy to the load.

The sixth operating stage (Figure 7f) starts when S_2 is turned off and, consequently, D_2 is forward-biased. In this stage, the voltage source V_{in}, L_{i1}, L_{i2} and L_{o2} supply energy to C_{i1}, C_{i4} and the load.

3. Theoretical Analysis

The theoretical analysis of the proposed converter operating in DCM is described in this section. All equations are generalized; that is, they are given in relation to the number of modules. Initially, this section presents the analysis in steady state, aiming at the design of the power components, and finally, the dynamic model is presented, which is employed to designed the controller for the closed-loop operation.

The current stress equations (RMS and mean values) were obtained from the waveforms in Figure 8. Every analysis developed in this section is valid when the input inductors are the same value ($L_{i1} = L_{i2}$) as well as the values of the magnetizing inductance of the coupled inductors ($L_{o1} = L_{o2} = \ldots = L_{oN}$).

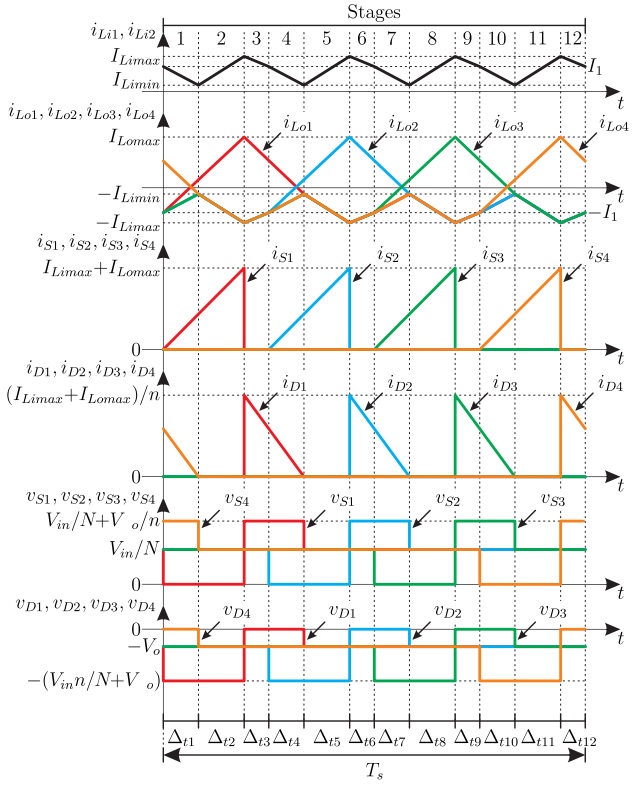


Figure 8. Ideal waveforms for the *M*3 command signal profile with four modules.

3.1. Time Intervals

Based on the operating stages and ideal waveforms, the time intervals of each stage are given by

$$\Delta_{t1} = \Delta_{t4} = \Delta_{t7} = \Delta_{t10} = \frac{V_{in}nD - V_o(1-ND)}{V_oNf_s}, \tag{7}$$

$$\Delta_{t2} = \Delta_{t5} = \Delta_{t8} = \Delta_{t11} = \frac{V_o - V_{in}nD}{V_oNf_s}, \tag{8}$$

and

$$\Delta_{t3} = \Delta_{t6} = \Delta_{t9} = \Delta_{t12} = \frac{1-ND}{Nf_s}, \tag{9}$$

where V_{in} is the input voltage, V_o is the average value of the output voltage, n is the turns ratio, D is the nominal duty cycle and f_s is the switching frequency.

3.2. Static Gain

The static gain (M) is obtained from the equations that represent the output current:

$$I_o = \frac{V_{in}D[2V_{in}nL_iD + V_oL_o(1-ND)]}{4V_onL_iL_of_sN}, \tag{10}$$

and

$$I_o = \frac{V_o}{R_o}. \tag{11}$$

By substituting (10) in (11) and carrying out mathematical operations, the static gain of the proposed converter is found, which is given by

$$M = \frac{V_o}{V_{in}} = \frac{D\left[L_oR_o(1-ND) + \sqrt{2{L_o}^2{R_o}^2 - 4{L_o}^2{R_o}^2ND + 2{L_o}^2{R_o}^2N^2D^2 + 32{L_i}^2L_oR_of_sn^2N}\right]}{8L_iL_of_snN}. \tag{12}$$

3.3. Design of the Inductors L_i and L_o

The input inductances L_{i1} and L_{i2} are defined as a function of the maximum input current ripple (peak-to-peak) during a switching period. Thus, they are given by

$$L_i = L_{i1} = L_{i2} = \frac{V_{in}(V_o - V_{in}nD)}{2V_o\Delta_{iLi}f_sN^2} \tag{13}$$

where Δ_{iLi} is the ripple current in the input inductors.

The magnetizing inductance L_o ($L_{o1} = L_{o2} = \ldots = L_{oN}$) is chosen to guarantee the DCM operation and is defined from the equation of static gain presented in (12). After some mathematical operations, it is found that

$$L_o = \frac{2{V_{in}}^2nD^2L_iR_o}{4{V_o}^2nL_if_sN - V_{in}V_oDR_o(1-ND)}. \tag{14}$$

The equations for the RMS current stress in the input (L_i) and output (L_o) inductors are given by:

$$I_{LiRMS} = \alpha_1 \sqrt{\begin{array}{c} 3{V_o}^2D^3{L_o}^2N^4\left(3{V_o}^2D + 4V_{in}nV_o - 3{V_{in}}^2n^2D\right) + 9{L_o}^2(V_{in}nD - V_o)^4 \\ -6V_{in}nV_oL_oN^3D^2\left[3{V_o}^2\left[D^2(2L_i + L_o) + 2L_o\right] - 8V_{in}nV_oL_oD + 3{V_{in}}^2n^2L_oD^2\right] \\ -3N^2D\left[\begin{array}{c} 6{V_o}^4DL_o{}^2 - 12V_{in}n{V_o}^3L_o{}^2(1+D^2) - 16{V_{in}}^3n^3V_oD^2L_o{}^2 + 3{V_{in}}^4n^4D^3L_o{}^2 \\ -3{V_{in}}^2n^2{V_o}^2D\left[D^2\left(4L_i{}^2 + 4L_iL_o - L_o{}^2\right) - 8L_o{}^2\right] \end{array}\right] \\ +6V_{in}nL_oN(V_{in}nD - V_o)^2\left[V_o\left(D^2(6L_i + 3L_o) - 2L_o\right) + 2V_{in}nDL_o\right] \end{array}}, \tag{15}$$

$$I_{LoRMS} = \alpha_1 \sqrt{\frac{1}{N}\left\{ \begin{array}{l} {L_o}^2 \left[\begin{array}{c} 3{V_{in}}^4 n^4 D^2 \left[4 - 3ND^2(N(N-4)+3) + D(2N(2N-7)+6)\right] \\ -6{V_{in}}^3 n^3 V_o D \left[\begin{array}{c} -ND^2(2N(4N-13)+18) + D(N(6N-19)+9) \\ 4 + 3N^2D^3(N(N-3)+2) \end{array} \right] \\ +3{V_{in}}^2 n^2 {V_o}^2 \left[\begin{array}{c} 4 - 3N^3D^4(N^2-3) + 2N^2D^3(N(8N-19)+6) \\ -2ND^2(2N(6N-17)+21) + 2D(2N(3N-8)+9) \end{array} \right] \\ -6V_{in} n {V_o}^3 (ND-1) \left[\begin{array}{c} 3N^3D^3(N-1) - N^2D^2(N(2N+1)-6) \\ +2ND(2N(N-3)+3) - 2N(N-2) - 3 \end{array} \right] \\ -3{V_o}^4 N(ND-1)^2(3N^2D^2 - 2ND(4N-3) - 4N + 3) \end{array} \right] \\ +12V_{in} n N L_i L_o D^2 \left[\begin{array}{c} {V_{in}}^2 n^2 V_o [2 + (2N-3)(3D(ND-1))] \\ +V_{in} n {V_o}^2 \left[3N^3D^2 + 4N - 6 - ND(10N-9)\right] \\ +3{V_o}^3 N(N(D-2)+1)(ND-1) \\ +{V_{in}}^3 n^3 D(3D(N-1)-2) \end{array} \right] \\ -12{V_{in}}^2 n^2 V_o N^2 {L_i}^2 D^3 [2V_{in} n(3D-2) + V_o N(3D-4)] \end{array} \right\}}, \quad (16)$$

where α_1 is determined by

$$\alpha_1 = \frac{1}{12V_o n L_i L_o f_s N^2}. \quad (17)$$

3.4. Design of the Capacitors C_i and C_o

The capacitances C_i and C_o are designed from the criteria of maximum voltage ripple (peak-to-peak) in the switching period. The input capacitance C_{i1} will always be designed using the equation given by

$$C_{i1} = \frac{\left[\begin{array}{c} 2V_{in} n V_o L_i N D(2-D) + L_o {V_o}^2 \left[N^2 D(D-2) + 2N - 1\right] \\ +{V_{in}}^2 n^2 D^2 L_o (N-1) - V_{in} n V_o D L_o (N-1)(2-ND) \end{array} \right]^2}{32 V_{in} n^2 {V_o}^2 {L_i}^2 L_o {f_s}^2 \Delta_{VCi} N^3} \quad (18)$$

where Δ_{VCi} is the ripple voltage in the input capacitors.

When the converter operates with two modules ($N = 2$), the input capacitor C_{i2} is determined from the same equation as C_{i1}, as described in (18). If the converter operates with three ($N = 3$) or four ($N = 4$) modules, C_{i4} is designed using (18), while C_{i2} and C_{i3} are designed as

$$C_{i3} = \frac{2V_{in} n L_i D^2 + V_o L_o D(1-ND)}{4 L_i L_o n {f_s}^2 \Delta_{VCi} N}. \quad (19)$$

The value of the output capacitor C_o is given by

$$C_o = \frac{V_{in} D (V_{in} n D - 2V_o)^2 [2V_{in} n L_i D + V_o L_o (1-ND)]}{16 {V_o}^3 n L_i L_o {f_s}^2 \Delta_{VCo} N^2} \quad (20)$$

where Δ_{VCo} is the ripple voltage in the output capacitor.

The maximum voltage on the input capacitors is equal to half of the input voltage when the converter operates with two modules (N = 2):

$$V_{Ci1max} = \frac{V_{in}}{2}. \quad (21)$$

When the converter operates with three (N = 3) or four (N = 4) modules, the maximum voltage across the capacitors C_{i1} and C_{i4} is given by (21), while the maximum voltage on capacitors C_{i2} and C_{i3} is

$$V_{Ci2max} = \frac{V_{in}(N-2)}{2N}. \quad (22)$$

The maximum voltage on the output capacitor (C_o) is equal to the output voltage V_o, which can be written as:

$$V_{Comax} = V_o. \tag{23}$$

The RMS values of the current in the input capacitors follow the same logic as the maximum voltage; that is, it depends on the number of modules used. Using two modules (N = 2), the RMS values of current in the capacitors C_{i1} and C_{i2} are given by

$$I_{Ci1RMS} = \alpha_1 \sqrt{3{L_o}^2 \begin{bmatrix} -3D^4\left[{V_o}^2N^2 + (N-1)[V_{in}n(V_{in}n + V_oN)]\right]^2 \\ +D^3\left[8{V_o}^4N^4 + (N-1)\left[\begin{array}{c} 4V_{in}n{V_o}^3N^2(N+3) + 4{V_{in}}^2n^2{V_o}^2N(4N-3) \\ +4{V_{in}}^3n^3V_o(4N-3) + 4{V_{in}}^4n^4 \end{array}\right]\right] \\ -6V_oD^2\left[\begin{array}{c} {V_o}^3N^2(2N-1) \\ +(N-1)\left[V_{in}n{V_o}^2N(2N-1) + {V_{in}}^2n^2V_o(4N-3) + 2{V_{in}}^3n^3\right] \end{array}\right] \\ +12V_{in}n{V_o}^2D(N-1)[V_{in}n + V_o(N-1)] + {V_o}^3[V_o(4N-3) - 4V_{in}n(N-1)] \\ +36V_{in}nV_oNL_iL_oD^2\left[\begin{array}{c} {V_o}^2(2N-1) - 2V_oD\left[V_oN^2 + V_{in}n(N-1)\right] \\ +D^2\left[{V_o}^2N^2 + (N-1)\left(V_{in}nV_oN + {V_{in}}^2n^2\right)\right] \end{array}\right] \\ -12{V_{in}}^2n^2{V_o}^2N^2{L_i}^2D^3(3D-4) \end{bmatrix}}. \tag{24}$$

Operating with three (N = 3) or four (N = 4) modules, the RMS current in capacitors C_{i1} and C_{i4} is obtained from (24), while the RMS current in capacitors C_{i2} and C_{i3} is obtained from

$$I_{Ci2RMS} = \frac{2V_{in}nL_iD + V_oL_o(1-ND)\sqrt{6D}}{6L_iL_onf_sN}. \tag{25}$$

The RMS value of the current in the output capacitor (C_o) is obtained with

$$I_{CoRMS} = \frac{2V_{in}nL_iD + V_oL_o(1-ND)}{12V_onL_iL_of_sN}\sqrt{\frac{3V_{in}D(4V_o - 3V_{in}nD)}{n}}. \tag{26}$$

3.5. Design of the Semiconductors

The switches are chosen from the maximum voltage, described in (1), and the RMS current stress is given by:

$$I_{SRMS} = \frac{2V_{in}nDL_i + V_oL_o(1-ND)\sqrt{3D}}{6L_iL_onf_sN}. \tag{27}$$

The maximum values of the controlled switch currents are determined by:

$$I_{Smax} = \frac{2V_{in}nL_iD + V_oL_o(1-ND)}{2L_iL_onf_sN}. \tag{28}$$

The diodes are designed from the maximum voltage value and its average current. The maximum voltage across the diodes is presented in (2), while the average value of the current is determined by:

$$I_{Davg} = \frac{V_{in}D[2V_{in}nL_iD + V_oL_o(1-ND)]}{4V_onL_iL_of_sN^2}. \tag{29}$$

To calculate the theoretical losses in the diodes, the RMS current equation is used, and its value is defined by

$$I_{DRMS} = \frac{2V_{in}nL_iD + V_oL_o(1-ND)}{6L_iL_onf_sN}\sqrt{\frac{3V_{in}D}{V_onN}}. \tag{30}$$

The maximum values of the diode currents are determined by:

$$I_{Dmax} = \frac{2V_{in}nL_iD + V_oL_o(1-ND)}{2n^2L_iL_of_sN}. \quad (31)$$

3.6. Restriction of Operation

The proposed converter in DCM presents up to three operating restrictions for each command signal profile: one related to the critical resistance and the other two associated with the minimum and maximum duty cycle values. It should be noted that only the critical resistances and the maximum duty cycle values of the *M*1 and *M*4 modes are related to the DCM operation. Other limits only define the command signal profiles. Table 2 details the expressions of the operating restrictions.

Table 2. Operating restrictions for *M*1, *M*2, *M*3 and *M*4.

Mode	Critical Resistance (R_{omin}) [1]	Minimum Duty Cycle (D_{min})	Maximum Duty Cycle (D_{max})
*M*1	$\frac{n\gamma_1}{N(1-D)^2\gamma_2}$	-	$1-\sqrt{\frac{n\gamma_1\gamma_2}{R_oN}}$ [1]
*M*2	$\frac{n\gamma_1}{(1-D)^2\gamma_3}$	-	$\frac{1}{N}-\sqrt{\frac{n\gamma_1\gamma_3}{R_oN}}$
*M*3	$\frac{V_oN\gamma_1}{V_{in}D(1-D)\gamma_3}$	$\frac{1}{N}-\sqrt{\frac{n\gamma_1\gamma_3}{R_oN}}$	$\frac{1}{N}$
*M*4	$\frac{V_oN\gamma_1}{V_{in}D(1-D)\gamma_3}$	$\frac{1}{N}$	$\frac{2V_o}{V_oN+V_{in}n}$ [1]

[1] Operating restrictions related to DCM; $\gamma_1 = 4nL_iL_of_s$; $\gamma_2 = \frac{1}{(2L_i+NL_o)}$; $\gamma_3 = \frac{1}{(2L_i+L_o)}$.

3.7. Control and Dynamic Model

The proposed SEPIC converter in DCM operation requires control of the output voltage [43]. Therefore, the control strategy shown in Figure 9a is used, which employs a single controller. The equivalent circuit shown in Figure 9b is analyzed to derive the dynamic model of the voltage output as a function of the duty cycle.

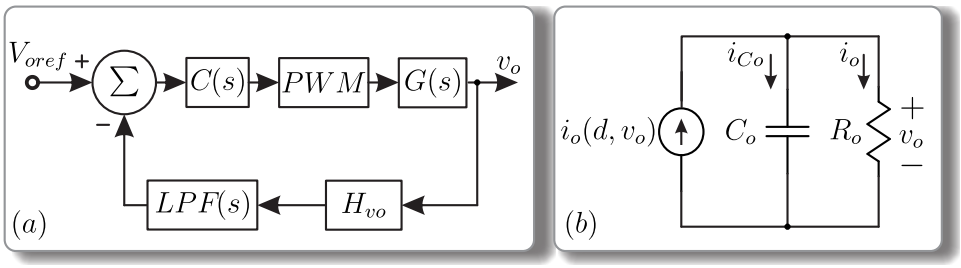


Figure 9. (**a**) Block diagram for output voltage control and (**b**) equivalent circuit for obtaining the dynamic model for output voltage control.

Applying the methodology proposed in [43], the transfer function of the converter to the small signal model is described by

$$TF_{M3} = \frac{\widehat{v}_o(s)}{\widehat{d}(s)} = \frac{\frac{V_{in}{}^2D}{V_oL_oC_oNf_s} + \frac{V_{in}(1-2ND)}{4L_inC_oNf_s}}{s + \frac{V_{in}{}^2D^2}{2V_o{}^2L_oC_oNf_s} + \frac{1}{R_oC_o}}. \quad (32)$$

The small signal model for control was validated by numeric simulation. The specifications used are listed in Tables 3 and 4. During the test, an increase of 2% is applied to the duty cycle at t = 0.092 s and after t = 0.004 s, the value returns to the previous value. The behaviors of the output voltage measured in the converter circuit (v_o) and in the proposed dynamic model (v_{o_TF}) in (32) are shown in Figure 10. The proposed model adequately represents the converter in steady and transient states, as shown by the waveforms.

The use of the proportional–integral (PI) controller is sufficient to maintain the stability of the converter, since the converter operates in DCM and requires only the voltage loop. The PI controller provides null error in steady state for a constant reference. The transfer function of the controller is defined by

$$C(s) = \frac{k_c(s + \omega_z)}{s}. \tag{33}$$

Table 3. Design Specifications.

Specification	Value
Input voltage (V_{in})	800 V
Output power (P_o)	500 W
Output voltage (V_o)	120 V
Duty cycle (D)	0.24
Switching frequency (f_s)	50 kHz
Ripple voltage in capacitors C_{i1} and C_{i4} (Δ_{VCi1})	7%
Ripple voltage in capacitors C_{i2} and C_{i3} (Δ_{VCi2})	14%
Ripple voltage in capacitor C_o (Δ_{VCo})	1%
Ripple current in inductors L_{i1} and L_{i2} (Δ_{iLi})	20%
Maximum snubber voltage ($V_{snubber}$)	550 V

Table 4. List of Components.

Component	Specification
Input inductors (L_{i1} and L_{i2})	L_{i1}: 803.357 µH; L_{i2}: 816.088 µH; Turns: 59; Wire gauge: Litz 22 × 38 AWG; Core: EFD-20/10/07
Coupled inductors ($L_{o1} \ldots L_{o4}$)	L_{o1}: 183.386 µH; L_{o2}: 186.928 µH; L_{o3}: 184.769 µH; L_{o4}: 185.101 µH; L_{k1}: 3.332 µH; L_{k2}: 2.963 µH; L_{k3}: 4.096 µH; L_{k4}: 2.92 µH; n: 0.5; N_p: 24; N_s: 12; Primary winding wire gauge: Litz 26x34 AWG; Secondary winding wire gauge: Litz 32 × 32 AWG; Core: EE 32/16/09-N87-TDK
Switches ($S_1 \ldots S_4$)	IXKH70N60C5 (600 V/70 A/45 mΩ)
Diodes ($D_1 \ldots D_4$)	C3D12065A (650 V/16 A)
Input capacitors (C_{i1} and C_{i4})	360 nF/630 V
Input capacitors (C_{i2} and C_{i3})	470 nF/630 V
Output capacitor (C_o)	9 µF/400 V
Snubber diodes (D_{g1}, D_{g2}, D_{g4}, D_{g5}, D_{g7}, D_{g8}, D_{g10} and D_{11})	MUR4100 (1000 V/4 A)
Snubber diodes (D_{g3}, D_{g6}, D_{g9} and D_{g12})	4D05120A (1200 V/5 A)
Snubber inductors ($L_{g1} \ldots L_{g8}$)	L_{g1}: 573.778 µH; L_{g2}: 568.13 µH; L_{g3}: 578.715 μH; L_{g4}: 567.514 μH; L_{g5}: 576.719 µH; L_{g6}: 573.1 µH; L_{g7}: 574.235 µH; L_{g8}: 571.748 µH; Turns: 88; Wire gauge: Litz 22 × 38 AWG; Core: EE 25/10/06-IP6-Thornton
Snubber capacitors ($C_{g1} \ldots C_{g8}$)	15 nF/1600 V

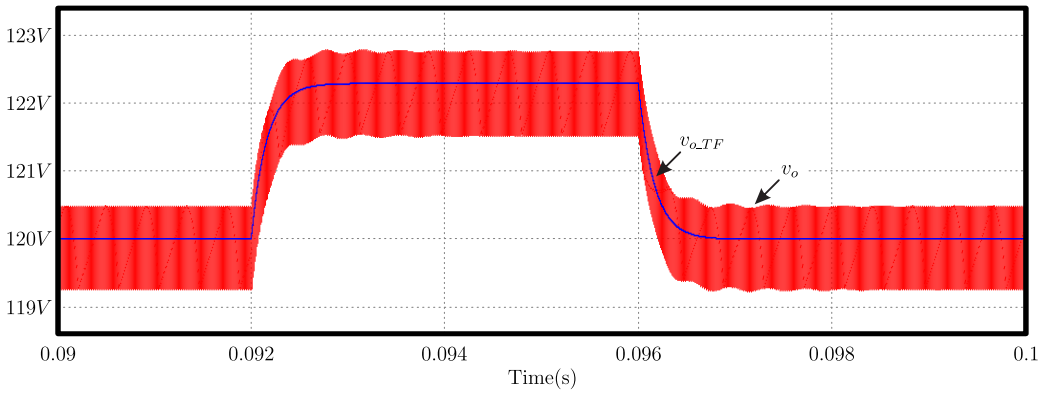


Figure 10. Numerical validation of the transfer function of the proposed converter.

4. Prototype and Experimental Results

A prototype of 800 V/120 V/500 W was built to verify the operation and the theoretical analysis of the proposed converter with four modules [$N = 4$], as depicted in Figure 11. The prototype was designed according to the specifications in Table 3, and the main components are listed in Table 4.

The experimental results reported herein were obtained in closed-loop operation and at rated power (500 W). Waveforms and curves were measured using the Tektronix DPO 5054 oscilloscope and Yokogawa's WT500 power analyzer. The leakage inductance values were acquired using an AGILENT 4294A impedance analyzer.

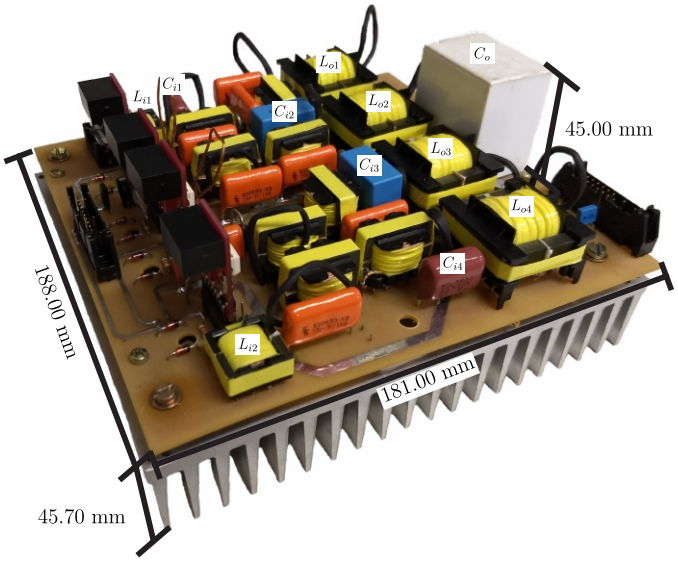


Figure 11. Photograph of the proposed converter with the regenerative snubber cells.

4.1. Design and Prototype Details

As can be seen in Figure 11, four isolated drivers were employed to drive the switches, since they do not have a common reference. To perform the control and generation of command pulses, a digital signal processor (DSP) (model TMS320F28027, Texas Instruments) was used. The controller defined in (33) is designed to allocate the crossover frequency at 100 Hz and the phase margin at 90 degrees, resulting in 30 V (25% of the nominal voltage) overshoot and undershoot for a load increment and load decrement, respectively. In both cases, the settling time was around 3 ms considering the criterion of $\pm 5\%$ of the set point. The Tustin method [44] was used to carry out the discretization of the compensator presented in (33). The sampling frequency used is equal to the switching frequency of the converter.

The $M3$ command signal profile was chosen for the realization of the prototype due to the duty cycle value. In $M2$ and with four modules, the duty cycle value is low (0.12). In $M4$, the minimum duty cycle value (0.25) was very close to the maximum value (0.273). In $M3$, the maximum duty cycle value is 0.25. Therefore, using a duty cycle of 0.24 reduces the maximum and RMS values of the current in the semiconductors and guarantees the DCM operation.

As the proposed converter has high-frequency galvanic isolation, a snubber circuit is needed to prevent overvoltage in the switches, which is caused by the leakage inductance (L_k). Therefore, the passive regenerative snubber circuit proposed in [15] was used. This snubber circuit stores the energy from the leakage inductance, and it transfers part of the energy to the output. In addition, it decreases the switching losses of the switches. As a result, compared to the passive dissipative snubber circuit RCD, the efficiency of the converter increases.

4.2. Experimental Results

The input voltage (v_{in}) and input current (i_{Li1}) (same current in L_{i1}) are presented in Figure 12a. Their respective average values are 798.1 V and 728.5 mA. The input current has high-frequency noise in Figure 12a, which is caused by low SNR (signal-to-noise ratio). The measure uses 400 mA per division for a current probe of 30 A. In addition, a high-frequency resonance between the input inductor and input DC source contributes to this noise. Furthermore, these noises do not interfere with the operation of the converter.

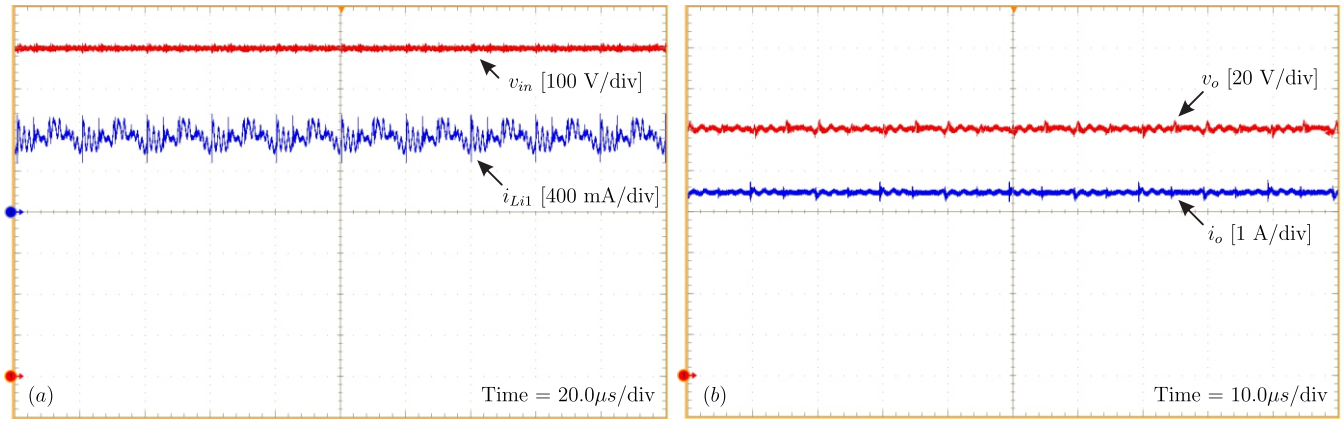


Figure 12. (**a**) Input voltage and current and (**b**) output voltage and current.

Figure 12b shows the experimental waveforms of the output voltage (v_o) and output current (i_o), with average values of 121.46 V and 4.403 A, respectively; i.e., the converter is processing approximately 534.79 W.

The voltages across S_1, S_2, S_3, and S_4 are shown in Figure 13a. The voltages and currents in S_1 and S_2 are seen in Figure 13b. The maximum theoretical voltage across the switches follows the relation given in (1), being equal to 440 V. On analyzing the experimental voltages after switching, these values are found to be: 445.61 V, 453.74 V, 459.49 V, and 410 V at S_1, S_2, S_3 and S_4, respectively (disregarding the switching phenomena). The maximum voltage values for the switches S_1, S_2, S_3 and S_4 are: 520 V, 552 V, 548 V and 504 V, respectively, that is, close to the specified value in the snubber circuit design ($V_{snubber}$ = 550 V). These values are analyzed at the instant the switches are turned off. The maximum and RMS values of the currents are 7.87 A and 2.21 A in S_1 and 8.03 A and 2.26 A in S_2.

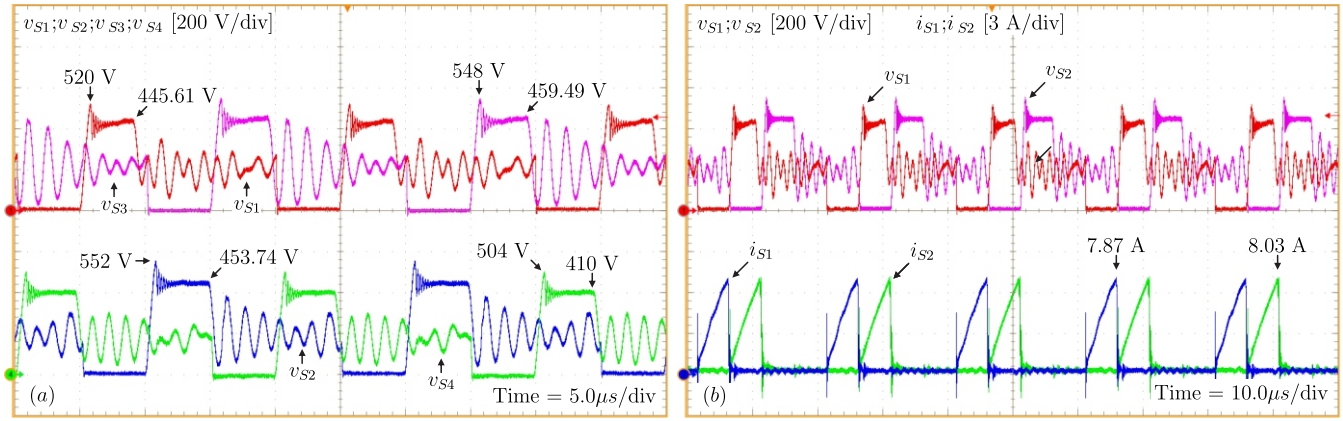


Figure 13. (**a**) Voltages across the switches (S_1, S_2, S_3, and S_4) and (**b**) voltages and currents in switches S_1 and S_2.

DCM operation presents soft commutation naturally when the switches are turned on (current starts from zero each switching period). Additionally, the passive regenerative

snubber provides soft commutation when the switches are turned off [15], as verified in Figure 14a. The oscillations in the waveforms refer to the converter discontinuity stage due to DCM operation.

The voltage waveforms for C_{i1}, C_{i2}, C_{i3} and C_{i4} can be seen in Figure 14b. The theoretical average voltage on C_{i1} and C_{i4} is equal to half the input voltage (400 V), while for C_{i2} and C_{i3}, it follows the relation $V_{in}(N-2)/2N$ (200 V). In the experimental results, the average values for C_{i1} and C_{i4}, respectively, are 401.8 V and 402.2 V, while for C_{i2} and C_{i3}, they are 203.4 V and 207.7 V, respectively.

On analyzing the waveforms for the voltages across D_1, D_2, D_3 and D_4 (Figure 15a) and the voltages and currents in diodes D_1 and D_2 (Figure 15b), it can be observed that the maximum voltages values are: -232 V on D_1, -240 V on D_2, -259.2 V on D_3 and -241.6 V on D_4. The maximum theoretical voltage value is -220 V, according to (2). The maximum and average currents, respectively, are 14.8 A and 1.18 A in diode D_1 and 14.5 A and 1.069 A in D_2. Additionally, the division of the output current between the diodes can be verified through the average current values.

The dynamic responses applying and removing 50% of the load step are shown in Figure 16a,b. When the load is removed, the overshoot is close to 35 V, while the settling time is approximately 4 ms. When the load is added, the undershoot is approximately 29 V and the settling time is close to 4.85 ms. For the settling time, the criterion of $\pm 5\%$ of the set point is considered. Comparing with the results obtained via design (30 V in both cases) and numerical simulation (34.7 V for overshoot and 27.8 V for undershoot), the overshoot and undershoot values were close. With respect to the settling times, the values were slightly different, with the experimental values being approximately 20% longer.

The efficiency curves (theoretical and experimental) obtained for the proposed converter are shown in Figure 17a. The theoretical peak efficiency value was 93.58% at rated power (500 W), while the maximum experimental efficiency was 94.42% at 538 W.

Figure 17b shows the distribution of theoretical losses of the proposed converter (at rated power) with four modules and the regenerative snubber cells. The theoretical analysis shows that most of the losses (59.7%) are concentrated on the semiconductors, while 21.5% relates to passive elements and 18.8% relates to snubber cells. It can be noted that 44.8% (being 43.03% in commutation and 1.77% in conduction) of the losses in semiconductors are in the switches. With an optimized design methodology in the output inductors, the leakage inductance could be lower, which would decrease the losses in the switches and also in the snubber cells. The theoretical losses are calculated based on the methodology from [45–47].

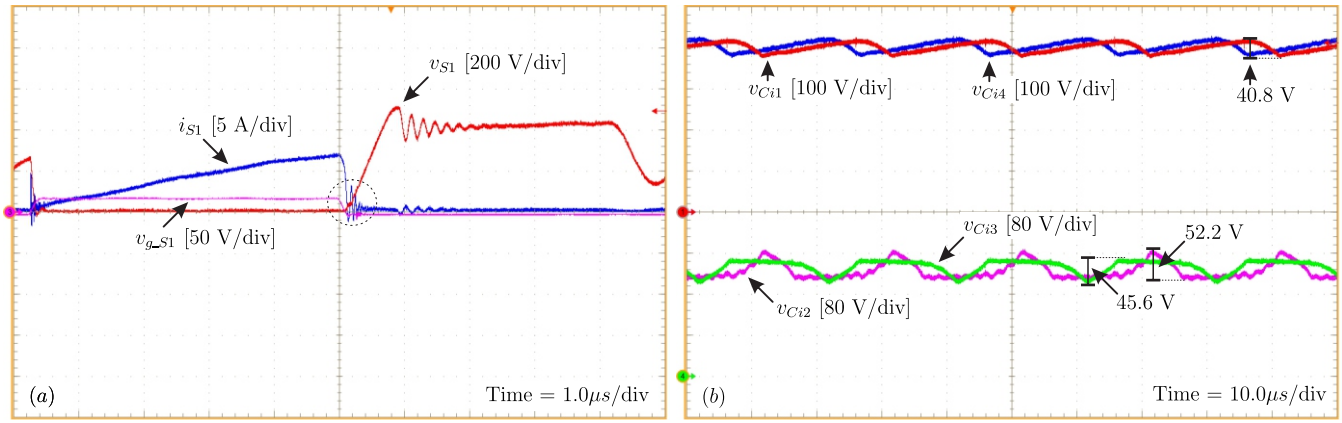


Figure 14. (**a**) Details of switching from switch S_1: voltage, current and pulse, and (**b**) voltage on input capacitors.

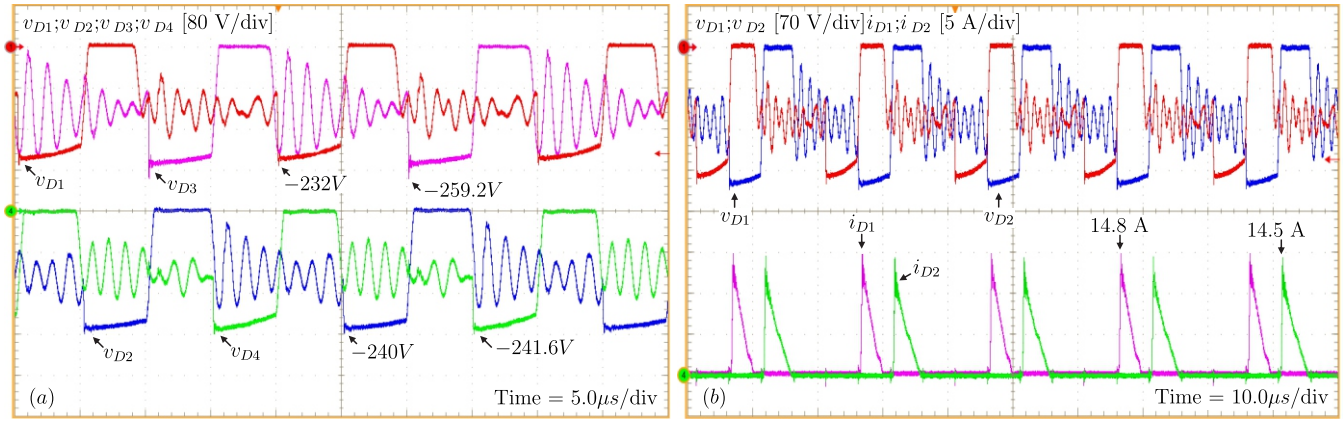


Figure 15. (**a**) Voltage across the output diodes (D_1, D_2, D_3 and D_4) and (**b**) voltage and current in output diodes D_1 and D_2.

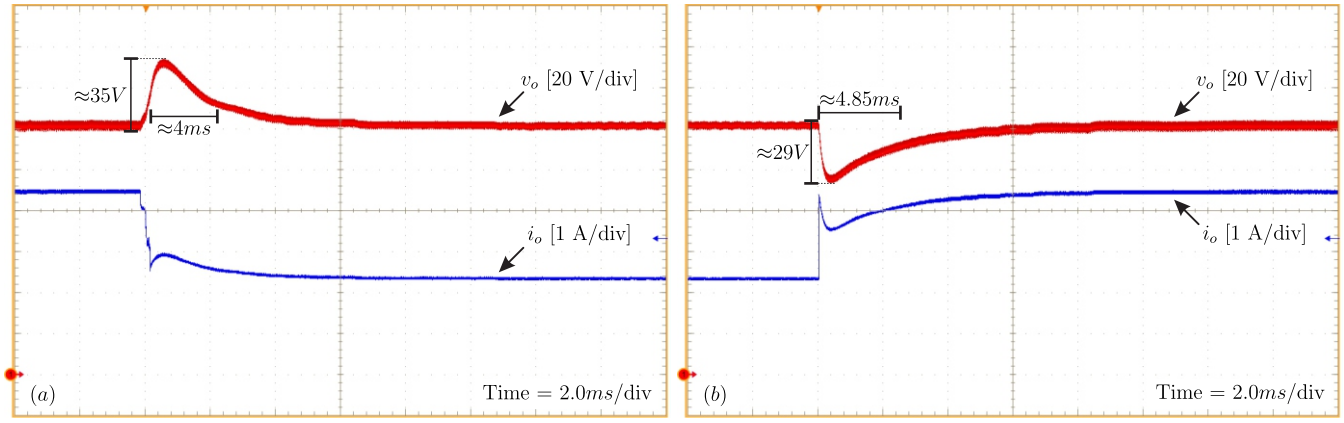


Figure 16. Transient responses of the output voltage and current to: (**a**) a decrease and (**b**) an increase in load.

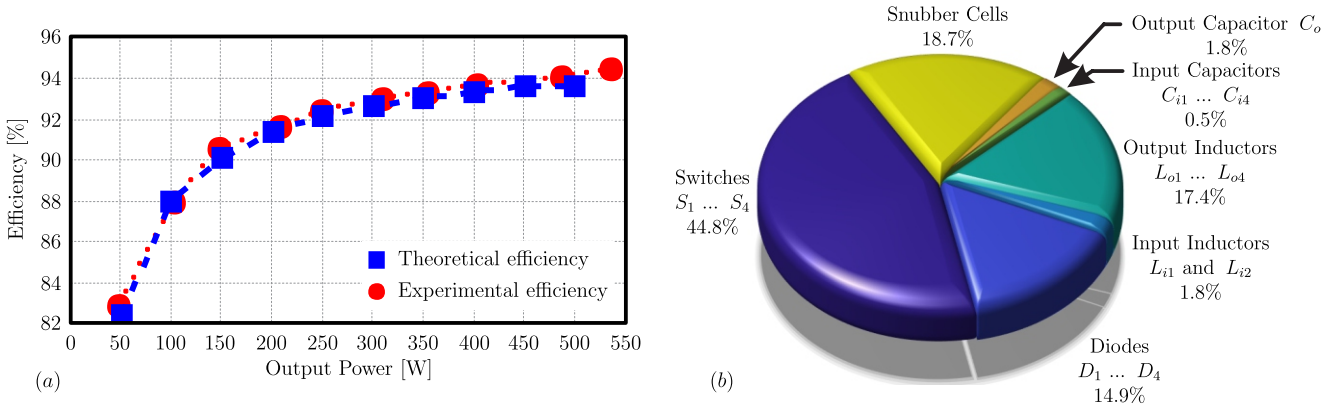


Figure 17. (**a**) Efficiency curves for the proposed converter with four modules and (**b**) distribution of losses for the proposed converter with four modules.

4.3. Comparison

In this section, the proposed multilevel SEPIC converter is compared with the ISOP forward [19], ISOP flyback [22] and ISOS flyback [23] converters operating in DCM and using four modules.

A quantitative comparison in relation to the number of components is given in Table 5. Regarding the differences compared with the ISOP forward [19], the proposed converter has seven, three, and four less inductors, capacitors and diodes, respectively. The proposed converter uses an extra inductor compared to the ISOP flyback [22], but it presents three less capacitors. In relation to the ISOS flyback [23], the proposed converter employs an extra inductor; however, it has three, four, and eight less capacitors, switches and diodes, respectively. It should also be noted that the proposed multilevel SEPIC converter presented in Figure 2c has two inductors at the input (L_{i1} and L_{i2}) that can be integrated into a single inductor, and thus, one of them does not count as an extra element in the quantitative analysis.

The qualitative analysis is reported in Table 6. The values are given in pu (per-unit), each variable being normalized by the respective value in the proposed converter. In relation to the ISOP forward [19], the voltage stresses on the semiconductors are similar for the design specifications used, while the current stresses on the magnetizing inductances and output capacitor are higher and those on other components are lower or equal. In comparison with the ISOP flyback [22], the voltage stresses on the semiconductors are also the same. The current stresses on the input capacitors and the output capacitor are greater. In the rest of the elements, the current stresses are similar. The ISOS flyback described in [23] presents reduced voltage stress across the semiconductors compared to the proposed converter. On the other hand, the current stresses in the magnetizing inductances are doubled, while the average current at the output diodes is four times greater. The current stresses on the input capacitors are lesser.

Table 7 presents a comparison of the experimental parameters of the proposed converter with other solutions. It should be noted that the proposed converter and [19] have a continuous current at the converter input with low ripple, while the converters in [22,23] have pulsed current with high ripple. In relation to the efficiency values, it can be observed that the converters present similar efficiencies, with a difference of 1%, except for the converter presented in [19], which does not show experimental efficiency data. The proposed converter and the converters proposed in [19,23] have lower gains compared to the converter from [22]. Additionally, the proposed converter and proposed in [23] present higher input voltage levels. In relation to the output power, the proposed converter and [19] were tested in similar power, while the converter from [22] operated with lower power level and the converter in [23] operated with higher power level.

In conclusion, the proposed converter has voltage stresses on semiconductors either equal to or similar to the structures presented in [19,22]. The current stresses on the elements of the proposed converter are also similar in comparison to [19,22,23]. The main contribution highlighted by the prototype is a reduction in the number of power components when compared to the structures presented in [19,22,23]. In additional, the proposed converter features continuous current at the input with low ripple, while the converters shown in [22,23] have pulsed current at the input with high ripple.

Table 5. Quantitative Analysis.

Characteristics	Proposed Multilevel SEPIC	ISOP Forward in [19]	ISOP Flyback in [22]	ISOS Flyback in [23]
Number of inductors	1	8	0	0
Number of coupled inductors	4	4	4	4
Number of capacitors	5	8	8	8
Number of switches	4	4	4	8
Number of diodes	4	8	4	12
Number of snubber cells	4	4	4	4

Table 6. Qualitative Analysis.

Characteristics	Proposed Multilevel SEPIC	ISOP Forward in [19]	ISOP Flyback in [22]	ISOS Flyback in [23]
Voltage stress on switches	$\frac{V_{in}}{N} + \frac{V_o}{n}$	$\frac{2V_{in}}{N}$	$\frac{V_{in}}{N} + \frac{V_o}{n}$	$\frac{V_{in}n+V_o}{2Nn}$
Voltage stress on diodes	$\frac{V_{in}n}{N} + V_o$	$\frac{V_{in}n}{N}$	$\frac{V_{in}n}{N} + V_o$	$\frac{V_{in}n+V_o}{N}$
RMS current value in input inductor	1 pu	1.5 pu	-	-
RMS current value in switch	1 pu	1.3 pu	1 pu	1 pu
RMS current value in magnetizing inductance	1 pu	0.5 pu	1 pu	2 pu
Average current value in output diode	1 pu	1 pu	1 pu	4 pu
RMS current value in output capacitor	1 pu	0.5 pu	0.5 pu	1 pu

Table 7. Experimental comparison of proposed converter and other solutions.

Parameter	Proposed Multilevel SEPIC	ISOP Forward in [19]	ISOP Flyback in [22]	ISOS Flyback in [23]
Input current	continuous	continuous	pulsed	pulsed
Δ_{in}	small	small	very high	very high
Frequency	50 kHz	200 kHz	50 kHz	50 kHz
Maximum efficiency	94.42%	-	95.5%	95.2%
Efficiency in full load	94.42%	-	95.3%	94.8%
Rated power	500 W	480 W	200 W	1500 W
Voltage gain	0.15	0.3	1	0.15
v_{in}/v_o (V)	800/120	160/48	200/200	1200/180

5. Conclusions

In this paper, a multilevel SEPIC converter in DCM was proposed, which is obtained from the integration of N conventional SEPIC converters. This integration reduces the voltage stress across the semiconductors and the division of the current stress in the output diodes, since the outputs are connected in parallel. The other components remain with the same current stress, regardless of the number of modules used. The voltage-stress reduction on the switches is the main contribution in relation to the conventional SEPIC, and this feature means that the SEPIC-converter family can be applied with higher input voltages (for instance, the converter can operate in dc microgrids with input voltage at 800 V).

The proposed converter employs N switches, and two different modulation strategies can be used to generate the command signals. The most advantageous modulation strategy is that with the command signals phase-shifted by $360^\circ/N$ degrees, because a multilevel converter is obtained, reducing the volume of the input inductors (L_{i1} and L_{i2}) and the output capacitor (C_o). Another advantage of using the phase-shifted signals ($M3$ and $M4$) is the reduction of the maximum and RMS values of the current in the output capacitor.

The experimental results obtained with the four-module 500 W prototype corroborated the results of the theoretical analysis for the proposed converter. A passive regenerative snubber was added to the circuit due to the leakage inductance of the coupled inductors. The maximum efficiency obtained was 94.42% at rated power (538 W). This efficiency value can be also increased with an optimized design of the output inductors.

In addition, the proposed multilevel dc–dc SEPIC converter can be used for higher voltages using components from lower voltage rates, and it may be applied in a dc microgrid for different levels of the input voltage bus simply by adjusting the number of modules.

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