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Dynamic-State Analysis of Inverter Based on Cascode GaN HEMTs for PV Application

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Abstract: With the increase in renewable energy generation, microgrid has put forward higher requirements on the power density and performance of the photovoltaic inverter. In this paper, the dynamic process of inverter based on the cascode Gallium nitride (GaN) high electron mobility transistor (HEMT) for the photovoltaic (PV) application is analyzed in detail. The parasitic inductors and capacitors have been considered in our proposed equivalent model, which can explain the phenomenon that the crossover time of the voltage and current is prolonged by the parasitic parameters. The influence of the parasitic parameters is identified through theoretical analysis. By analyzing the influence of parasitic parameters, the design process of high-frequency inverter can be optimized. A 500 W inverter based on the cascode GaN HEMT is built, and the correctness of theoretical and simulation analysis is verified by the experimental results.

Keywords: PV; GaN HEMT; cascode; inverter; microgrid

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1. Introduction

The development of microgrids presents the trend of high efficiency and high power density, especially with the increase of renewable energy power generation [1,2]. Nowadays, single-phase photovoltaic (PV) inverters have been widely applied, especially in the Microgrid background. Unlike conventional PV inverters, single-phase PV inverters will most likely reach a high level of efficiency at a low cost, for the single-stage structure without a transformer [3,4]. However, traditional single-phase PV inverters suffer from low power density because of large passive components. The passive components, such as the inductors, have critical effects on the efficiency, performance, and cost of PV inverters [5,6]. Moreover, the switching loss of the power devices has been a bottleneck for further improvements in power density and efficiency. One key issue of high-power density must be solved by increasing the switching frequency. Since the switching frequency of the Si-based inverter normally is limited up to 20 kHz~30 kHz, the passive components are always large so as to reduce the switching loss, which decreases the power density.

The traditional power devices based on Si materials have basically reached their theoretical limits and gradually cannot meet the stringent requirements of the microgrid [7–10]. The emergence of the wide-bandgap device has changed the existing structure of the semiconductor industry and opened a new situation for the semiconductor industry [11,12]. Wide bandgap semiconductors have become ideal substitutes for power converters [13–15]. GaN HEMT devices have excellent electrical and physical properties and huge market potential [16,17]. It has been widely concerned and has been applied in many fields, including DC/AC GaN HEMT-based inverters [18,19], AC/DC GaN HEMT-based PFC circuits [20,21], and DC/DC GaN HEMT-based converters [22–24], etc.

Parasitic inductance is an important parameter of the power device, which has an important influence on the dynamic characteristics of power devices. The most critical parasitic parameter affecting the dynamic performance of devices is the common source inductance (CSI) [25,26]. CSI is defined as the inductance shared by the main power and drive circuit. Recently, the research on parasitic parameters of SiC and GaN HEMT mainly focuses on enhancement types, which are all single switch structures. Their conclusions are similar to those of Si MOSFETs [27]. Because of the special structure of cascode GaN HEMT, its dynamic characteristics are more complex than the enhancement device. At the same time, it is more easily affected by the CSI. Therefore, the dynamic process analysis of cascode GaN HEMT also needs to be analyzed, especially in the application of a high-frequency inverter.

On the other hand, the turn-on and turn-off speed of GaN HEMT devices is significantly higher than that of silicon devices. And the turn-on rate of current can reach 3000 A/us, so the oscillation of voltage and current is easy to occur, especially in the bridge structure [28–31]. In high-power applications, the bridge circuit is one of the most widely used topologies, so the dynamic-state analysis of GaN HEMT in bridge structure needs to be solved urgently [31–33]. The dynamic-state operation mode of the cascode GaN HEMT and its application are important areas that need further research [34–38]. In [4,5], a third-quadrant operation mode of the enhancement GaN HEMT was demonstrated. However, the mechanism of the cascode GaN HEMT is different from either S_i MOSFET or enhancement GaN HEMT. The device characteristics of Cascode GaN HEMT are analyzed in reference [34,35]. Based on the buck circuit, the switching process of cascode GaN HEMT is analyzed and modeled, and an accurate mathematical model is obtained, which provides theoretical support for loss analysis. At the same time, the mathematical model is used to optimize the simulation model to make the simulation model match the experimental results well. The results of this paper are of great significance to the application and loss analysis of GaN HEMT. However, the performance of the freewheeling diode has a great influence on the double pulse test results. Further, the freewheeling diode used is the GaN Schottky diode which has been discontinued by Transphrom Corporation for some reason and cannot be purchased from the market at present. Therefore, in practical applications, users can only select part of the test results for reference. The switching characteristics of cascode GaN HEMT and GaN diodes of 600 V/20 A are tested in reference [36]. On this basis, the mathematical model of GaN HEMT switching loss and reverse recovery charge is given. However, this paper uses a sampling resistor to measure the current, leading to serious distortion of the measured current. The drain current oscillates seriously at turn-on time, which is different from the real situation. The switching characteristics of the cascode GaN HEMT were tested in reference [37,38]. In this paper, the reason for bridge circuit oscillation is analyzed, which provides an important idea for the application of GaN HEMT bridge circuit. However, the layout of the switches is not clear, and the parasitic parameters of the main power layout were not given, so the accuracy of the waveform cannot be ensured.

Cascode GaN HEMT is a typical device for high voltage application of wide-bandgap devices. Its special structure makes the working process of the device more complex than that of traditional S_i MOSFET and the enhancement of GaN HEMT. In this paper, a 600 V cascode GaN HEMT-based inverter for PV application is evaluated. Based on the working process analysis of cascode GaN HEMT, the dynamic process analysis of cascode GaN HEMT based single-phase inverter circuit is presented. In addition, the influence of parasitic parameters is considered in the model, and the key equations of each mode are obtained. Further, the influence of parasitic parameters on the switching process of the switch is discussed. Finally, a 500 W cascode GaN HEMT-based single-phase inverter is established, and experiment results verify the correctness of theoretical and simulation analysis.

2. Characteristic and Model of Cascode GaN HEMT

Cascode GaN HEMT comprises low voltage enhanced silicon MOSFET and high voltage depletion GaN HEMT. The internal structure is shown in Figure 1a, and the equivalent diagram considering parasitic inductors and capacitors is shown in Figure 1b [4], in which the red loop represents the drive circuit of the S_i MOSFET, the bule loop represents the main power loop and the green loop represents the drive loop of GaN HEMT. Because of the complex structure of cascode GaN HEMT, its parasitic parameters are more than that of E-mode GaN HEMT. It includes the parasitic capacitance and inductance in the device and the parasitic inductance in the main power circuit and drive circuit. The parasitic capacitance in the device includes gate-source parasitic capacitance C_{GS_Si}, gate-drain parasitic capacitance C_{GD_Si}, drain-source parasitic capacitance C_{DS_Si} of the low voltage S_i MOSFET and Gate-source parasitic capacitance C_{GS_GaN}, gate-drain parasitic capacitance C_{GD_GaN} and drain-source parasitic capacitance C_{DS_GaN} of high voltage depletion GaN HEMT. The parasitic inductors in the device include L_{int1}, L_{int2}, L_{int3}, and L_S, L_G, and L_D on the pins. It can be seen that for Si MOSFET, L_{int3} and L_S are shared by the S_i MOSFET drive circuit and main power circuit, so L_{int3} and L_S are common source inductors of Si MOSFET. Similarly, for GaN HEMT, the blue loop is still the main power loop, while the drive loop of GaN HEMT is the green loop. Therefore, the common source inductances of GaN HEMT are L_{int3} and L_{int1}. L_{int3} is the common source inductor of GaN HEMT and Si MOSFET, so L_{int3} is the most critical parasitic inductor. The common source inductor of high-voltage GaN HEMT is L_{int1}, which affects the main loss of the switch, and is the second key parasitic inductance. L_S is the third most critical parasitic inductance. Among them, L_{int1}, L_{int2}, and L_{int3} are parasitic parameters inside the device which cannot be tested and changed. Therefore, this paper only considered the effect of L_S in the experiment section.

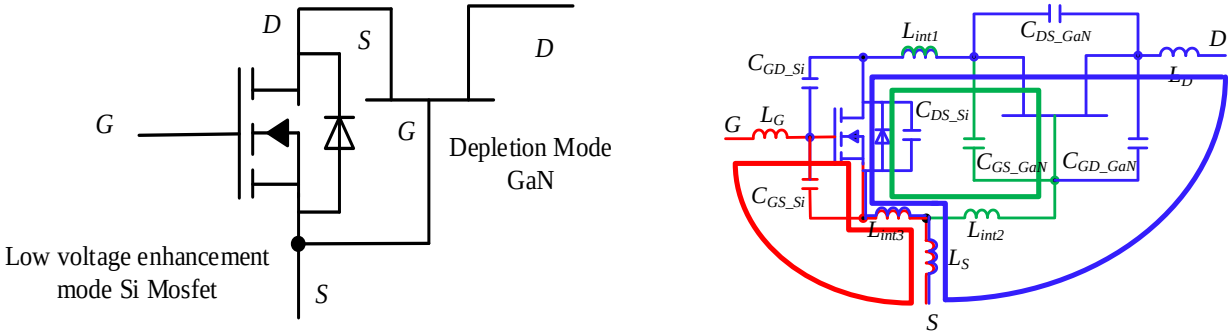
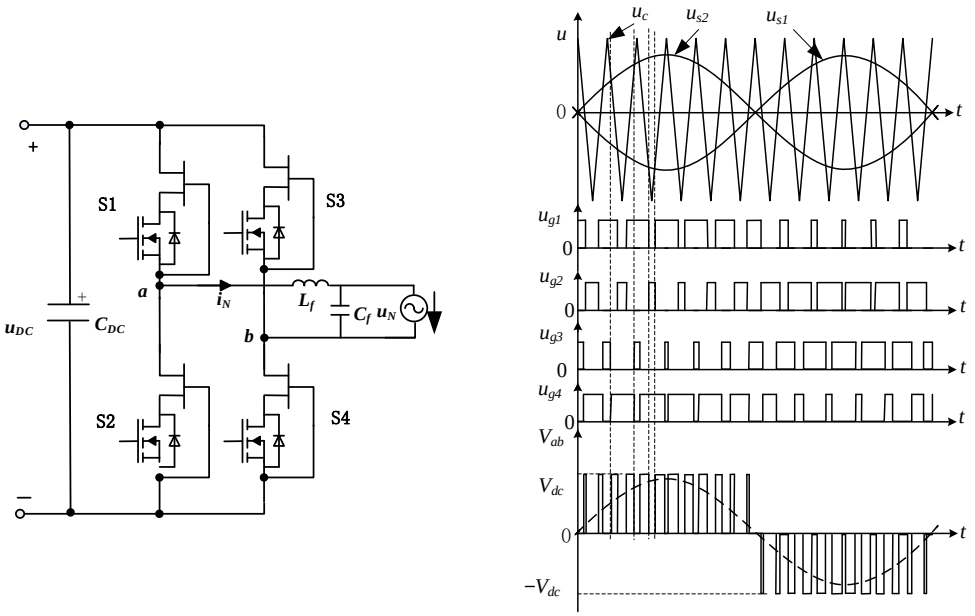


Figure 1. Configuration and equivalent circuit of cascode GaN HEMT. (**a**) The internal structure of the cascode GaN HEMT; (**b**) The equivalent diagram of the cascode GaN HEMT considering the parasitic inductors.

3. Dynamic Analysis of Inverter Based on Cascode GAN HEMT

The cascode GaN HEMT is applied in a single-phase full bridge inverter, and the unipolar SPWM control strategy is adopted, as shown in Figure 2a,b, respectively. The dynamic-state analysis of the cascode GaN HEMT can be distinguished as follows:



(**a**) (**b**)

Figure 2. The topology of the cascode GaN HEMT-based inverter and its control strategy. (**a**) The topology of the cascode GaN HEMT-based inverter; (**b**) The control strategy of the cascode GaN HEMT-based inverter.

3.1. Positive Turn-On Process of the Bridge Leg Switches

Before S_1 turns on, The $v_{gs\_S2} = 0$ and $v_{gs\_S4} = V_G$, and the current is positive, as shown in Figure 2b. The inductance I_L current conducts through S_2 and S_4. The positive turn-on process of cascode GaN HEMT is analyzed as follows.

Stage I: C_{GS1_Si} charged state.

When the gate voltage V_G is applied on S_1, the gate-source equivalent capacitance C_{GS_Si} is charged. As S_1 is turned off, current I_L keeps flowing through S_2 and S_4. This stage ends when $v_{gs1\_Si} = V_{TH\_Si}$. From Figure 3a, the following equations can be obtained:

$$\begin{cases} i_{g\_S1} = C_{GS1\_Si}\frac{dv_{gs1\_Si}}{dt} \\ V_G = (L_{G\_S1} + L_{int3\_S1} + L_{S\_S1})\frac{di_{g\_S1}}{dt} + R_{G\_S1}i_{g\_S1} + v_{gs1\_Si} \end{cases} \tag{1}$$

Stage II: S_i MOSFET drain-source voltage v_{ds1_Si} of S_1 falling stage.

When v_{gs_S1} is equal to V_{TH_Si}, S_i MOSFET of S_1 begins conducting. At this point, C_{GD_Si}, C_{DS_Si}, and C_{GS_GaN} begin to discharge through the channel of Si MOSFET. This stage continues until $v_{gs\_GaN} = V_{TH\_GaN}$. The equivalent circuit of this stage is shown in Figure 3b. The formula for this stage is shown in Equation (2).

$$\begin{cases} V_G = (L_{G\_S1} + L_{int3\_S1} + L_{S\_S1})\frac{di_{g\_S1}}{dt} + R_{G\_S1}i_{g\_S1} + v_{gs1\_Si} \\ i_{g\_S1} = C_{GS1\_Si}\frac{dv_{gs1\_Si}}{dt} + C_{GD1\_Si}\frac{d(v_{gs1\_Si} - v_{ds1\_Si})}{dt} \\ g_{m1\_si}(v_{gs1\_Si} - V_{TH\_Si}) = C_{GD1\_Si}\frac{d(v_{gs1\_Si} - v_{ds1\_Si})}{dt} - (C_{DS1\_Si} + C_{GS1\_GaN})\frac{dv_{ds1\_Si}}{dt} \end{cases} \tag{2}$$

Stage III: i_{ch1_GaN} of S_1 rising stage.

When v_{gs1_GaN} reaches V_{TH_GaN}, the channel of S_1 starts to turn on and equivalent capacitors C_{DS1_GaN} and C_{GD1_GaN} start discharging through the channel of GaN HEMT. It causes v_{ds1_GaN} to fall. As S_2 still conducts, the voltage difference between V_{dc} and v_{ds1_GaN} forces the load current i_L to increase. The equivalent circuit of this stage is shown in Figure 3c. Then, Equation (3) could be derived.

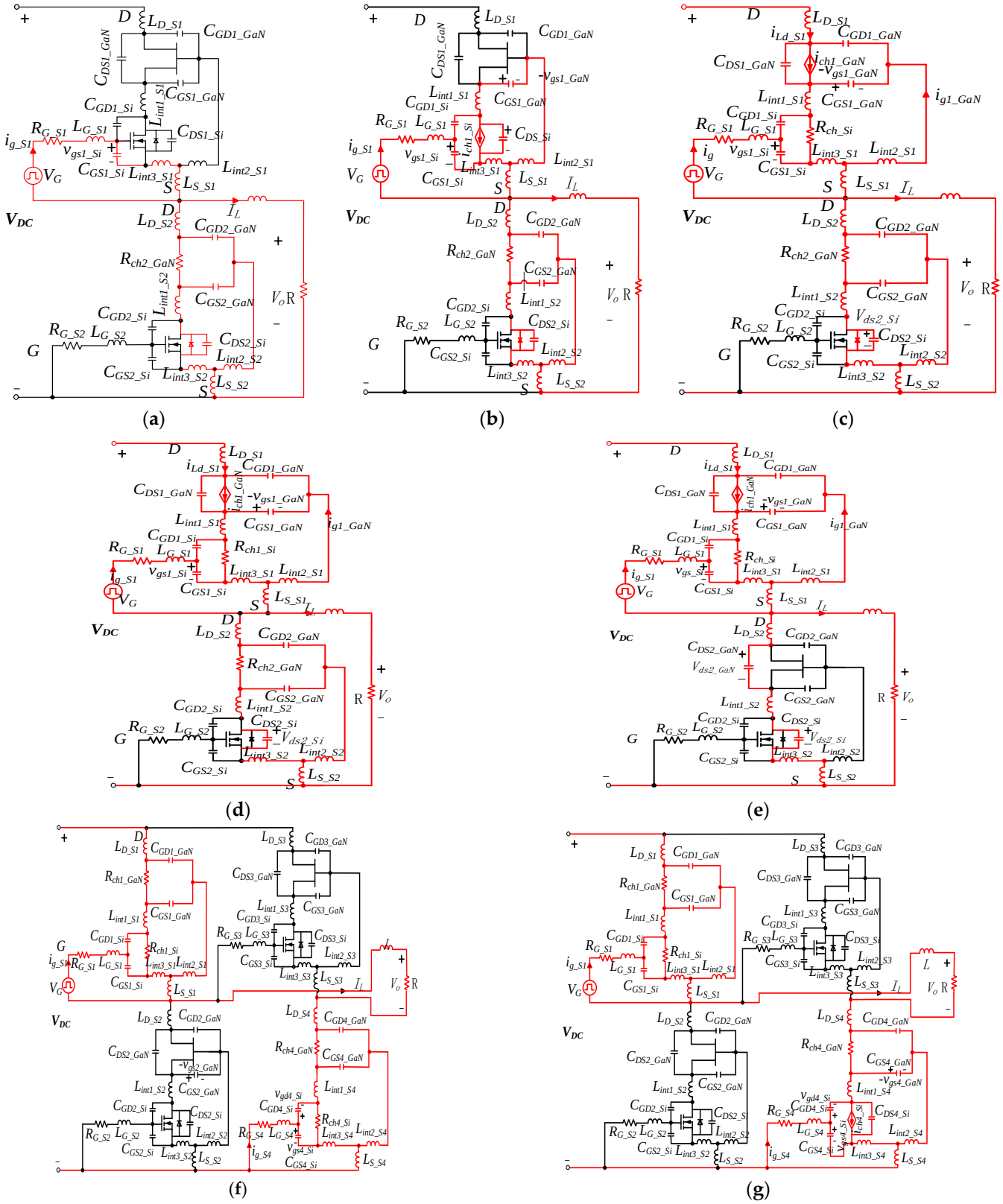


Figure 3. The equivalent circuit of positive turn-on stage and positive turn-off stage. (**a**) Positive turn-on I; (**b**) Positive turn-on II; (**c**) Positive turn-on III and IV; (**d**) Positive turn-on V; (**e**) Positive turn-on VI; (**f**) Positive turn-off I; (**g**) Positive turn-off II.

Stage IV: S_2 MOSFET reverse recovery stage.

When the i_{Ld_S1} reaches I_L, the reverse recovery of S_2 begins. The equivalent circuit and equations are the same as stage III.

Stage V: S_2 GaN HEMT turns off stage.

When the reverse recovery is complete, the voltage v_{ds_S1} rises since the $v_{ds\_S1} < -V_{TH\_GaN}$, the GaN HEMT channel of S_2 turns on. When $v_{ds\_S2} = V_{TH\_GaN}$, this stage ends. The equivalent circuit of this stage is shown in Figure 3d. Then, Equation (4) could be derived.

Stage VI: drain-source voltage of S_2 rising stage.

When $v_{ds\_S2} = V_{TH\_GaN}$, the GaN HEMT channel of S_2 turns off, the equivalent capacitance is charged, and the voltage v_{ds_S2} rises until the voltage v_{ds_S1} decreases to zero, as shown in Figure 3e. Then, Equation (5) could be derived.

$$\begin{cases} v_{gs1\_GaN}+(L_{int1\_S1}+L_{int2\_S1}+L_{int3\_S1})\frac{di_{g1\_GaN}}{dt}+(L_{int1\_S1}+L_{int3\_S1})\frac{di_{Ld\_S1}}{dt}+R_{ch1\_Si}(i_{g1\_GaN}+i_{Ld\_S1})=0 \\ i_{g1\_GaN}=C_{GS1\_GaN}\frac{dv_{gs1\_GaN}}{dt}+C_{GD1\_GaN}\frac{d(v_{gs1\_GaN}-v_{ds1\_GaN})}{dt} \\ g_{m1\_GaN}(v_{gs1\_GaN}-V_{TH\_GaN})=C_{GD1\_GaN}\frac{d(v_{gs1\_GaN}-v_{ds1\_GaN})}{dt}+C_{DS1\_GaN}\frac{dv_{ds1\_GaN}}{dt}+i_{Ld\_S1} \\ V_{dc}=(L_{D\_S1}+L_{S\_S1}+L_{int1\_S1}+L_{int3\_S1})\frac{di_{Ld\_S1}}{dt}+(L_{int1\_S1}+L_{int3\_S1})\frac{di_{g1\_GaN}}{dt}+v_{ds1\_GaN}+R_{ch1\_Si}(i_{g1\_GaN}+i_{Ld\_S1}) \end{cases} \tag{3}$$

$$\begin{cases} V_{dc}=(L_{D\_S1}+L_{S\_S1}+L_{int1\_S1}+L_{int3\_S1})\frac{di_{Ld\_S1}}{dt}+(L_{int1\_S1}+L_{int3\_S1})\frac{di_{g1\_GaN}}{dt} \\ +C_{ds2\_Si}R_{ch2\_GaN}\frac{dv_{ds2\_Si}}{dt}+v_{ds1\_GaN}+R_{ch1\_Si}(i_{g1\_GaN}+i_{Ld\_S1})+v_{ds2\_Si} \\ i_{Ld1}=I_L+C_{ds2\_Si}\frac{dv_{ds2\_Si}}{dt} \end{cases} \tag{4}$$

$$\begin{cases} i_{Ld\_S1}=I_L+(C_{DS2\_Si}+C_{DS2\_GaN})\frac{dv_{ds2}}{dt} \\ V_{dc}=(L_{D\_S1}+L_{S\_S1}+L_{int1\_S1}+L_{int3\_S1})\frac{di_{Ld\_S1}}{dt}+(L_{int1\_S1}+L_{int3\_S1})\frac{di_{g1\_GaN}}{dt}+v_{ds1\_GaN}+R_{ch1\_Si}(i_{g\_GaN}+i_{Ld})+v_{ds2} \end{cases} \tag{5}$$

3.2. Positive Turn-off Process of the Bridge Leg Switches

Before S_4 turns off, $v_{gs\_S1} = v_{gs\_S4} = V_G$, and the current is positive. The positive turn-off process of S_4 is analyzed as follows.

Stage I: C_{GS4_Si} discharged stage.

As the gate voltage V_G of S_4 falls to zero, the equivalent capacitor C_{GS4_Si} of S_4 is discharged. The equivalent circuit of this stage is shown in Figure 3f. When the S_i MOSFET enters the amplification region and satisfies the requirements of G_{Si} $(v_{gs\_Si} - V_{TH\_Si}) = I_L$, this stage ends. The key formula for this stage is shown in Equation (6).

$$\begin{cases} i_{g\_S4}=(C_{GS4\_Si}+C_{GD4\_Si})dv_{gs4\_Si}/dt \\ (L_{G\_S4}+L_{S\_S4})di_{g\_S4}/dt+R_{G\_S4}i_{g\_S4}+v_{gs4\_Si}=0 \end{cases} \tag{6}$$

Stage II: v_{ds4_Si} of S_4 rising stage.

As v_{gs4_Si} continues to decrease, the channel current of S_i MOSFET is controlled by transfer characteristics, which is less than I_L. The excess current charges the drain-source equivalent capacitors, and v_{ds4_Si} increases. Because C_{DS4_Si} is in parallel with C_{GS4_GaN}, v_{gs4_GaN} decreases. The equivalent circuit of this stage is shown in Figure 3g, and the key formula for this stage is shown in Equation (7). This stage ends when the GaN HEMT of S_4 enters the saturation region.

Stage III: Channel current of S_4 decreasing stage.

As the GaN HEMT gate-source voltage of S_4 continues to decrease, the GaN HEMT channel saturation current of S_4 is less than I_L. The excess current charges drain-source equivalent capacitors and v_{ds4_GaN} increases. This stage ends when the channel of depletion GaN HEMT is completely closed, as shown in Figure 4a. The key formula for this stage is shown in Equation (8).

Figure 4. The equivalent circuit of positive tun-off, reverse turn-on, and reverse turn-off stage. (**a**) Positive turn-off III; (**b**) Positive turn-off IV; (**c**) Reverse turn-on state I; (**d**) Reverse turn-on state II; (**e**) Positive turn-on VI; (**f**) Reverse turn-off state I; (**g**) Reverse turn-off state II; (**h**) Reverse turn-off state III.

Stage IV: The drain-source voltage of the S_4 rising stage.

After the v_{gs4_GaN} dropping below the threshold value of GaN HEMT, S_4 totally turns off. The junction capacitors of S_4 are charged by i_{LD_S4}, then the drain-source voltage of S_4

increases, as shown in Figure 4b. This stage ends when the drain-source voltage of S_3 falls to a threshold value of GaN HEMT. The formula for this stage is shown in Equation (9).

Stage V: The GaN HEMT channel of the S_3 conducting stage.

After the drain-source voltage of S_3 is smaller than the threshold value of GaN HEMT, the GaN HEMT channel of S_3 turns on. The drain-source voltage of S_3 continues to reduce. This stage ends when the MOSFET body diode of S_3 is forward-biased. Thus, inductor current flows through S_3, as shown in Figure 4c, and the formula is the same as stage IV.

$$\begin{cases} (L_{G\_S4} + L_{S\_S4})di_{g\_S4}/dt + R_{G\_S4}i_{g\_S4} + v_{gs4\_Si} = 0 \\ i_{g\_S4} = C_{GS4\_Si}dv_{gs4\_Si}/dt + C_{GD4\_Si}d(v_{gs4\_Si} + v_{ds4\_Si})/dt \\ g_{m4\_Si}(v_{gs4\_Si} - V_{TH\_Si}) = C_{GD4\_Si}\frac{d(v_{gs4\_Si} - v_{ds4\_Si})}{dt} - (C_{DS4\_Si} + C_{GS4\_GaN})\frac{dv_{ds4\_Si}}{dt} + I_L \end{cases} \tag{7}$$

$$\begin{cases} i_{Ld\_S4} = I_L + (C_{DS3\_GaN} + C_{DS3\_Si})dv_{ds\_S3}/dt \\ (L_{D\_S4} + L_{S\_S4} + L_{int1\_S4} + L_{int3\_S4})di_{Ld\_S4}/dt + v_{ds4\_GaN} - v_{gs4\_GaN} + v_{ds\_S3} = V_{dc} \\ i_{Ld\_S4} = -(C_{GS4\_GaN} + C_{DS4\_Si} + C_{GD4\_Si})dv_{gs4\_GaN}/dt - C_{GD4\_GaN}d(v_{gs4\_GaN} - v_{ds4\_GaN})/dt \\ g_{m4\_GaN}(v_{gs4\_GaN} - V_{TH\_GaN}) = C_{GD4\_GaN}d(v_{gs4\_GaN} - v_{ds4\_GaN})/dt - C_{DS4\_GaN}dv_{ds4\_GaN}/dt + i_{Ld\_S4} \end{cases} \tag{8}$$

$$\begin{cases} (C_{GS4\_GaN} + C_{DS4\_Si} + C_{GD4\_Si}//C_{GS4\_Si})dv_{ds4\_Si}/dt = C_{DS4\_GaN}dv_{ds4\_GaN}/dt \\ i_{Ld\_S4} = C_{GD4\_GaN}d(v_{ds4\_GaN} + v_{ds4\_Si})/dt + C_{DS4\_GaN}dv_{ds4\_GaN}/dt \end{cases} \tag{9}$$

3.3. Reverse Turn-on Process of the Bridge Leg Switches

Before $v_{gs\_S3} = V_G$, the $v_{gs\_S1} = V_G$. The current is positive, flowing through S_1 and S_3. The reverse turn-on process is analyzed as follows.

Stage I: C_{GS3_Si} charged stage.

This stage is the same as the C_{GS1_Si} charged period, as shown in Figure 4d. Then, the equations could be derived as follow.

$$\begin{cases} V_G = (L_{G\_S3} + L_{int3\_S3} + L_{S\_S3})di_{g\_S3}/dt + R_{G\_S3}i_{g\_S3} + v_{gs3\_Si} \\ i_{g\_S3} = C_{GS3\_Si}dv_{gs3\_Si}/dt \end{cases} \tag{10}$$

Stage II: the MOSFET channel of S_3 conducting stage.

Since S_3 is in the freewheeling state, the GaN HEMT of S_3 is totally turned on. When the $v_{gs\_S3} > V_{TH\_Si}$, the channel of S_3 is totally turned on. I_L transfers from MOSFET's body diode to the MOSFET's channel, as shown in Figure 4e.

3.4. Reverse Turn-Off Process of the Bridge Leg Switches

Before $v_{gs\_S3} = 0$, the $v_{gs\_S1} = v_{gs\_S3} = V_G$. The current is positive, flowing through S_1 and S_3. The channel turning off transition of S_3 can be divided into three stages as follow:

Stage I: C_{GS3_Si} discharged stage.

This stage is the same as the C_{GS4_Si} discharged state, as shown in Figure 4f. Then, Equation (11) could be derived.

$$\begin{cases} (L_{G\_S3} + L_{S\_S3})di_{g\_S3}/dt + R_{G\_S3}i_{g\_S3} + v_{gs3\_Si} = 0 \\ i_{g\_S3} = (C_{GS3\_Si} + C_{GD3\_Si})dv_{gs3\_Si}/dt \end{cases} \tag{11}$$

Stage II: The v_{ds3_Si} of S_3 rising stage.

This stage is the same as the v_{ds4_Si} of the S_4 rising stage. This stage ends when v_{ds4_Si} rises to diode forward voltage V_F, as shown in Figure 4g. Then, Equation (12) could be derived.

Stage III: MOSFET body diode of S_3 conducting stage.

When v_{ds4_Si} rises to diode forward voltage V_F, the MOSFET body diode of S_3 is forward-biased, and the inductor current IL transfers from the MOSFET channel to the MOSFET body diode. This stage ends when the S_i MOSFET channel of S_3 totally shuts down, as shown in Figure 4h. Thus, Equation (13) could be calculated.

As we can see from the theoretical analysis, the parasitic parameters influence the dynamics to the state of the switching state. The main switching waveforms of the cascode GaN HEMT-based single-phase inverter is shown in Figure 5.

$$\begin{cases} i_{g\_S3} = C_{GS3\_Si} dv_{gs3\_Si}/dt + C_{GD3\_Si} d(v_{gs3\_Si} + v_{ds3\_Si})/dt \\ (L_{G\_S3} + L_{S\_S3}) di_{g\_S3}/dt + R_{G\_S3} i_{g\_S3} + v_{gs3\_Si} = 0 \\ g_{m3\_Si}(v_{gs3\_Si} - V_{TH\_Si}) = C_{GD3\_Si} d(v_{gs3\_Si} - v_{ds3\_Si})/dt - (C_{DS3\_Si} + C_{GS3\_GaN}) dv_{ds3\_Si}/dt + I_L \end{cases} \tag{12}$$

$$\begin{cases} v_{ds3\_Si} = V_F \\ (L_{G\_S3} + L_{S\_S3}) di_{g\_S3}/dt + R_{G\_S3} i_{g\_S3} + v_{gs3\_Si} = 0 \\ i_{g\_S3} = C_{GS3\_Si} dv_{gs3\_Si}/dt + C_{GD3\_Si} d(v_{gs3\_Si} + v_{ds3\_Si})/dt \\ g_{m3\_Si}(v_{gs3\_Si} - V_{TH\_Si}) = C_{GD3\_Si} d(v_{gs3\_Si} + v_{ds3\_Si})/dt - (C_{DS3\_Si} + C_{GS3\_GaN}) dv_{ds3\_Si}/dt - i_{D3\_Si} + I_L \end{cases} \tag{13}$$

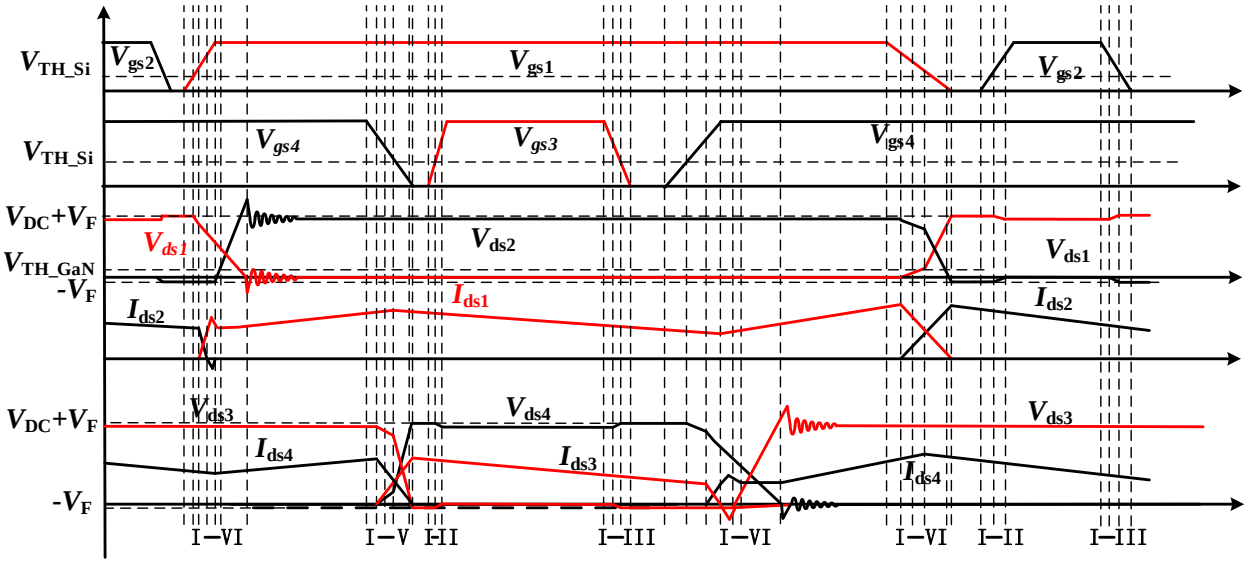


Figure 5. Main switching waveforms of cascode GaN HEMT-based inverter.

4. Simulation and Experimental Verifications

The single-phase inverter circuit base on cascode GaN HEMTs is simulated and verified using LTSpice. The simulation conditions are V_{in} = 380 V, V_o = 220 V, P_o = 500 W. The working waveforms of cascode GaN HEMT are shown in Figure 6a. In addition, the simulation results of drain-source voltage waveforms are shown in Figure 6b,c with parasitic parameters L_S = 5 nH and L_S = 20 nH, respectively. As we can see, the voltage spike of GaN HEMT is larger with the increase of L_S.

A 500 W prototype was built to verify the performance of a cascode GaN HEMT-based single-phase inverter. The experimental waveforms are obtained. The voltage spike of GaN HEMT is larger with the increase of L_S, as shown in Figure 7a,b. Finally, waveform of 500 W single-phase inverter is given under the condition that V_{in} = 380V, and V_o = 220V, as shown in Figure 7c. The inverter inductance current I_L, and drain-source voltage v_{ds} of S_1 and S_4 are shown, respectively. The parasitic parameters L_S should be controlled within 5nH, so as to reduce the drain-source voltage spike of the cascode GaN HEMT. The efficiency curves of the single-phase inverter base on TP65H150G4PS at different switching frequencies (20 kHz, 50 KHz, 100 kHz) are shown in Figure 7d. The switching loss increases as the switching frequency increases, and the overall efficiency of the inverter decreases. It can be seen that the maximum efficiency point is around 300 W in Figure 7d, which is a balance of the switching loss and the filter loss. When the power is low, the switching loss is dominant. With the increase of the power, the loss of the filter inductance increases and becomes dominant.

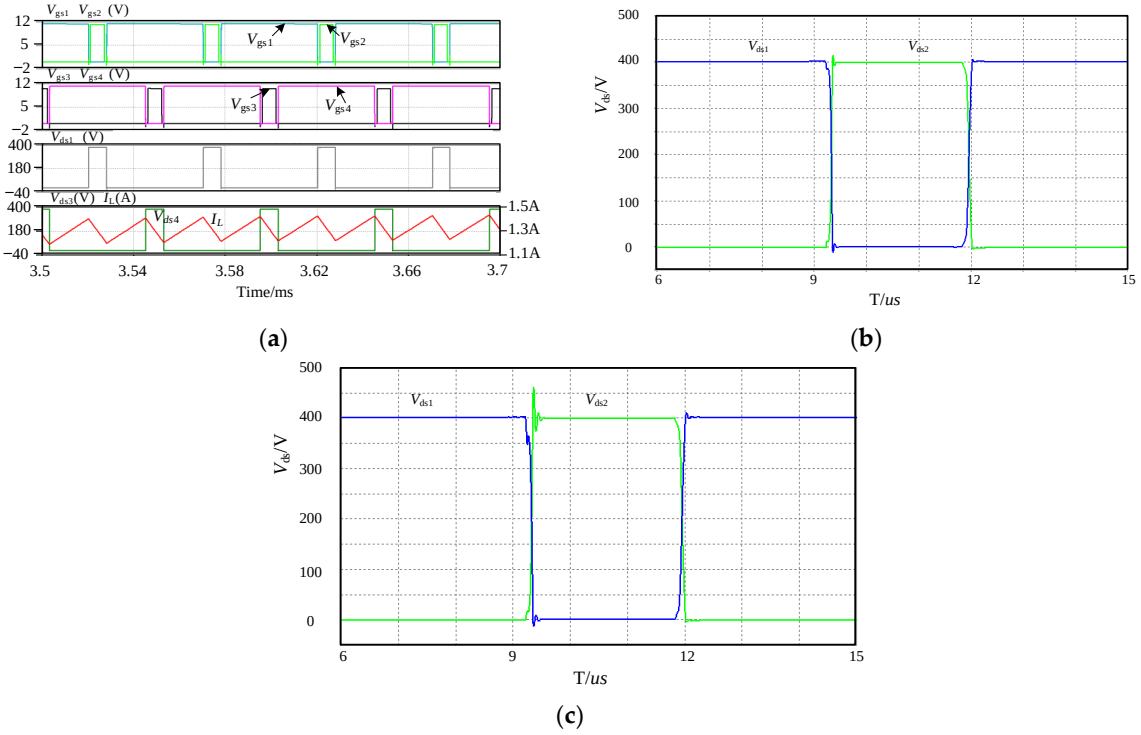


Figure 6. Simulation results of the cascode GaN HEMT-based single-phase inverter. (**a**) Waveforms of cascode GaN HEMT-based inverter; (**b**) Voltage spike of GaN HEMT with L_S = 5 nH; (**c**) Voltage spike of GaN HEMT with L_S = 20 nH.

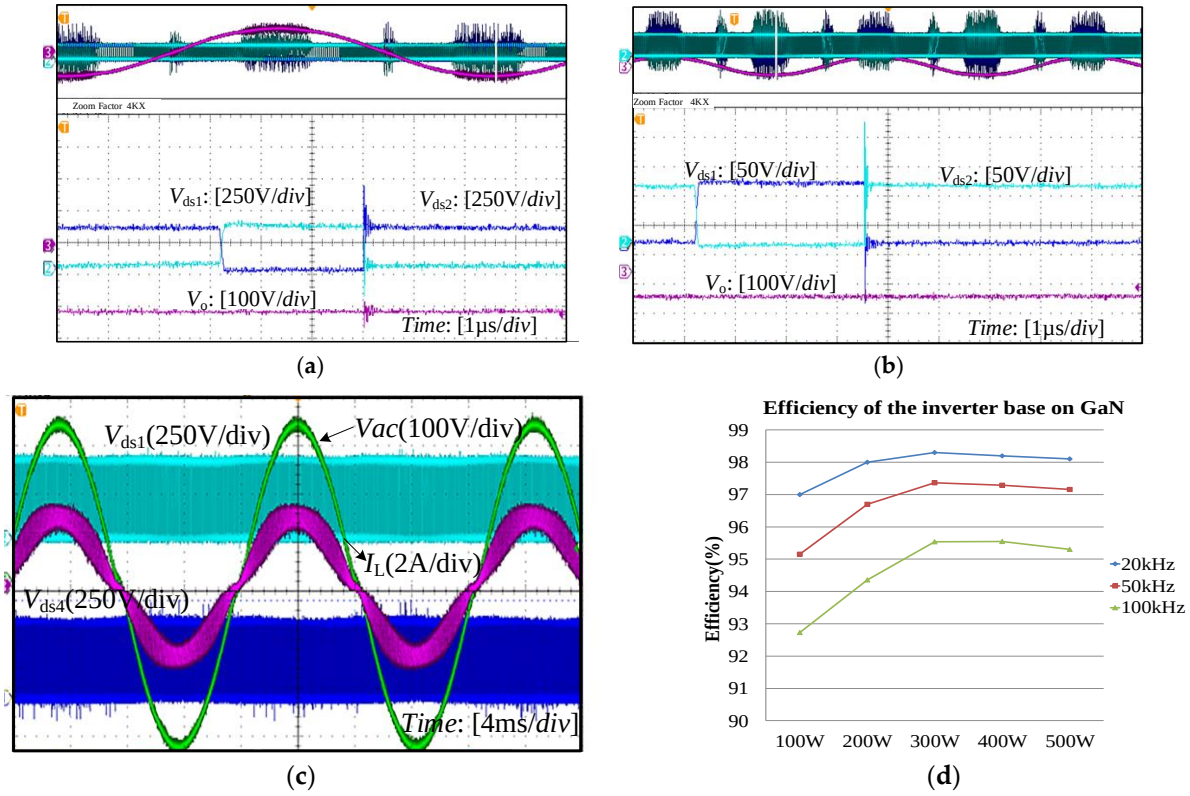


Figure 7. Experiment results of the cascode GaN HEMT-based single-phase inverter. (**a**) Experiment results of the cascode GaN HEMT-based inverter with L_S = 5 nH; (**b**) Experiment results of the cascode GaN HEMT-based inverter with L_S = 20 nH; (**c**) Experiment results of the cascode GaN HEMT-based inverter with full load; (**d**) Efficiency curve of cascode GaN HEMT based single-phase inverter.

5. Conclusions

Dynamic-state process of the 600 V cascode GaN HEMT is analyzed in this paper. We apply cascode GaN HEMT in a single-phase DC/AC inverter. L_{int2}, L_{int3}, and L_S are the most critical parasitic, which will significantly affect the dynamic performance of the cascode GaN HEMT. The influence of the parasitic inductance is identified through theoretical analysis and verified by simulation and experiment results. With the increase in frequency, the parasitic parameter *Ls* should be reduced as much as possible to reduce the influence on the drain-source voltage of the cascode GaN HEMT. Finally, a 500 W cascode GaN HEMT-based single-phase inverter is established, and the experiment results verified the correctness of theoretical and simulation analysis.

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