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Unipolar Arc Ignited Partial Discharge for 650-V AlGaN/GaN HEMTs during the DC Breakdown Voltage Measurement

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Abstract: Without the Fluorinert solution and proper pad design, the high–voltage (HV) transistor used during the DC breakdown voltage (V_{bk}) measurement might be damaged by the partial discharge (PD) in the air if its V_{bk} is close to one thousand volts or more. From the waveform measurement, the PD in the air occurred at 650 V HV GaN HEMTs during the V_{bk} measurement, it is ignited by the unipolar arc, and it is not ignited by the avalanche breakdown. This is based on the fact that the current falls below zero ampere to become a negative current, and the voltage rises so that it is higher than the setting voltage of the DC meter at the onset of the PD, thus corresponding with the electrons, leaving the plasma to cathode, and enabling a build–in potential to exist in the plasma. Then, the PD ignites because the current starts to rise in order to allow for a positive spike current; the voltage level subsequently falls and a lower voltage reading is obtained.

Keywords: partial discharge; ARC; GaN HEMTs; buck converter

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1. Introduction

Partial discharge (PD) in the insulation systems of high voltage (HV) electrical power systems has been studied since the early nineteenth century [1–3]. Currently, most PD phenomena [4–9], theories [10–12], physical mechanisms [13], and models [14–21] have been extensively and intensively explored, clarified, developed, and published, inasmuch as it might occur in the solids, liquids, and gases that cause PD. PD can result in the failure of most systems, and it occurs when a current flows in a conductor that is connected to the external world with a sufficient repetition rate [11]; therefore, the PD caused by insulation system defects can be categorized as being the result of discharges in gases or gas–insulator surfaces, discharges in liquids or liquid–solid interfaces, and discharges in solids (charge injection, electrical trees, and water trees) [14]. To the best of our knowledge, the PD behavior of semiconductor devices during the wafer–level DC measurement has never been reported. This is because most device engineers in this field have only considered how to increase the breakdown voltage (V_{bk}) of the transistor from the architecture and process, and they often ignore the effects caused by the environment surrounding it; however, a transistor will inevitably be exposed to air. Since the dielectric strength of air is much lower than that of the materials that are used to create the transistor, the PD will occur in the air surrounding the transistor, and not occur at the inside of transistor. For a transistor, the pad is the only component used to connect it with the external environment. If the pad is not properly designed, during the DC measurement, the transistor might be damaged at a voltage below its breakdown voltage V_{bk} point, due to the PD in air that will occur at the stress pad and its adjacent pads. This is why HV transistors, during DC measurements, are often immersed in the electronic liquid, Fluorinert (FC-770), to prevent PD in the air [22–24]; this is because its dielectric strength is four times higher than the air's dielectric

strength [24]. According to earlier studies in the literature [25–29], the 'turn-on' conditions for PD are:

a. the voltage should be higher than the avalanche breakdown voltage.
b. Electrons must exist for impact–ionization generation.
c. The electric field should be larger than the critical field.

In this paper, the behavior of the third-generation semiconductor device, the GaN high-electron-mobility transistor (HEMT), under the conditions of a PD event, is presented. Moreover, the 'turn-on' mechanism of a PD in the air, using a HV transistor during a DC breakdown voltage V_{bk} measurement, is also explored in the waveform analysis. From this investigation, we find that PD can be ignited repeatedly, even it does not completely fulfil the three abovementioned turn-on conditions.

2. Experiment

The transistor used in this PD study was the 650 V GaN HEMTs and it was manufactured using 8–inch ceramic substrate technology (QST^{TM}). It is an enhancement-mode (E-mode) GaN HEMT, and it uses PGaN in the gate stack of the un-doped AlGaN/GaN heterostructure to shift the potential of its channel so that it can form a transistor that is usually off, as shown in Figure 1. The gate of this GaN HEMTs is very vulnerable to electrostatic-discharge (ESD) stress, and it needs the ESD protection circuit, as shown in Figure 2 [30]. The total width of the GaN HEMTs is 36 mm, and for each ESD HEMT, the width is 3 mm. The GaN HEMT was designed with a long drain for gate space (S_D > 10 μm) so that it may sustain 650 V, whereas the S_D of the ESD HEMT is very short (<1 μm), since it only needed to sustain 6 V. The ESD protection circuit of the gate of the GaN HEMTs in Figure 2 is a cascade ESD HEMT. The top gate, and a resistor R3, were connected in a series with the source terminal (S). Its bottom gate, and a resistor R2, were connected in a series with the gate terminal (G). This made sure that one of the two ESD HEMTs could not turn on, regardless of whether it received positive or negative signals.

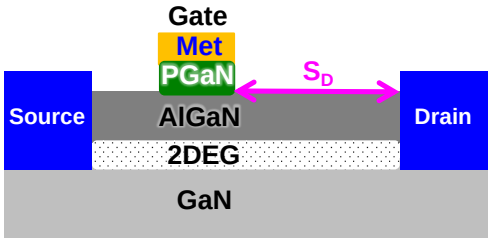


Figure 1. Cross-section of a 650 V GaN E–Mode HEMTs.

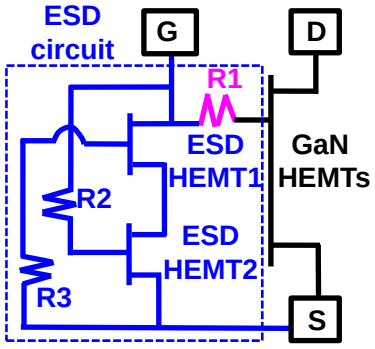


Figure 2. Schematic diagram of a 650 V GaN HEMT with the gate ESD protection circuit.

The apparatus used to measure the DC breakdown voltage V_{bk} of the GaN HEMTs used in this PD study was the Keysight B1505 semiconductor device analyzer. For this measurement, the width and time taken for the rate of the pulse to increase, was 50 ms and

2 ms, respectively. To gain more detailed insight into the complex interaction between PD and GaN HEMTs, an oscilloscope was used to measure the voltage and current waveforms of the GaN HEMTs under the conditions of the high voltage pulse event, for which the bandwidth and sample rate are 1 GHz and 5 GS/sec, respectively. The set–up for this measurement is shown in Figure 3.

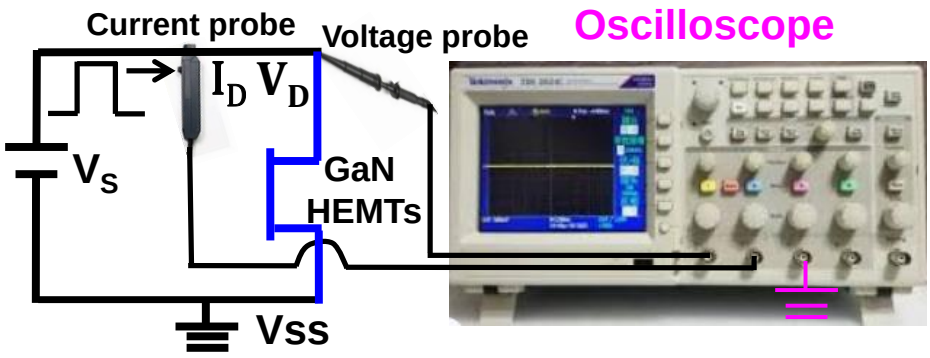


Figure 3. Setup for the PD observation of the GaN HEMTs during the breakdown voltage V_{bk} measurement.

3. Results

The PD of the GaN HEMTs was affected by defects [11,14], atmosphere pressure, temperature, and the space between pads (d), in accordance with $V_{bk} = k_2 d$, where k_2 = 97 V/μm [31]. The atmosphere pressure and temperature are external to the GaN HEMTs, whereas the defects are internal. The component of the GaN HEMTs that is used to connect its interior and exterior is the pad, which is the only conductive material of the transistor that is exposed to air. In this experiment, the parameter used to study the PD behavior of this GaN HEMTs was the temperature. From the measurement result, the threshold temperature of the PD in the air for this GaN HEMTs was 150 °C. Below this temperature, no PD occurred with the GaN HEMTs in Figure 2, since the voltage required to induce a PD in the air would have been higher than its breakdown voltage V_{bk}. In this paper, the temperature used to investigate the PD phenomenon for the GaN HEMTs was 175 °C.

3.1. Measurement Result

Figure 4 shows the drain voltage (V_D) waveform of the 650 V GaN HEMTs with the gate protection circuit in Figure 2 immersed in the electronic liquid, Fluorinert (FC–770), under an 800 V, 50 ms single pulse, at 175 °C. Since the device breakdown voltage was greater than 900 V at 175 °C, the drain voltage V_D of this 650 V GaN HEMTs remained constant, without any changes during the whole stress period as it was immersed in the electronic liquid to prevent a PD in the air; however, it is evident that the drain voltage V_D and current I_D were only able to remain at 800 V and 0 A for a while (from 10 ms to 25 ms in Figure 5a) as the 650 V GaN HEMTs was then exposed to air, and it was no longer immersed in the electronic liquid. Consequently, the drain voltage V_D oscillated between ~800 V and ~200 V, and a spike in current occurred at the voltage drop-down transient due to a PD in the air during the period of time between 25 ms and ~31 ms (region A of Figure 5a,b). Eventually, the drain voltage V_D dropped to zero, and it could only increase to ~250 V; it then remained at this voltage and did not reach 800 V again (region B of Figure 5a,c). Moreover, the drain current I_D became higher than zero (~10 mA), with some spikes (Figure 5c) caused by damage to the device.

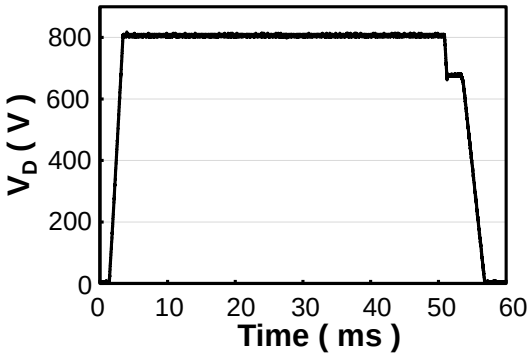
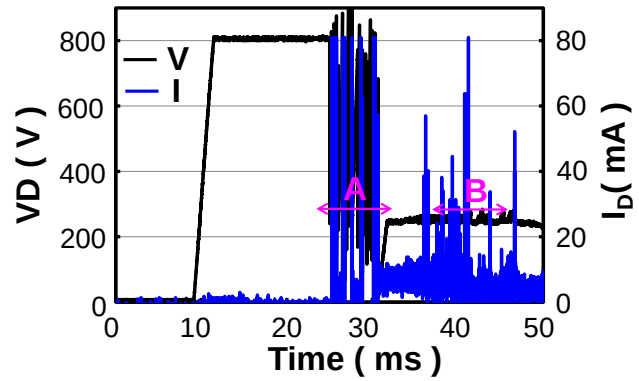
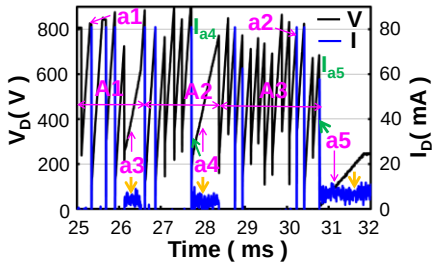


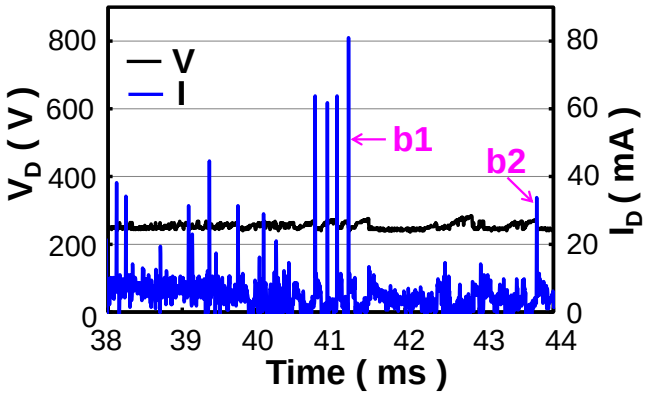
Figure 4. Drain voltage waveform of the GaN HEMTs with the gate protection circuit (Figure 2) immersed in the electronic liquid, Fluorinert (FC-770), under an 800 V, 50 ms single pulse at 175 °C.



(**a**)

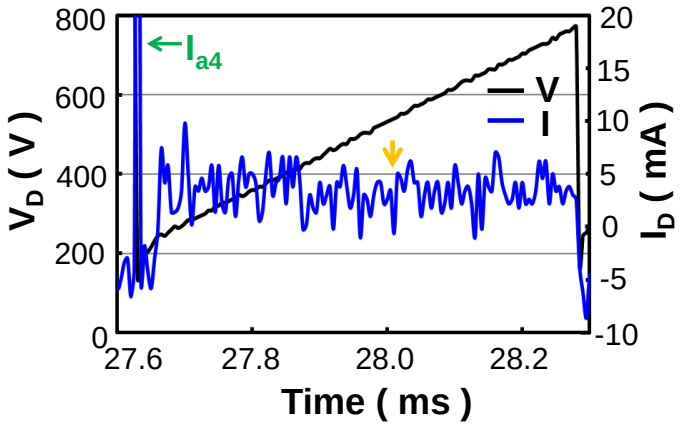


(**b**)



(**c**)

Figure 5. *Cont.*



(**d**)

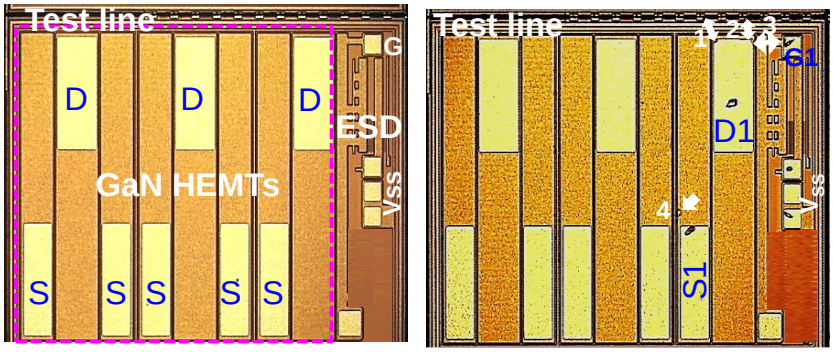
Figure 5. Drain voltage and current waveforms of the GaN HEMTs with gate protection circuit in Figure 2 under a 50 msec, 800-V pulse as it is exposed in air for (**a**) whole stress period, (**b**) zoomed-in picture of the region A in Figure 5a (at PD), (**c**) zoomed-in picture of region B in Figure 5a (after PD), (**d**) zoomed-in picture of the region a4 in Figure 5b.

3.2. Failure Analysis Result

Figure 6 shows images of the GaN HEMTs, with the gate ESD protection circuit in Figure 2, exposed to air before and after being subjected to the 800 V, 50 ms pulse, as described in Figure 5. In Figure 6a, the GaN HEMTs can be located within the pink dot square, where there are three drain pads (D) at the top, and five source pads (S) at the bottom. Outside the pink dot square, there is one test line, and the gate ESD protection circuit. There are 12 pads in the test line and one gate pad, and there are three Vss pads in the gate ESD protection circuit. The pulse is applied to the drain pad (D1), the grounded source pad (S1), the gate pad (G1), and the Vss pad, and there is a probe mark on each pad, as shown in Figure 6b. After the pulse, it is evident that there is damage caused by erosion on the edges of the drain pad (D1), gate pad (G1), and the pads near pad D1 in the test line (white arrows in Figure 6b). From the zoomed-in view of these regions (1 to 4 in Figure 6b), it is evident that residue clots exist in the regions facing each other, on two different pads, due to the PD that induced high temperatures (Figure 7a–c). The damage caused to region 1 can be seen between the upper-left corner of the drain pad (D1) and one pad on the test line, whereas the damage in region 2 can be seen between the upper-right corner of the drain pad (D1) and another pad in the test line. The damage caused to region 3 can be seen between the upper-right corner of the drain pad (D1) and gate pad (G1). The damage caused to region 4 can be seen between the bottom drain pad and source pad (S1). This provides direct evidence to prove that a PD occurred in the air between pads, and that it did not occur in the interior of the transistor. From the TEM picture, no damage can be seen on the metal system of the pad (M2, IMD, and M1). Figure 7e shows the top-view SEM picture of the pad in Figure 7a; the pink mark region was used for delayering, with a focused-ion beam (FIB), the cross-section of the TEM. Figure 7f shows the TEM picture for the layers that were below the pink region in Figure 7e. There is an extra layer of film (residue in Figure 7) on the metal-2 (M2); however, M2 is the top layer of the pad. The only layer higher than M2, using this technology, is the passivation layer, thus implying that the extra layer of film should be the passivation layer that is migrating from the region adjacent to the pad, and this is caused by the PD-induced temperature being higher than the layer's melting point; therefore, exploring the passivation layer for migration prevention will be a very important subject for passivation layer engineering in the development of thousand volt transistors.

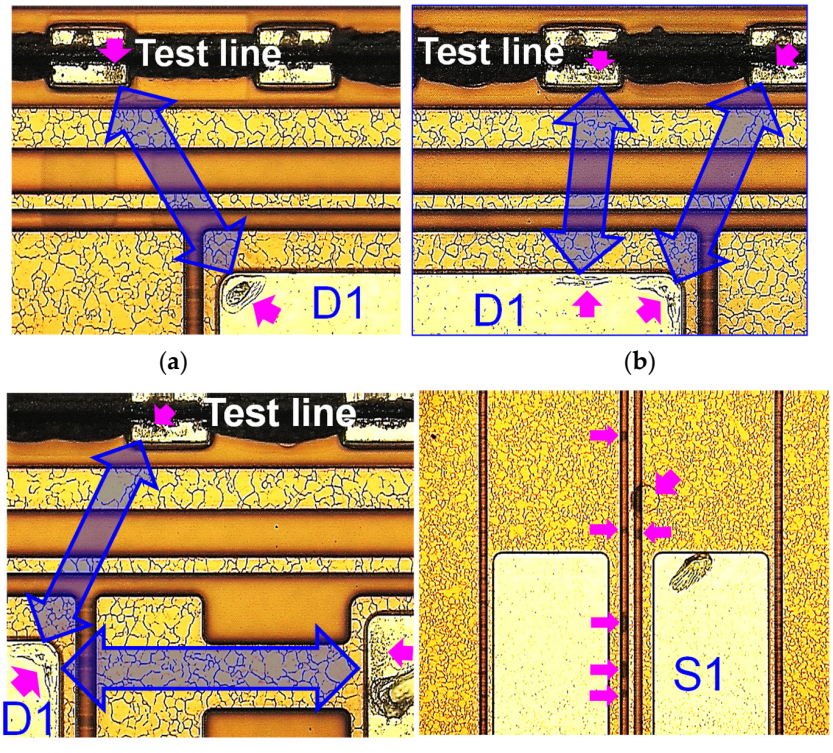
If the transistor is not damaged, the current can go back to zero after each PD-induced spike to the current; this occurred, except during the time periods of a3, a4, and a5 in Figure 5b. As opposed to the other three regions, region 4 in Figure 6b is in the S/D

region of the GaN HEMTs, thus implying transistor damage. This is caused by a PD occurring in the GaN HEMTs due to the prior PD in the air causing the temperature of the transistor to increase. As a result, the current (yellow arrow) and the voltage exceed the time periods a3 and ora4 in Figure 5b,d, which take place after the first PD event (I_{a4}); this is different from the results obtained during the other time periods. This implies that the GaN HEMTs remains undamaged; even the PD that occurs in the GaN HEMTs happens before a5. Eventually, the voltage is stopped at ~250 V, and it can no longer reach 800 V, which is caused by the fact that the GaN HEMTs has been damaged by the previous PD (a5 in Figure 5a); therefore, the challenge of how to design a metal system for the pads and the metal routing of a transistor for heat dissipation, in order to prevent it from damage by the PD-induced high temperature, will pose an issue for the development of thousand volt transistors. Moreover, the damage mechanism of the transistor, which may be triggered by the PD event that induces high temperatures, is still an unexplored field of study.



(**a**) (**b**)

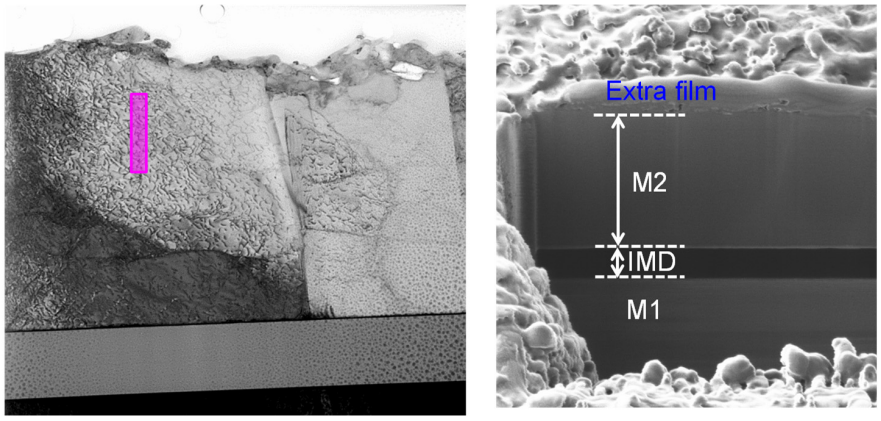
Figure 6. Images of the GaN HEMTs with the gate ESD protection circuit in Figure 2 exposed to the air (**a**) before and (**b**) after a 800 V, 50 ms pulse. The arrows show the damage regions after this pulse.



(**a**) (**b**)

(**c**) (**d**)

Figure 7. *Cont.*



(**e**) (**f**)

Figure 7. Zoomed−in view of the damage sites at regions (**a**) 1, (**b**) 2, (**c**) 3, and (**d**) 4 in Figure 6b, where are all at the corner regions of the pads facing each other (arrows) (**e**) the top view SEM picture of the pads in the test line in Figure 7a (**f**). TEM picture for the layers below the pink region are shown in (**e**).

4. Discussion

Figure 5a shows that the 800 V DC pulse cannot instantly lead to a PD occurring in the GaN HEMTs, as per the diagram in Figure 2, as the voltage can be kept at 800 V for about 15 ms. Then, it decreases and increases in accordance with the spike current due to the PD. This behavior is similar to the high current IV characteristics of HV-LDNMOS, under the conditions of the 100 ns transmission-line pulse (TLP) event, which was first driven into the high-voltage and low-current region, and then triggered into the low-voltage and high-current snapback region [32,33]. This is attributed to the fact that the turn-on threshold voltage of the parasitic NPN bipolar transistor decreases as the temperature increases due to joule–heating generation in the high voltage and low current region [34]. Although this phenomenon has been reported [28], the time delay mechanism of the PD after reaching the ignition voltage has not yet been investigated.

Figures 8 and 9 show the zoomed-in view of the drain voltage and the current waveforms for the time periods a1, a2, b1, and b2, as shown in Figure 5, in order to investigate the PD behavior of GaN HEMTs during the breakdown measurement. Except in Figure 9b, it is evident that the drain current I_D falls below zero as the drain voltage V_D increases to a voltage measurement that is higher than 800 V at the inception of each PD event. Then, the drain current I_D increases and the drain voltage V_D decreases rapidly until the current and voltage peaks reach their lowest values (<200 V). At this point, the transistor no longer complies with the abovementioned conditions, the voltage reading becomes greater than the avalanche breakdown voltage measurement, and the electric field is greater than the critical field, thus causing a PD. Eventually, the drain current I_D falls below zero again, even if the drain voltage V_D still does not increase to 800 V when the GaN HEMTs is not damaged (Figure 8).

In order to investigate the turn-on mechanism of the PD, zoomed-in parts of the waveform, from Figure 5, are shown in Figures 8 and 9. According to the waveform, the drain current I_D decreases and increases during each PD event; in Figures 8 and 9, this can be attributed to the unipolar arc model (UA) [16–21], as shown in Figure 10. As the voltage reaches a critical level, electrons are emitted from a spot on the cathode surface. Then, these electrons are emitted at an accelerated rate as the high electric field collides with the neutrons above the cathode surface, which causes the neutrons that lost electrons to generate electron–ion pairs. Subsequently, the impact of ionization creates more electron–ion pairs, leading to the formation of high-density plasma at the region above the cathode spot, since the ion has a positive charge. As electron mobility is much greater than ion mobility, most positive ions accumulate at the tip of the cathode [19,20], whereas many

unreleased electrons accumulate in the region below the tip to maintain charge neutrality; therefore, the region above the spot on the cathode forms the region where charge exists, similarly to a PN diode [1]. This enables sheath potential to accrue on the cathode's surface [19,20]. The local plasma pressure P_e above the cathode spot induces the electric field in the radial direction ($Er = -\nabla P_e/en_e$), where e is the elementary charge and n_e is the electron density [20]; therefore, the plasma sheath potential decreases in the radial direction, with a ring-like area around the cathode spot, and it allows build-in potential to exist at some distance r_f from the cathode spot, as per [16,18,20]

$$V_f = \frac{kT_e}{2e} Ln\left(\frac{M_i}{2\pi m_e}\right) \quad (1)$$

where M_i/m_e is ion/electron mass ratio.

As the V_f exceeds and sustains an arc, a strong local emission of electrons will occur from a spot on the cathode plate, and it will be directed into the plasma. Since plasma sheath potential decreases in the radial direction, the electrons can return the cathode plate if the potential in the region near the spot is lowered by more than V_f. The return flow of electrons forms the unipolar arc current J_s, which follows the following equation, as proposed by Robson and Thonemann [16].

$$J_S = -\frac{1}{4}|e|n_e v\left\{\exp\left(-\frac{|e|V_s}{kT_e}\right) - \exp\left(-\frac{|e|V_f}{kT_e}\right)\right\} \quad (2)$$

where v is the average velocity of the electron, and k is the Boltzmann constant.

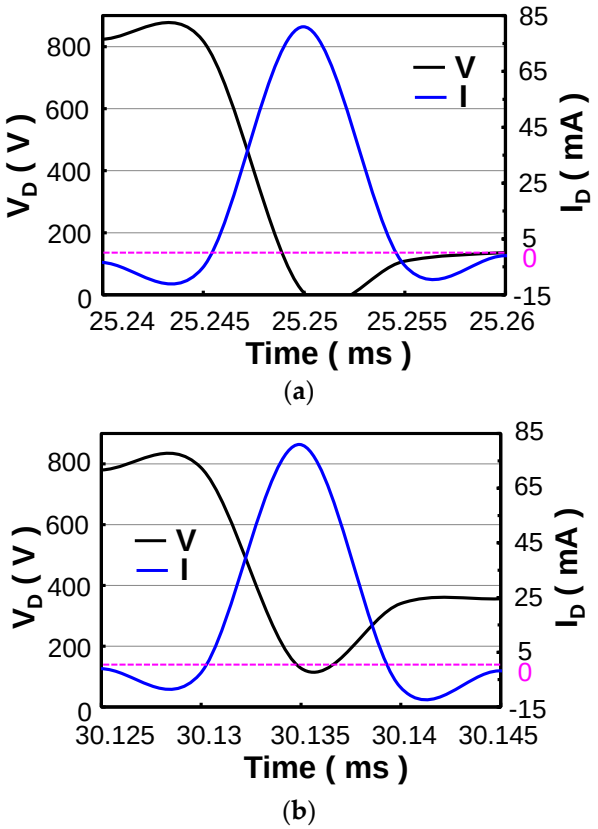


Figure 8. Zoomed–in view of the voltage and current waveforms in Figure 5b, during the time periods (**a**) a1 and (**b**) a2.

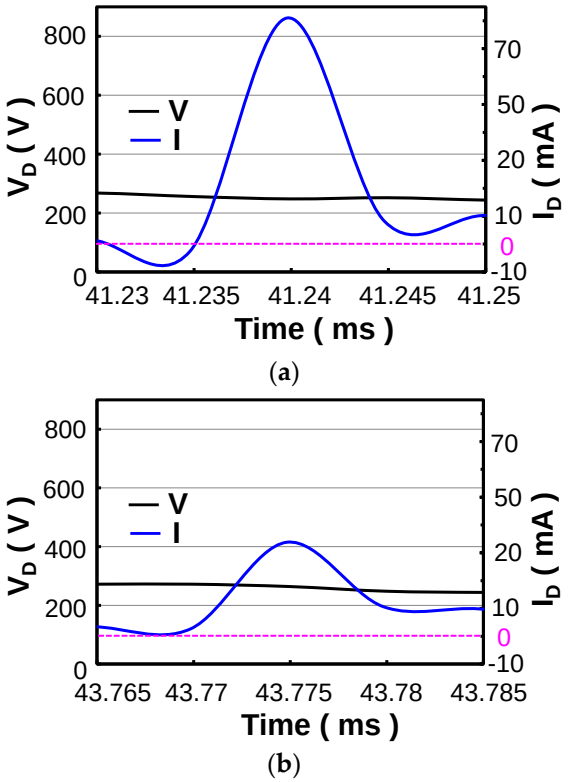


Figure 9. Zoomed–in view of the voltage and current waveforms in Figure 5c, during the time periods (**a**) b1 and (**b**) b2.

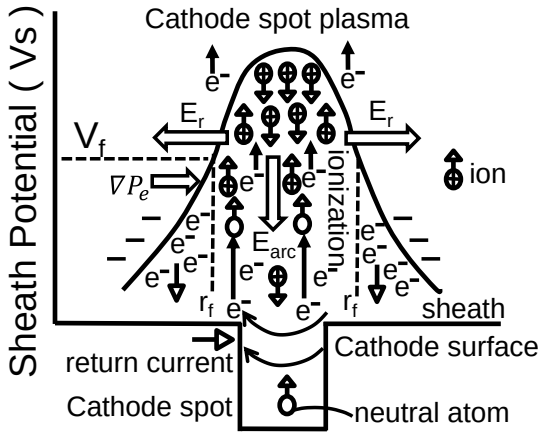


Figure 10. Unipolar arc (UA) model.

From this equation, the current density J_s is negative if the potential at this region is lower than V_f. It implies that more electrons leave the plasma for the cathode than ions, and the current direction is in the opposite direction of the sheath electric field E_{arc} [20]; therefore, the drain current I_D at the onset of the PD is negative, as shown in Figures 8 and 9. With the build-in potential V_f of the plasma, the drain voltage V_D at the onset of the PD, as shown in Figure 8, is higher than the output voltage of the DC meter (800-V). Although this model was proposed in 1959 [16], it has never been proven with any electrical data until now. The sheath electric field is enhanced further as more electrons than ions leave the plasma. It elevates the ion flux in the plasma, raising the ion bombardments and recombination rates in order to increase the local surface temperature. This leads to the desorption of neutral gas molecules and the evaporation of metal atoms from the surface into the plasma, which, in turn, further increases the plasma density, ionization rate, and

build-up of space for charging ions above the cathode spot. Then, a positive feedback mechanism is formed to further increase the ionization rates [19,20]; therefore, the plasma expands its area and continually increases in size. Eventually, it ignites the PD to form a low impedance path between the anode and cathode, discharging some of the charges stored in its capacitor C_{OUT} from the output stage of supplying power (converter) [35,36], and the capacitor C_D of GaN HEMTs (Figure 11) also takes part in the discharging of stored charges as the plasma expands toward the anode. This causes the output voltage (drain voltage V_D) to fall, resulting in low voltage, and the drain current I_D increases, rapidly forming a high current, as shown Figure 8. This provides direct evidence to prove that the PD is ignited by the UA, and that it is not ignited by the avalanche breakdown. As some of the electrons and ions move away from the plasma, the area shrinks, which causes the drain current I_D to fall, whereas the drain voltage V_D still remains at a level of low voltage since the capacitors, C_{OUT} and C_D, are only slightly charged. Without enough voltage to create the high electric field for new electron–ion pair generation, the remaining ions and electrons follow the UA model, and they move until they are discharged completely. This is why the drain current I_D falls below zero again, as shown in Figures 8 and 9a. The converter of the power supply is composed of two big drivers (HS-D and LS-D) [35,36], an external inductor, and a big external capacitor ($\geq$100-μF) to regulate the input voltage (V_{IN}) to the setting voltage (V_{OUT}). With regard to the big capacitor, the output voltage V_{OUT} of converter is supposed to be very stable and does not vary with the loading current. From Figure 5 or Figure 8, the PD current is less than 100 mA, which is not a large current for a power supply. The reason as to why the small current induces the voltage fluctuation of the power supply has not yet been discussed. From Figure 8, the PD event cannot be equivalent to the passive components (resistors and capacitors) [15]. It is evident that the current falls, whereas the voltage increases, and then the current increases as the voltage decreases; this opposes the current direction of the passive component based on $I = C\,dV/dt$. This is because the generated electrons and ions during a PD can make the current flow back and forth between the power supply and transistor, as shown in Figure 11. The interaction between the PD and power supply is a very interesting area of study, and it has not yet been explored in the literature.

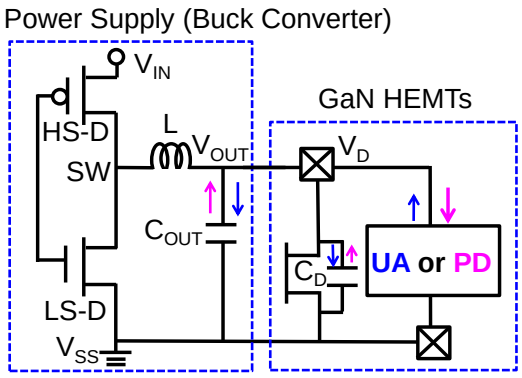


Figure 11. Interaction between the GaN HEMTs and the output stage of supplying power (buck converter) during the breakdown voltage measurement.

5. Conclusions

The partial discharge (PD) caused damage to the 650 V GaN HEMTS under DC measurement conditions. The damage was evident at the passivation layer, which was adjacent to the pad and transistor, since it occurs in the spaces between pads. As a result, the pad arrangement and passivation layer material are very important for ultra-high voltage (UHV) transistor designs. Without enough space between pads, a PD will occur in the air, which will cause transistor damage to the UHV transistor during the breakdown voltage measurement; therefore, exploring passivation layers that can withstand high temperatures,

and investigating the mechanism of PD-induced transistor damage, will be important subjects to consider during UHV transistor development.

The PD event for the 650 V GaN HEMTS, which occurred during the DC measurement, did not occur instantaneously as it reached the ignition voltage. The time delay mechanism for the PD event of the semiconductor device is an interesting topic for further study on UHV transistors. Moreover, the phenomena of the unipolar arc (UA) can be found at the onset of the PD as a result of the waveforms. The negative current demonstrates how the electrons are moving from the plasma to the cathode, and here, the fact that the voltage is higher than the applied voltage of the power supply proves that a build-in potential existed in the plasma. Eventually, the PD is ignited as the current increases to become a positive spike current, whereas the voltage decreases to a low voltage level. Theses give direct evidence that demonstrates that the PD for the 650 V GaN HEMTs, during the DC measurement, is ignited by the UA, and not by the avalanche breakdown.

During the PD event, the current alternately flows from negative to positive while the voltage increases and decreases repeatedly; this cannot be depicted by the passive component model. This implies that the PD event for the UHV transistor during the DC measurement cannot be equivalent to the passive components (resistors and capacitor) since their current directions are opposite to each other. For the PD, the negative current occurs with positively charged voltage, and the positive current occurs with negatively charged voltage; however, the current flows from the power supply to the passive components, as the positively charged voltage flows from the passive components to the power supply, which uses negatively charged voltage, as per $I = C\,dV/dt$. The voltage fluctuation for the UHV transistor during the DC measurement occurred due to the interaction between the PD and the circuit of the power supply; this is a field that has never been explored and is worthy of investigation.

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