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Research on Single-Phase and Three-Phase Compatible Isolated On-Board Charger and Control Technology

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Abstract: This paper presents a single-phase and three-phase compatible isolated on-board charger for electric vehicles. The charger is compatible with the single-phase and three-phase AC voltage input and is composed of two-stage circuits. Based on the three-phase six-switch power factor correction (PFC) circuit, by switching on and off, the front stage is transformed into a cascade topology of a totem-pole PFC circuit and boost circuit. The rear stage is a full-bridge LLC resonant converter. In the single-phase or three-phase working mode, the front-stage control strategy is a double closed-loop control. The current inner loop controller is improved for the three-phase six-switch PFC circuit. The PI controller and repetitive controller are connected in parallel to form the current inner loop compound controller, which can effectively reduce the total harmonic distortion of the input current. By using simulation software MATLAB/Simulink, the circuit model was built. The simulation results verify the correctness of the theoretical analysis.

Keywords: on-board charger; single-phase and three-phase compatibility; power factor correction; compound controller

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1. Introduction

With the development of the automobile industry, electric vehicles have gradually been promoted. The electric vehicle draws energy from the AC grid through the on-board charger (OBC) and charges the power battery after the electric energy is transformed. Therefore, the OBC is an important part of electric vehicles [1]. The input power supply of OBC mainly includes single-phase AC voltage and three-phase AC voltage. At present, most OBCs mainly work under single-phase input conditions, with low output power and long charging time. With the increase in the capacity of the power battery of new energy vehicles and the demand for faster charging, the market demand for three-phase input high-power car chargers is also increasing [2]. The design of the OBC should be compatible with single-phase and three-phase power inputs so that electric vehicles can meet the use of different power occasions through flexible charging.

The early OBC is the single-stage structure, which has the advantages of a simple circuit structure and convenient control, but its efficiency and power factor are difficult to achieve satisfactory results, and the output voltage range is narrow [3]. Nowadays, the mainstream topology of OBC is mainly composed of a front-stage power factor correction (PFC) circuit and a rear-stage isolated DC–DC circuit. The front-stage PFC circuit can realize PFC, reduce harmonic pollution, and provide the rear-stage DC–DC circuit with a smaller ripple DC bus voltage. The rear stage can output stable and adjustable high-voltage DC supply power to the power battery [4]. Reference [5] proposes a two-stage OBC consisting of a single-phase bridgeless boost PFC circuit and a full-bridge LLC resonant converter. Through the cascade control strategy between modules, the two-stage structure circuit can be started smoothly, the shock in the starting process is eliminated, and the output voltage has no drastic impact. However, the traditional bridgeless PFC circuit has an

obvious common mode interference problem. Reference [6] using SiC-MOSFET to design the interleaved parallel totem-pole bridgeless PFC circuit in continuous current mode (CCM) can effectively overcome the common mode interference problem and improve efficiency. Reference [7] designed a 1 kW OBC based on SiC-MOSFET. The front stage of the circuit is a single-ended primary-inductor converter (SEPIC) PFC converter, and the rear stage is a full-bridge LLC resonant converter. Among them, the SEPIC PFC converter can make the DC bus voltage follow the battery pack voltage so that the LLC resonant converter can keep operating near the resonant frequency to realize the optimization of the operating efficiency of the whole machine. The total efficiency from 20% of the rated load to full load is 88.5% to 93.5%. Reference [8] proposes a passive auxiliary converter structure with a three-phase 380 V AC input. The front-stage three-phase six-switch circuit can effectively suppress voltage spikes, and the electric energy can be transferred to the load by itself, thereby reducing the stress of the main circuit. Reference [9] designed a three-phase bidirectional isolated soft-switch OBC. The front stage is a bidirectional 3-phase 4-switch rectifier. Compared with the common three-phase bridge rectifier, the number of switch tubes is reduced by two, which reduces the complexity of the control circuit. The rear stage is a double-bridge series resonant converter with phase-shift control, which can realize bidirectional power flow. However, the topologies proposed in the reference [5–9] can only meet the power supply mode of a single-phase or three-phase input. In recent years, some OBC topologies that can satisfy single-phase and three-phase compatible inputs have been proposed [10–13]. Reference [10] proposed a modular single-stage electrolytic capacitorless OBC compatible with single-phase and three-phase voltage input, and used relays and decoupling capacitors to transform single-phase and three-phase circuit topologies. Reference [11] proposes a variable front-stage OBC with dual closed-loop interval type II fuzzy control. Based on the interleaved parallel totem pole bridgeless PFC circuit, the third bridge arm and the corresponding control switch are added to design the front stage variable PFC circuit, and the rear stage adopts the full bridge LLC resonant converter. The feasibility of the proposed topology scheme being compatible with a single and three-phase input is verified by simulation experiments. Generally speaking, the DC bus voltage of the single-phase PFC circuit is usually set at about 400 V, and the output DC bus voltage of the three-phase PFC circuit is usually set at about 700~800 V. However, the variable circuit of the front stage proposed in the reference [11] cannot meet the same output voltage of the DC bus, so it will bring inconvenience to the parameter design of the rear stage circuit. Reference [12] considers the efficiency of the rear-stage DC–DC circuit, combined with the requirements of the same DC bus, and uses the relay to achieve a VIENNA topology compatible with different power supply methods. Reference [13] designs the front-stage compatible PFC circuit of OBC. The rectifier has extended voltage gain characteristics in the case of single-phase input and can convert the input AC voltage of 110 V into high-voltage DC of 750 V, realize the same DC bus voltage in the two input modes, and achieve 93.6% efficiency at full load.

As a key technology of OBC, the control strategy directly determines the operation efficiency, battery life, and charging safety of OBC. For the control system of single and three-phase PFC circuits, the double closed-loop PI control strategy using the current inner loop and the voltage outer loop is the most common. However, when the traditional double closed-loop PI control strategy is applied to the three-phase PFC circuit, it is easy to have some problems, such as waveform distortion and an uneven current. Reference [14] adopts a fractional-order PID control strategy to improve steady-state control accuracy and reduce ripple. The results show that the control performance of the system is enhanced, and the steady-state and dynamic performance is improved, but the parameter tuning process is more complicated. Reference [15] proposed an adaptive cosine inner membrane control method to suppress grid-side current harmonics based on traditional PI control, which effectively suppressed the low-frequency harmonics of the grid-side current. Reference [16] analyzed the shortcomings of traditional PI control, where a simplified form of control transfer functions based on the small-signal model was proposed with segmented control

action. The methodology has the advantages of both simplified control strategies and segmented PI-repetitive control to achieve high-power factor performance and reduce THD in a broad range of load conditions.

The parameter design of the rear-stage DC–DC circuit is affected by the DC bus voltage output of the front stage. If the DC bus voltage can be the same in the two power supply modes, it will be conducive to the optimal design of the overall circuit. Inspired by the above references, after the rear-stage circuit is determined to be a full-bridge LLC resonant converter, in order to realize the same DC bus voltage under two power supply modes, a two-stage OBC topology that can realize the compatible input of single-phase and three-phase AC voltage is proposed. Based on the three-phase six-switch PFC circuit topology, the front stage transforms into a cascade topology structure of a totem-pole PFC circuit and boost circuit through switching on and off. After the design of compatible inductors and compatible capacitors, the PFC circuit can achieve a compatible input of single-phase and three-phase voltages and provide the same DC input voltage for the rear-stage full-bridge LLC resonant converter. The full-bridge LLC resonant converter establishes an equivalent model through the fundamental wave analysis method and obtains the optimal parameters of the circuit. Aiming at the control strategy of the front-stage three-phase PFC circuit, the current inner loop controller is improved, and the current inner loop PI controller and the repetitive controller are connected in parallel to form the current inner loop compound controller. Compared with the traditional double closed-loop PI control, it can effectively reduce the THD rate of the grid-side current under different load conditions.

2. Topological Structure and Working Principle of the OBC System

Figure 1 shows the basic topology of a single-phase and three-phase compatible isolated OBC. Single-phase and three-phase topology was switched through relays K_1–K_4. When the front stage was a three-phase voltage input, K_1–K_3 was open and K_4 was closed. The topology was a three-phase six-switch PFC circuit. When the front stage was a single-phase voltage input, K_1–K_3 was closed and K_4 was open. The topology was a combination circuit of a totem-pole PFC circuit cascaded boost circuit, and the rear stage was a full-bridge LLC resonant converter. The front-stage PFC circuit included an AC inductor L, field-effect transistors (FETs) S_1–S_6 (SiC-MOSFET), and DC bus capacitances $C_{dc\text{-}s}$ and C_{dc}. The rear-stage LLC resonant converter included FETs Q_1–Q_8, resonant capacitance C_r, resonant inductor L_r, excitation inductance L_m, transformer T, holding capacitance C_o, and load equivalent resistance R_L.

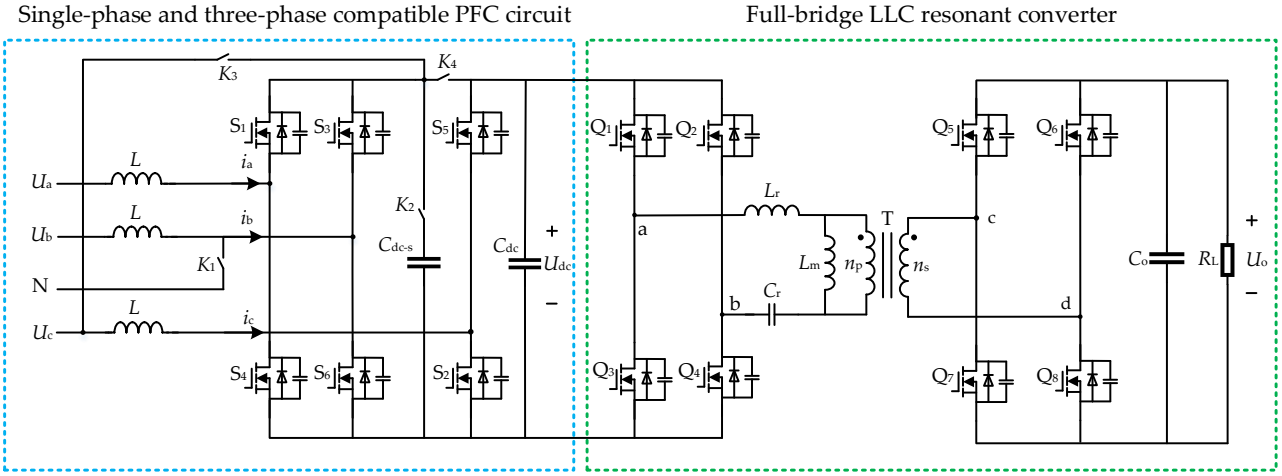


Figure 1. Single-phase and three-phase compatible isolated on-board charger (OBC).

2.1. Three-Phase Working Mode

Figure 2 shows the charging circuit in the three-phase working mode. The front stage was the three-phase six-switch PFC circuit, which can essentially be equivalent to three

pulse-width modulation (PWM) rectifiers. U_a, U_b, and U_c were the three-phase input grid voltage, and the AC inductance $L_a = L_b = L_c = L$.

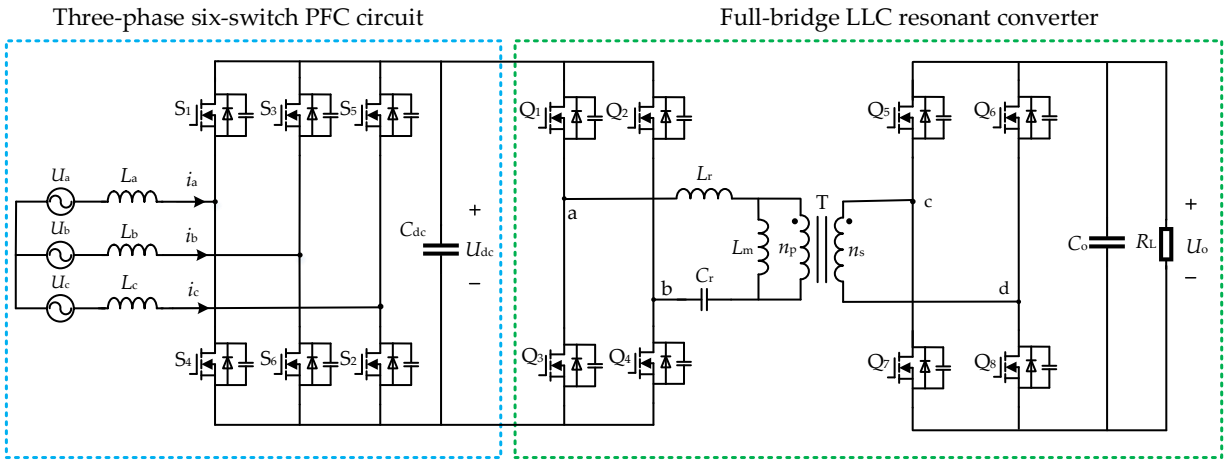


Figure 2. Three-phase working mode.

The switching function shown in Equation (1) was used to represent an off-conduction state of the FET, and then the operating state of the six FETs of the three-phase bridge arm.

$$S_k = \begin{cases} 1 & \text{The upper bridge arm is on, the lower bridge arm is off} \\ 0 & \text{The upper bridge arm is off, the lower bridge arm is on} \end{cases} k = a, b, c \quad (1)$$

It can be seen from Equation (1) that there were a total of eight switch state combinations of $S_aS_bS_c = 000$, $S_aS_bS_c = 001$, $S_aS_bS_c = 010$, $S_aS_bS_c = 011$, $S_aS_bS_c = 100$, $S_aS_bS_c = 101$, $S_aS_bS_c = 110$, and $S_aS_bS_c = 111$, corresponding to the path topology of different PWM rectifier converters. By controlling the on–off of S_1–S_6, the input current was in phase with the input voltage, and the waveform was similar to a sine wave, so as to achieve the purpose of PFC.

The rear stage was the full-bridge LLC resonant converter, which converts the high-voltage DC transmitted from the front-stage PFC circuit into high-frequency voltage pulses. The resonant converter converts the high-frequency voltage pulse into sine wave voltage, and finally converts the sine wave voltage into DC voltage output through the rectifier circuit [17]. According to the charging protocol curve of the OBC, the output voltage variation range is controlled by changing the switching frequency of Q_1–Q_4.

2.2. Single-Phase Working Mode

Figure 3 shows the charging circuit in the single-phase working mode. The front stage was the topology of the cascade of the totem-pole PFC circuit and boost circuit. The use of SiC-MOSFET enabled the totem-pole PFC circuit to achieve higher efficiency and can work in CCM. When three-phase AC voltage was input, the DC output voltage after passing through the three-phase six-switch PFC circuit was U_{dc}, and its rated value was 700 V. When single-phase AC voltage was input, it could output a stable DC voltage $U_{dc\text{-}s}$ after passing through the totem-pole PFC circuit, and its rated value was 400 V. To make the input voltage of the rear-stage full-bridge LLC resonant converter have the same value in the two input modes, a boost circuit was added after the totem-pole PFC circuit to increase the DC voltage from 400 V to 700 V.

When the totem-pole PFC circuit is in a steady-state operation, a power cycle can be divided into four modes, and the working modes of the positive and negative cycles are similar. The two modes of the positive half cycle of the AC input power were taken as an example. For mode one, turn off S_1 and S_3, turn on S_4 and S_6, U_a charges L_a through L_a, S_4, and S_6 loops, and $C_{dc\text{-}s}$ discharges the subsequent circuit. For mode two, turn off S_3 and S_4, turn on S_1 and S_6, U_a and L_a charge $C_{dc\text{-}s}$ through the S_1 and S_6 circuits, and L_a is in a

discharged state at this time. When the boost circuit part is in a steady-state operation, it can be divided into two working modes. That is, when S_2 is turned on, $U_{dc\text{-}s}$ charges L_c; when S_2 is turned off, $U_{dc\text{-}s}$ and L_c charge C_{dc} through the S_5 loop, and L_c is in a discharged state at this time.

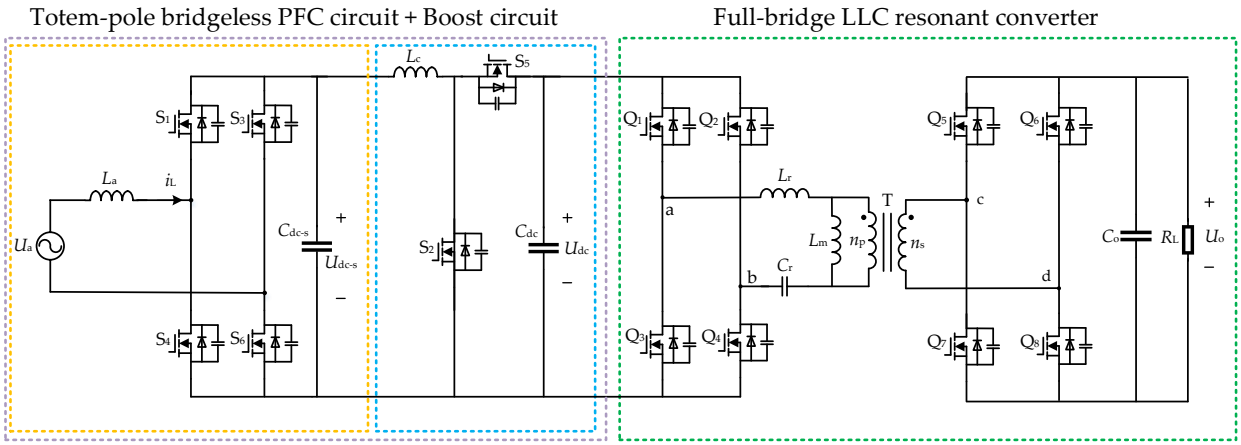


Figure 3. Single-phase working mode.

3. Parameter Design

The performance indicators of OBC are the main reference for the design of circuit parameters. According to the main performance indicators shown in Table 1, the parameter design should be carried out in the case of the rated output power of single-phase 3.3 kW and three-phase 6.6 kW.

Table 1. Main performance indicators of on-board charger (OBC).

Performance Indicator	Value
Input phase voltage range (U_{in})	176~264 V
Input voltage frequency range (f)	45~65 Hz
DC bus voltage ($U_{dc\text{-}s}$)	400 V
Front-stage output voltage (U_{dc})	700 V
Output voltage range (U_o)	280~420 V
Rated output voltage (U_{o_nor})	350 V
PFC circuit switching frequency (f_{sw})	50 kHz
Power factor	≥0.99
Efficiency (η)	≥93%

3.1. Parameter Design of the Front-Stage PFC Circuit

(1) AC inductance L

When the single-phase voltage was input, for the totem-pole PFC circuit, the selection of L required that the maximum value of the input current ripple was less than 10% of the maximum input current. The calculation is expressed as:

$$\frac{U_{dc\text{-}s} \cdot T_{sw}}{8L} < 10\% \cdot \frac{\sqrt{2}P_{o\text{-}s}}{\eta \cdot U_{in_min}}, \quad (2)$$

where $U_{dc\text{-}s}$ is the DC bus voltage, $U_{dc\text{-}s}$ = 400 V; T_{sw} is the switching period, T_{sw} = 20 μs; $P_{o\text{-}s}$ is the rated output power in single-phase operation, $P_{o\text{-}s}$ = 3.3 kW; η is the efficiency, η = 93%; and U_{in_min} is the minimum input voltage, U_{in_min} = 176 V.

From Equation (2), L > 0.36 mH was obtained.

For the boost circuit, when the inductor current was in the CCM state, the selection of the AC inductor needed to satisfy Equation (3):

$$L = \frac{U_{dc\text{-}s}D(1-D)}{\gamma f_{sw} I_{omin}} = \frac{400 \times 0.43 \times (1-0.43)}{2 \times 50 \times 10^3 \times 4} = 0.25 \text{ mH}, \quad (3)$$

where D is the duty cycle; γ is the current ripple coefficient; and I_{omin} is the critical continuous load current.

From Equation (3), if the inductor current was required to work in continuous mode, $L > 0.25$ mH.

When the three-phase voltage was input, L was determined by the AC current following the performance index and the current harmonic suppression performance index. The calculation is expressed as:

$$\frac{U_{\text{m}} T_{\text{sw}} (2U_{\text{dc}} - 3U_{\text{m}})}{2U_{\text{dc}} \Delta i_{\text{max}}} \leq L \leq \frac{2U_{\text{dc}}}{3\omega I_{\text{m}}}, \tag{4}$$

where U_{m} is the phase voltage fundamental wave, U_{m} = 311 V; U_{dc} is the output voltage of the front stage, U_{dc} = 700 V; I_{m} is the fundamental peak value of phase current, I_{m} = 19 A; and Δi_{max} is the maximum peak value of current ripple, $\Delta i_{\text{max}} = 20\% I_{\text{m}}$ = 3.8 A.

From Equation (4), 0.55 mH $\leq L \leq$ 78.2 mH.

Based on the actual situation and simulation experiment, take L = 1 mH.

(2) DC bus capacitance $C_{\text{dc-s}}$

When the single-phase voltage was input, for the totem-pole PFC circuit, the choice of the $C_{\text{dc-s}}$ was mainly determined by the low-frequency voltage ripple and the load holding time, which needed to meet Equations (5) and (6). The holding time Δt was the time required for $U_{\text{dc-s}}$ to drop from the rated voltage to β% of the rated voltage after the power outage.

$$C_{\text{dc-s}} \geq \frac{P_{\text{o-s}}}{\omega U_{\text{ripple-s}} \cdot U_{\text{dc-s}}^2} = \frac{3300}{2 \times \pi \times 50 \times 10 \times 400^2} = 2626.06\ \mu\text{F}, \tag{5}$$

where $U_{\text{ripple-s}}$ is the ripple value of the $U_{\text{dc-s}}$.

$$C_{\text{dc-s}} \geq \frac{2P_{\text{o-s}} \Delta t}{U_{\text{dc-s}}^2 - (\beta\% \cdot U_{\text{dc-s}})^2} = \frac{2 \times 3300 \times 0.02}{400^2 - (0.8 \times 400)^2} = 2291.67\ \mu\text{F}, \tag{6}$$

where Δt = 0.02 s; β% = 80%.

According to Equations (5) and (6), $C_{\text{dc-s}} \geq$ 2626.06 μF. Based on the actual situation and simulation experiment, take $C_{\text{dc-s}}$ = 2700 μF.

(3) DC bus capacitance C_{dc}

In the case of single-phase input voltage, C_{dc} is part of the boost circuit parameters, and the selection of capacitance mainly controls the output ripple within the specified range. In CCM, the capacitance depends on the output current, switching frequency, and desired output voltage ripple value. Therefore, the capacitance value can be selected according to Equation (7):

$$C_{\text{dc}} \geq \frac{I_{\text{omax}} \cdot D}{f_{\text{sw}} \cdot U_{\text{ripple}}} = \frac{4.71 \times 0.43}{50 \times 10^3 \times 14} = 2.89\ \mu\text{F}, \tag{7}$$

where I_{omax} is the maximum output current; and U_{ripple} is the ripple value of U_{dc}.

When the three-phase voltage was input, the larger the value of C_{dc}, the smaller the U_{ripple} and the stronger the anti-load disturbance ability. However, if the value is too large, it will affect the following performance of the voltage outer loop. Therefore, the selection of C_{dc} mainly needed to meet the maximum output power and the response time of the voltage loop. The calculation is expressed as:

$$C_{\text{dc}} \geq \frac{P_{\text{o}} T_{\text{r}}}{2U_{\text{dc}} U_{\text{ripple}}} = \frac{6600 \times 0.001}{2 \times 700 \times 14} = 336.73\ \mu\text{F}, \tag{8}$$

where T_{r} is the response time of the voltage loop, and P_{o} is the rated output power during three-phase operation.

Based on the actual situation and simulation experiment, take C_{dc} = 2000 μF.

3.2. Parameter Design of the Rear-Stage Full-Bridge LLC Resonant Converter

Voltage gain is an important characteristic of the LLC resonant converter. A fundamental wave analysis was used to analyze the gain characteristic of the LLC resonant converter [18]. The equivalent circuit of the rear-stage LLC resonant converter is shown in Figure 4.

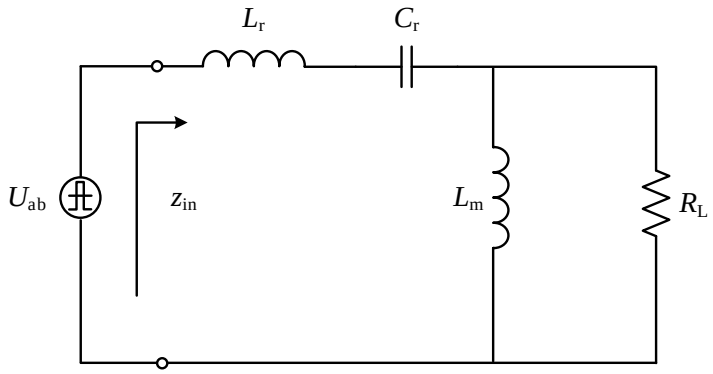


Figure 4. Equivalent circuit of LLC resonant converter.

The normalized voltage gain M can be expressed as:

$$M(f_n, L_n, Q_e) = \frac{1}{\sqrt{(1+\frac{1}{L_n}-\frac{1}{L_n f_n^2})^2 + Q_e^2(f_n-\frac{1}{f_n})^2}}, \tag{9}$$

where f_n is the normalized frequency; Q_e is the quality factor; and L_n is the inductance coefficient.

Figure 4 shows that the input impedance Z_{in} of the rear-stage LLC resonant converter is expressed as:

$$Z_{in} = \sqrt{\frac{L_r}{C_r}}[\frac{L_n^2}{1+Q_e^2 f_n^2 L_n^2} + j(f_n - \frac{1}{f_n} + \frac{f_n L_n}{1+Q_e^2 f_n^2 L_n^2})], \tag{10}$$

When the imaginary part of Z_{in} is zero, the maximum quality factor of the converter working in the inductive region can be expressed as:

$$Q_{e_max} = \sqrt{\frac{1}{L_n(1-f_n^2)} - \frac{1}{f_n^2 L_n^2}}. \tag{11}$$

(1) Transformer ratio n

The transformer ratio is expressed as:

$$n = \frac{U_{dc}}{U_{o_nor}} = 2, \tag{12}$$

where U_{o_nor} is the rated output voltage, U_{o_nor} = 350 V.

(2) Maximum gain M_{max} and minimum gain M_{min}

When U_{dc} is minimum and U_o is maximum, the maximum gain M_{max} is expressed as:

$$M_{max} = \frac{n \cdot U_{o_max}}{U_{dc_min}} = 1.24, \tag{13}$$

where U_{o_max} is the maximum output voltage, U_{o_max} = 420 V; and U_{dc_min} is the minimum front-stage output voltage, U_{dc_min} = 680 V.

When U_{dc} is maximum and U_o is minimum, the minimum gain M_{min} is expressed as:

$$M_{min} = \frac{n \cdot U_{o_min}}{U_{dc_max}} = 0.78, \tag{14}$$

where U_{o_min} is the minimum output voltage, U_{o_min} = 280 V; and U_{dc_max} is the maximum front-stage output voltage, U_{dc_max} = 720 V.

(3) Inductance coefficient L_n

When the L_n is larger, the amplitude of voltage gain is smaller, causing the working frequency range of the resonant converter to widen. When the L_n is smaller, the excitation current is larger, the turn-off loss of the FET increases, and the efficiency of the converter decreases. Generally, the empirical value of the L_n is between 1–6, and L_n = 2.5 was selected in this design.

(4) Quality factor Q_e

From the impedance characteristics of the rear-stage LLC resonant converter, the maximum quality factor Q_{e_max} can be expressed as:

$$Q_{e_max} = \frac{1}{L_n \cdot M_{max}} \sqrt{L_n + \frac{M_{max}^2}{M_{max}^2 - 1}} \approx 0.747, \tag{15}$$

The value of the quality factor is Q_e = 0.95 Q_{e_max},

$$Q_e = 0.95 \cdot Q_{e_max} \approx 0.71. \tag{16}$$

(5) Maximum operating frequency and minimum operating frequency

Figure 5 exhibits the characteristic operating curve of normalized voltage gain M with normalized frequency f_n when L_n = 2.5.

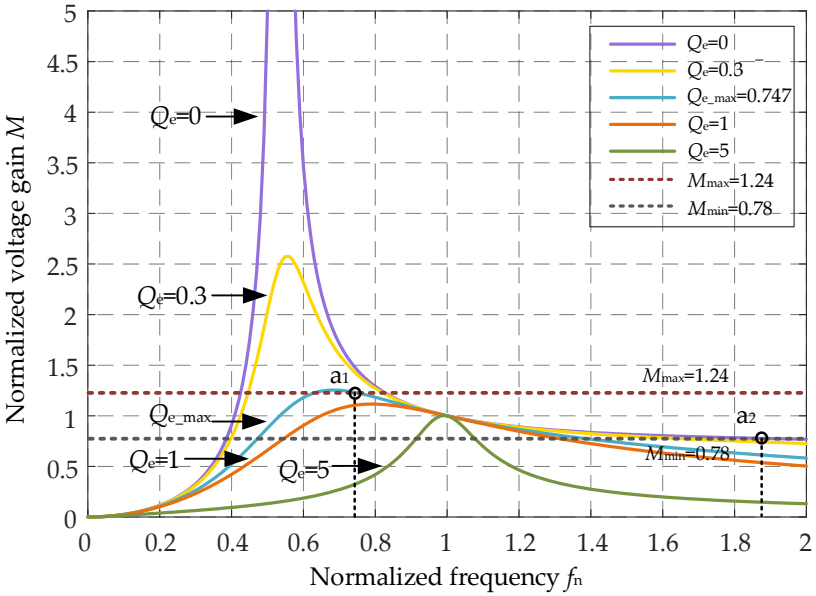


Figure 5. Normalized voltage gain curve.

When the quality factor Q_e = 0, the LLC resonant converter is in a no-load operation state. The intersection of normalized voltage gain curve and minimum voltage gain curve is a_2, and its abscissa is the maximum normalized frequency. The maximum switching frequency is expressed as:

$$f_{s_max} = f_r \cdot \sqrt{\frac{1}{L_n \frac{M_{min}-1}{M_{min}} + 1}} \approx 184 \text{ kHz}, \tag{17}$$

where f_r is the resonant frequency, f_r = 100 kHz.

When the quality factor Q_e = Q_{e_max}, the intersection of the normalized voltage gain curve and the maximum voltage gain curve is a_1, and its abscissa is the minimum normalized frequency. The minimum switching frequency is expressed as:

$$f_{s_min} = f_r \cdot \sqrt{\frac{1}{L_n \frac{M_{max}^2 - 1}{M_{max}^2} + 1}} \approx 73 \text{ kHz}. \quad (18)$$

(6) The equivalent impedance R_{ac} of the primary side of the transformer

The equivalent impedance of the secondary side circuit of LLC resonant converter converted to the primary side is expressed as:

$$R_{ac} = \frac{8n^2}{\pi^2} \cdot \frac{U_{o_nor}^2}{P_o} \approx 60.18\ \Omega. \quad (19)$$

(7) Resonant inductor L_r, resonant capacitance C_r, and excitation inductor L_m

According to the value of Q_e and resonant frequency f_r, the expressions and calculated values of L_r and C_r can be obtained with the following:

$$L_r = \frac{0.95 \cdot Q_{e_max} \cdot R_{ac}}{2\pi f_r} \approx 68\ \mu\text{H}, \quad (20)$$

$$C_r = \frac{1}{(2\pi f_r)^2 L_r} \approx 37.25\text{nF}, \quad (21)$$

The excitation inductance L_m is expressed as:

$$L_m = L_n \times L_r = 170\ \mu\text{H}. \quad (22)$$

4. Control Strategy

In the single-phase and three-phase working modes, the control strategy of the front stage was a double closed-loop control. Figure 6 shows the control strategy of OBC in the single-phase working mode. For the totem-pole PFC circuit, the average current control of the double closed-loop PI algorithm was adopted [19]. First, the $U_{dc\text{-}s}$ was sampled and then compared with the reference voltage $U_{dc\text{-}s_ref}$ to obtain the output voltage error signal. After passing through the PI controller, the output voltage error signal was multiplied by the input voltage U_{in} as the reference current i_{ref} of the inner current loop. The sampled inductor current i_L was compared with the i_{ref} and then passed through the current loop PI controller, which was then compared with the sawtooth wave in the PWM module to generate a specific duty cycle drive signal. The boost circuit adopted the traditional double closed-loop PI control. The current loop was the inner loop, and the voltage loop was the outer loop, which increased the DC bus voltage from 400 V to 700 V.

The rear-stage LLC resonant converter operated in constant-voltage charging mode and constant-current charging mode. Together, the converter only needed to control one variable, namely the output voltage U_o or output current I_o. Although the dynamic response of the single-loop control is poor, the output current and voltage will not change greatly in the charging process, so the single-loop control can meet the charging requirements.

When the charging circuit was in the three-phase working mode, for the three-phase PFC circuit, there were problems such as waveform distortion and uneven current flow under the traditional double closed-loop PI control strategy. The current inner loop controller was improved and a repetitive controller was added to achieve a better harmonic suppression effect. The PI controller and the repetitive controller were connected in parallel to form the current inner loop compound controller, which can effectively reduce the THD rate of the current on the grid side.

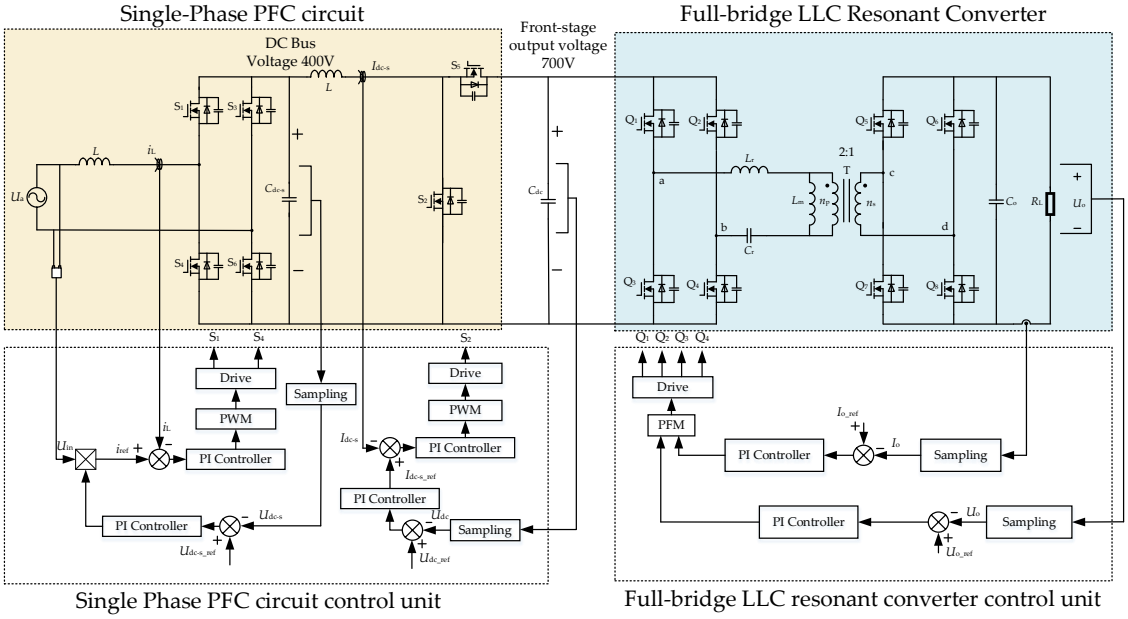


Figure 6. Single-phase working mode control strategy.

Figure 7 shows the control strategy of the OBC in the three-phase working mode. The difference between the DC voltage reference U_{dc_ref} and the U_{dc} was made, and the error signal obtained passed through the PI regulator of the voltage outer loop, whose output was the given value of i_d. After coordinated transformation and phase-locked loop (PLL) algorithm, the d-axis and q-axis components e_d and e_q and phase signal ωt of ac side voltage U_a, U_b, and U_c were respectively obtained. The AC side current i_a, i_b, and i_c also went through the corresponding coordinate transformation, and the d- and q-axis feedback quantities i_d and i_q were obtained. The obtained i_d and i_q were differenced with the reference values i_d* and i_q*, and the error value was obtained through the current inner loop repetitive controller and the decoupling algorithm to obtain the output of u_d and u_q. After the u_d and u_q went through the reverse park transformation, the control signal of the power switching device was obtained through the space vector pulse-width modulation (SVPWM) algorithm to achieve the PFC function.

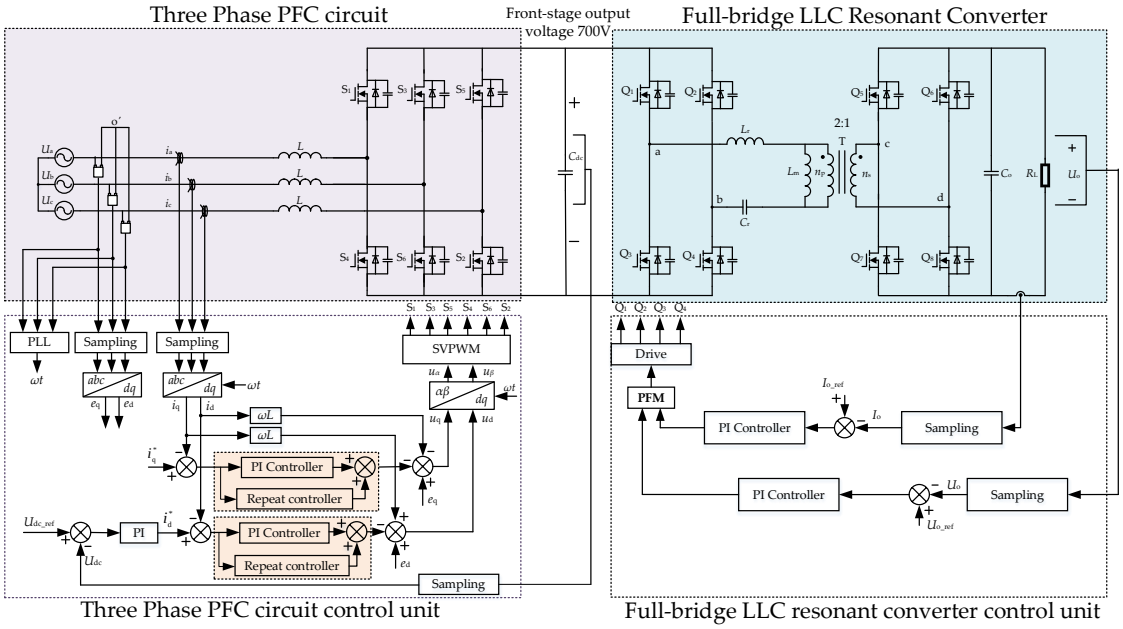


Figure 7. Three-phase working mode control strategy.

4.1. Front-Stage Three-Phase PFC Circuit Current Inner Loop Compound Controller

Figure 8 shows the design of the current inner loop compound controller with the d-axis as the analysis object. i_d* is the d-axis reference of the AC side current, i_d is the d-axis output of the AC side current, e(z) is the error between i_d* and i_d, $C(z)$ is the compensator, P(z) is the transfer function of the discretized controlled object, d(z) is the disturbance signal, and PI(z) is the discretized PI regulator. When the d(z) is ignored, the error e(z) is acted by the PI regulator and repetitive controller together, and the generated control signal acts on the controlled object P(z).

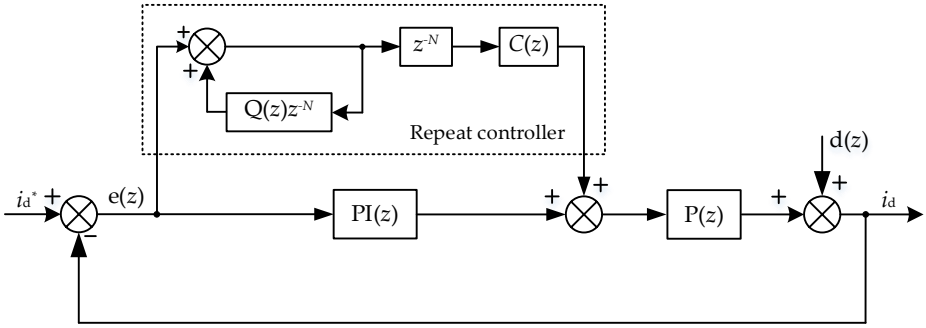


Figure 8. Current inner loop composite control block diagram.

4.1.1. Design of Repetitive Controller

Repetitive control is a new control method based on the internal model principle, which can effectively restrain periodic disturbance error. In the three-phase PFC circuit, due to the influence of the power tube dead zone time, periodic errors of the power grid current will occur, thus increasing the harmonic component of the power grid current. For periodic errors in the three-phase PFC circuit, although the PI controller will compensate and adjust, the effect is not ideal [20].

The transfer function of the repetitive controller is expressed as:

$$\mathrm{H}(z) = \frac{z^{-N} \cdot C(z)}{1 - \mathrm{Q}(z) z^{-N}}, \tag{23}$$

where Q(z) = 0.97; N is the sampling times of one cycle; and $C(z)$ is the compensator.

The transfer function of compensator $C(z)$ is expressed as:

$$C(z) = k_r \cdot z^k, \tag{24}$$

where k_r is the amplitude compensation coefficient; and z^k is the phase compensation link.

k_r has a greater influence on the error convergence rate, and the value range of k_r is $0 < k \leq 1$. The larger the value, the faster the error convergence, so k_r is taken as 1.

According to Equations (23) and (24), the transfer function of the repetitive controller can be obtained by:

$$\mathrm{H}(z) = \frac{z^{-N+k}}{1 - \mathrm{Q}(z) \cdot z^{-N}}. \tag{25}$$

4.1.2. Design of Current Inner Loop PI Controller

After feedforward decoupling, the d-axis and q-axis components are independent of each other. Since the current inner loop adopts digital control, its sampling and calculation process will have a time-delay effect. Figure 9 shows the control system of the current inner loop, where e^{-sTs} is the calculation delay link, $(1 - e^{-sTs})/s$ is the zero-order hold link, and $1/(R_s + sL)$ is the controlled object of the current inner loop.

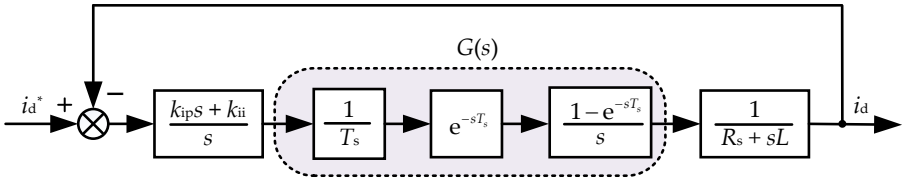


Figure 9. Current inner loop control block diagram.

The transfer function $G(s)$ of the digital controller consisting of the calculation delay link and the zero-order hold link is expressed as:

$$G(s) = \frac{1}{T_s} \cdot e^{-sT_s} \cdot \frac{1 - e^{-sT_s}}{s} \approx e^{-1.5sT_s} \approx \frac{1}{1 + 1.5sT_s}, \tag{26}$$

The current inner loop transfer function $G_{oi}(s)$ can be expressed as:

$$G_{oi}(s) = \frac{k_{ii}(As + 1)}{R_s s(1 + 1.5sT_s)(1 + s\frac{L}{R_s})}, \tag{27}$$

where L is the filter inductance; R_s is the parasitic resistance of filter inductor; and $A = k_{ip}/k_{ii}$ is the parameter ratio of the current inner loop PI regulator.

According to the classic control theory, the zero point of the PI regulator is introduced into the current inner loop gain to offset the complex poles in the system, making the system a type I system [21]. When $A = L/R_s$, the expression of current inner loop transfer function $G_{oi}(s)$ can be simplified as:

$$G_{oi}(s) = \frac{k_{ii}}{R_s s(1 + 1.5sT_s)}, \tag{28}$$

Using the setting method of the second-order system, and taking the damping coefficient $\zeta = 0.707$, then:

$$\begin{cases} \omega_n^2 = \frac{k_{ii}}{1.5R_sT_s} \\ 2\zeta\omega_n = \frac{1}{1.5T_s} \end{cases}, \tag{29}$$

where ω_n is the undamped oscillation frequency; ζ is the damping coefficient; and T_s is the sampling time of the current inner loop.

Through calculation, the closed-loop transfer function $G_{ci}(s)$ of the current inner loop can be expressed as:

$$G_{ci}(s) = \frac{G_{oi}(s)}{1 + G_{oi}(s)} \approx \frac{1}{1 + 6sT_s}. \tag{30}$$

4.2. Front-Stage Three-Phase PFC Circuit Voltage Outer Loop Controller

The output current of the DC bus can be expressed as:

$$i_{dc} = 0.75 \cdot i_d \cdot m \cdot \cos(\theta), \tag{31}$$

where m is the modulation coefficient of the pre-stage PFC circuit; and θ is the initial phase angle of the switching function.

Figure 10 is the voltage outer loop control block diagram, where $G_{ci}(s)$ is the closed-loop transfer function of the current inner loop, k_{vp} and k_{vi} are the parameters of the voltage outer loop PI regulator, T_v is the sampling time of the front-stage output voltage, and $1/sC_{dc}$ is the controlled object of the voltage outer loop.

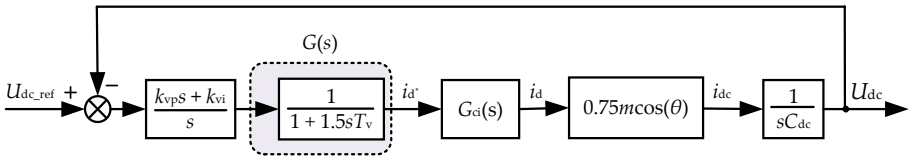


Figure 10. Control block diagram of voltage outer loop.

Figure 11 is the simplified voltage outer loop control block diagram, combining the time constant 1.5 T_v of the digital controller in the voltage outer loop with the time constant 6 T_s in $G_{ci}(s)$ to simplify the voltage outer loop control system.

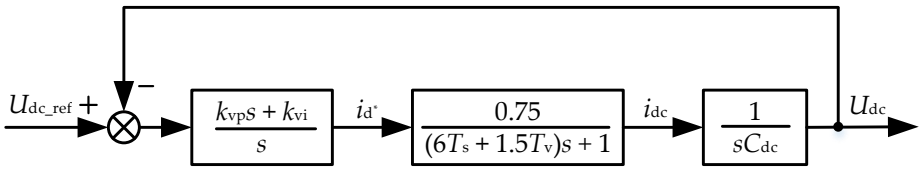


Figure 11. Simplified voltage outer loop control block diagram.

The voltage outer loop transfer function $G_{ov}(s)$ can be expressed as:

$$G_{ov}(s) = \frac{0.75 \cdot k_{vi}(\frac{k_{vp}}{k_{vi}}s + 1)}{s^2 C_{dc}[(6T_s + 1.5T_v)s + 1]}, \tag{32}$$

Let $\omega_1 = k_{vi}/k_{vp}$ and $\omega_2 = 1/(6\ T_s + 1.5\ T_v)$, then the frequency width of the voltage outer loop h is expressed as:

$$h = \frac{\omega_2}{\omega_1} = \frac{k_{vp}}{k_{vi}(6T_s + 1.5T_v)}, \tag{33}$$

According to the parameter design of a typical type II system [22], Equation (34) can be obtained:

$$\frac{0.75k_{vi}}{C_{dc}} = \frac{1}{h\sqrt{h}(6T_s + 1.5T_v)^2}, \tag{34}$$

where T_v = 1 ms and the sampling time of the current inner loop T_s = 0.1 ms.

According to Equations (33) and (34), the parameters of the voltage outer loop PI regulator k_{vp} and k_{vi} are:

$$\begin{cases} k_{vi} = \frac{C_{dc}}{330.75 \times h\sqrt{h}T_s^2} \\ k_{vp} = \frac{C_{dc}}{15.75 \times \sqrt{h}T_s} \end{cases}. \tag{35}$$

4.3. Control Strategy of Rear-Stage Full-Bridge LLC Resonant Converter

Since the LLC resonant converter contains a variety of working modes, a corresponding state-space model is established by using the piecewise linear space method, and nonlinear terms in system equations are linearly approximated by using the extended description function method [23]. The transfer function expression from switching frequency to the output voltage of the full-bridge LLC resonant converter is obtained as follows:

$$G_{vf}(s) = \frac{K_{vf}(sC_o r_c + 1)}{(sC_o R_L + 1)(\frac{s^2}{f_s^2} + \frac{s}{f_s \cdot Q_e} + 1)}, \tag{36}$$

where f_s is the operating frequency of the full-bridge LLC resonant converter, f_s = 85 kHz; Q_e is the quality factor of the resonant converter; C_o is the output holding capacitance; R_L is the equivalent output load; and r_c is the series equivalent resistance of the holding capacitance, $r_c \approx 0.4\ \Omega$.

$$K_{vf} = \frac{u_{dc}}{n}\left[\frac{f_r^3 f_s\left(1+\frac{1}{L_n}-\frac{f_r}{L_n f_s}\right)}{2\pi L_n f_r^2 f_s^3\left[\left(1+\frac{1}{L_n}-\frac{f_r}{L_n f_s}\right)+Q_e^2\left(\frac{f_s}{f_r}-\frac{f_r}{f_s}\right)^2\right]^{\frac{3}{2}}}+\frac{L_n Q_e^2\left(f_s^2-f_r^2\right)\left(f_s^2+f_r^2\right)}{2\pi L_n f_r^2 f_s^3\left[\left(1+\frac{1}{L_n}-\frac{f_r}{L_n f_s}\right)+Q_e^2\left(\frac{f_s}{f_r}-\frac{f_r}{f_s}\right)^2\right]^{\frac{3}{2}}}\right], \quad (37)$$

Equation (37) is simplified to obtain $K_{vf} = 7.77 \times 10^{-5}$.

According to Equations (36) and (37), the transfer function from the switching frequency to the output voltage of the LLC resonant converter can be expressed as:

$$G_{vf}(s) = \frac{7.77 \times 10^{-5}\left(1.2 \times 10^{-5} s + 1\right)}{\left(5.29 \times 10^{-4} s + 1\right)\left(\frac{s^2}{7.23 \times 10^9} + \frac{s}{6.03 \times 10^4} + 1\right)}, \quad (38)$$

According to Equation (38), the Bode diagram of the transfer function without adding the voltage PI controller is obtained, as shown in Figure 12.

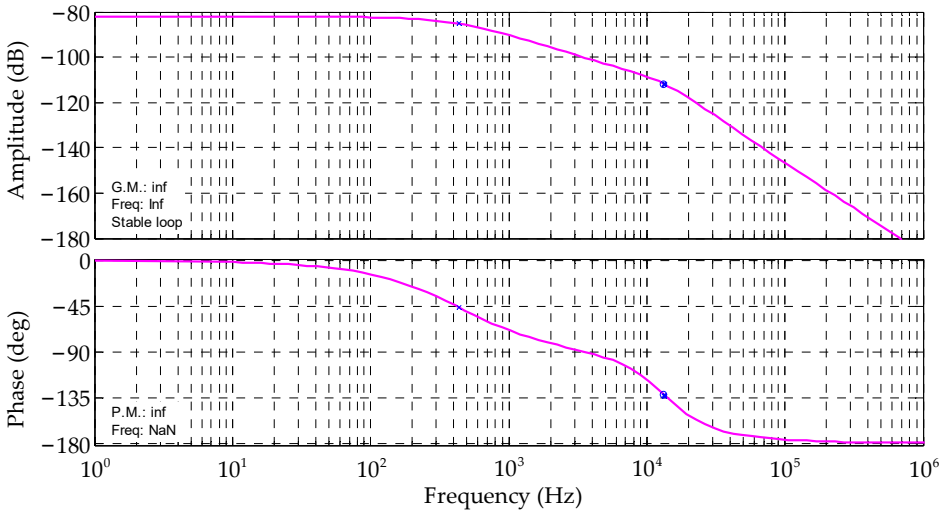


Figure 12. Bode diagram of transfer function without voltage PI controller.

Since the LLC resonant converter before correction is a 0-type system, it is necessary to add a PI controller to improve the system type, so that the mid-frequency band of the system drops at a slope of −20 dB/dec and crosses the 0 dB line, thereby improving the phase margin of the system and ensuring that the system has good stability.

In the constant voltage charging mode, the control block diagram of the LLC resonant converter after adding the voltage PI controller is shown in Figure 13.

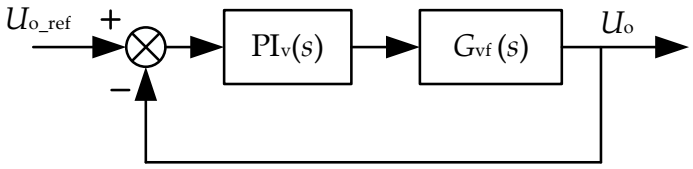


Figure 13. Control block diagram of adding voltage PI controller.

The voltage outer loop PI controller can be expressed as:

$$\mathrm{PI}_v(s) = \frac{3.62 \times 10^7\left(1 + 1.1 \times 10^{-4} s\right)}{s}, \quad (39)$$

In the constant voltage charging mode, the transfer function of the LLC resonant converter with the voltage PI controller is expressed as:

$$\varphi_{\mathrm{LLC}_v}(s) = \mathrm{PI}_v(s) \cdot G_{vf}(s), \quad (40)$$

From Equation (40), the system transfer function of the voltage PI controller is obtained, and the Bode diagram is shown in Figure 14.

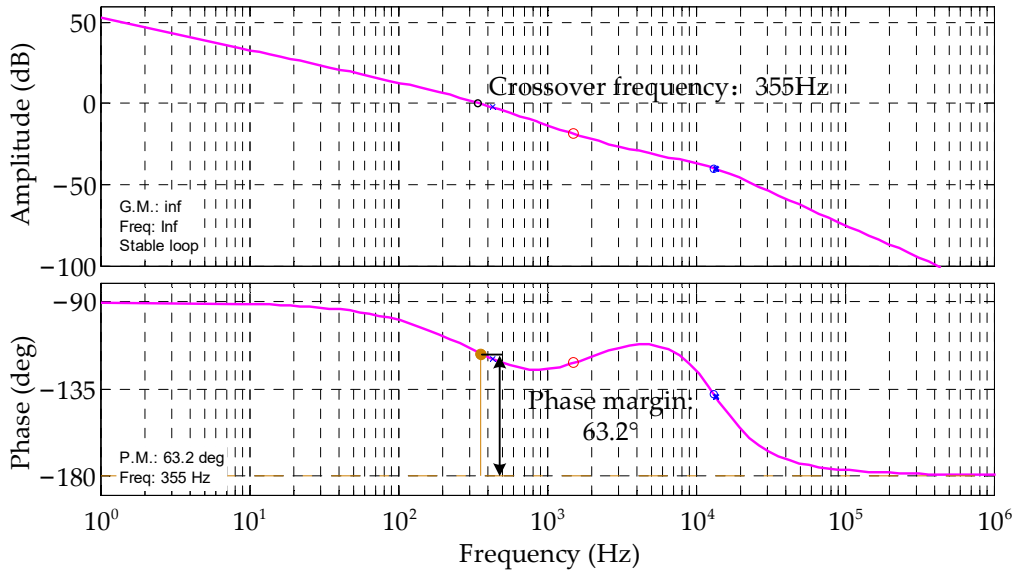


Figure 14. Bode diagram of transfer function with voltage PI controller.

It can be seen from Figure 14 that the LLC resonant converter has a crossing frequency of 355 Hz and a phase margin of 63.2°, which can meet the requirements of the stable regulation of the system and has a relatively stable middle frequency bandwidth. When the LLC resonant converter works in constant voltage mode, the working frequency of the primary side FET has a small variation range, and its output voltage range is 280–420 V. The transfer function of the LLC resonant converter has a small change, which is conducive to the design of a single-loop controller.

5. System Simulation Analysis

The circuit was simulated and analyzed in MATLAB/Simulink to examine the correctness and feasibility of the proposed single-phase and three-phase compatible isolated OBC and the control effect of the improved control strategy under the three-phase input condition. Figure 15 shows the main circuit model and control model built in the simulation software. The simulation parameters of the OBC are shown in Table 2.

Table 2. The OBC simulation parameters.

Simulation Parameter	Value
Filter inductance (L)	1 mH
DC bus capacitance ($C_{dc\text{-}s}$)	2700 μF
DC bus capacitance (C_{dc})	2000 μF
Resonant inductance (L_r)	68 μH
Resonant capacitance (C_r)	37.25 nF
Excitation inductance (L_m)	170 μH
Output holding capacitance (C_o)	4000 μF

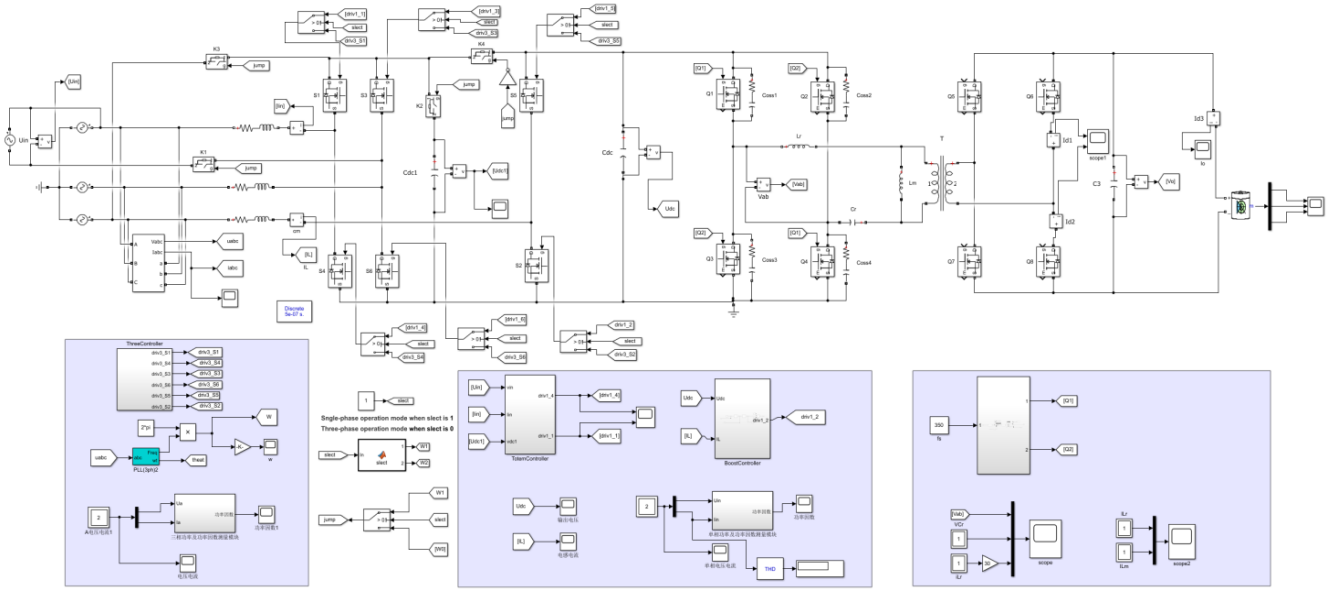


Figure 15. Simulation model of OBC.

5.1. Single-Phase Input Mode Simulation Waveform

(1) Grid current waveform

Figure 16 shows the waveform of the power grid voltage and current under the single-phase input condition. It can be seen from the figure that the sine characteristic of the power grid current is good, the frequency and phase of power grid voltage are the same, and the circuit has a high-power factor. Figure 17 shows the power factor value, which is 0.997, and the correction effect is ideal.

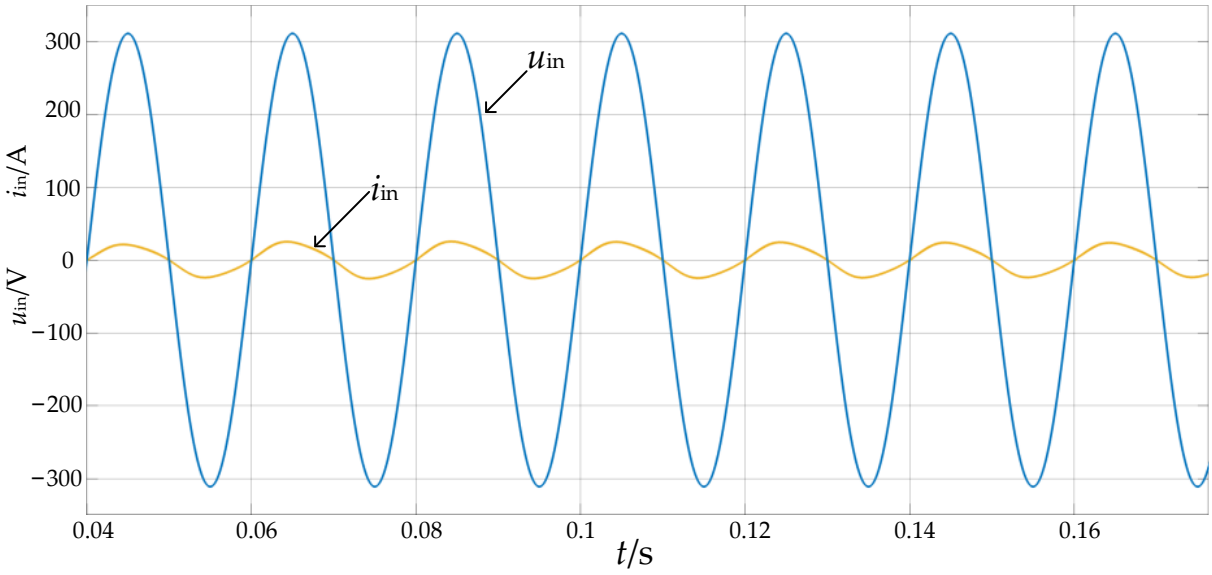


Figure 16. Power grid voltage and current waveform (single-phase input).

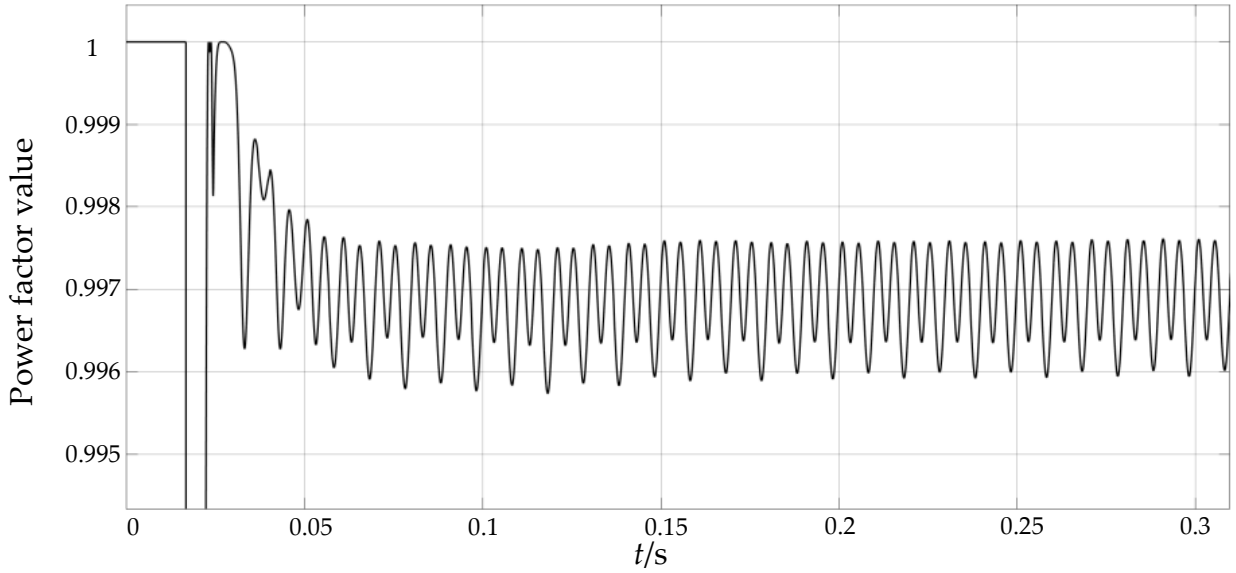


Figure 17. Power factor (single-phase input).

(2) Output voltage waveform

Figure 18 shows the output waveform of DC bus voltage $U_{dc\text{-}s}$. After 0.1 s, the voltage is stable at about 400 V. The control effect is good and meets the design requirements. By amplifying the waveform of the labeled part, the peak-to-peak value of the voltage ripple is about 14 V, which is less than the ripple rate requirement of 5%.

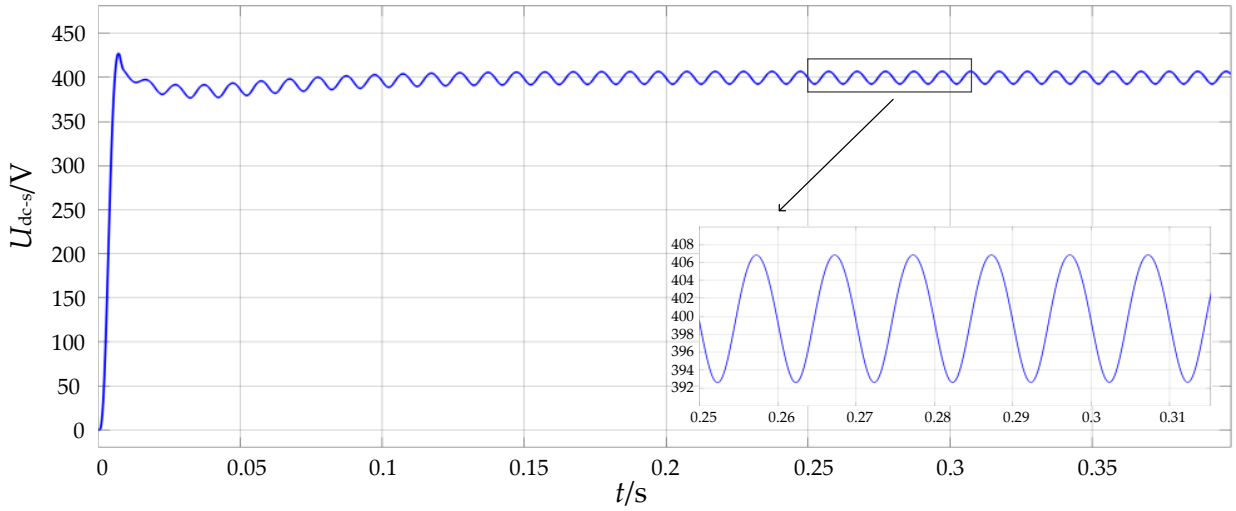


Figure 18. DC bus voltage $U_{dc\text{-}s}$.

Figure 19 shows the output waveform of the front-stage output voltage U_{dc}. The voltage reaches stability after rapidly rising to 700 V and the overshot is small. The voltage ripple peak in the amplification area is about 1 V, which is far less than the ripple rate requirement, indicating that the front-stage circuit meets the design requirements under the single-phase working mode.

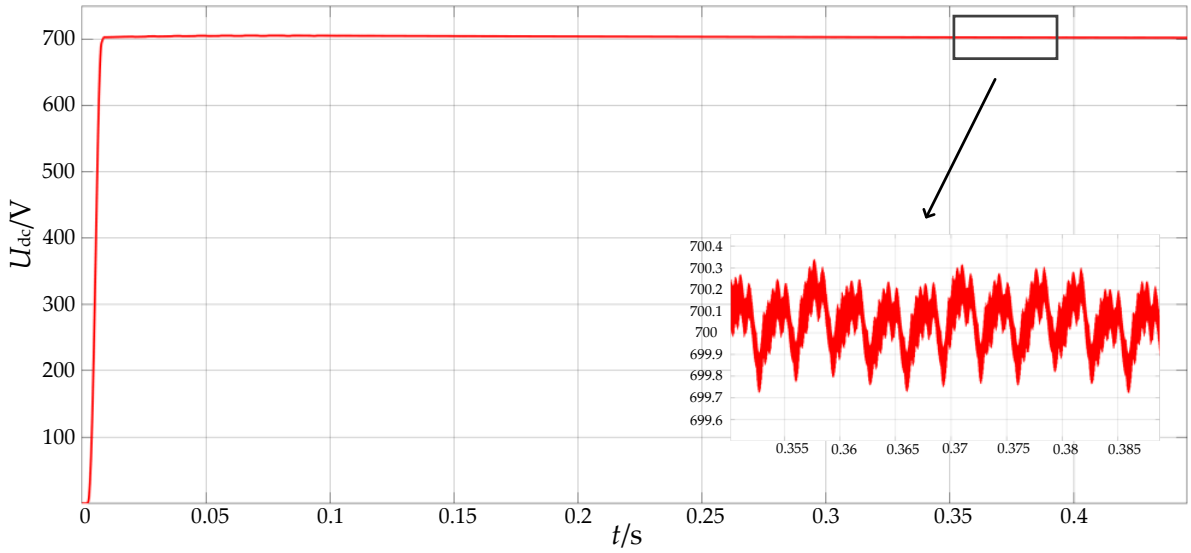


Figure 19. Front-stage output voltage U_{dc}.

5.2. Three-Phase Input Mode Simulation Waveform

(1) Power grid current wave type

As shown in Table 3, under the condition that all parameters are the same, the THD of the input current is compared between current inner loop PI control and current inner loop parallel PI-repetitive control under full load, half load, and 25% load, respectively.

Table 3. Under different load conditions, the THD of the input current obtained by PI control and PI-repetitive control.

Load	Current Inner Loop PI Control	Current Inner Loop PI-Repetitive Control
	THD (%)	THD (%)
Full Load	3.82	2.41
Half Load	6.74	4.36
25% Load	10.82	8.65

It can be seen from Table 3 that under different load conditions, the input current THD with parallel PI-repeat control is always lower than that with PI control. Taking the full load case as an example, the input current waveform and the THD analysis figures of current inner loop with PI control and parallel PI-repetitive control are shown in Figures 20 and 21, respectively. By comparing Figures 20a and 21a, it can be seen that after the controller of current inner loop is improved, the waveform of input current is smoother. Compared with Figures 20b and 21b, it can be seen that the THD of the current inner loop parallel PI-repetitive control is significantly reduced, indicating that the repetitive control has a better inhibition effect on the periodic error.

Figure 22 shows the waveform of the power grid voltage and current under the three-phase input condition. In the steady-state operation, the three-phase input current is a smooth sine wave shape after compound control, and the current distortion is small. The phase of a-phase input current is always consistent with the phase of input voltage. Figure 23 shows the power factor value. It can be seen from the figure that the circuit works in a state of high-power factor, and the power factor value is higher than 0.99, which meets the expected setting requirements.

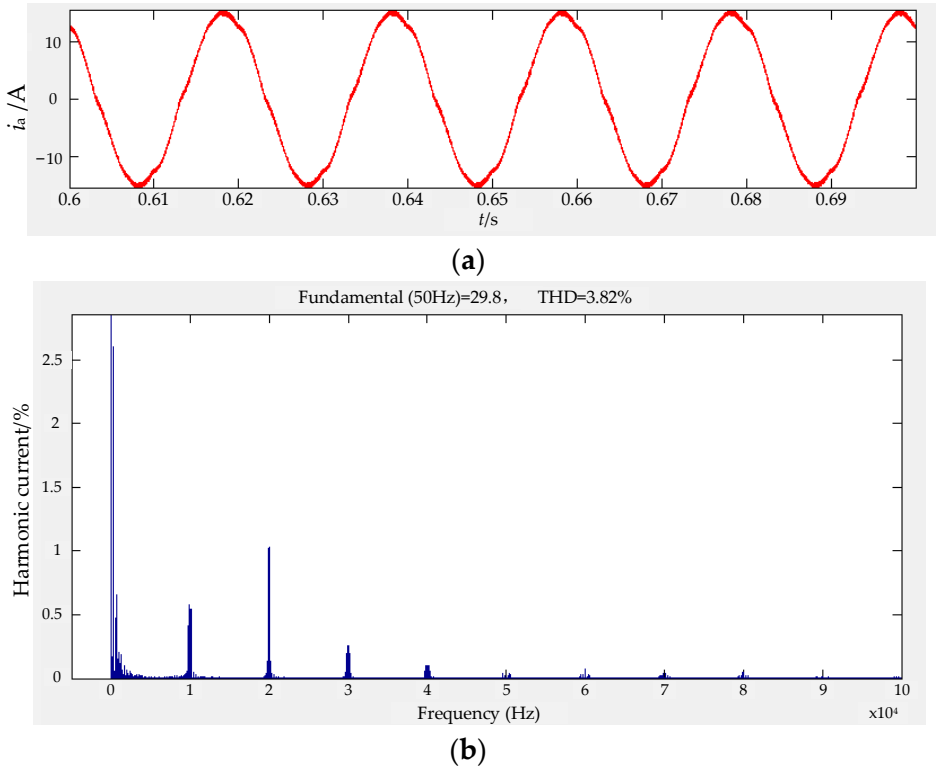


Figure 20. Current inner loop with PI control. (**a**) the waveform of the input current; (**b**) the THD analysis of the input current.

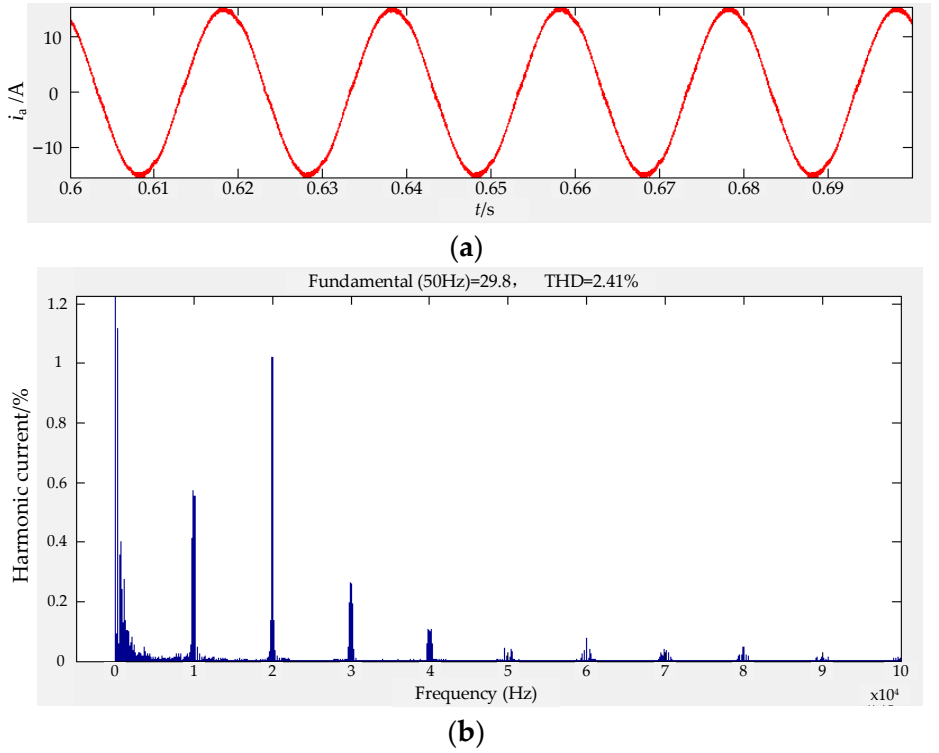


Figure 21. Current inner loop with parallel PI-repetitive control. (**a**) the waveform of the input current; (**b**) the THD analysis of the input current.

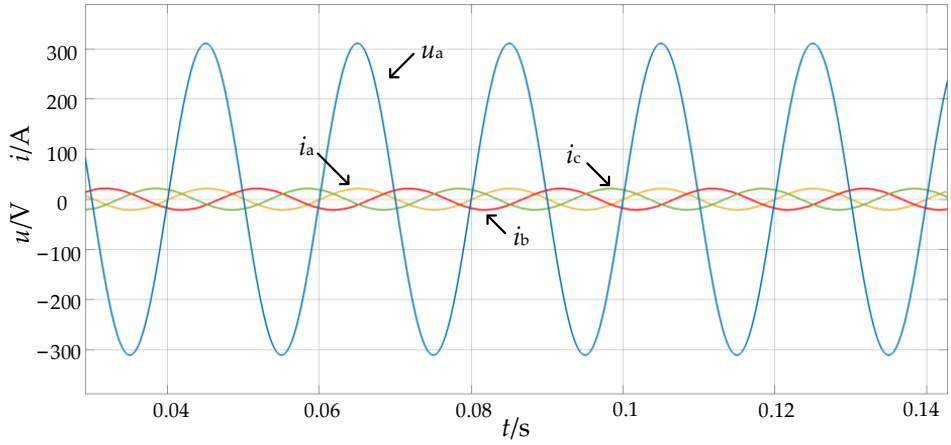


Figure 22. Power grid voltage and current waveform (three-phase input).

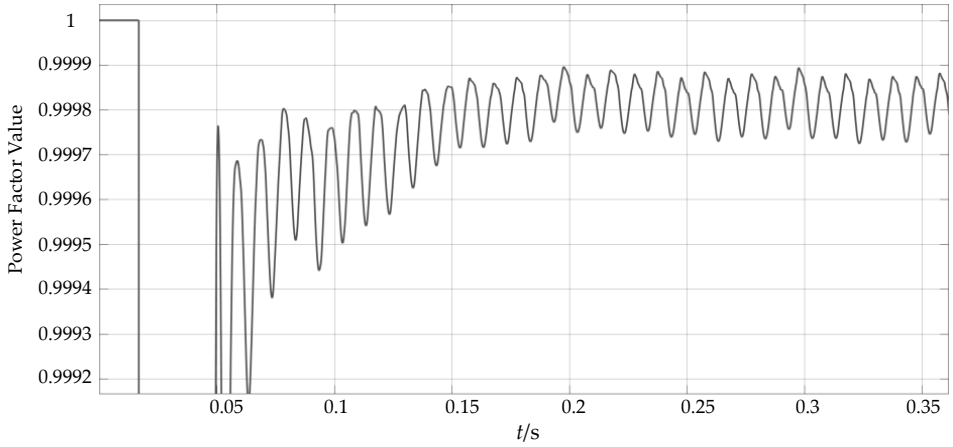


Figure 23. Power factor (three-phase input).

(2) Output voltage waveform

Figure 24 shows the output bus voltage waveform of the three-phase PFC circuit. After about 0.1 s, the system enters a steady state, and the bus voltage follows the given voltage value, and the overshoot is small. At the same time, the ripple value of the voltage is about 0.2 V, which is far less than the ripple rate of 5% and meets the design expectation.

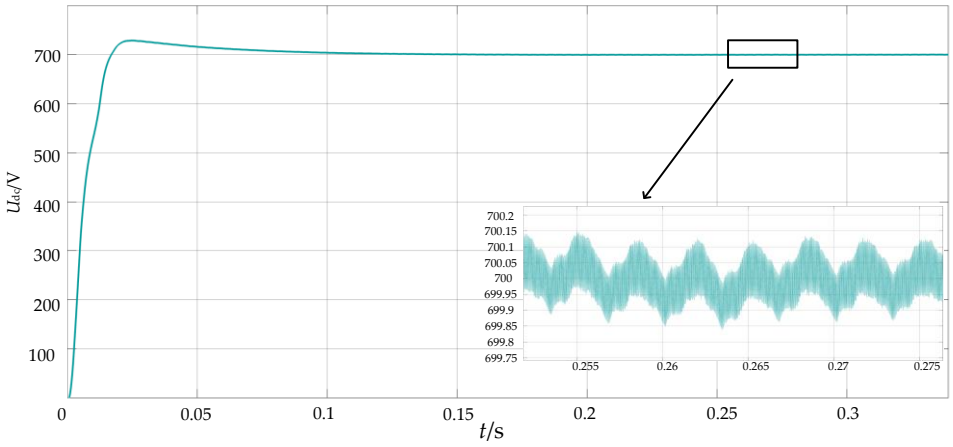


Figure 24. Output bus voltage.

5.3. Simulation Waveform of Rear-Stage Full-Bridge LLC Resonant Converter

Figure 25 shows the driving waveform of the FET of the LLC resonant converter when the charger is working. $U_{gs\text{-}1}$ is the driving signal of Q_1 and Q_3, and $U_{gs\text{-}2}$ is the driving signal of Q_2 and Q_4. On the same bridge arm, the driving signals of two sets of FETs are complementary and have dead time. Figure 26 shows the waveforms of the drain-source voltage and the driving voltage of the MOSFET. After the drain-source voltage U_{ds_1} of the MOSFET drops to zero, the corresponding driving voltage U_{gs_1} begins to rise, and the primary side MOSFET realizes zero voltage switching (ZVS).

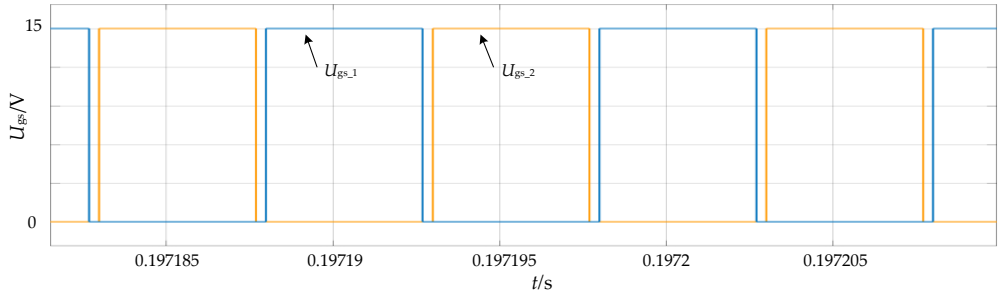


Figure 25. FET driving waveform.

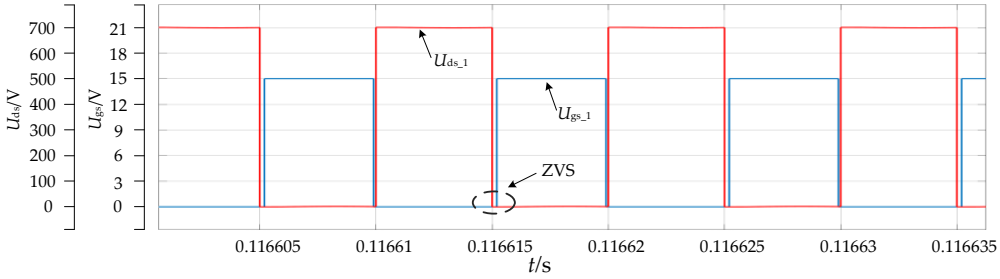


Figure 26. FET drain-source voltage and driving voltage waveform.

Figure 27 shows the waveform of the resonant capacitance voltage U_{Cr}, resonant current I_{Lr}, and the central point voltage U_{ab} of the original side when no load. At this point, the resonant current appears as a triangular wave shape. When the voltage at the central point of the primary side falls, the resonant current is greater than zero, indicating that the primary side FETs have ZVS characteristics.

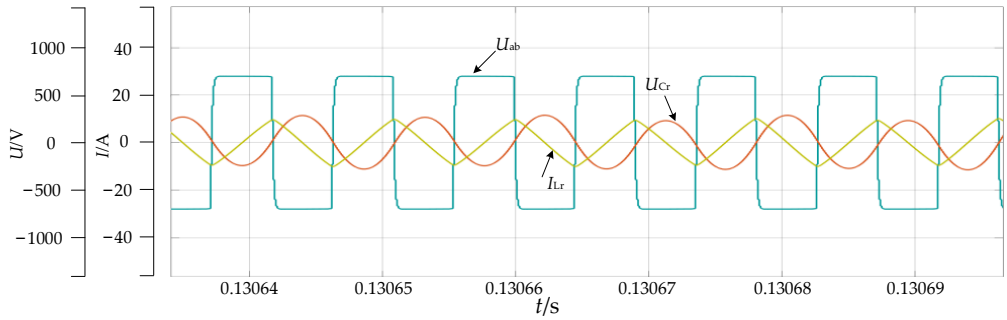


Figure 27. Voltage waveform of the resonant capacitance, resonant current, and the voltage waveform at the center point of the original side of LLC at no-load condition.

Figure 28 shows the waveform of the resonant capacitance voltage U_{Cr}, resonant current I_{Lr}, and the central point voltage U_{ab} of the original side at full load. When the switching frequency of the LLC resonant converter is equal to the resonant frequency, the waveform of the resonant current is approximately sine wave. When the voltage at the central point of the primary side falls, the resonant current is greater than zero, and the resonant cavity presents sensibility, and the primary side FETs can realize ZVS.

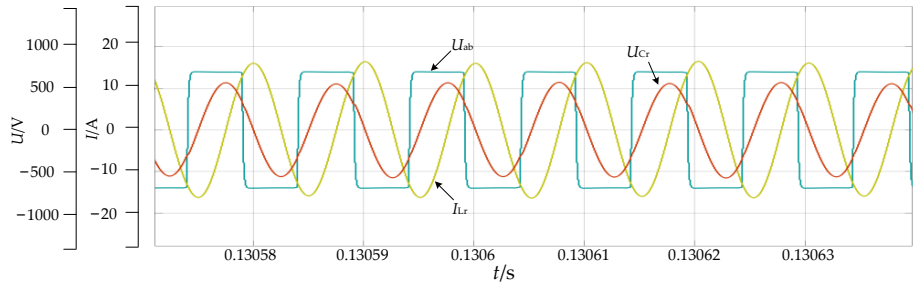


Figure 28. Voltage waveform of the resonant capacitance, resonant current, and the voltage waveform at the center point of the primary side of LLC at full-load condition.

Figure 29 shows the rated output voltage waveform of the LLC resonant converter at full load. At about 0.02 s, the output voltage can reach a stable value of 350 V. When 50% load jump is set at 0.3 s, the output voltage will have a small fluctuation, which can be restored to a stable value after about 0.08 s.

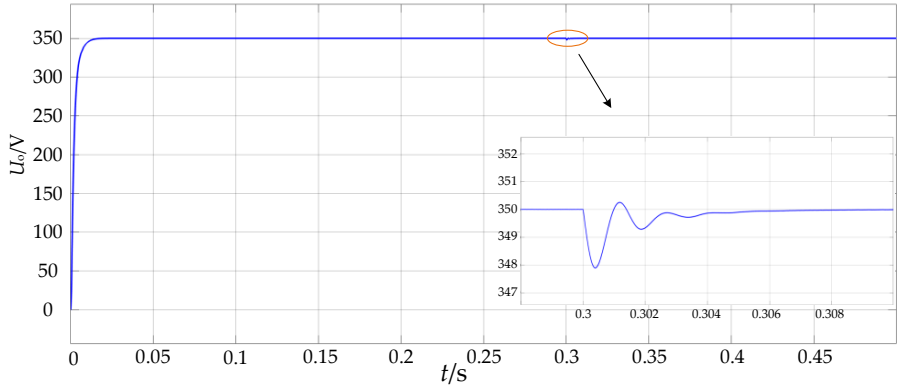


Figure 29. Waveform of rated output voltage.

6. Conclusions

This paper proposes a two-stage isolated OBC that can be compatible with single-phase and three-phase AC voltage inputs. By switching the relay on and off, the front stage can realize the switching of single-phase and three-phase PFC circuits. The rear-stage circuit is the full-bridge LLC resonant converter. When the single-phase voltage input, the front stage circuit is the totem pole PFC circuit cascade boost circuit; When the three-phase voltage input, the front stage circuit is the three-phase six-switch PFC circuit. The control strategy of the three-phase PFC circuit is optimized, and a repetitive controller is introduced into the current inner loop to reduce the harmonic distortion rate of input current. By designing and calculating the parameters of the OBC, the effectiveness of the proposed circuit structure and control strategy is verified in simulation software. The simulation results show that the vehicle charger can realize the single-phase and three-phase AC voltage input and realize the PFC function, the DC output voltage level of the front stage is the same under the two working conditions. At the same time, the rear-stage LLC resonant converter can realize soft switching in the full load range. After the repetitive controller is introduced into the current inner loop of the three-phase PFC circuit, the waveform of input current is improved, and the THD of input current is lower than that of current inner loop PI control under different load conditions, which has a good control effect.

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