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The Effect of Replacing Si-MOSFETs with WBG Transistors on the Control Loop of Voltage Source Inverters

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Abstract: The operation of a voltage source inverter (VSI) depends on its output LC filter and the PWM modulator delay. The VSI model includes serial equivalent resistance based on the resistances of the active inverter bridge transistors, the filter coil winding, and additional PCB elements, such as traces and connectors, in addition to the large equivalent resistances that result from power losses in the coil core and switches. These dynamic power losses depend on the switching frequency and the inverter load. This paper investigates the change in equivalent serial resistance that occurs if the standard Si-MOSFET switches are replaced with wide bandgap (WBG) transistors with correspondingly lower equivalent serial resistance. The paper further investigates how such a change influences the design of the controller, given that replacement of the switches shifts the roots of the closed-loop characteristic equation. Theoretical analyses of the influence of equivalent serial resistance for a multi-input single-output passivity-based controller and a single-input single-output coefficient diagram method are also presented. These analyses are applied to both types of switches. Two methods are used to measure the serial equivalent resistance for a given VSI using Si and WBG switches. The possibility of replacing switches with WBG technology in existing inverters was assessed, and the corresponding controller adjustment that would be required. The theoretical analysis is verified via the use of an experimental VSI.

Keywords: voltage source inverter; passivity-based control; coefficient diagram method; nonlinear load; pulse width modulation; control systems; power conversion systems; wide bandgap transistors



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1. Introduction

Contemporary power converters operate only in switching mode. For this purpose, different types of semiconductor power switches can be used. Power converters of small or medium size most commonly use Si-MOSFET enhancement mode switches. This typically includes converters of up to 10 kW power, although the IEC 62040-3 standards [1] define the boundaries of parameter measurement methods at 3 kW or 4 kW. N-channel switches have a driving threshold voltage of greater than zero, and are much cheaper than wide bandgap (WBG) transistors. They are relatively fast and easy to drive, even when a “current attack” is accounted for. However, n-channel switches have two disadvantages. First, the conduction channel, which is the drain-to-source resistance R_{DS} , has a large resistivity. Second, the inductive load (e.g., the output filter inductance) suffers dynamic power losses when the gate-to-source capacitance C_{gs} is loaded and, critically, the gate-to-drain capacitance C_{gd} at the Miller plateau [2,3], which exists while the MOSFET is within the active region. Key MOSFET parameters include the reverse transfer capacitance $C_{rss} = C_{gd}$, the input capacitance $C_{iss} = C_{gs} + C_{gd}$, and the output capacitance $C_{oss} = C_{gd} + C_{ds}$. Another relevant parameter [2,4] is the gate charge Q_g but the switching power losses occur during loading of the charge Q_{sw} (the charge stored in the gate capacitance from when the gate-source voltage has reached V_{th} until the end of the Miller plateau), where $Q_{sw} < Q_g$, $Q_{sw} > Q_{gd}$.

The static power losses of the R_{DS} resistance are caused by the vertical structure of power MOSFETs, and are proportional to the maximum drain to source V_{DS} voltage: a larger V_{DS} gives a larger R_{DS} . As such, the static and dynamic power losses of an Si-MOSFET switch are determined by R_{DS} and C_{iss} (primarily C_{gd}), which are proportional to the charge Q_g (strictly Q_{sw}). The total power losses can be presented as serial equivalent resistance.

This paper examines the use of different switch technologies for voltage source inverters (VSI). For this purpose, the serial equivalent resistance was measured, including the power losses in the switches and in the core of the output filter coil [5,6], and all other serial resistances, including those of the coil winding, PCB connections, and connectors. The equivalent resistances of different switching devices were compared for a given voltage, current, and switching frequency of the inverter. To do this, an experimental model of the inverter was assembled and programmed. Although this approach cannot isolate the equivalent resistance of only the semiconductor switch, the design of the inverter control loop requires total serial equivalent resistance. The objective of this paper is to demonstrate the dependence of complex equivalent resistance on the type of switch technology used, and determine how this influences control loop design.

In recent years, wide bandgap semiconductor devices have been introduced to the market [7–10]. Many variants of such devices exist, including GaN, GaAs, and SiC technologies. Enhanced channel WBGs have threshold voltages greater than zero; however, certain types of n-channel SiC-MOSFETs require a negative switching-off voltage. Devices with high V_{DS} voltages were chosen because WBG transistors with V_{DS} voltages of less than 100 V have very low R_{DS} resistance, on the order of milliohms. High-electron-mobility transistors (HEMTs), also known as heterostructure FETs (HFET) or modulation-doped FETs (MODFET), are the typical structure of GaAs or GaN technology. Instead of using a doped region as a channel, these FETs incorporate a junction between two materials with different bandgaps—a heterojunction. The primary charge carriers within a MODFET are majority carriers, which have a high speed. GaN-HEMTs can operate with reduced inverter bridge dead times, which results in higher efficiency and lower total harmonic distortion (THD) of the VSI output voltage. Compared to Si-MOSFETs, GaN-HEMTs have lower on-state resistance and smaller capacitances, making them useful for high-speed switching power conversion. One such example of these transistors is Infineon's CoolGaN™, which operates in a voltage range of up to 600 V. Given their high-power performance, GaN-HEMTs will be one of the options tested for the VSI.

A typical approach to creating a normally off device combines high-voltage GaN-HEMT technology and low-voltage Si-MOSFET technology with a cascade device structure. This combination (Cascode Device Structure) offers high reliability and strong performance. Other contemporary power conversion WBG devices are based on SiC technology. Acceptable junction temperatures are higher for SiC devices than for Si devices, engendering their use in automotive applications. The primary advantage of SiC technology is the reduced energy loss within the body diode of SiC-MOSFETs during the reverse recovery phase. This loss accounts for approximately 1% of all energy lost by Si devices. Insulated-gate bipolar transistors (IGBT) typically feature tail currents. However, such currents are absent in SiC-MOSFETs, allowing for faster turn-off and substantially lower energy losses. Given that there is less energy to dissipate, SiC devices can switch at higher frequencies and with improved efficiency. SiC-MOSFETs are designed to be fast and rugged, offering up to ten times greater dielectric breakdown field strength, double the electron saturation velocity, triple the higher energy bandgap, and triple the thermal conductivity of comparable Si devices. Such performance characteristics qualify SiC-MOSFETs for use in automotive and industrial applications. Further advantages include high power conversion efficiency due to reduced power loss, greater power density, higher operating frequency, increased ranges of acceptable operating temperatures, and reduced electromagnetic interference when compared with Si-MOSFETs. Previous disadvantages of SiC-MOSFETs include the requirement for a negative gate-driving voltage for the off-state (for an n-channel device). However, modern devices can have a positive threshold voltage. This is particularly im-

portant for our research, as the equivalent serial resistance will be measured for each type of switching transistor when part of the same 4H bridge VSI experimental model with identical drivers and output filter (a coil with a Super-MSS or FluxSan core [5]). The control changes required due to a reduction in equivalent resistance will be investigated for certain SISO and MISO control methods. There are some papers [11,12] concerning the control in the inverters with WBG transistors, but they do not consider the problem of changing the Si transistors to WBG transistors in the existing inverter. The basic static and dynamic properties of the tested Si, SiC, and GaN transistors are presented in Table 1.

Table 1. Basic properties of the tested transistors.

	V_{DS} [V], I_D [A]	R_{DS} [m Ω] ($T_j = 25^\circ\text{C}$)	C_{iss} , C_{oss} , C_{rss} [pF] ($V_{GS} = 0\text{ V}$, $f = 1.0\text{ MHz}$)
Standard Si-MOSFET IRFP360 (Vishay)	400 V, 23 A	200 ($V_{GS} = 10\text{ V}$, $I_D = 14\text{ A}$)	4500, 1100, 490 ($V_{DS} = 25\text{ V}$)
GaN + Si-MOSFET Cascode Device Structure GAN041-650WSB	650 V, 47.2 A	35 ($V_{GS} = 10\text{ V}$; $I_D = 32\text{ A}$)	1500, 147, 5 ($V_{DS} = 400\text{ V}$)
SiC-MOSFET AIMW120R060M1H	1200 V, 36 A	60 ($V_{GS} = 18\text{ V}$, $I_D = 13\text{ A}$)	1060, 58, 6.5 ($V_{DS} = 800\text{ V}$)

The remainder of this paper is laid out as follows. Section 2 investigates the theoretical influence of equivalent serial resistance on the maximum gains of multi-input single-output passivity-based (MISO-PBC) control. Section 3 investigates the theoretical influence of equivalent serial resistance on the coefficients of single-input single-output coefficient diagram method (SISO-CDM) control, and determines how a change in resistance shifts the poles of the closed-loop system transfer function, designed for different resistances. Section 4 presents Bode plots of measurements of the inverter's control transfer function for the different switch technologies, different coil core materials, and different switching frequencies. The VSI equivalent dynamic serial resistances are then calculated [13]. The power loss serial resistances for the same cases are calculated using the power efficiency measurements of the VSI, and compared with the dynamic serial resistances. Section 5 presents the experimental testing of the VSI using SISO-CDM control for the different types of switches. Section 6 summarizes the results of the previous sections. Section 7 concludes the paper, and considers the feasibility of changing VSI switch technology when using SISO-CDM control.

2. The Theoretical Influence of Equivalent Serial Resistance on the MISO-PBC Control Loop

As shown in Figure 1, the load current of an MISO controller is treated primarily as an independent disturbance (e.g., [14,15]). Although this approach allows the load impedance to be eliminated from the control law, it also eliminates feedback from the output voltage to the load current. In some cases, this simplification changes the locus of the characteristic equation poles for a closed-loop system [16]. However, this does not usually result in instability. Hence, the modulator model consists of the following: the state variables: inductor current i_{LF} and output voltage v_{OUT} ; an independent disturbance, load current i_{OUT} ; and delay equal to T_s . For a high switching frequency, the delay can be omitted.

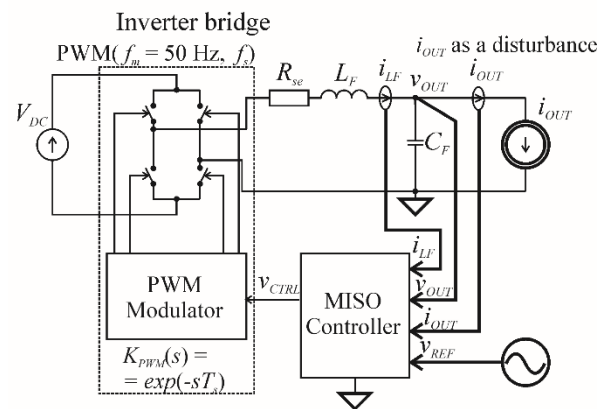


Figure 1. MISO control of a VSI. Load current i_{OUT} is treated as an independent disturbance.

The influence of the equivalent serial resistance R_{se} must now be determined, which varies with the use of different switching technologies, on the design of the control loop. The system is passive whenever the energy supplied to the system exceeds the stored energy. Within an inverter, energy is stored in two non-dissipative components—the filter coil and the filter capacitor. The energy stored within a system is described by the Hamiltonian function $H(x)$ (also known as the Lyapunov function [17]). The Hamiltonian function of the error vector $\mathbf{e}$ is Equation (1).

$$H(\mathbf{e}) = \frac{1}{2}(L_F(i_{LF} - i_{LFref})^2 + C_F(v_{OUT} - v_{OUTref})^2) = \frac{1}{2}\mathbf{e}^T \mathbf{P}^{-1} \mathbf{e} \quad (1)$$

where

$$\mathbf{e} = \begin{bmatrix} L_F(i_{LF} - i_{LFref}) \\ C_F(v_{OUT} - v_{OUTref}) \end{bmatrix}, \quad \mathbf{P}^{-1} = \begin{bmatrix} 1/L_F & 0 \\ 0 & 1/C_F \end{bmatrix} \quad (2)$$

The equilibrium of a closed-loop system is asymptotically stable [18], and is achieved if $H(\mathbf{e})$ has a minimum at $\mathbf{x} = \mathbf{x}_{ref}$ (3):

$$\left. \frac{\partial H(\mathbf{e})}{\partial \mathbf{x}} \right|_{\mathbf{x}=\mathbf{x}_{ref}} = 0, \quad \left. \frac{\partial^2 H(\mathbf{e})}{\partial \mathbf{x}^2} \right|_{\mathbf{x}=\mathbf{x}_{ref}} > 0, \quad \text{where } \mathbf{x} = [L_F i_{LF} \quad C_F v_{OUT}]^T. \quad (3)$$

The system is passive if the time derivative of $H(\mathbf{e})$ is negative Equation (4):

$$\frac{dH(\mathbf{e})}{dt} < 0. \quad (4)$$

The control law of improved PBC v.2 (IPBC2) in single-phase inverters is based on the creation of a control law for interconnection and damping assignment PBC (IDAPBC) [14,18,19], Equations (9) and (10). The IPBC2 control law can be calculated [20,21] as the difference between the equation for a closed-loop PBC system (5) and the equation for an open-loop PBC system (6).

$$\dot{\mathbf{e}} = [\mathbf{J} - (\mathbf{R} + \mathbf{R}_a)] \mathbf{P}^{-1} \mathbf{e}, \quad (5)$$

$$\dot{\mathbf{x}} = [\mathbf{J} - \mathbf{R}] \mathbf{P}^{-1} \mathbf{x} + \begin{bmatrix} V_{DC} \\ 0 \end{bmatrix} m + \begin{bmatrix} 0 \\ -1 \end{bmatrix} i_{OUT} \quad (6)$$

where the interconnection matrix $\mathbf{J}$, the damping matrix $\mathbf{R}$, and the PBC controller matrix $\mathbf{R}_a$, are defined as Equation (7)

$$\mathbf{J} = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}, \quad \mathbf{R} = \begin{bmatrix} R_{se} & 0 \\ 0 & 0 \end{bmatrix}, \quad \mathbf{R}_a = \begin{bmatrix} R_i & 0 \\ 0 & K_v \end{bmatrix}. \quad (7)$$

Note that $\mathbf{R}_a$ includes the injected damping values—the current error gain R_i and the voltage error conductive gain K_v . Subtracting Equation (6) from Equation (5) gives the control law Equation (8):

$$\dot{\mathbf{e}} - \dot{\mathbf{x}} = [\mathbf{J} - \mathbf{R}]\mathbf{P}^{-1}(\mathbf{e} - \mathbf{x}) - \mathbf{R}_a\mathbf{P}^{-1}\mathbf{e} - \begin{bmatrix} V_{DC} \\ 0 \end{bmatrix}m - \begin{bmatrix} 0 \\ -1 \end{bmatrix}i_{OUT} \quad (8)$$

The PWM registers are set in one period, and the pulse widths are set in the following switching period. If the switching frequency is sufficiently high (25,600 Hz or greater), the switching period delay T_s of the digital PWM modulator can be omitted. The final form of the IPBC2 control law is then Equations (9) and (10):

$$v_{CTRL}(t) = L_F di_{LRef}/dt + (R_{se} + R_i)i_{LRef} + v_{OUTref} - R_i i_{LF}, \quad (9)$$

$$i_{LRef} = C_F dv_{OUTref}/dt - K_v(v_{OUT} - v_{OUTref}) + i_{OUT}. \quad (10)$$

IPBC requires that appropriate values of the injected resistance R_i (inductor current gain) and conductance K_v (output voltage gain) be chosen. The values $R_{se} + R_i$ and the value of K_v should be positive to fulfil the requirements of the negative real components of the roots $\lambda_{1,2}$ of the characteristic polynomial of the closed-loop IPBC system [21]: Equation (11)

$$\lambda_{1,2} = \frac{\left\{ -[(R_{se} + R_i)C_F + L_F K_v] \pm \sqrt{[(R_{se} + R_i)C_F + L_F K_v]^2 - 4L_F C_F [1 + (R_{se} + R_i)K_v]} \right\}}{2L_F C_F} \quad (11)$$

This equation does not provide the upper boundaries for the current and voltage gains. The higher the gains, the greater the convergence of the error tracking. However, IPBC2 gain values that are too high cause oscillations of the VSI output voltage. This is because the control voltage increases too quickly when compared to the speed of the PWM. This creates a saturation-like effect within the control loop. For a higher switching frequency with correspondingly faster PWM, higher gains can be used [22]. Estimating PWM speed can be difficult. For double-edge symmetrical regular modulation, the PWM signal increases as $V_{DC}/(T_s/2)$ [17]. However, the fastest change of modulation in one switching period is V_{DC} during one T_s (V_{DC}/T_s), what was taken in care of in [22]. All the time, the T_s delay of the modulator is omitted.

The mutual dependency of the two PBC controller gains is highly important. During a single sampling period, the approximation $d(v_{OUTref})/dt \approx 0$ can be made. Therefore, from Equations (10), (12)–(14) were obtained:

$$i_{LRef}(kT_s) \approx -K_v[v_{OUT}(kT_s) - v_{OUTref}(kT_s)] + i_{OUT}(kT_s), \quad (12)$$

$$i_{LRef}(kT_s) \approx \left(\frac{1}{R_{LOAD}} - K_v \right) v_{OUT}(kT_s) + v_{OUTref}(kT_s), \quad (13)$$

$$\frac{di_{LREF}(kT_s)}{dt} \approx \left(\frac{1}{R_{LOAD}} - K_v \right) \frac{dv_{OUT}(kT_s)}{dt}. \quad (14)$$

From Equations (9), (13)–(16) were obtained:

$$\frac{dv_{CTRL}(kT_s)}{dt} \approx L_F \frac{d^2 i_{LRef}(kT_s)}{dt^2} + (R_{se} + R_i) \frac{di_{LRef}(kT_s)}{dt} - R_i \frac{di_{LF}(kT_s)}{dt}, \quad (15)$$

$$\frac{dv_{CTRL}(kT_s)}{dt} \approx L_F \left(\frac{1}{R_{LOAD}} - K_v \right) \frac{d^2 v_{OUT}(kT_s)}{dt^2} + (R_{se} + R_i) \left(\frac{1}{R_{LOAD}} - K_v \right) \frac{dv_{OUT}(kT_s)}{dt} - R_i \frac{di_{LF}(kT_s)}{dt} \quad (16)$$

During a single switching cycle, for $R_{LOAD} \gg 1/(2\pi f_s C_F)$, the following approximations, Equations (17) and (18), can be made:

$$\left. \frac{di_{LF}(kT_s)}{dt} \right|_{\max, \min} \approx \pm \frac{V_{DC}}{L_F}, \quad \left. \frac{dv_{OUT}(kT_s)}{dt} \right|_{\max} \approx \frac{i_{LF}}{C_F}, \quad \left. \frac{d^2 v_{OUT}(kT_s)}{dt^2} \right|_{\max} \approx \frac{d}{dt} \left(\frac{i_{LF}}{C_F} \right) \bigg|_{\max} \approx \pm \frac{V_{DC}}{L_F C_F}, \quad (17)$$

$$\left| \frac{dv_{CTRL}(kT_s)}{dt} \right|_{\max} \approx K_v [L_F + (R_i + R_{se}) T_s] \frac{V_{DC}}{L_F C_F} + R_i \frac{V_{DC}}{L_F}. \quad (18)$$

From Equation (18), the final boundary on PBC gains, R_i and K_v Equation (19), was obtained:

$$K_v [1 + (R_i + R_{se}) \frac{T_s}{L_F}] \frac{1}{C_F} + R_i \frac{1}{L_F} < f_s \quad (19)$$

Equation (19) demonstrates the influence of switching frequency $f_s = 1/T_s$ and equivalent serial resistance R_{se} on the maximum values of the IPBC2 gains. These relationships are portrayed in Figure 2. The lower the value of T_s/L_F , the lower the influence of the equivalent serial resistance R_{se} . For high values of f_s , the influence of R_{se} will be negligible, and the maximum voltage and current gains will be higher [22]. This demonstrates the weak influence of equivalent serial resistance on maximum gains.

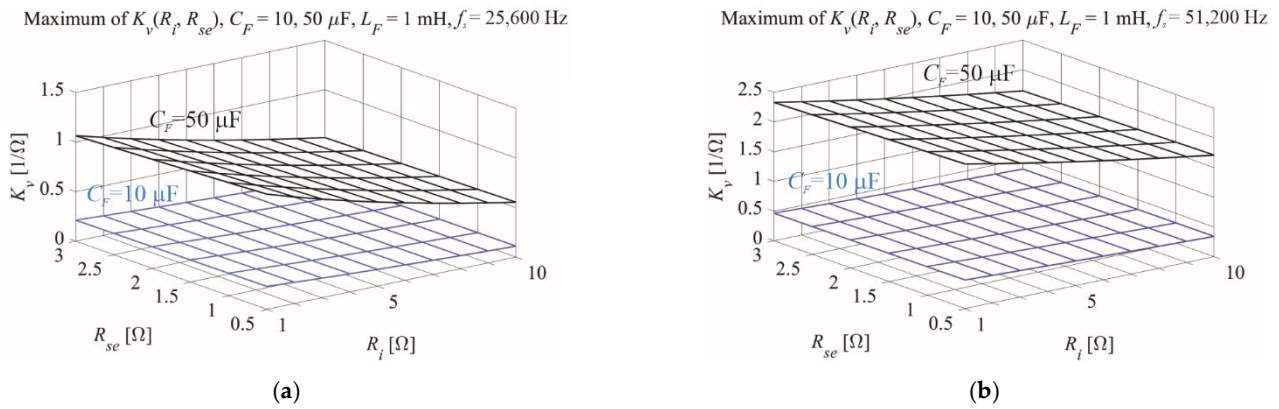


Figure 2. The dependence of maximum voltage gain K_v on current gain R_i and equivalent serial resistance R_{se} for (a) $f_s = 25,600$ Hz and (b) $f_s = 51,200$ Hz. In practical terms, the gains do not depend on R_{se} for the assigned VSI parameters, $L_F = 1$ mH and $C_F = 50 \mu F$.

The presented gain values are derived from simulation models featuring a reference voltage amplitude of unity, a bridge supplied by V_{DC} , and controller input signals from the inverter model output scaled by a factor of $1/V_{DC}$. Amplification of the voltage trace was adjusted for the real inverter such that for the nominal amplitude of the output voltage fundamental harmonic for a 50Ω load, for the ADC range -4095 – 4095 , provided a value of 3000 units. The 3000 output value was adjusted for the unity voltage scaling ratio. For the 50Ω load resistance, which was assumed to be nominal, the amplification of the current trace was adjusted until the ADC provided a reading of 2000 units. This gave an output current scaling ratio of $(3000/2000)/50 = 0.03$. For a small output capacitance of $1 \mu F$, it was performed the same adjustment procedure was performed for the inductor current trace, and the same current scaling ratio of 0.03 was obtained. The voltage and current scaling factors require careful adjustment because they are multiplied by the PBC controller gains. For the experimental inverter, reference amplitudes of 1640 and 820 for the 25,600 Hz and 51,200 Hz switching frequencies, respectively, were used. For each set of values, 3000 units were used for the voltage and 2000 units for the current as nominal ADC values. Therefore, the gain scaling factors between simulation and experiment were $r(25,600 \text{ Hz}) = 3000/1640 = 1.829$, and $r(51,200 \text{ Hz}) = 3000/820 = 3.659$ for 25,600 Hz and 51,200 Hz, respectively. The scaled gains were assigned as $R_{iinverter} = R_{isym}/r$ and $K_{vinverter} = K_{vsym}/r$. The MISO-PBC system is robust against a decrease in serial equivalent resistance. As such, this paper presents no further research on the subject.

3. The Theoretical Influence of Equivalent Serial Resistance Influence on the SISO-CDM Control Loop

A schematic of the SISO system is presented in Figure 3 [23–26].

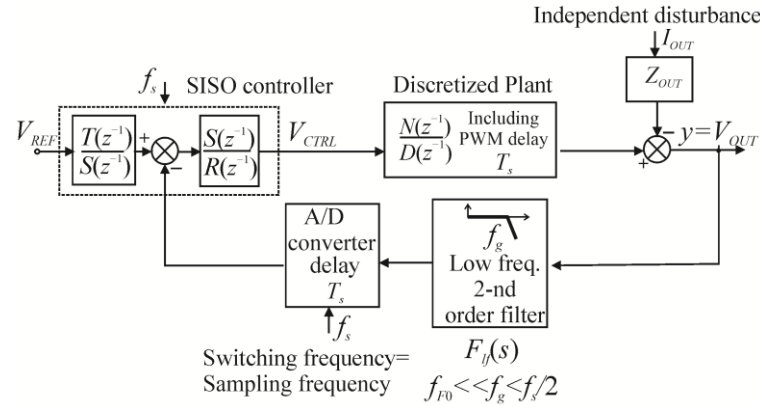


Figure 3. An advanced discretized SISO system.

The design of the Manabe CDM [23–26] controller (T , S , and R polynomials) requires the assumed values of the coefficients of the closed-loop characteristic equation. In the simplest case of the Manabe standard form, these coefficients are defined as functions of the time constant τ of the closed-loop system. The output voltage of a closed-loop system is given by Equation (20):

$$v_{OUT}(z^{-1}) = \frac{TN}{RD + SN} v_{REF}(z^{-1}) - \frac{Z_{OUT}RD}{RD + SN} I_{OUT}(z^{-1}), \quad (20)$$

where S includes the additional loop delay T_s measured from the Bode plots of the loop. The characteristic equation of a closed-loop system in Manabe standard form is given by Equation (21):

$$P(z^{-1}) = R(z^{-1})D(z^{-1}) + S(z^{-1})N(z^{-1}) = \sum_{i=0}^n p_{zi}z^{-i}. \quad (21)$$

The VSI is initially modeled as an output $L_F C_F$ filter, and described by the state equations

$$\mathbf{x} = [v_{OUT} \quad i_{LF} \quad i_{OUT}]^T, \quad (22)$$

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u}, \quad (23)$$

$$\mathbf{A} = \begin{bmatrix} 0 & \frac{1}{C_F} & -\frac{1}{C_F} \\ -\frac{1}{L_F} & -\frac{R_{LF}}{L_F} & 0 \\ 0 & 0 & 0 \end{bmatrix}, \quad \mathbf{B} = \begin{bmatrix} 0 \\ \frac{1}{L_F} \\ 0 \end{bmatrix}. \quad (24)$$

The state equations are solved for a single k -th switching period T_s , for double edge 3-level PWM, with a switching-on time period T_{ONk} . The dependence of $\mathbf{x}_{k+1}$ on T_{ONk} is described by linearized exponential function Equations (25)–(28) [21]:

$$\mathbf{x}_{k+1} = \mathbf{A}_D \mathbf{x}_k + \mathbf{G}_D T_{ONk}, \quad (25)$$

$$\mathbf{A}_D = e^{\mathbf{A}T_s} = \Phi(T_s) = L^{-1}[(s\mathbf{I} - \mathbf{A})^{-1}] \Big|_{t=T_s}, \quad (26)$$

$$\mathbf{G}_D = e^{\mathbf{A}T_s/2} \mathbf{B} V_{DC} = \Phi(T_s/2) \mathbf{B} V_{DC}, \quad (27)$$

$$\mathbf{A}_D = \Phi(T_s) = \begin{bmatrix} \phi_{11} & \phi_{12} & \phi_{13} \\ \phi_{21} & \phi_{22} & \phi_{23} \\ \phi_{31} & \phi_{32} & \phi_{33} \end{bmatrix}, \mathbf{G}_D = \begin{bmatrix} g_{11} \\ g_{21} \\ g_{31} \end{bmatrix}, \quad (28)$$

where

$$\begin{aligned} \zeta_F &= \frac{1}{2} R_{se} \sqrt{\frac{C_F}{L_F}}; \omega_{F0} = \frac{1}{\sqrt{L_F C_F}}, \\ \phi_{11} &= [\cos(\omega_{F0} T_s) + \zeta_F \sin(\omega_{F0} T_s)] \exp(-\zeta_F \omega_{F0} T_s), \\ \phi_{12} &= \frac{1}{\omega_{F0} C_F} \sin(\omega_{F0} T_s) \exp(-\zeta_F \omega_{F0} T_s), \\ \phi_{13} &= -\phi_{12} + R_{LF}(\phi_{11} - 1), \\ \phi_{21} &= -\frac{C_F}{L_F} \phi_{12}, \\ \phi_{22} &= [\cos(\omega_{F0} T_s) - \zeta_F \sin(\omega_{F0} T_s)] \exp(-\zeta_F \omega_{F0} T_s), \\ \phi_{23} &= 1 - \phi_{11}; \phi_{31} = 0; \phi_{32} = 0 \phi_{33} = 1, \\ g_{11} &= V_{DC} \omega_{F0} \sin(\omega_{F0} \frac{T_s}{2}) \exp(-\zeta_F \omega_{F0} \frac{T_s}{2}), \\ g_{21} &= \frac{V_{DC}}{L_F} [\cos(\omega_{F0} \frac{T_s}{2}) - \zeta_F \sin(\omega_{F0} \frac{T_s}{2})] \exp(-\zeta_F \omega_{F0} \frac{T_s}{2}), \\ g_{31} &= 0. \end{aligned}$$

The gain of the VSI, with double edge PWM and a digital modulator inserting a switching period delay T_s , is given by Equation (29):

$$K_{VSI} = \frac{N(z^{-1})}{D(z^{-1})} = \frac{a_2 z^{-2} + a_3 z^{-3}}{1 + b_1 z^{-1} + b_2 z^{-2}}, \quad (29)$$

where

$$a_2 = \frac{T_s}{V_{DC}} g_{11}; a_3 = \frac{T_s}{V_{DC}} (\phi_{12} g_{21} - \phi_{22} g_{11}); b_1 = -(\phi_{11} + \phi_{22}); b_2 = \phi_{11} \phi_{22} - \phi_{12} \phi_{21}.$$

In our system, the load current I_{OUT} was treated as an independent disturbance, although it can be treated as a state variable. For a system with a disturbance, the degrees of R and S are greater than or equal to $n - 1$, where n is the degree of D . The second degree of S and the third degree of R were assumed because of the additional loop delay in Equation (30):

$$S(z^{-1}) = z^{-1} \sum_{i=0}^2 s_i z^{-i}, R(z^{-1}) = \sum_{i=0}^3 r_i z^{-i}, r_0 = 1. \quad (30)$$

Equation (21) is Diophantine; to obtain equal r_i and s_i coefficients for equal degrees of z , the following equation should be solved with $r_0 = p_0 = 1$ Equation (31):

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ b_1 & 1 & 0 & 0 & 0 & 0 \\ b_2 & b_1 & 1 & a_2 & 0 & 0 \\ 0 & b_2 & b_1 & a_3 & a_2 & 0 \\ 0 & 0 & b_2 & 0 & a_3 & a_2 \\ 0 & 0 & 0 & 0 & 0 & a_3 \end{bmatrix} \begin{bmatrix} r_1 \\ r_2 \\ r_3 \\ s_0 \\ s_1 \\ s_2 \end{bmatrix} = \begin{bmatrix} p_{z1} - b_1 \\ p_{z2} - b_2 \\ p_{z3} \\ p_{z4} \\ p_{z5} \\ p_{z6} \end{bmatrix}. \quad (31)$$

The coefficients p_i of Manabe standard form for a continuous system are required for the 6th degree of $P(s)$. They are given by:

$$\begin{aligned} p_0(s^0) &= 1, p_1(s^1) = p_0 \tau, p_2(s^2) = 0.4 p_0 \tau^2, p_3(s^3) = 0.08 p_0 \tau^3, p_4(s^4) = 0.008 p_0 \tau^4, \\ p_5(s^5) &= 0.0004 p_0 \tau^5, p_6(s^6) = 0.00001 p_0 \tau^6, \end{aligned}$$

where τ is the time constant of a closed-loop system. Satisfactory results were obtained for the control of the tested experimental model, with $\tau = 8T_s$.

Using the zero-order hold method, let us define a discrete-time transfer function using the *c2d* MATLAB function with a discretization cycle $T_s = 1/25600$ s [14] (32):

$$K(z) = c2d\left(\frac{1}{\sum_{i=0}^6 p_i(s)s^i}, T_s\right) = \frac{\sum_{i=0}^6 w_i(z)z^{-i}}{\sum_{i=0}^6 p_{zi}(z^{-1})z^{-i}}. \quad (32)$$

Consider the case for which $\tau = 8T_s$ ($T_s = 1/25600$ s):

$$p_{z0}(z^0) = 1, p_{z1}(z^{-1}) = -2.3166, p_{z2}(z^{-2}) = 2.0436, p_{z3}(z^{-3}) = -0.8693, p_{z4}(z^{-4}) = 0.2126, p_{z5}(z^{-5}) = -0.0452, p_{z6}(z^{-6}) = 0.0067$$

The final calculation enables $v_{OUT} = v_{REF}$ to hold in the steady state if the following condition is met (33):

$$t_0 = \frac{P(z=1)}{N(z=1)} = \frac{V_{DC}}{T_s} \frac{1 + p_{z1} + p_{z2} + p_{z3} + p_{z4} + p_{z5} + p_{z6}}{\varphi_{12}g_{21} + (1 - \varphi_{22})g_{11}}. \quad (33)$$

For our experimental model, $L_F = 2$ mH, $C_F = 51$ μ F, and $R_{se} = 1$ Ω was assumed. Using these values, and with $\tau = 8T_s$, the solutions of Equation (31) are:

$$r_0 = 1, r_1 = -0.3659, r_2 = 0.3644, r_3 = 0.0709, s_0 = 16.7152, s_1 = -16.5485, s_2 = 0.9253, t_0/V_{DC} = 2.1612$$

The coefficient t_0 can be adjusted individually. The resultant difference control law is:

$$v_{CTRL}(k) = -r_1 v_{CTRL}(k-1) - r_2 v_{CTRL}(k-2) - r_3 v_{CTRL}(k-3) + t_0 v_{REF} - s_0 v_{OUT}(k-1) - s_1 v_{OUT}(k-2) - s_2 v_{OUT}(k-3) \quad (34)$$

Figure 4 shows the shifts in the poles of the closed-loop CDM system (with $L_F = 2$ mH, $C_F = 51$ μ F, and $\tau = 8T_s$) caused by changes in R_{se} . Figure 4a,b shows a system that was configured for $R_{CDM} = R_{se} = 2$ Ω , before R_{se} was decreased to 0.4 Ω . Figure 4c,d shows a system that was configured for $R_{CDM} = 0.4$ Ω , before R_{se} resistance was increased to 2 Ω . Figure 4a,c are for $S(z^{-1})$ order 2, $R(z^{-1})$ order 2, $P_z(z^{-1})$ order 5, while Figure 4b,d for $S(z^{-1})$ order 2, $R(z^{-1})$ order 3, $P_z(z^{-1})$ order 6, which is required if the additional delay of the plant was taken into care. The examples presented in Figure 4a,c show that for the lower order of the controller, SISO-CDM control is not robust to a decrease or increase in the equivalent serial resistance, and the system can be unstable, depending on the time constant τ . Figure 4b,d shows that the system is more robust for the higher order of the controller for the same time constant τ . The SISO-CDM control was chosen for further investigation. The time constant of $\tau = 8T_s$ was chosen because lower values caused small oscillations in the nonlinear rectifier RC for all types of transistors. It is difficult to analytically estimate changes in the dynamic properties of the inverter following the replacement of the transistors in the bridge, as the poles are shifted within the unity circle. As such, tests of the experimental model were conducted.

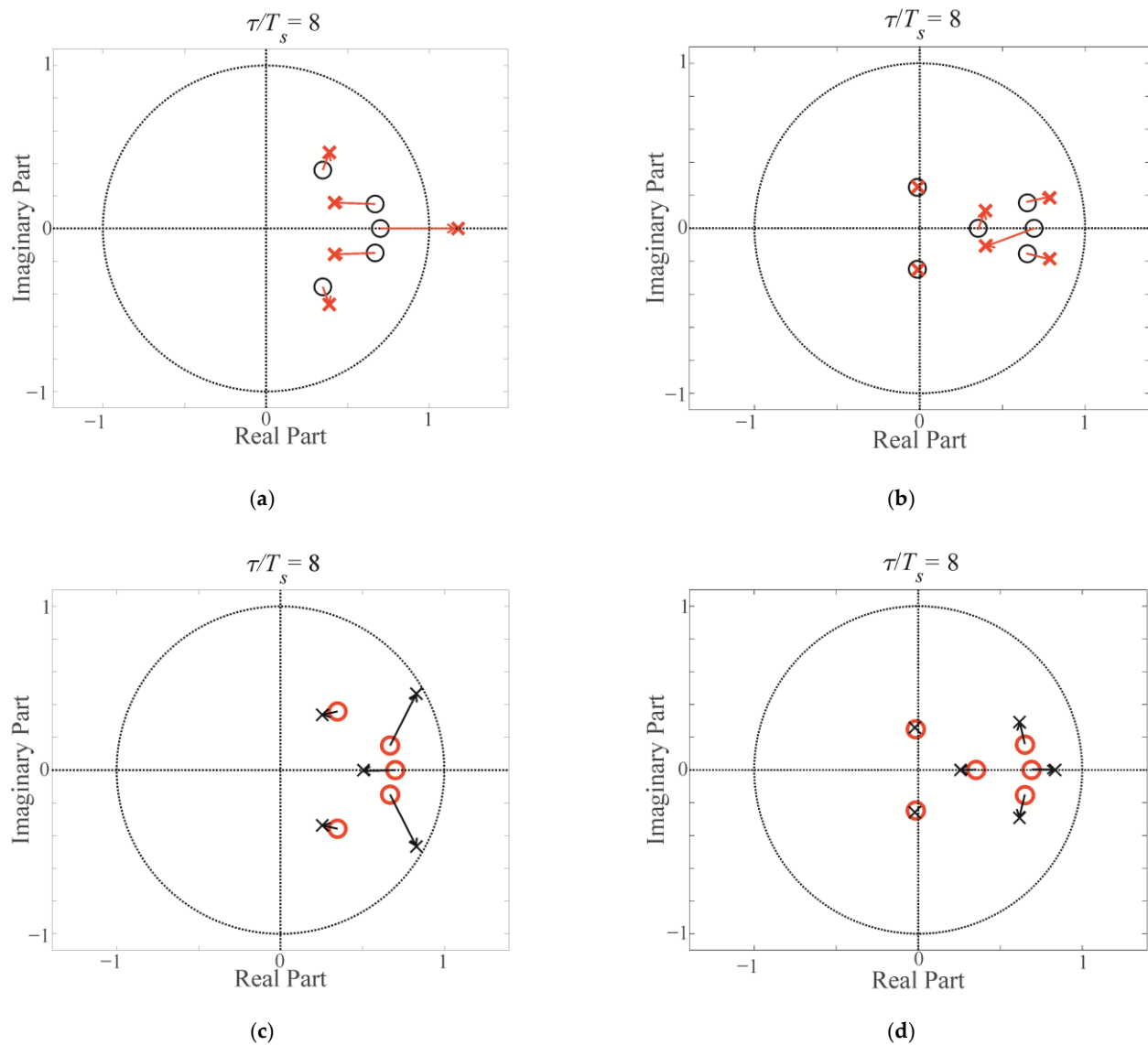


Figure 4. Pole shifts of the closed-loop CDM system (with $L_F = 2$ mH, $C_F = 51$ μ F, and $\tau = 8T_s$), showing (a,b) a system configured for $R_{CDM} = R_{se} = 2$ Ω (black circles) subjected to a decrease in R_{se} to 0.4 Ω (red crosses), and (c,d) a system configured for $R_{CDM} = R_{se} = 0.4$ Ω (red circles) subjected to an increase in R_{se} to 2 Ω (black crosses); (a) $S(z^{-1})$ order 2, $R(z^{-1})$ order 2, $P_z(z^{-1})$ order 5; (b) $S(z^{-1})$ order 2, $R(z^{-1})$ order 3, $P_z(z^{-1})$ order 6 (given additional plant delay); (c) $S(z^{-1})$ order 2, $R(z^{-1})$ order 2, $P_z(z^{-1})$ order 5; (d) $S(z^{-1})$ order 2, $R(z^{-1})$ order 3, $P_z(z^{-1})$ order 6 (given additional plant delay).

4. The Difference in the Static and Dynamic Equivalent Serial Resistance of the Same VSI When Using Si and WBG Switches

As shown in Figure 5, the elementary VSI model is based on the output filter transfer function and the PWM modulator transfer function. The output filter transfer function is given by Equation (35):

$$K_{CTRL}(s) = F_{LC}(s) = \frac{\omega_{F0}^2}{[s^2 + 2\zeta_F \omega_{F0}s + (1 + R_{se}/R_{LOAD})\omega_{F0}^2]} \quad (35)$$

where

$$\omega_{F0} = \frac{1}{\sqrt{L_F C_F}}, \zeta_F = \frac{1}{2} \left(R_{se} \sqrt{\frac{C_F}{L_F}} + \frac{1}{R_{LOAD}} \sqrt{\frac{L_F}{C_F}} \right). \quad (36)$$

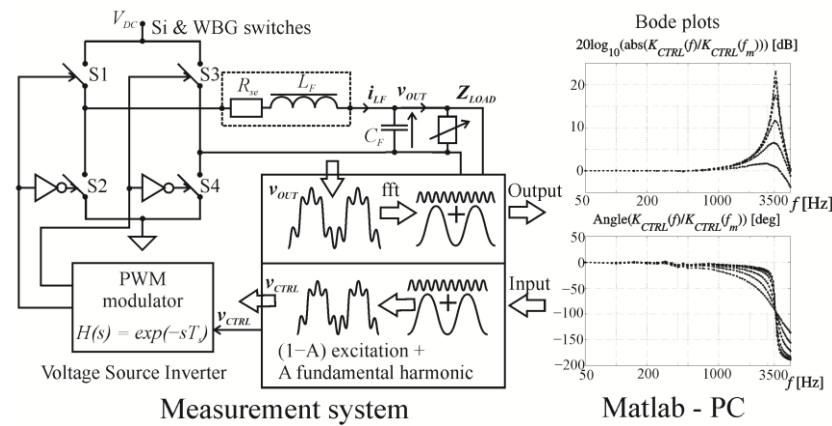


Figure 5. Measurement of VSI power conversion losses using Bode plots.

A digital PWM modulator introduces a single switching period delay because the pulse width data that are calculated and stored during the current period will be in its output in the next switching period:

$$K_{CTRL_PWM}(s) = H(s)F_{LC}(s) = \exp(-snT_s) \frac{\omega_{F0}^2}{[s^2 + 2\zeta_F\omega_{F0}s + (1 + R_{se}/R_{LOAD})\omega_{F0}^2]}, \text{ where } n = 1 \text{ or } 2 \quad (37)$$

An additional delay can be introduced by double edge modulation [27]. The sum of these delays is relevant for control system design if the switching frequency f_s is insufficiently high. However, as shown by Equations (4) and (11), the delay is compensated for during the relative measurement [13] of the control transfer function of the bridge and filter K_{CTRL} , because a delay of period nT_s concerns both the fundamental harmonic and the excitation. As presented, the relative appointment of the magnitude and phase cancels this delay.

The equivalent serial resistance of the VSI [25,28] is measured using the resultant power conversion losses. The static and dynamic power losses in the switches and the filter coil core can be measured from the magnitude of a Bode plot of the inverter (operating with the assigned switching frequency f_s), within the range of frequencies where a maximum magnitude is located Equation (38):

$$K_{CTRL}(\omega)|_{f_s, R_{LOAD}} \Rightarrow R_{se}(P_{loss})|_{f_s, R_{LOAD}}. \quad (38)$$

Switching frequencies f_s of 12,800 Hz, 25,600 Hz, or 51,200 Hz were used for the test inverter. However, the frequency of the coil voltage pulses was double that of f_s in the first PWM scheme [29]. The basic sinusoidal waveform had a fundamental frequency $f_m = 50$ Hz. The excitation sinusoidal waveforms had variable frequencies. The load resistance R_{LOAD} and the DC supply voltage V_{DC} were then set for the selected operating point. The generated test signal V_{CTRL} Equation (39) was the sum of the fundamental harmonic and the n -th harmonic [13,28]. For $k = 1, \dots, (f_s/f_m)$,

$$V_{CTRL}(k) = \text{round}\left(M \cdot \text{floor}\left(\frac{1}{2} \frac{f_{PWMINPUT}}{f_s}\right)\right) \left(A \sin\left(k \frac{2\pi}{f_s/f_m}\right) + (1 - A) \sin\left(nk \frac{2\pi}{f_s/f_m}\right) \right), \quad (39)$$

where M is the modulation depth (typically $M \leq 1$, e.g., $M = 0.9$ to avoid distortions of the fundamental harmonic), $f_{PWMINPUT}$ is the microprocessor PWM unit comparator input frequency (84 MHz for the STM32F407VG), and A is the relative amplitude of the fundamental harmonic ($A < 1$, typically $A = 0.8$ – 0.9 depending on the damping).

In the case for which the switching frequency $f_s = nf_m$, there are $f_s/50$ samples of the sinusoidal reference during the fundamental period $T_m = 20$ ms. From Equation (10), the number of samples of the n -th harmonic during this period is $f_s/(n50)$. The value $n_{max} = 100$ was used for both $f_s = 25,600$ Hz and $f_s = 51,200$ Hz to provide a minimum of five and 10 samples per harmonic period, respectively. The possible distortion of the n_{max} harmonics was not important because of damping for harmonics above the output filter

resonance frequency, which was adjusted below the 20th harmonic. Precise measurement of the magnitude of the harmonics was not required across the range of frequencies defined by the filter resonant frequency, where $\omega_{F0} = 475$ or $\omega_{F0} = 498$ Hz for the used filter coil inductance of $L_F = 2$ mH or 2.2 mH, although these values can vary by several percent [28] for the coil core consisting of the low power loss materials Super MSS and FluxSan [5]. An MKP $C_F = 51$ μ F filter capacitor was used. The filter resonant frequency ω_{F0} , as defined by Equation (36), was calibrated to be much lower than $2\pi n_{max} 50$ Hz.

The accuracy of the search for maximum gain was dependent on the frequency step grid. A low level of damping increases the error caused by the frequency step grid, causing difficulty in finding the exact maximum magnitude between the two measured points. However, a high level of damping can also cause ambiguity in the measurement of the maximum on the Bode plot. The L_F and R_{se} parameters can be calculated directly only when the maximum of the damping coefficient can be found: $\zeta_F^2 < (1 + R_{se}/R_{LOAD})/2$, where $R_{LOAD} \gg R_{se}$. The measured fundamental harmonic amplitude should be equal to 50–75% of the ADC range. Given that a 13-bit bipolar ADC with a range of -4093 – 4093 units was used, the required amplitude was 2000–3000 units. The excitation amplitude $|h_{mIN}| = 1$ – A was set to the highest possible value (typically 10–20%) that did not cause the output voltage for the filter resonant frequency to exceed the range of the ADC.

The complex test signal v_{CTRL} , defined by Equation (39), has an amplitude of $\text{floor}(0.5 f_{PWMINPUT}/f_s)$. A higher value of $f_{PWMINPUT}$ corresponds to a more accurate synthesis of the control signal waveform by the STM32F407VG. A frequency $f_{PWMINPUT} = 84$ MHz is sufficient for $f_s = 25,600$ Hz. It was assumed that the fundamental harmonic is not damped within the inverter, and is delayed by T_s or $2T_s$ within the PWM modulator, as all components of the control signal are delayed. Hence, this delay is not present in the relevant calculations. Comparison of the output and input signals presents a problem, as the output voltage is measured in volts or ADC units, and the input control voltage is measured in PWM modulator comparator units. This problem is overcome by comparing the input and output excitations relative to the fundamental harmonics of the input and output, respectively. However, this approach is predicated upon the 50 Hz component not being damped. The amplitudes and phases of the harmonic components of the complex input and output signals are calculated using the fast Fourier transform [25]. For $n = 1, \dots, n_{max}$,

$$K_{CTRL}(j2\pi f_n) = \frac{|V_{OUT}(nf_m)|/|V_{OUT}(f_m)|}{|V_{IN}(nf_n)|/|V_{IN}(f_m)|} \exp(j\{[\arg(V_{OUT}(nf_m)) - \arg(V_{OUT}(f_m))] - [\arg(V_{IN}(nf_n)) - \arg(V_{IN}(f_m))]\}) \quad (40)$$

The magnitude Bode plot is then

$$|K_{CTRL}(nf_n)| = 20 \log \frac{|V_{OUT}(nf_m)|/|V_{OUT}(f_m)|}{|V_{IN}(nf_n)|/|V_{IN}(f_m)|}. \quad (41)$$

The phase Bode plot is not required for further calculations.

$$\arg(nf_m) = [\arg(V_{OUT}(nf_m)) - \arg(V_{OUT}(f_m))] - [\arg(V_{IN}(nf_n)) - \arg(V_{IN}(f_m))] \quad (42)$$

The measuring trace of the system influences the signal. As such, the trace characteristics (both magnitude and phase) were measured and subtracted from the corresponding initially measured data. The trace was subjected to negligible damping of less than 0.5 dB in the range of up to 500 Hz, with a phase shift corresponding to a delay of approximately $2T_s$. The corrected data of the control transfer function magnitude and phase were then plotted on a PC using MATLAB. The maximum values of the function $|K_{CTRL}|$ and the frequency ω_{max} for which $|K_{CTRL}|_{max} = |K_{CTRL}(\omega_{max})|$ can then be identified to calculate the damping coefficient ζ_F Equation (43), and the serial equivalent resistance R_{se} (44) [25,28]. The real value of L_F can also be measured; however, this is not necessary for our pur-

poses. Under the assumption that $R_{LOAD} \gg R_{se}$, ζ_F and R_{se} can be calculated as follows Equations (43) and (44):

$$\zeta_F \approx \sqrt{\frac{1}{2} \left[1 - \sqrt{\left(1 - \frac{1}{|K_{CTRL}|_{\max}^2} \right)} \right]}, \quad (43)$$

$$R_{se} = \left(2\zeta_F \frac{\omega_{\max}}{\sqrt{1 - 2\zeta_F^2}} - \frac{1}{R_{LOAD} C_F} \right) \frac{1 - 2\zeta_F^2}{\omega_{\max}^2 C_F} \text{ for } R_{LOAD} > \frac{\sqrt{1 - 2\zeta_F^2}}{2\zeta_F \omega_{\max} C_F} \text{ and } \zeta_F^2 < 0.5 \quad (44)$$

Using a 50 Hz grid ($\Delta\omega = 25$ Hz), the frequency $\omega_{\max}$ can be approximated as Equation (45):

$$\omega_{\max}^2 \approx (1 - 2\zeta_F^2) \omega_{F0}^2, \text{ for } \zeta_F^2 < 0.5. \quad (45)$$

It was assumed that this approximation is the primary source of error in the calculation of R_{se} . The error Equation (46) in the calculation of the damping coefficient ζ_F is caused by the $\Delta\omega_{\max}$ error associated with appointing $\omega_{\max}$:

$$\Delta\zeta_F = \frac{\partial\zeta_F}{\partial\omega_{\max}} \Delta\omega_{\max} = -\frac{1}{2} \frac{1 - 2\zeta_F^2}{\zeta_F} \frac{\Delta\omega_{\max}}{\omega_{\max}}. \quad (46)$$

$$\Delta R_{se} = \frac{\partial R_{se}}{\partial\zeta_F} \Delta\zeta_F + \frac{\partial R_{se}}{\partial L_F} \Delta L_F \approx 2\sqrt{\frac{L_F}{C_F}} \Delta\zeta_F, \quad (47)$$

$$|\Delta R_{se}| = \sqrt{\frac{L_F}{C_F}} \frac{1 - 2\zeta_F^2}{\zeta_F} \frac{\Delta\omega_{\max}}{\omega_{\max}} = \frac{\sqrt{1 - 2\zeta_F^2}}{\zeta_F} \Delta\omega_{\max} L_F. \quad (48)$$

The error presented in Equations (47) and (48) is larger for low-load currents because such conditions hamper the determination of a maximum when compared to the two closest measured points. Typically, this error causes higher measured resistance for low-load currents. Another source of error when using a high-load current is a Bode plot magnitude with an insufficiently steep gradient. This makes determining the maximum difficult. Equations (47) and (48) show that the error of the serial equivalent resistance measurement increases with the damping coefficient, and depends on the test signal frequency grid. As described by Equation (39), the lowest grid frequency used for the generation of the test signal was 50 Hz, which corresponded to $\Delta\omega = 25$ Hz.

At the outset of the experiments, the magnitude and phase Bode plots of the experimental VSI were measured. A digital-to-analogue converter (DAC) was used to generate the test signal connected to the input of the measuring trace. Figure 6 presents the magnitude and phase Bode plots $K_{TRACE}(s)$ of this trace, which can be approximated by the second-order transfer function with an additional $2T_s$ delay:

$$K_{TRACE}(s) = K_1(s)K_2(s, f_s) = \frac{\omega_0^2}{s^2 + 2\zeta\omega_0 s + \omega_0^2} e^{-s2T_s}, \quad \omega_0 = 2\pi 5000, \quad \zeta = 1.8. \quad (49)$$

The delay of the DAC is equivalent to that of the PWM modulator. As such, the pure trace has a delay of a single T_s . The corner frequency of the output filter for $L_F = 2$ mH and $C_F = 51$ μ F is 498 Hz, allowing K_{TRACE} Equation (50) to be approximated in the range up to 1000 Hz, using only the delay $2T_s$ and omitting the second-order transfer function. All the measured signal traces are identical outside of the voltage and current inputs; these measurements are provided by the isolated amplifier and the AC current transducer, respectively. However, across the restricted frequency range, all traces are approximately identical.

$$K_{TRACE}(s) \approx e^{-s2T_s} \text{ for } \omega < 2\pi 1000 \text{ 1/s}. \quad (50)$$

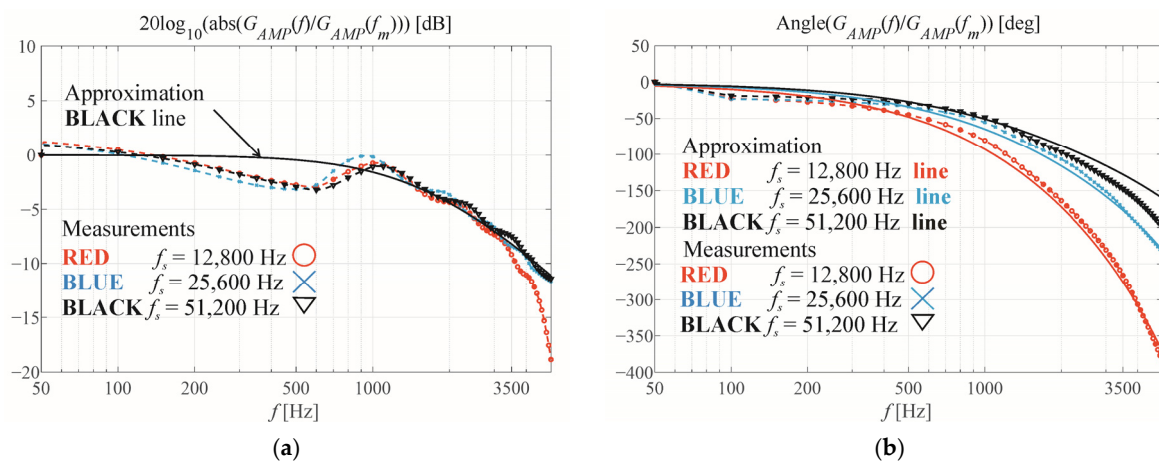


Figure 6. The measured and approximated Bode plots (a) magnitude and (b) phase of the voltage-measuring trace.

Three switching frequencies were implemented in the test system: 12,800 Hz, 25,600 Hz, and 51,200 Hz. Three types of transistors were used: the Si-based IRFP360, the SiC-based AIMW120R060M1H, and the GaN-based Cascode Device Structure GAN041-650WSB. Five resistive loads were used in the range of 12.5–100 Ω . This gave us a total of (transistors of 3 types) $\times$ (3 switching frequencies) $\times$ (5 load resistances) $\times$ (2 magnetic materials) = 90 different combinations of variables, and therefore 90 magnitude and phase Bode plots. Figures 7 and 8 present selected examples of the Bode plots. The selection of the examples has to show the influence of the transistor technology on the inverter Bode plots (Figure 7a,b) and finally on the dynamic serial resistances R_{se} for the two coil core materials (Figure 7c,d). Figure 7a shows that the Si transistors have lower damping than the SiC transistors for $R_{LOAD} = 50 \Omega$ and a FluxSan coil core. The same result was observed for the Super MSS core. It was assumed that this was caused by higher power losses in the coil for faster SiC switches. The resultant equivalent resistances are shown in Figure 7c,d for the Super MSS core and FluxSan core, respectively. Figure 7 shows that the lowest equivalent serial resistance R_{se} was obtained for GaN transistors. However, the differences between the three transistor types are small for the chosen switching frequencies when using the same coil core material and load current. Figure 8a presents the exemplary influence of the load current on the magnitude Bode plot of the inverter with GaN transistors, and Figure 8b shows the exemplary influence of the switching frequency.

Using Equations (43) and (44), the equivalent serial resistances can be calculated from the magnitude Bode plots as a function of the VSI inductor current. The inductor current is higher than the load current, and flows through the bridge switches. The accuracy of the calculations is limited by the resolution by which the maximum magnitude can be found. This is demonstrated in Figure 8a; for the lowest load resistance of 12.5 Ω , the curve maximum is difficult to locate precisely via interpolation between the measured points. The amplitude of the test signal relative to the fundamental must be carefully selected. Figure 9 presents the serial equivalent resistance measurements for test signal amplitudes of 10% and 20% for $f_s = 12,800$ Hz, GaN transistors, and a Super MSS core. All presented calculations used a 10% test signal.

Measurement of the serial resistance R_{se} is based on the invariability of the fundamental 50 Hz harmonic of both the input and output control trace signals. As such, static serial resistance was not measured. The efficiency of the experimental VSI was measured directly to calculate serial resistance R_{LOSSES} . Figure 10 shows the exemplary measurements of R_{LOSSES} as a function of load current for both core types at $f_s = 25,600$ Hz. This resistance comprises the full losses from the DC source in addition to the dynamic losses and, as such, should be higher than the previously measured dynamic serial resistance R_{se} of the control

trace. It can be assumed that $R_{LOSSES} = R_{50Hz} + R_{se}$, where R_{50Hz} represents the losses of the fundamental harmonic at 50 Hz in addition to the static losses.

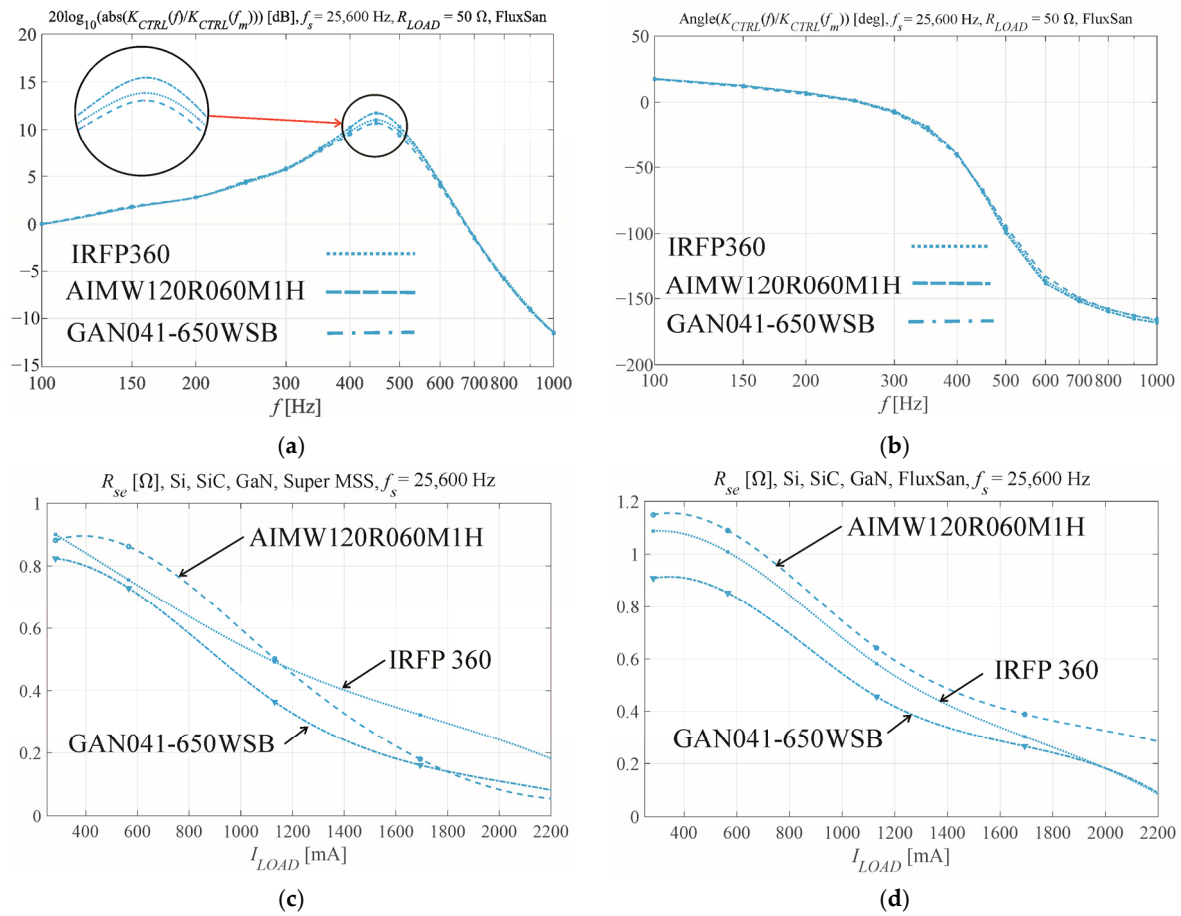


Figure 7. (a) Magnitude and (b) phase Bode plots of the VSI control function with a bridge composed of Si, SiC, and GaN transistors using a FluxSan coil core and a switching frequency f_s of 25,600 Hz; (c) the calculated dynamic serial resistances R_{se} for the Super MSS core with $f_s = 25,600$ Hz; (d) calculated dynamic serial resistances R_{se} for the FluxSan core with $f_s = 25,600$ Hz.

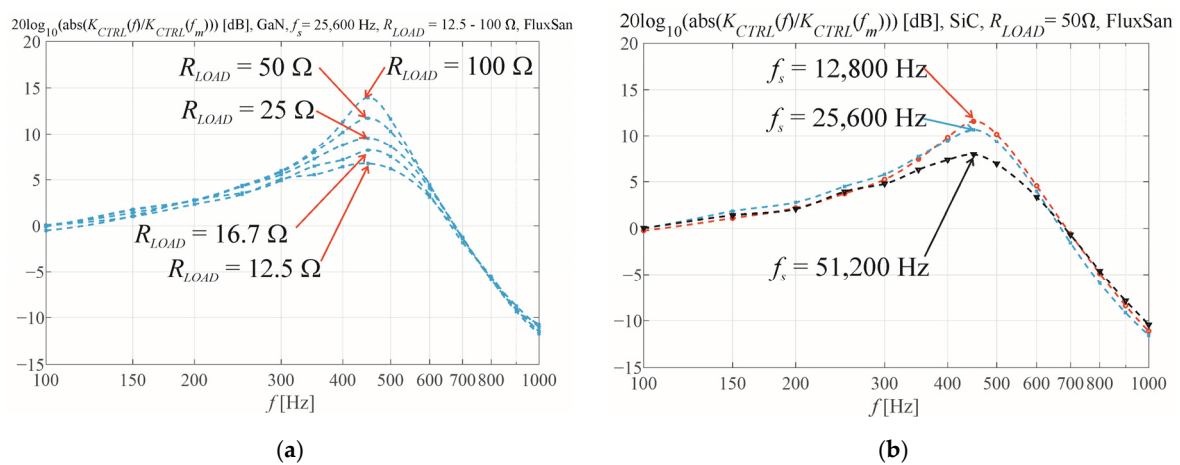


Figure 8. (a) Magnitude Bode plots for a bridge composed of GaN transistors, with switching frequency $f_s = 25,600$ Hz and $R_{LOAD} = 12.5$ – 100Ω ; (b) magnitude Bode plots for $R_{LOAD} = 50 \Omega$, using SiC transistors and FluxSan core, for $f_s = 12,800$, 25,600, and 51,200 Hz.

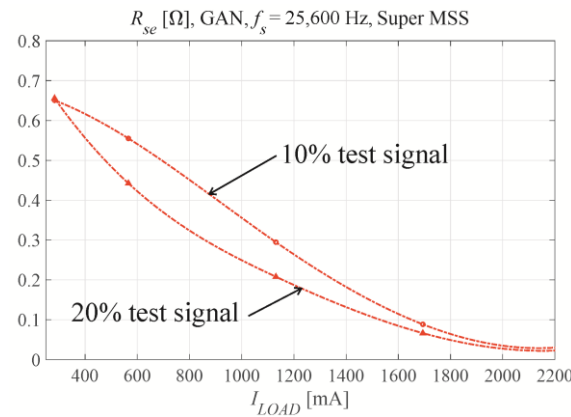


Figure 9. The influence of the relative test signal amplitude on the equivalent serial resistance measurement.

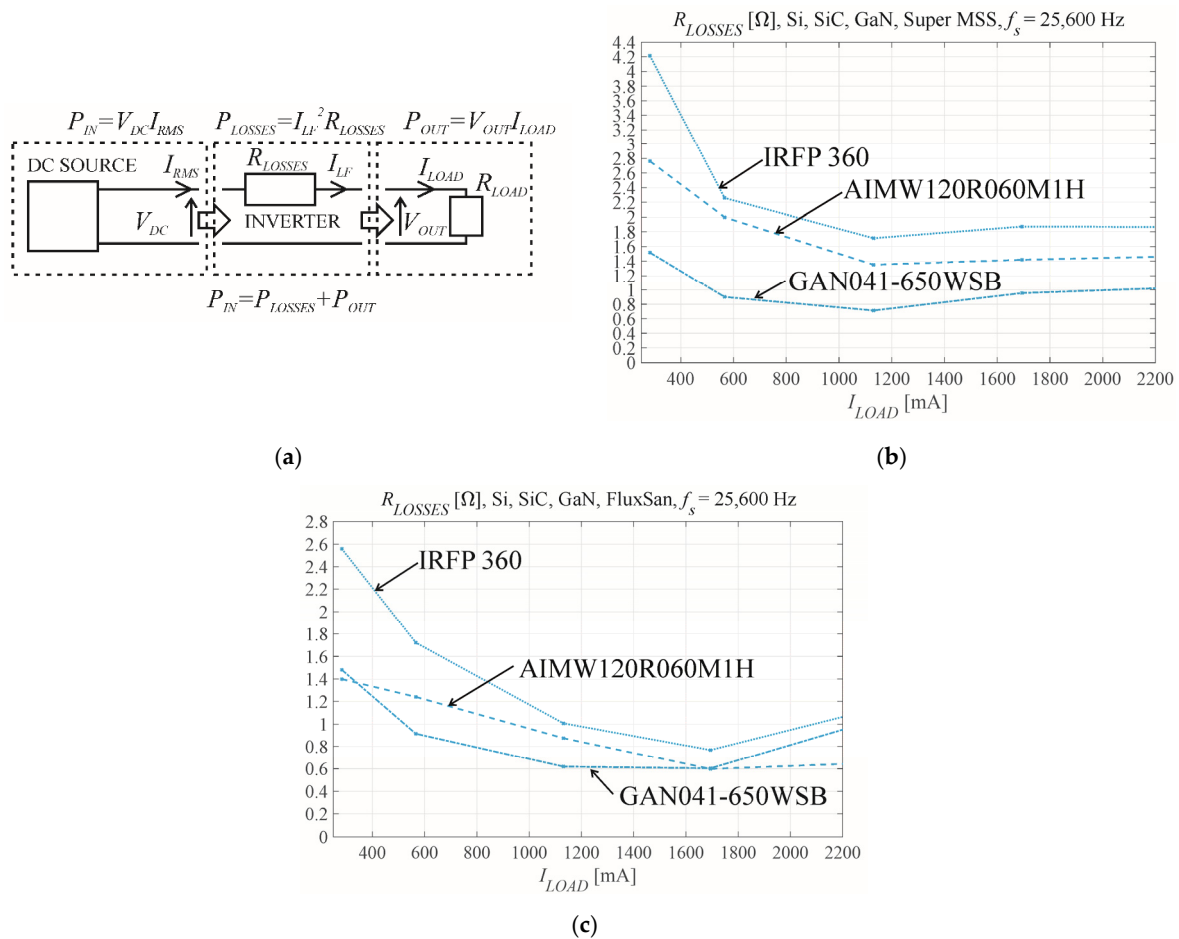


Figure 10. The power loss resistance R_{LOSSES} measured from the power loss, showing (a) the method of measuring R_{LOSSES} , and (b) exemplary values of R_{LOSSES} for the Super MSS coil core at $f_s = 25,600$ Hz, and (c) exemplary values of R_{LOSSES} for the FluxSan coil core at $f_s = 25,600$ Hz.

Figures 11 and 12 show all the measurements of the serial resistances R_{se} and R_{LOSSES} for the Super MSS and FluxSan core materials, respectively. The resistances were measured from the magnitude Bode plots or input and output powers for each transistor type. The dynamic serial resistance R_{se} shows a slight dependence on transistor type at a given switching frequency and load current. However, the R_{se} values are similar for both coil core

materials. The full loss resistance R_{LOSSES} displays significant dependence on the transistor type, switching frequency, and type of coil core material.

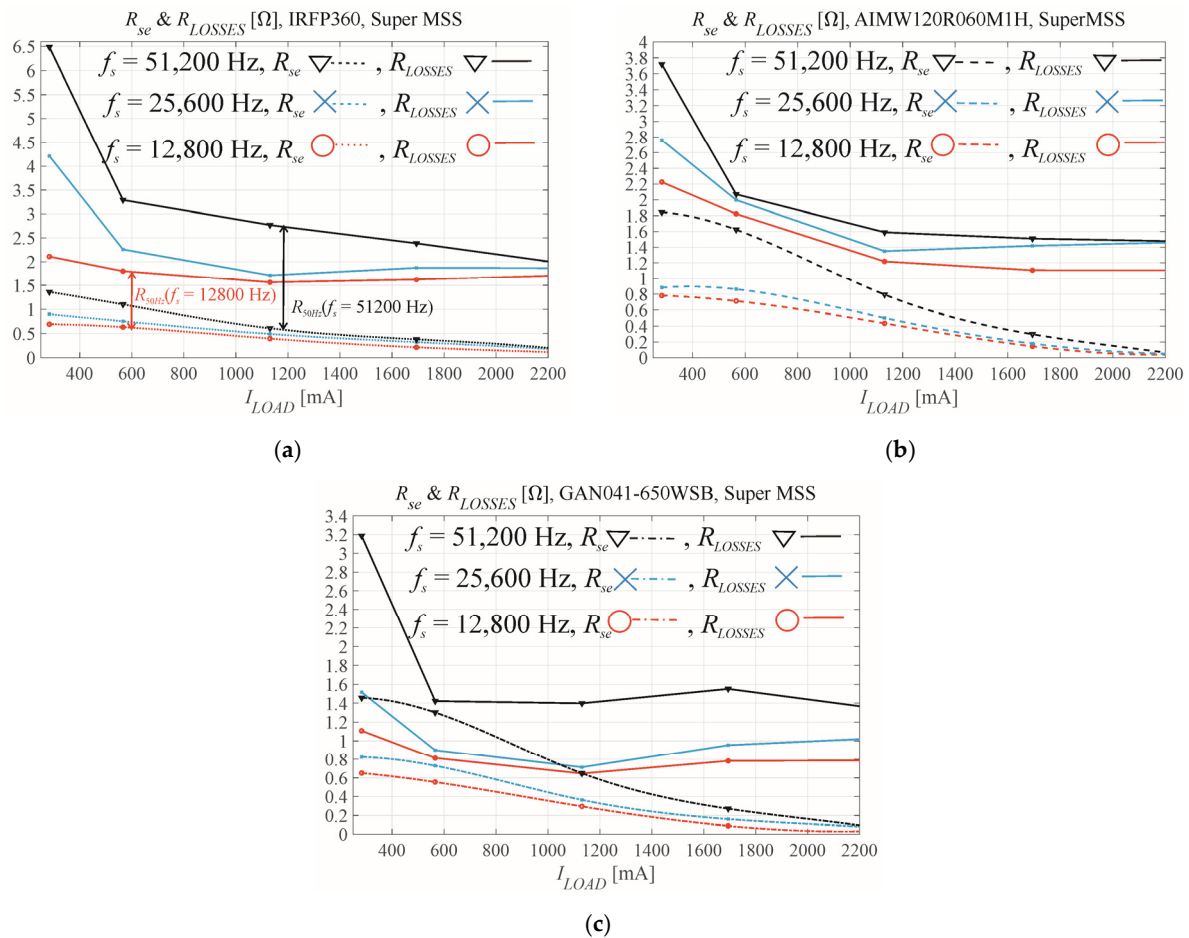


Figure 11. The serial resistances R_{se} and R_{LOSSES} for (a) Si, (b) SiC, and (c) GaN transistors when using coil core material Super MSS.

The results of the two approaches to measure the equivalent serial resistance of the VSI are demonstrated in Figures 11 and 12. The first is based on measuring the magnitude Bode plot of the control transfer function of the VSI (Figure 5). This method is ideal for the estimation of the control loop parameters but has one disadvantage: it requires that the 50 Hz signal—the fundamental harmonic—is subjected to no damping. To correct the row measurements, the Bode plots of the measuring trace must be known (Figure 6). Figures 11 and 12 show that no substantial difference (less than 0.2 Ω) exists between the R_{se} values of different transistor types at the same switching frequency when using the same coil core material. However, GaN-based transistors always produce the lowest R_{se} .

The complex equivalent resistance R_{LOSSES} can be calculated from the power losses of the VSI (Figure 10). However, this resistance can include the component of the equivalent resistance that is outside the control loop and does not influence the quality of the output voltage. Both equivalent serial resistances R_{se} and R_{LOSSES} depend on the type of transistor used (Si, SiC, and GaN), their static and dynamic losses, switching frequency, and the coil core material (Super MSS and FluxSan).

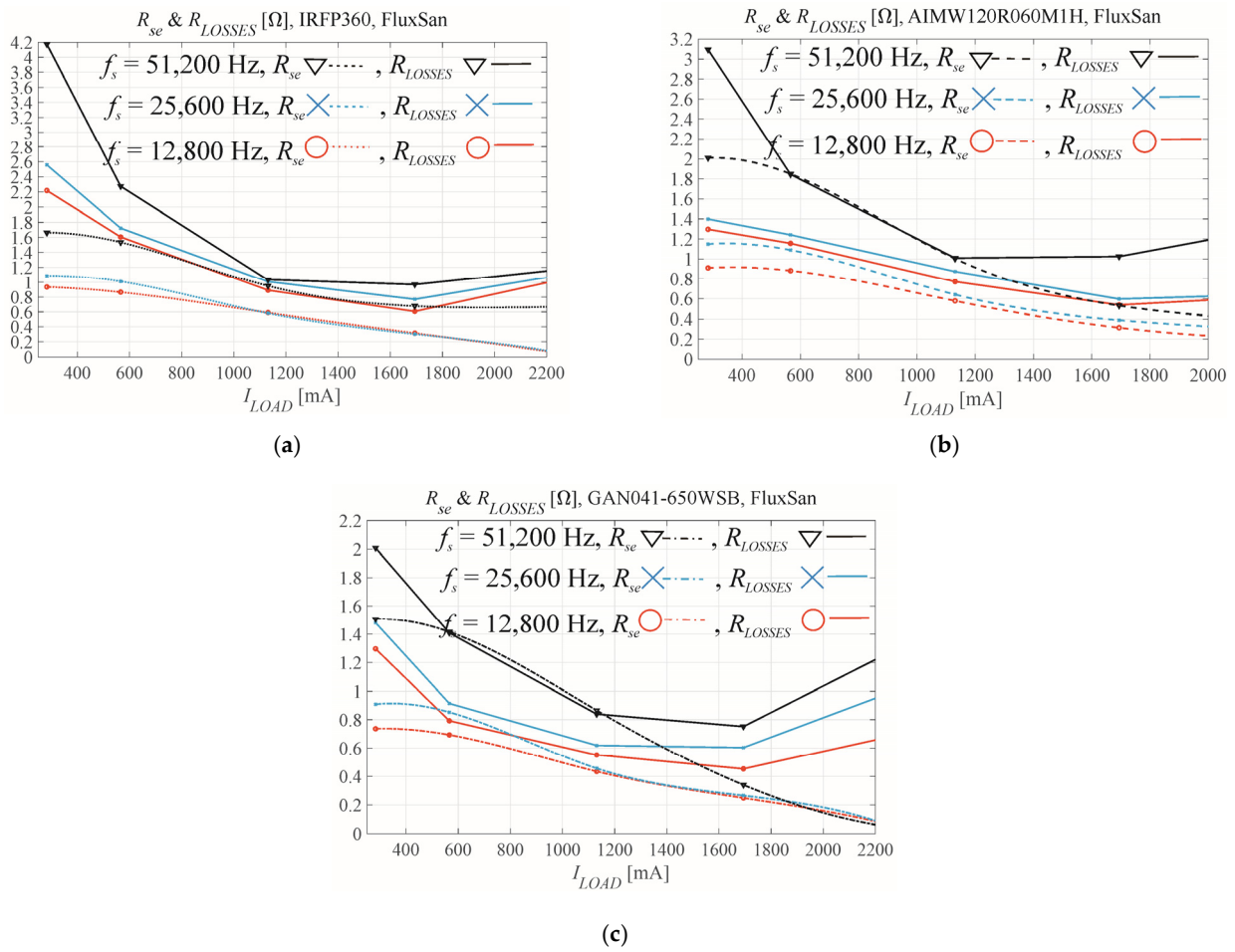


Figure 12. The serial resistances R_{se} and R_{LOSSES} for (a) Si, (b) SiC, and (c) GaN transistors when using the coil core material FluxSan.

5. Tests of the VSI Using CDM Control for Different Switch Types and Coil Core Materials

The experimental VSI was used to validate the effect of implementing the correct equivalent resistance within the controller. Figure 4b,d shows that for $f_s = 25,600$ Hz and a time constant $\tau = 8T_s$, for the changes of the equivalent serial resistance, when the resistance R_{CDM} in the CDM control law is the same, the system is stable, but the poles of the closed loop system are shifted. For the lower time constant, measuring the unstable system (Figure 4a) is impossible. It is possible to show that keeping the same resistance R_{CDM} in the control law for different transistor technology in the bridge for the same output filter coil core material can increase distortions of the output voltage. The idea behind the experimental verification of the previous theoretical considerations (Section 3) is to find the resistance R_{CDM} in the SISO-CDM control law for which there are the lowest distortions of the output voltage and to show that it is connected with the equivalent serial resistance of the bridge (dependent on the type of switching transistors).

The various resistances R_{CDM} were used in the control law of the CDM controller for the different equivalent serial resistances of the VSI when using the nonlinear rectifier RC load defined in IEC 62040-3 (PF = 0.7) [1]. The THD of the output voltages was measured for SiC transistors at $f_s = 25,600$ Hz using Super MSS coil core material, with both open-loop control and CDM control with $\tau = 8T_s$. Figure 13 shows the output voltage and current.

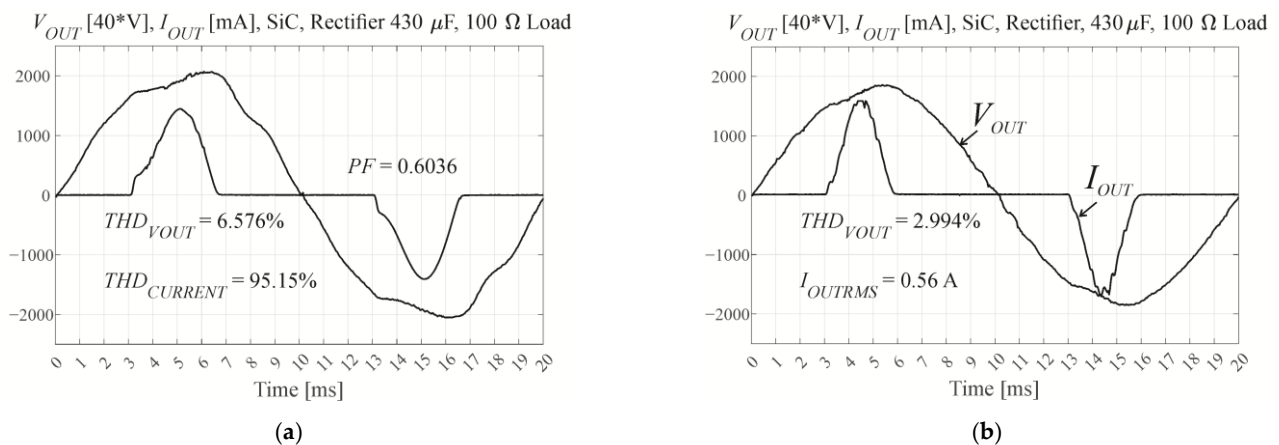


Figure 13. The VSI output voltage and current when using the nonlinear rectifier RC load ($PF = 0.6$) for (a) open-loop control and (b) CDM control ($\tau = 8$) with SiC bridge transistors and the Super MSS coil core material.

Figure 14 presents the THD_{VOUT} values for the different types of transistors and different sets of R_{CDM} resistances in the CDM control law. Both types of coil materials are shown with a switching frequency of $f_s = 25,600$ Hz and a time constant $\tau = 8T_s$. The lowest THD_{VOUT} is obtained for the particular R_{CDM} that is comparable with R_{LOSSES} . Table 2 presents the R_{LOSSES} resistances for $I_{OUTRMS} \approx 0.5$ A at the THD_{VOUT} minima, for the Si, SiC, and GaN transistors, and the Super MSS and FluxSan core materials. Figure 14 shows that for the high time constant when the system is stable, no matter whether the serial resistance in the control law is, the choice of the proper resistance R_{CDM} for the particular type of transistors and the coil core material improves the quality of the output voltage.

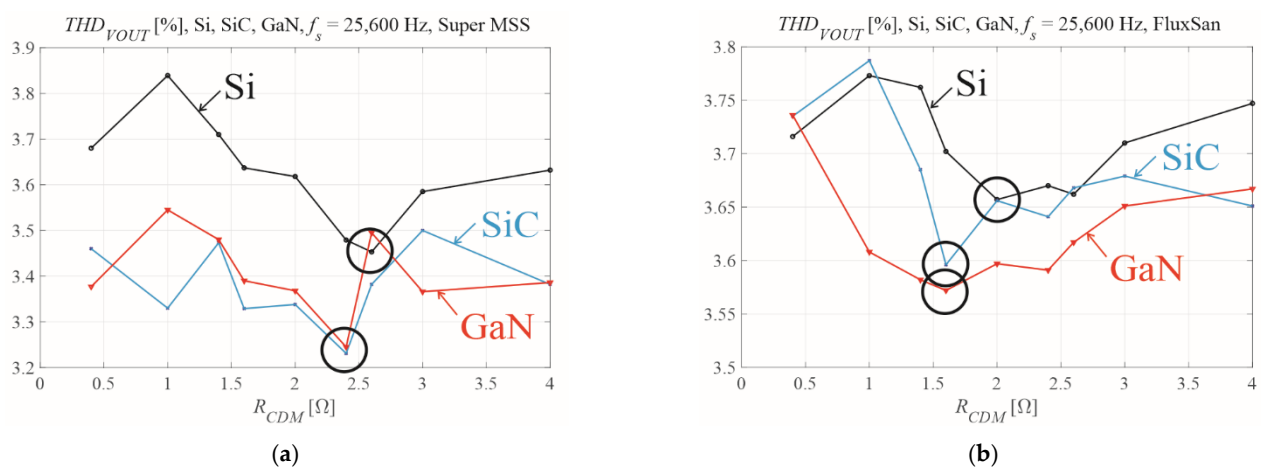


Figure 14. Graphs of THD_{VOUT} for the different R_{CDM} values at $f_s = 25,600$ Hz for the Si, SiC, and GaN transistors with (a) Super MSS and (b) FluxSan coil cores for the standard rectifier RC load. Black circles highlight the THD_{VOUT} minima.

Table 2. THD minima for each R_{CDM} , transistor type, and coil core material.

$I_{OUTRMS} \approx 0.5$ A	Si–Super MSS	SiC–Super MSS	GaN–Super MSS	Si–Flux San	SiC–Flux San	GaN–Flux San
R_{LOSSES} [Ω]	2.8	2.2	1	2.8	1.3	1.1
R_{CDMmin} [Ω]	2.6	2.4	2.4	2	1.6	1.6
THD_{min} [%]	3.453	3.231	3.245	3.657	3.596	3.572
THD_{min}/THD_{max}	10.05%	7.69%	8.46%	3.07%	5.04%	4.39%

Figure 15 presents our experimental VSI setup for the measurement of Bode plots and R_{LOSSES} resistances.

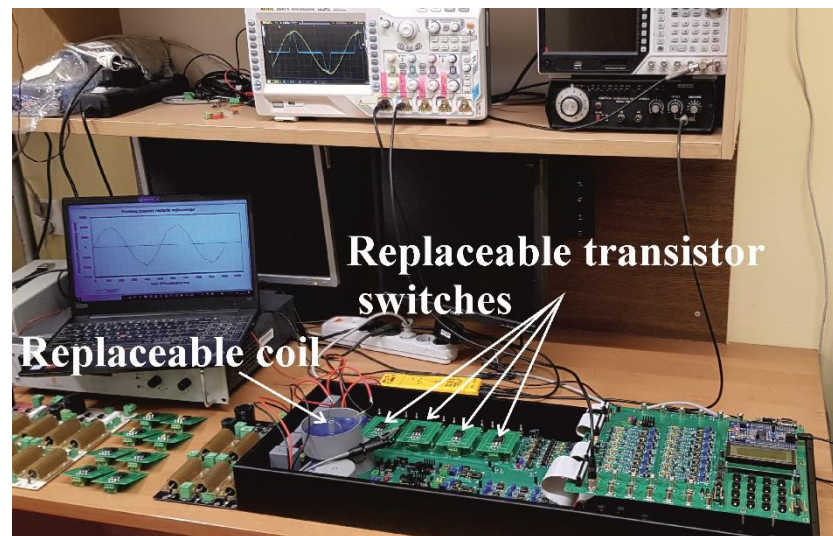


Figure 15. The experimental VSI shows the replaceable coil and transistors.

When changing transistors, gate-driving circuits should be checked for oscillations. WBG transistors can oscillate due to associated parasitic elements. Switching oscillations can be damped using RC snubbers, ferrite beads, a reduction in di/dt , or novel gate driver designs [30]. Printed circuit boards (PCBs), which feature long traces between the gate driver output and the gate source terminal, can lead to high parasitic inductance in the gate loop and cause damage to SiC transistors [31]. Moreover, SiC-MOSFETs are sensitive to parasitic components in the measurement probe. Measuring certain values (e.g., the gate-source voltage) can introduce parasitic inductance between the test point and the ground lead of the probe, thereby decreasing the stability of the SiC-MOSFET. However, if drain-source oscillations are noticed in a previously designed PCB, the simplest solution is often to increase the value of the serial resistor in the gate-driving circuit [32].

Table 2 shows that the R_{CDM} resistance for which THD_{VOUT} was minimal was of comparable size to R_{LOSSES} and was higher than R_{se} . The relative change in THD_{VOUT} for different values of R_{CDM} was small—between 5 and 10%. GaN and SiC transistors produce the THD_{VOUT} minimum at the same R_{CDM} resistance for both coil core materials. The Si transistors produce the THD_{VOUT} minimum at different R_{CDM} resistance. These results demonstrate that SiC and GaN transistors can be mutually replaced without requiring any change in control, but that the replacement of Si transistors requires the control value of R_{CDM} to be adjusted.

6. Results

The initial theoretical calculations showed that the value of the serial resistance in the control law did not seriously influence the controller gains when using the MISO-PBC control (Figure 2). When using SISO-CDM control and measuring only the output voltage, the difference between the value of R_{CDM} used in the control law and the real value of serial equivalent resistance causes changes in the assigned roots of the closed-loop system characteristic equation (Figure 4). The static R_{LOSSES} and dynamic R_{se} equivalent serial resistances were measured (Figures 11 and 12) for different types of transistors used (Si, SiC, and GaN), switching frequencies (12,800 Hz, 25,600 Hz, 51,200 Hz), and two coil core materials (Super MSS and FluxSan).

The system SISO-CDM for $S(z^{-1})$ order 2, $R(z^{-1})$ order 3, $P_z(z^{-1})$ order 6, $\tau = 8T_s$ (Figure 4b,d) was tested by means of changing the used R_{CDM} value (the equivalent serial resistance used in the control law) to get the lowest THD of the output voltage for the

standard (EN 62040-3) rectifier RC load for the 25,600 Hz switching frequency, for Si, SiC and GaN transistors, for two filter coil core materials. The results of the measurements showed (Figure 14a,b and Table 2) that it is possible to get the minimum THD for the adjusted R_{CDMmin} that depends on the type of transistors and the coil core material. This adjusted value is higher than R_{se} (Figures 11 and 12) and closer to R_{LOSSES} . However, the adjustments R_{CDMmin} for both WBG transistors were the same but different than for Si transistors. According to the theoretical prediction shown in Figure 4b,d, the system was stable for the different R_{CDM} .

7. Conclusions

This paper showed how changing the type of transistor used in a VSI bridge can change the results produced by the controller. Two equivalent serial resistances were measured—the dynamic R_{se} and the complex R_{LOSSES} . Dynamic R_{se} was found to be lowest for GaN-based transistors. However, different transistor types show only small differences of approximately 0.2Ω , at the same switching frequency, load current, and coil core material. Much higher differences were observed in the measurement of R_{LOSSES} . The measurements showed that changes between WBG transistors—SiC and GaN—can be made without any adjustment of the control. However, changing between Si and WBG transistors requires such an adjustment. The best control results were produced for the SiC transistors. However, these superior results could have been due to the driving circuits used. The adjustment of the R_{CDM} resistance to a value close to R_{LOSSES} in the control law of the SISO-CDM controller can slightly reduce the output voltage THD. Oscillations can occur in the transistor gate-driving circuit. For certain values of the additional serial resistance R_G , there are oscillations in the gate circuit when using WBG transistors, while no oscillations are present for Si transistors. For the $R_G = 10 \Omega$ resistor chosen for the Si transistors, the VSI with GaN transistors was oscillated in the experimental model. Increasing the value of the resistor was sufficient to prevent oscillations.

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