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Improved Sampled Average Modulation Technique for the Modular Multilevel Converters

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Abstract: In this article the improved sampled average modulation technique is proposed, this technique has $2N + 1$ levels in the output voltage waveform of MMC and it is considered as of low complexity of implementation for any number of submodules per arm. For that, characteristics such as dynamic response, implementation complexity, inverter output voltage waveform levels, and switching frequency are considered to evaluate and validate the proposed modulation technique. The proposed technique is compared with other three previously proposed techniques, its considering parameters such as the THD and the fundamental value of the output voltage, and also the peak-to-peak variation of the submodule capacitor voltage. Several simulations were performed in the Matlab/Simulink software and with these results, it was validated the proposed modulation technique, and also it is verified that the proposed technique is computationally more efficient. This last one shows its potential for multiphase multilevel applications.

Keywords: modular multilevel converter; sampled average; modulation techniques; $2N + 1$ voltage levels

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1. Introduction

The multilevel converters (MLCs) over time got to make a place in low/medium/high-voltage specific power electronics applications, the most known MLCs topologies, are the: neutral point clamped (NPC), flying capacitor (FC) and cascade half-bridge (CHB) [1–3]. However, there is a limitation with respect to the number of achievable levels for these MLCs, due to the number of electronic devices that would need (transistors, diodes, capacitors or DC sources),

So to solve this limitation, the advancement of technology has enabled the development of the Modular Multilevel Converter (MMC), which was introduced in the literature by Marquardt, Lesnicar and Hildinger in 2002 [4]. The MMC is a promising MLC for medium/high-voltage applications, emphasizing mainly in qualities as [4–27]: modularity, flexible operation, standard components, redundancy, operating at different switching frequency, lower presence of harmonics in the output voltage, higher efficiency, efficient management against failures, and so on. This converter was projected considering the semiconductors nominal power limitations, taking advantage of serial submodules connection to reach high operating voltages [5].

The MMC revolutionized the market of power electronic converters based on VSCs, and several niche applications such as: energy storage [6,7], active power filtering [8], medium/high-voltage motor drive [9,10], photovoltaic energy conversion [11,12], offshore wind farms connection [13,14], interconnection of asynchronous AC electrical grids [6,14], railway traction system conditioner [15], electric vehicles [16], electric ships [17,18], DC de-icer [19], medium-voltage static compensators (STATCOM) [20], high-voltage direct-current (HVdc) [21–24], among others.

To date, several papers have been reported to improve the reliability and performance of MMC that include mainly: circulating current minimization [7,28], capacitor voltage balancing [7,23,29], output current control [7,25], types of SM topologies [5,7,25], continuous/discrete time modeling [5,25–27], operating mechanisms [25,26], fault tolerance on DC-link system terminals faults [20], fault tolerance on internal device in the submodules [22], control strategies [6–8,18,19,24–28], modulation techniques [29–50] and so on.

Modulation techniques were evolved and adapted to different requirements (depending on the type of application and voltage level), in [34] a comparison of three main modulation techniques based on switching frequency (low, medium and high) was made. This is, to identify that despite having various modulation techniques, each one can have a specific niche where it will have better performance and its natural characteristics can be better exploited. And for this, there are different quantitative and qualitative parameters that allow to properly choose a modulation technique for specific MMC application, it can be classified mainly based on:

- Dynamic response;
- Implementation complexity;
- Inverter output waveform levels;
- Switching frequency.

Many research efforts have been made to develop many modulation techniques. An overview of power converter modulation techniques applied to MMC developed in the literature can be summarized according to Table 1, including the proposed technique. The modulation techniques are generally grouped into families and differ among them according to the way process the modulating signals, therefore, the way generates the command signal for the submodules (i.e., step wave or pulse width modulation).

Table 1. Brief overview of power converter modulation techniques applied to MMC.

Family	Techniques	Refs.	Dynamic Response	Implementation Complexity	Inverter Output Waveform Levels	Switching Frequency
Nearest Voltage Level	SCM	[35]	fast	low	$N+1$	fund.
	i-SCM	[32,33]	fast	low	$2N+1$	fund.
Level Shifted Carrier	PD-PWM	[30,36]	moderate	medium	$N+1$	high
	POD-PWM	[30,36]	moderate	medium	$2N+1$	high
	APOD-PWM	[30,36]	moderate	medium	$2N+1$	high
	VF-PWM	[37,38]	moderate	medium	$N+1$	high
	VFb-PWM	[38]	moderate	medium	$2N+1$	high
Reprogrammed PWM	SHE	[39]	fast	medium	$N+1$	fund.
	i-SHE	[40]	fast	medium	$2N+1$	fund.
	SHM	[41]	fast	medium	$N+1$	fund.
Sub-harmonics	PSC-PWM	[30,31]	moderate	medium	$N+1$	med.–high
	PSC-PWM wIA	[31,42]	slow	medium	$2N+1$	high
	SD-PWM	[30]	moderate	medium	$N+1$	med.–high
	HPS-PWM	[37]	moderate	medium	$2N+1$	high
Space Vector	SV-PWM	[43]	slow	medium	$N+1$	low
	dual SV-PWM	[44]	slow	high	$2N+1$	low
	vector selector	[45]	slow	medium	$N+1$	fund.–var.
Submodules Unified	SU-PWM	[46]	moderate	medium	$N+1$	low
	i-SU-PWM	[47]	moderate	medium	$2N+1$	low
Sampled Average Mod.	SAM	[29]	fast	medium	$N+1$	low–med.
	improved SAM		fast	medium	$2N+1$	low–med
CO-PWM		[36]	moderate	medium	$N+1$	med.–high
SO-PMW		[48]	moderate	medium	$N+1$	fund./low
Modulated MPC-PWM		[49]	fast	high	$N+1$	variable
Multiband Hysteresis Modulation		[50]	moderate	medium	$N+1$	variable

The sampled average modulation (SAM) technique proposed in [29] does not present $2N+1$ levels, because it was initially performed in an MMC with submodules three-level flying capacitor (FC-3L), if the submodule is replaced by half submodule, it generates $N+1$ levels. This technique does not require a transformation from *abc* coordinate frame to $\alpha\beta$ coordinate frame, eliminates the voltage-second error found in nearest voltage level (NVL) techniques and can be applied to an MMC with a fewer/largest number of submodules per arm. However, this modulation technique can only generate $N+1$ levels at output voltage (line-to-neutral voltage), where N is the number of submodules per arm. Therefore, it has a high THD in the output waveform (the THD value increases when the number of submodules is lower).

To solve these inconveniences, in this article is proposed a simple and effective method to increase the output voltage for $2N+1$ levels. Thus, the THD value of the inverter output voltage will decrease, improving the quality of the conventional SAM technique. This technique can be applied to any number of SMs/arm. Also, is analyzed in single-phase and the mathematical equations are suitable for single-phase and three-phase systems.

The presented concept is known and an extended version of the SAM [29] and the improved staircase modulation (i-SCM) based on a step wave modulation [32,33]. In [32] an improvement of traditional NVL is proposed using a rounding function at 0.25 compared to the traditional one doing this at 0.5; this leads to being able to obtain $2N+1$ levels, and as a method obtaining an advantage for an MMC with a large number of SMs/arm due to its simplicity in processing, however, this leads to a high voltage-second error and making it impossible to use for an MMC with a small number of SMs/arm. However, in order to improve this disadvantage related before, in [33] it is proposed that by adding an alternate signal of double fundamental frequency to the reference signal, this creates a pulse pattern can solve the application of this technique for a MMC with a low amount of SMs/arm. The presented $2N+1$ modulation technique is similar to individual control of upper and lower arms, due to the way interleaving the positive and negative carriers by a fixed angle to generate $2N+1$ levels. The concept is a combination of these known techniques.

Also, a comparison between different modulation techniques developed in the literature is adopted to take on board the proposed technique, between these: i-SCM [32,33], phase-shifted carrier (PSC-PWM) based on interleaved carrier signals technique [30,31], SAM [29] and the proposed technique.

(1) The THD of the inverter output voltage (line-to-ground), [$\text{THD}_{v_{xi}}$ (%)], it is probably the most important parameter when considering a suitable modulation technique, due to this parameter defines the inherent passive components sizing (submodule capacitor and arm inductor) and external components to the MMC (line filters, rated power devices, according to the application).
(2) The output voltage fundamental value, [$v_{xi,1}$ (V)], it is observed to check if the technique used ensures an adequate value without compromising the effectiveness of the MMC, this parameter is important for MMC with reduced number of submodules, which usually tends to be a problem as in Staircase modulation technique, this issue is widely discussed in [33].
(3) The peak-to-peak variation of the capacitor voltage of upper and lower arm submodules, [$\Delta V_{c,pp}$ (V)], this parameter characterizes the suitable capacitor sizing and for that, firstly, it is necessary to define the modulation technique and then a suitable sizing method is applied for the inherent components. Since, the capacitor and the inductor inherent to the MMC should be sized relative to a modulation technique, so that, the dynamic behavior of the converter will be adequate for that specific method. In this case, standard sizing methods studied in Section 2 are used and, when compared to other modulation techniques, it was obtained an acceptable performance.

In summary, the proposed modulation technique is of medium implementation complexity with a fast dynamic response at low/medium switching frequency that allows its use in any MMC with a varied number of submodules (large or small). Also, the capacitor

voltage balancing method is suitable for use with any type of modulation, in this paper it is presented together with the proposed modulation but it can also be adapted for any other.

The rest of this paper is organized as follows. In Section 2, a brief mathematical analysis of the MMC is presented. In Section 3, the conventional SAM technique is introduced. In Section 4, the operation of the improved SAM technique is proposed and explained in detail. In Section 5, the operation of the proposed voltage balance algorithm is detailed. In Section 6, the simulation results for validate this modulation technique is presented. Also, the conclusions are detailed in Section 7.

2. The MMC Operating Principles

2.1. Basic Principles

The three-phase MMC is composed of six arms and each arm contains an N-number of identical submodules, one arm at the top and one arm at the bottom of each x-phase. Due to its modular design, the MMC is well scalable and flexible in structure for any medium/high-application. The Figure 1 shows the circuit configuration of the three-phase MMC. In this article, each SM represents a conventional half-bridge submodule.

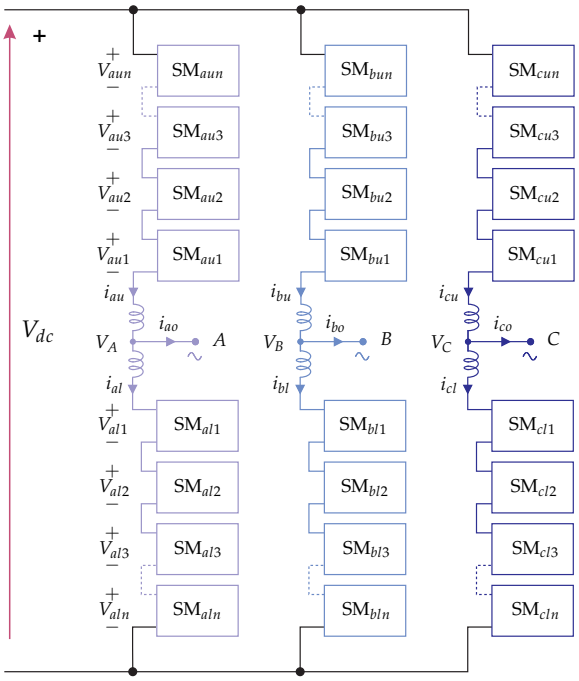

Figure 1. Three-phase equivalent circuit and main parts of MMC.

2.2. Mathematical Model

The N-submodules in series with an arm inductor in each arm, the upper and lower arm submodules are modeled as controlled AC voltage sources. The DC system is modeled as two DC voltage sources. The single-phase equivalent model of MMC under ideal conditions is shown in Figure 2, each arm is formed by N-submodules connected in series.

Applying kirchhoff's voltage and current laws. The upper and lower arm voltages are given by:

$$v_{xu} = \frac{V_{dc}}{2} - v_{xo} - L_a \frac{di_{xu}}{dt} - r_a\, i_{xu} \tag{1}$$

$$v_{xl} = \frac{V_{dc}}{2} + v_{xo} - L_a \frac{di_{xl}}{dt} - r_a\, i_{xl} \tag{2}$$

where V_{dc} is the DC-bus voltage, v_{xu} is the upper arm voltage, v_{xl} is the lower arm voltage, v_{xo} is the AC output voltage, i_{xu} is the upper arm current, i_{xl} is the lower arm current, L_a is the arm inductor and r_a is the resistance associated with the arm inductor.

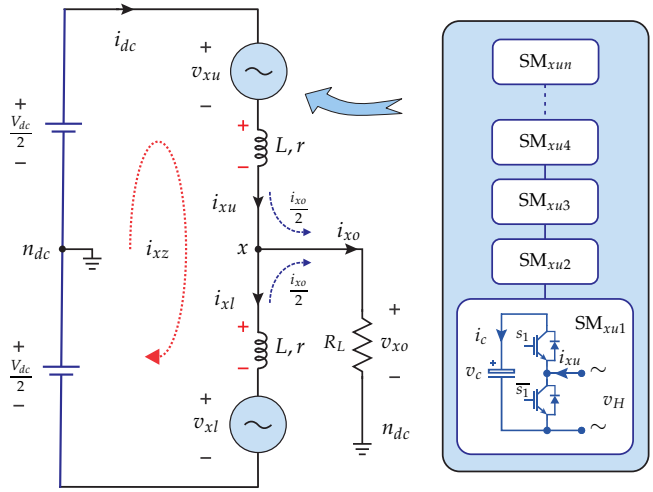

Figure 2. Single-phase equivalent circuit of MMC.

The arm modulation signals at steady-state are given by:

$$v_{xu} = \frac{V_{dc}}{2} - v_{xo} - v_{xz} \tag{3}$$

$$v_{xl} = \frac{V_{dc}}{2} + v_{xo} - v_{xz} \tag{4}$$

The upper and lower instantaneous arm currents are given by:

$$i_{xu} = \frac{i_{dc}}{\kappa} + i_{xz} + \frac{1}{2} i_{xo} \tag{5}$$

$$i_{xl} = \frac{i_{dc}}{\kappa} + i_{xz} - \frac{1}{2} i_{xo} \tag{6}$$

where i_{dc} is the DC current component, i_{xz} is the AC circulating current, i_{xo} is the AC output current, v_{xz} is the voltage drop across arm inductor and κ is the number phase index. It is considering, $\kappa = 3$ for three-phase and $\kappa = 1$ for single-phase.

2.3. AC Circulating Current

This current component flows between the legs of MMC only. From (5), its instantaneous value is given by:

$$i_{xz} = \frac{i_{xu} + i_{xl}}{2} - \frac{i_{dc}}{\kappa} \tag{7}$$

2.4. Submodule Capacitor Sizing

The submodule capacitor is sized based on trade off energy in voltage ripple [51], when the ripple factor ($0 < \Delta V_c < 0.1$). Then, the necessary capacitance for each submodule capacitor is given by:

$$C_{sm} = \frac{S}{3\,N\,m_a\,V_c^2\,\Delta V_c\,\omega_o\,cos\phi}\left[1 - \left(\frac{m_a\,cos\phi}{2}\right)^2\right]^{3/2} \tag{8}$$

where S is the apparent power, N is the no. of SM/arm, m_a is the arm modulation index, V_c is the rated voltage of submodule capacitor, ΔV_c is the ripple factor of V_c and $cos\phi$ is the power factor.

2.5. Arm Inductor Sizing

The arm inductor is sized based on equality of instantaneous power, considering the suppressing of the circulating current [52]. It is considering the existence of the double-fundamental-frequency in the equivalent phase, it is given by:

$$L_a = \frac{1}{8\,\omega_o^2\,C_{sm}\,V_c}\left(\frac{S}{3\,I_{2f}} + V_{dc}\right) \tag{9}$$

where ω_o is the load frequency operation in rad/s, I_{2f} is the double-fundamental-current component and V_{dc} is the total DC-bus voltage.

3. Conventional SAM Technique

This technique basically is the average voltage given by the integral of the instantaneous voltage in each sampling interval, and the instantaneous output voltage is generated by the average value of two nearest voltage levels [29]. This instantaneous voltage must be normalized. Therefore:

$$V = \frac{1}{T_s}\int_0^{T_s} v_{xi}^{*n}(t)\,dt \tag{10}$$

Applying the volt-second balance theory in the reference phase voltage expressed in terms of two nearest voltage, it is:

$$\begin{aligned} v_{xi}^{*n}\,T_s &= V_{x1}\,T_{x1} + V_{x2}\,T_{x2} \\ T_s &= T_{x1} + T_{x2} \end{aligned} \tag{11}$$

where V is the average voltage; v_{xi}^{*n} is the normalized reference phase voltage with offset; V_{x1} and V_{x2} represents the nearest phase voltage levels; T_{x1} and T_{x2} represents the dwell times and T_s is the sampling time. The implementation of this modulation technique consists of three main steps:

3.1. Identification of Two Nearest Voltages

To identify the nearest voltages, it is necessary to generate the phase modulation signals for open/close-loop converter control, this reference output voltage is defined by:

$$V_{xi} = \frac{V_{dc}}{2} \times m_a sin(\omega t + \theta_x) \tag{12}$$

$$V_{dc} = NV_c \tag{13}$$

where: V_{dc} is the total DC-bus voltage, V_c is the submodule capacitor voltage, N is the number of submodules in normal operation, m_a is the arm modulation index (0 to 1), ω is the fundamental angular frequency and θ_x is the phase angle $\in \{0, -\frac{2\pi}{3}, \frac{2\pi}{3}\}$ (represents a balanced three-phase system).

The reference phase voltage in terms of submodules number and its capacitor voltage is given by:

$$V_{xi} = \frac{NV_c}{2} \times m_a sin(\omega t + \theta_x) \tag{14}$$

The normalized reference phase voltage is obtained dividing this voltage by a submodule's rated capacitor voltage, this results in:

$$v_{xi}^{n} = \frac{N}{2} \times m_a sin(\omega t + \theta_x) \tag{15}$$

And then, an offset value of $\frac{N}{2}$ is added:

$$v_{xi}^{*n} = \frac{N}{2} \times [1 + m_a sin(\omega t + \theta_x)] \tag{16}$$

Normally, this normalized voltage-level has steps in range from 0 to $N + 1$ and represents the number of submodules per arm in ON-state.

The lower (V_{x1}) and the upper (V_{x2}) phase voltage levels are obtained from Equation (16), these two are known as the nearest voltage levels, given by:

$$\begin{aligned} V_{x1} &= \text{floor}(v_{xi}^{*n}) \\ V_{x2} &= \text{floor}(v_{xi}^{*n}) + 1 \end{aligned} \tag{17}$$

3.2. Calculation of Dwell Times

During a time T_{x1} and T_{x2} the voltages V_{x1} and V_{x2} are applied, respectively, over a sampling interval of T_s. From the volt-second balance given in (11), is considering the duty cycles $\delta_1 = T_{x1}/T_s$ and $\delta_2 = T_{x2}/T_s$. Finally, the dwell times are given by:

$$\begin{cases} T_{x2} = \dfrac{(v_{xi}^{*n} - V_{x1})}{V_{x2} - V_{x1}} T_s \\ T_{x1} = T_s - T_{x2} \end{cases} \tag{18}$$

The duty cycle is compared with a symmetrical triangular waveform over a sampling interval T_s to generate the pulses g_t and $\overline{g_t}$, respectively, these interactions are shown in Figure 3.

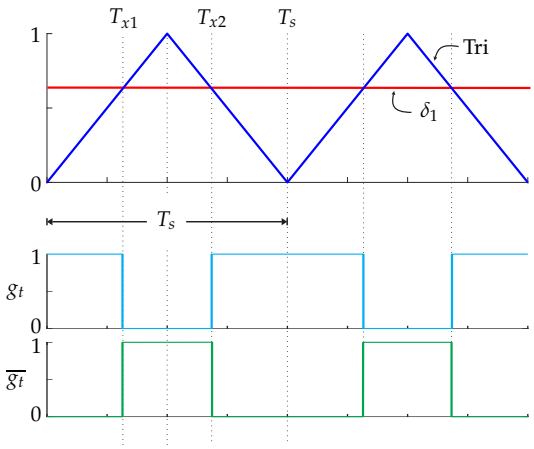

Figure 3. Dwell times of voltage levels, conventional SAM technique.

The pulse g_t and $\overline{g_t}$ are applied to the submodules in the upper and lower arms to generate the instantaneous arm voltage level.

3.3. Calculation of the Arm Voltage Levels

The instantaneous upper and lower arm voltage level is calculated by applying the following principle:

- In each sampling period, the number of submodules in ON-satate, considering the upper and lower arm, is maintained constant and equal to N (remember that the total number of submodules in one leg is equal to $2N$).

This means that, for obtain N-submodules combinations exists $2N$ options in each sampling period, i.e., C_N^{2N} [5,29,53].

Consequently:

$$m_{xl} = V_{x1} + g_t \tag{19}$$

$$\begin{aligned} m_{xu} + m_{xl} &= N \\ m_{xu} &= N - m_{xl} \end{aligned} \tag{20}$$

Also, the instantaneous arm voltage-level of one-phase, considering the upper arm (m_{xu}) and lower arm (m_{xl}) voltage-level, it is given by:

$$m_x = \begin{bmatrix} m_{xu} & m_{xl} \end{bmatrix} \tag{21}$$

Figure 4 shows the operation principle of the conventional SAM, where is obtained the instantaneous arm voltage levels, considering $N = 10$ and $m_a = 0.98$. The phase voltage level is obtained through the interaction of the arms voltage level, obtaining $N + 1$ levels, the objective of this paper is to improve this technique for $2N + 1$.

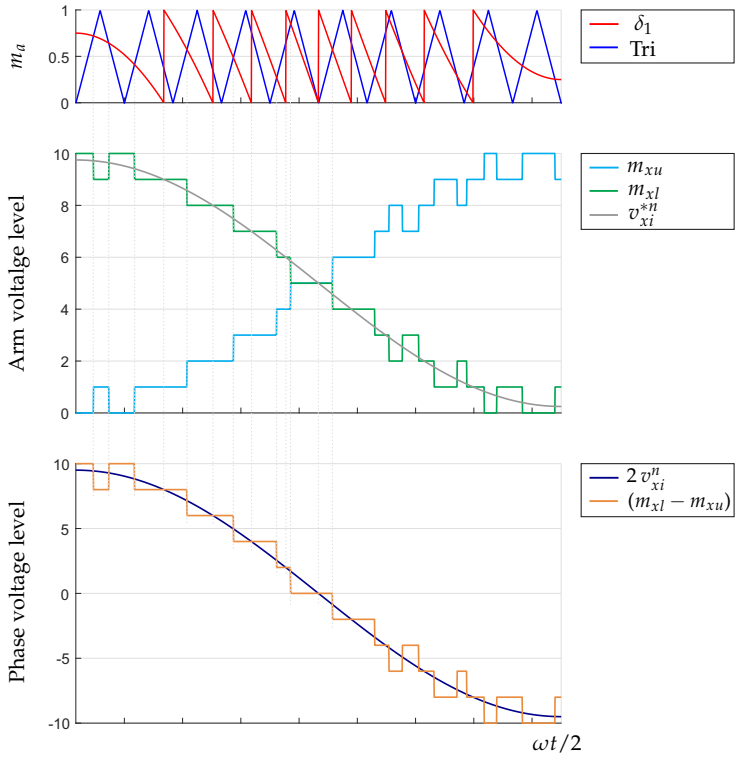

Figure 4. Operational principles of the conventional SAM.

4. Improved SAM Technique

The main drawbacks of the previously analyzed SAM technique are:

- The phase voltage waveform has $N + 1$ levels only.
- The high THD's value of the inverter output voltage.

In order to improve these parameters, it is proposed this technique.

4.1. Identification of Two Nearest Voltages

For the identification of two nearest voltages, the same calculations are considered until arriving at (16) which represents the number of submodules per arm in ON-state and it has steps in the range from 0 to $N + 1$. Where v_{xi}^{*n} is the normalized reference inverter output voltage.

4.2. Calculation of Dwell Times

In order to calculate the pulses patterns, term widely used to define the waveform that contains the state of the pulses (added) of the upper or lower arm switches. It is necessary to obtain the reference waveform that takes on values between 0 to 1, and it is given by:

$$\begin{cases} T_{x2} = \dfrac{(v_{xi}^{*n} - V_{x1})}{V_{x2} - V_{x1}} T_s \\ T_{x1} = T_s - T_{x2} \\ T_{x4} = \dfrac{(V_{x2} - v_{xi}^{*n})}{V_{x4} - V_{x3}} T_s \\ T_{x3} = T_s - T_{x4} \end{cases} \tag{22}$$

Note that, for the commutation, the duty cycles $\delta_2 = T_{x2}/T_s$ and $\delta_4 = T_{x4}/T_s$ are associated with the dwell times T_{x2} and T_{x4}.

The dwell times calculated in Equation (22) will be compared with a symmetrical triangular waveform over a sampling interval T_s. The pulse g_{ta} is applied to the submodules in the upper arm to generate the upper arm voltage level and the lower arm voltage level is obtained by using the pulse duration g_{tb}, of the corresponding phase. These interactions are shown in Figure 5.

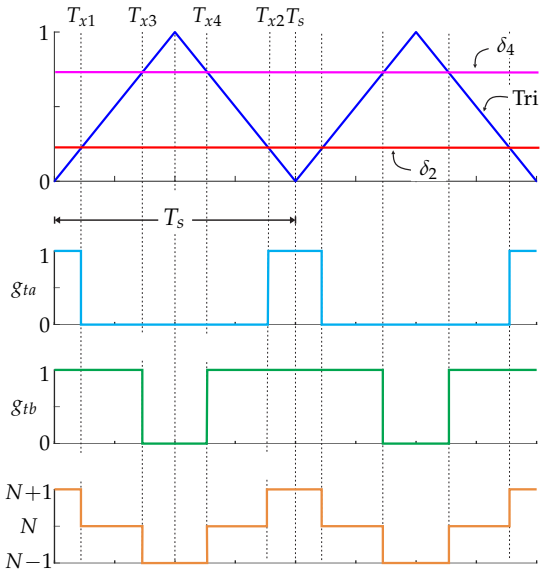

Figure 5. Dwell times of voltage levels, proposed SAM technique.

One way to improve the quality of the inverter output voltage is to look at the performance of the total number of inserted submodules. In the proposed technique, the inserted submodules number varies among $N-1$ and $N+1$ during a sample time T_s, and the average value of inserted submodules number is still equal to N.

The nearest voltage level corresponding to each duty cycle, are given by:

$$\begin{aligned} V_{x1} &= \text{floor}(v_{xi}^{*n}) \\ V_{x2} &= V_{x1} + 1 \\ V_{x3} &= (N-1) - V_{x1} \\ V_{x4} &= V_{x3} + 1 \end{aligned} \tag{23}$$

Figure 6 shows the arm voltage level corresponding to the instantaneous arm voltage level for the upper and lower arm.

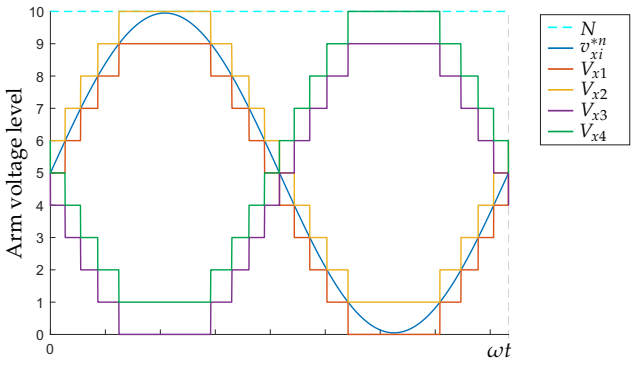

Figure 6. Corresponding voltage levels for v_{xi}^{*n}.

4.3. Calculation of Arm Voltage Levels

The instantaneous arm voltage levels are obtained between the ratio of the nearest voltage level and the gating pulses, given by:

$$\begin{aligned} m_{xl} &= V_{x3} + g_{ta} \\ m_{xu} &= V_{x1} + g_{tb} \end{aligned} \tag{24}$$

Likewise, to illustrate how this step works, it is considered an MMC with 10 submodules per arm and m_a equal to 0.98, the resulting waveforms are shown in Figure 7.

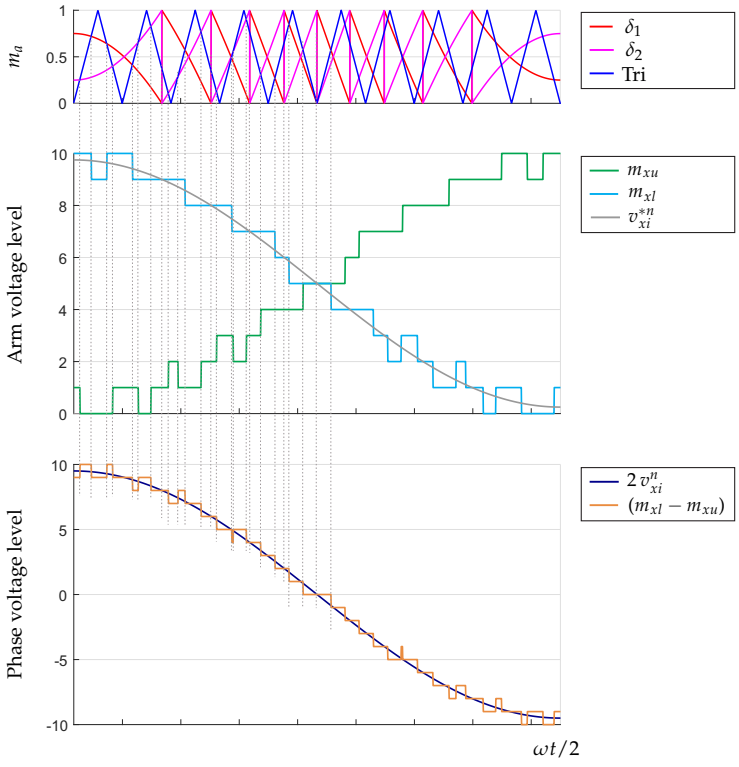

Figure 7. Operational principles of the improved SAM technique.

5. Voltage Balancing Algorithm Proposed

The voltage balancing stage is of great importance to maintain the capacitor voltage of the submodules at the same voltage level, this allows the MMC to have a symmetrical operation between the arms of the same phase. Through the Fast Voltage Sorting algorithm and the Reduced Switching Frequency (RSF) algorithm proposed, it is possible to balance the voltage of the submodules and distribute the switching pulses for the submodules, each part will be explained in detail below.

5.1. Fast Voltage Sorting Algorithm

The Fast Voltage Sorting (FVS) algorithm proposed unlike the traditional sorting algorithm, swaps the SM voltage (looking only for the highest or lowest value, depending on the sign of the arm current i_{xy}) with the objective of obtaining only the position of said voltage in the vector that contains all the voltages of the same arm. This arrangement lightens the processing since by means of the permutation it is not necessary to store the pivot element in a buffer.

In Figure 8 is shown the normalized SM voltage together with its associated index, these two together indicate the voltage of j-submodule, where j is the j-th element, for explanatory purposes, at the beginning, the elements of the array (SM voltages and the SM index) are displayed randomly and, as the sweep occurs (from right to left), if the condition is fulfilled, the elements are exchanged.

In the initial array, the first two elements are each compared (if the condition is met, they are swapped with themselves), these elements have been marked (pink) and the comparison proceeds from right to left until reaching the other end. Note that at each new cycle the position of the elements will change depending on the value of their voltage and the index of the SMs, and array will be sorted again.

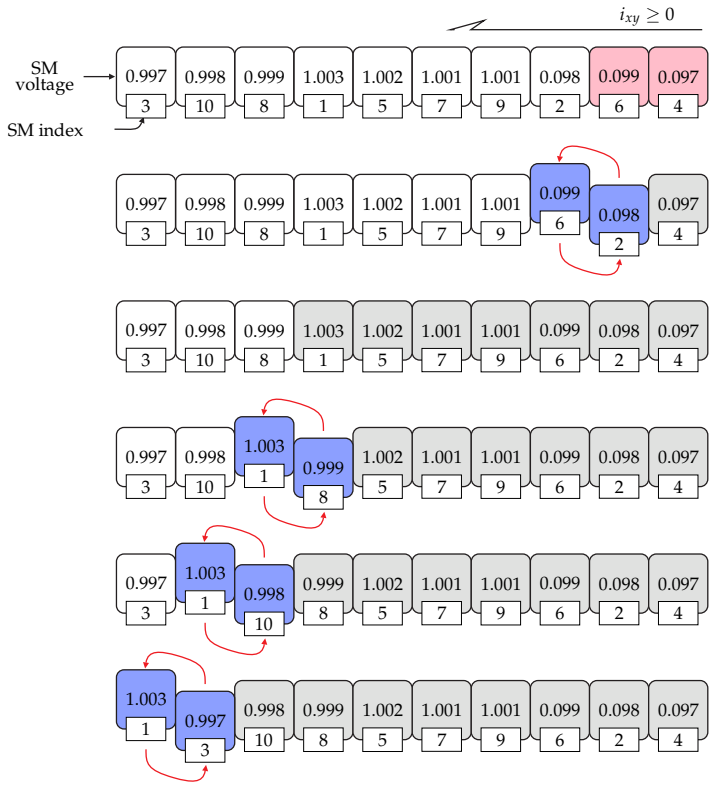

Figure 8. Submodule voltage sorting process.

5.2. Reduced Switching Frequency

Once the index vector $\mathbf{X}_{xy}$ is obtained (after the fast classification), the commutation pulses are generated for each SM, according to the priority provided by $\mathbf{X}_{xy}$, from the last example $\mathbf{X}_{xy} = [1\ 3\ 10\ 8\ 5\ 7\ 9\ 6\ 2\ 4]$, this vector is updated at each sampling time. However, only the first $m_{xy}-$SMs are turned on (according to the instantaneous pulse pattern) of the $\mathbf{X}_{xy}$ vector, and the rest are in the off state, this process means that only by necessity charging/discharging of the capacitors, the SMs are turned on or off (for the next sample time).

Therefore, for the example used above, when the instantaneous pulse pattern $m_{xl} = 6$ and $i_{xl} \geq 0$, then the first six elements of the vector $\mathbf{X}_{xy}$ indicate which SMs should be turned on. Therefore, the sequence of SMs in ON-state is $\mathbf{S}_{xy} = [1\ 0\ 1\ 0\ 1\ 0\ 1\ 1\ 0\ 1]$.

Figure 9 shows the algorithm procedure and the gating pulses to the SMs, for the period of time defined by the observation point.

Figure 10 shows the flowchart of the general submodule voltage balancing algorithm divided into three main parts, detailed in the previous sections. The proposed FVS and RSF are used for each arm, however i-SAM provides output signals for the upper and lower arms, thus implementing the Voltage balancing algorithm for each phase of the MMC.

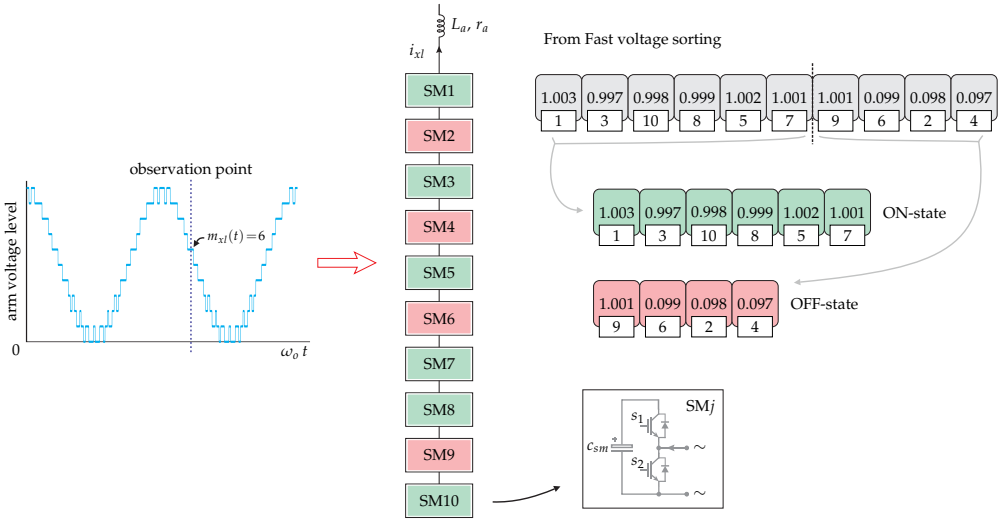

Figure 9. Reduced switching frequency process.

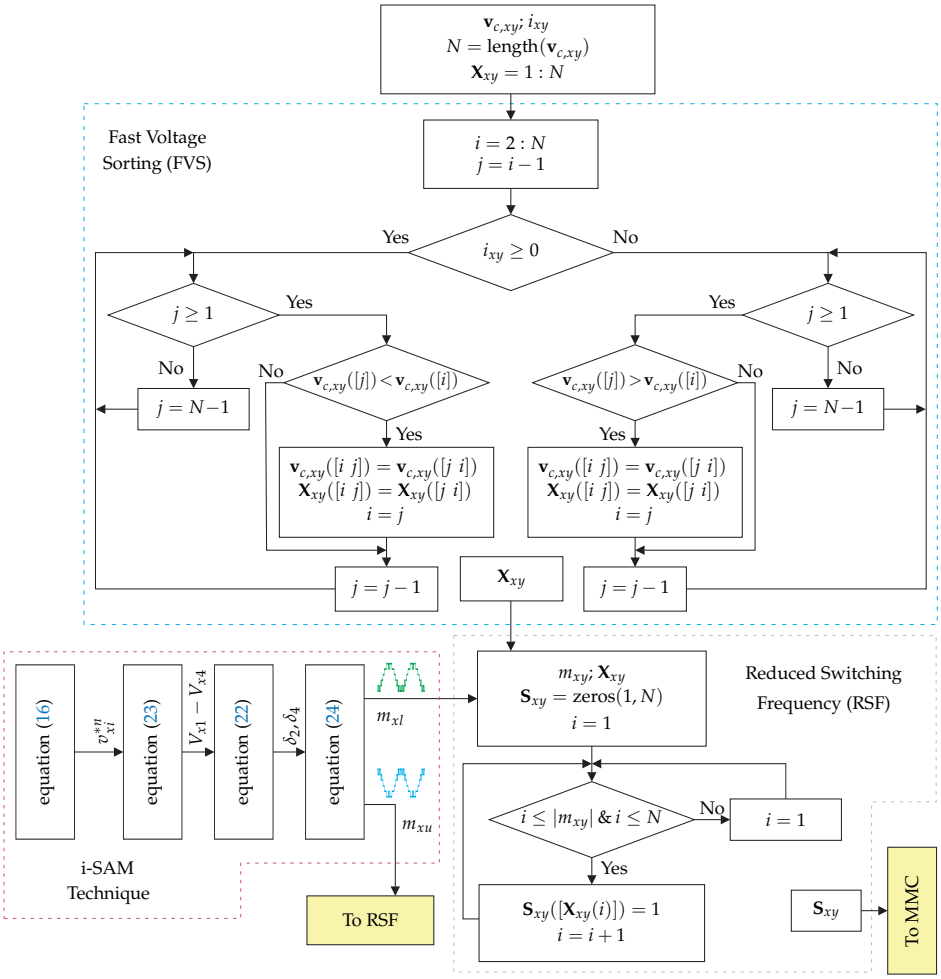

Figure 10. General submodule voltage balancing algorithm.

6. Simulation Results

It was performed by simulation various tests for validating purpose of the proposed modulation technique; for different quantities of submodules per arm (from 3 to 30). To achieve this, the parameters of Table 2 are considering.

Table 2. Simulation parameters.

Item	Variable	Value	Unit
Rated apparent power	S	8000	VA
DC-link voltage	V_{dc}	1000	V
Inverter output frequency	f_o	60	Hz
Switching frequency	f_{sw}	1200	Hz
Load resistance	R_L	125	Ω
Power factor	PF	0.95	
Arm modulation index	m_a	0.99	
Sample time	T_s	50 µs	
Simulink solver		ode23t (mod. stiff/Trapezoidal)	
Processor AMD A8-5500B APU		3.20	GHz

The submodule capacitor value used in each simulation is presented in Table 3, and the arm inductor used in all tests is $L_a = 5.70$ mH. Both of inner components are calculated using (8)–(9).

Table 3. Inner MMC component parameters.

No. of SMs/arm	C_{sm} (mF)	No. of SMs/arm	C_{sm} (mF)
3	0.62	12	2.25
4	0.84	15	3.12
5	1.01	16	3.32
8	1.74	20	4.15
10	2.18	30	6.24
		120	25.4

To validate the proposed modulation technique. Initially, the CPU-time of four modulation techniques is compared. Figure 11 shows the CPU-burning time, this is the time that takes 1 s of system simulation in Simulink.

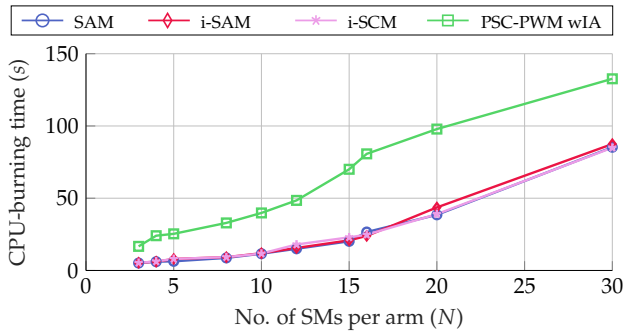

Figure 11. Number of submodules per arm vs. CPU-burning time.

This CPU-burning time is analyzed in order to determine the computational burn of the proposed technique, when compared to the other three modulation techniques, over the same conditions. Also, three parameters considered of great importance are analyzed, these are:

(1) The THD of the inverter output voltage (line-to-ground), [$\text{THD}_{v_{xi}}$ (%)], it is probably the most important parameter when considering a suitable modulation technique,

due to this parameter defines the inherent passive components sizing (submodule capacitor and arm inductor) and external components to the MMC (line filters, rated power devices, according to the application).

(2) The output voltage fundamental value, [$v_{xi,1}$ (p.u.)], it is observed to check if the technique used ensures an adequate value without compromising the effectiveness of the MMC, this parameter is important for MMC with reduced number of submodules, which usually tends to be a problem as in Staircase modulation technique, this issue is widely discussed in [33].

(3) The peak-to-peak variation of the capacitor voltage of upper and lower arm submodules, [$\Delta V_{c,pp}$ (%)], this parameter characterizes the suitable capacitor sizing and for that, firstly, it is necessary to define the modulation technique and then a suitable sizing method is applied for the inherent components. Since, the capacitor and the inductor inherent to the MMC should be sized relative to a modulation technique, so that, the dynamic behavior of the converter will be adequate for that specific method. In this case, standard sizing methods studied in Section 2 are used and, when compared to other modulation techniques, it was obtained an acceptable performance.

A comparison of these parameters is shown in Figure 12, it is considering four modulation techniques: the conventional sampled average modulation (SAM), the improved staircase modulation (i-SCM), the phase-shifted carrier with interleaved angle (PSC-PWM wIA) and the proposed technique.

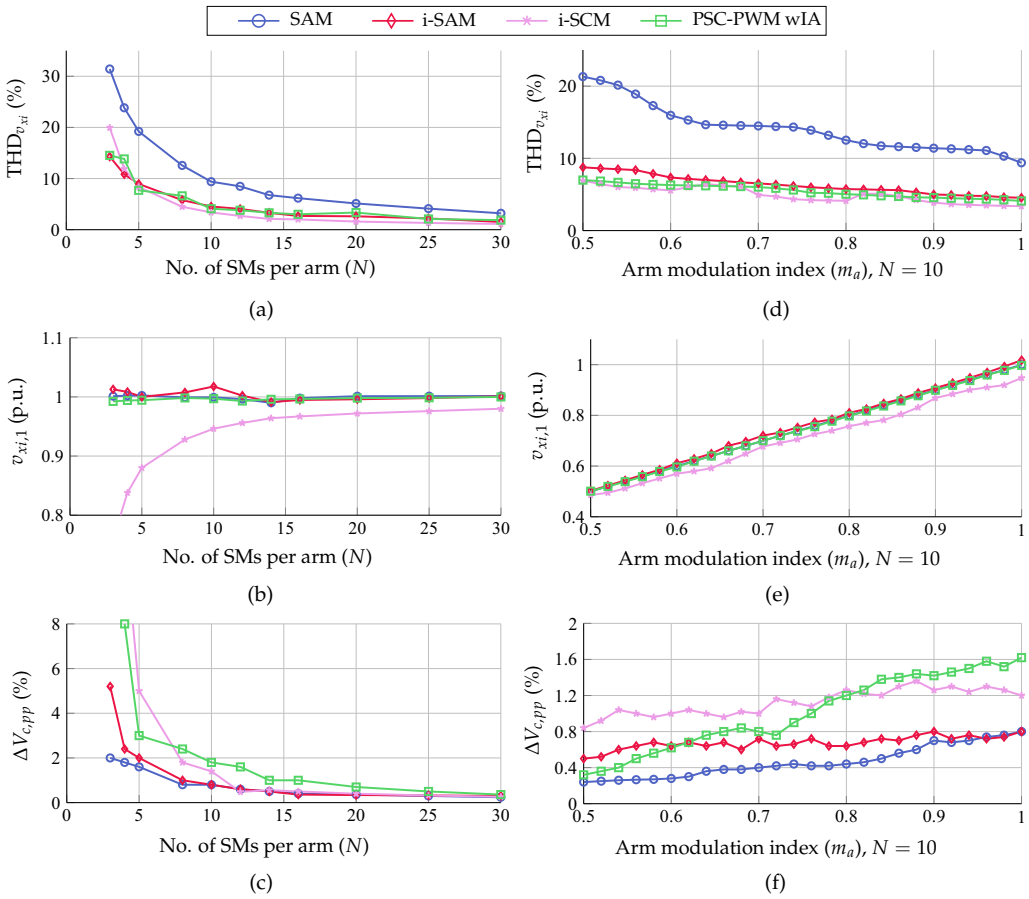

Figure 12. Comparative graphics of the proposed modulation technique versus known modulation techniques. Number of submodules per arm "N", (**a**) front THD of the inverter output voltage, (**b**) front fundamental of output voltage, (**c**) front peak-to-peak variation of the submodule capacitor voltage. Arm modulation index "m_a" with $N = 10$, (**d**) front THD of the inverter output voltage, (**e**) front fundamental of output voltage, (**f**) front peak-to-peak variation of the submodule capacitor voltage.

As shown in Figure 12, the i-SCM technique has the lower $\text{THD}_{v_{xi}}$ value, on the other hand, the $\text{THD}_{v_{xi}}$ value of the conventional SAM technique is double when compared to other techniques, mostly for smaller amounts of submodules, due that its output voltage has $N + 1$ levels.

However, the proposed SAM technique has a low $\text{THD}_{v_{xi}}$, because the output voltage has $2N + 1$ levels. In fact, the $\text{THD}_{v_{xi}}$ of the proposed technique presents values similar to those shown by more complex techniques and well developed in the literature, e.g., over PSC-PWM wIA and i-SCM, this analysis is shown in Figure 12a.

As shown in Figure 12b (for $N = 10$ SMs), the proposed technique obtains a good dc-link voltage utilization, this means that the peak value of fundamental output voltage is higher, when compared with the other techniques, even though the modulation index (m_a) remains constant. On the other hand, as the number of SMs increases, the dc-link voltage utilization is not affected.

The Figure 12c shows the comparison of $\Delta V_{c,pp}$ taking into account different quantities of SMs per arm, for the four modulation techniques analyzed. It is observed that the proposed technique has a good performance for a lower number of SMs when compared with i-SCM and PSC-PWM wIA techniques and, as the SMs quantity increases this voltage variation value tends to decrease similarly to the other techniques.

Figure 12d–f shown the effect of variations of the arm modulation index (m_a) in the $\text{THD}_{v_{xi}}$, $v_{xi,1}$ and $\Delta V_{c,pp}$ indexes, respectively. All these results were obtained considering $N = 10$ SMs.

Case of Study: Single-Phase

In this case, it is compared the dynamic performance of the MMC with the conventional and the proposed improved SAM technique. The simulations were performed considering the following parameters: rated apparent power $S = 8$ kVA, output frequency $f_o = 60$ Hz, power factor PF= 0.95, DC-link voltage $V_{dc} = 1000$ V, the number of SMs/arm $N = 10$, arm inductance 5.70 mH, submodule capacitor $C_{sm} = 2.18$ mF and switching frequency $f_{sw} = 2500$ Hz.

The upper and lower voltages are 180° out of phase with each other, it is shown in Figure 13a, these pulse patterns are processed by a capacitor voltage balancing algorithm (fast sorting algorithm), this algorithm will generate the firing pulses to the gates of the IGBTs. Figure 13b shows the displacement factor that is generated by adding the arm voltage level of both arms of the same phase, this factor determines the level increased in the current and voltage of converter output.

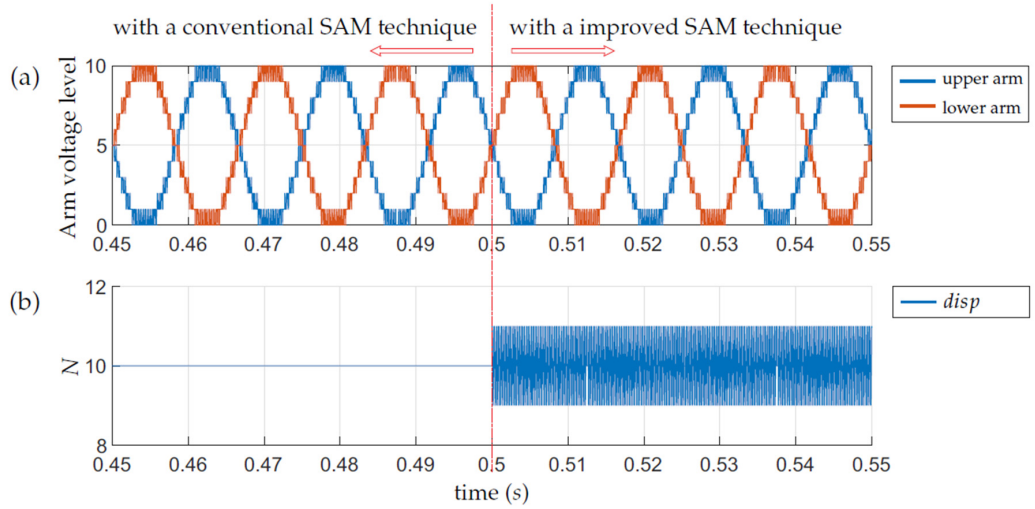

Figure 13. Dynamic performance of MMC, whit SAM and improved SAM techniques. (**a**) the upper and lower arm voltage levels; (**b**) the total inserted submodule number.

The total inserted submodule number in the conventional SAM is a constant value of N as calculated in Equation (20), this value is obtained adding the upper and lower arm voltages ($disp$). However, with the improved SAM this value is alternated from $N-1$ to $N+1$, but the average value in each sampling interval is N, according to described in Section 4, this waveform is the displacement factor.

The output voltage waveform is shown in Figure 14a, this waveform is measured at the inverter output with a resistive load, for $t < 0.5$ the reference is modulated by the conventional SAM, this means that $N+1$ levels at output is obtained. However, when $t > 0.5$ the reference is modulated with the proposed SAM technique and this leads to obtaining $2N+1$ levels at output. Therefore, the output voltage THD with the proposed techniques is lower (3.98%) when compared to the conventional SAM (4.91%), for this specific case ($N = 10$). In Figure 14b is presented the THD values.

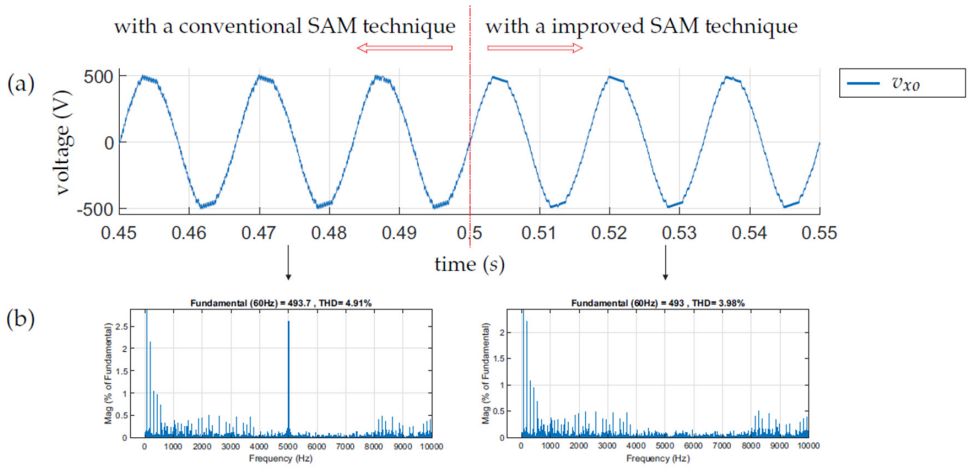

Figure 14. (**a**) the phase voltage levels; (**b**) the phase voltage harmonics detail.

In the conventional SAM, the upper half-cycle is identical to the lower half-cycle, this is because the algorithm performs a subtraction based on the assumption of: The number of submodules per arm of an MMC under healthy operating conditions is N.

Figure 15 shows the voltage of all the submodules of the same phase as well as details demonstrating the balancing of the voltages.

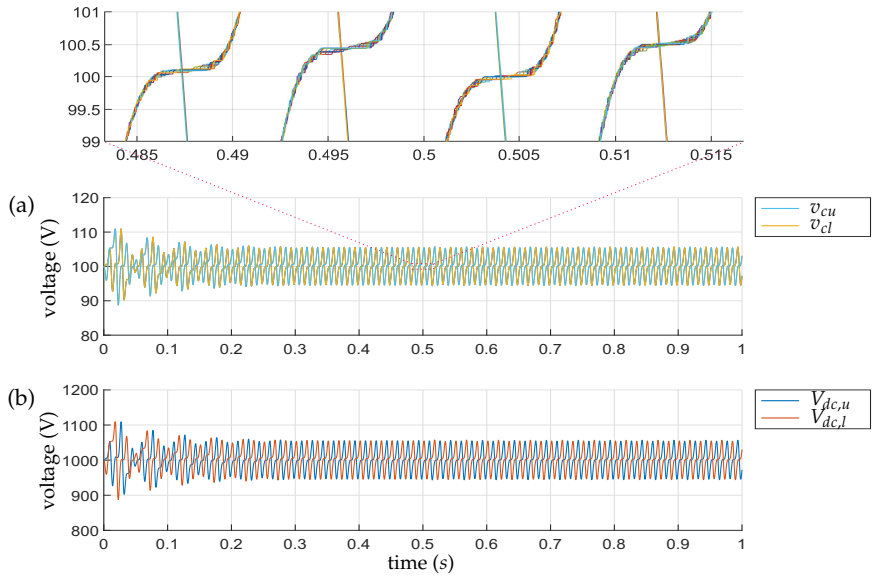

Figure 15. (**a**) The submodule capacitor voltages, whit SAM and improved SAM techniques; (**b**) The leg voltages.

Figure 15a shows the voltage of all submodules capacitors, these voltages are balanced by the fast sorting algorithm (the upper arm capacitor voltages are superimposed on each other, similarly in the lower arm). With the conventional SAM it is observed that $\Delta V_{c,pp} = 8.2$ V, and with the improved SAM is $\Delta V_{c,pp} = 8.4$ V which represents around 8% at steady-state operation, these values are not very distant from each other.

Figure 15b shows the sum of the voltage of all the submodules of the same arm (upper and lower), at the beginning there are transients that come from the charging of the capacitors and when it is in steady-state it can be seen that the two voltages are balanced, this guarantees a symmetrical waveform at the output of the MMC.

7. Conclusions

This article presents the improved SAM, this improved technique makes it possible to obtain $2N + 1$ levels at the inverter's output compared to the conventional SAM. By simulation were compared four modulation techniques: the peak-to-peak variation of the submodule capacitor voltage, THD of the inverter output voltage and the fundamental value of the output voltage. These parameters were analyzed taking into account several quantities of SMs/arm, and also, for the arm modulation index with a fixed number of SMs/arm, being able to demonstrate good performance in comparison to other modulation techniques.

Another parameter that is considered is the CPU-burning time, this numerical value is obtained by simulating the system for one second. The proposed technique has a low CPU-burning time due to the low switching frequency and the number of interactions, this is, that as N increases the number of interactions also increases. The proposed modulation technique can be on par with simple techniques like staircase modulation, with a faster dynamic response when compared with multiple carriers techniques.

There is still a great gap within the modulation techniques because the MMC is complex, each variation, either in the form of application or simply increasing or decreasing the number of submodules per arm, the MMC needs a specific modulation technique, that is , the modulation needs to be adapted because the dynamic behavior of the MMC is different for each type of application and for a different number of submodules per arm due to which less interactions will be obtained in the intermediate voltage levels ($N > 1$ and $N < N$) and more interactions at extreme voltage levels ($N = 1$ and $N = N$), directly observed in the output voltage of the MMC. On the other hand, voltage balancing is called fast sorting algorithm due to the fast classification of the voltages of the submodules, this is done depending on the direction of the current, a quick verification to organize the elements that meet the condition without interfering with the elements that do not comply, without the need to use a pivot element.

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Abbreviations

The following abbreviations are used in this manuscript:

VSC	Voltage Source Converter
MLC	Multilevel Converter
MMC	Modular Multilevel Converter
PWM	Pulse Width Modulation

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