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A Novel Single-Phase Shunt Active Power Filter with a Cost Function Based Model Predictive Current Control Technique

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Abstract: For a single-phase Shunt Active Power Filter (SAPF) with a two-step prediction, this research presents a modified current control based on a Model Predictive Current Control (MPCC) technique. An H-bridge inverter, a DC link capacitor, and a filter inductor comprise the single-phase SAPF topology. The SAPF reference current is computed using the DC-link capacitor voltage regulation-based PI control technique. The weighting factor-based model predictive current controller is used to track the current commands. The essential dynamic index for evaluating waveform quality is the Total Harmonic Distortion (THD) of a source current and switching frequency of power switches. The conventional methods the THD and switching frequency are not considered as an objective function, so that a weighting factor-based MPCC technique is used to obtain a good compromise between the THD of the source current and switching frequency of power switches. Through MATLAB simulation and experimentation with the Cyclone-IV EP4CE30F484 FPGA board, the usefulness of the proposed control technique is proven. As compared with hysteresis, predictive PWM, and conventional MPCC control methods, the cost function-based MPCC algorithm provides a lower switching frequency (13.4 kHz) with an optimal source current THD value.

Keywords: cost function; model predictive current control; single-phase shunt active power filter; THD

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1. Introduction

Exclusively, for commercial and household applications, a single-phase active power filter has emerged as a very promising converter technology for enhancing power quality. The deterioration of power quality has become the most significant issue in modern society. The presence of harmonics in the commercial and domestic applications causes equipment heating, malfunctioning of electrical and electronics equipment, and transformer heating. Compared with traditional passive filters, the active power filter has promising features in power semiconductor device losses, power quality, structural simplicity, power regulation ability, and expanding flexibility. According to filter connection, the active power filter is classified into shunt, series, series shunt, and hybrid. Due to their small size, low cost, ability to adjust both current harmonics and reactive power, and improved efficiency, SAPF are mostly employed in medium- and low-power installations. The voltage source inverter and passive energy storage devices, such as filter inductance and DC-link capacitor, make up the basic construction of the shunt active power filter.

The primary control goal of SAPF is to adjust for harmonics and reactive power produced by the Nonlinear Load (NLL). During the harmonic compensation procedure, current control is one part and reference harmonic current extraction is the other part.

Several approaches have been presented to determine the compensation current, such as DC-link capacitor voltage control, PQ theory, and DQ theory [1–6]. The author in [6] used a DC-link capacitor voltage management approach that did not require sophisticated calculations and was simple to apply. Various current control strategies, such as hysteresis control [7,8], double-band hysteresis current control [9], and the predictive PWM control technique [10], were advocated, and their quality was appraised in many research publications that can be found in the literature. Over the last decade, many researchers have focused on power converters using model predictive control due to its simplicity, rapid transient response, easy inclusion of constraints, and nonlinearities [11,12]. To reduce the algorithm complexity and shaping, traditional MPC approaches rely on one sample forward prediction. Long prediction horizons were proposed by the authors in [13] in order to enhance power converter performance control. The two-sample-ahead predictive control approach for an NPC inverter with an output LC filter was suggested, experimentally tested, and proven in [14].

The main issue in using the MPC approach is determining the way in which the weighting factors affect future system operations in order to produce the lowest feasible error in the controlled variables [11]. The approach of selecting appropriate weighting factors is another non-trivial multi-objective optimization issue [15]. Thus, MPCC is one of the most interesting techniques for SAPF application to achieve a good dynamic performance [16–19]. The authors in [16] used an MPCC method to a single-phase shunt active power filter for harmonics and reactive power compensation. In [17], the author proposed an MPC based on three-phase SAPFs to avoid using the weighting factor to compensate the unbalanced current and current harmonic components produced by single-phase nonlinear loads. The DC-link voltage during load fluctuations was measured using a multi-objective predictive control approach applied to a single-phase three-level neutral-point-clamped (NPC)-based active power filter (APF) for harmonic compensation and self-support in [18]. In [19], the author suggested a modified U-cell five-level inverter (MPUC5) for a single-phase Active Power Filter (APF) using a Model Predictive Control (MPC) technique. Authors in [20] proposed a PV-based dual-stage, multi-functional grid-connected inverter. This approach offers better efficiency and more stability under load changing conditions.

The majority of work reported in the literature focuses on the dynamic performance of SAPF and THD of the source current. The lowering of power converter switching frequency is still a study area in the realm of FCS-MPC-based SAPFs [20].

This manuscript presents a novel current control technique based on the cost function-based MPCC of a single-phase SAPF. The novelty of this manuscript is the use of a weighting factor in the cost function, which reduces the switching frequency and enhances the reactive power in the utility and removes harmonic currents in the PCC. The outcomes were compared with various traditional current control methods, and it was found that it effectively tracked references with reduced switching frequency. Complete simulations were conducted using the MATLAB/Simulink environment, and real-time analysis was performed using a single-phase SAPF prototype with the Cyclone-IV EP4CE30F484 FPGA control board to confirm the efficacy of the suggested method control approach. The main aims and contributions of this manuscript are as follows.

Designs and analyzes a weighting factor-based MPCC technique to improve power quality.

To minimize the switching frequency of power switches and THD of the source current.

To assess the results using MATLAB/Simulink and verify them in real time using Cyclone-IV EP4CE30F484 FPGA technology.

The rest of this paper is organized as follows: Section 2.1 describes and models the single-phase SAPF; Section 2.2 elaborates on the weighting factor-based MPCC approach and Section 2.3 elaborates DC-link PI control scheme; Section 3 contains simulation outcomes; Section 4 provides hardware results where MPCC-based single-phase SAPF is also described; And, finally, the conclusions are presented in Section 5.

2. A Modeling and Control Algorithm

2.1. Single-Phase SAPF Description and Modeling

The single-phase MPCC-based SAPF was designed to compensate for reactive power and current harmonics. Figure 1 illustrates how the single-phase SAPF comprises a single-phase VSI with four power switches and a DC side capacitor. While connected in parallel to the grid, the DC side capacitor supplies a DC voltage to the VSI and acts as an energy buffer. The SAPF is directly linked to the low-voltage grid via filter inductance (Lf) at the point of common coupling (PCC). This supplies a compensating current, which eliminates harmonics. The compensatory current is achieved via the use of DC-link capacitor voltage control method.

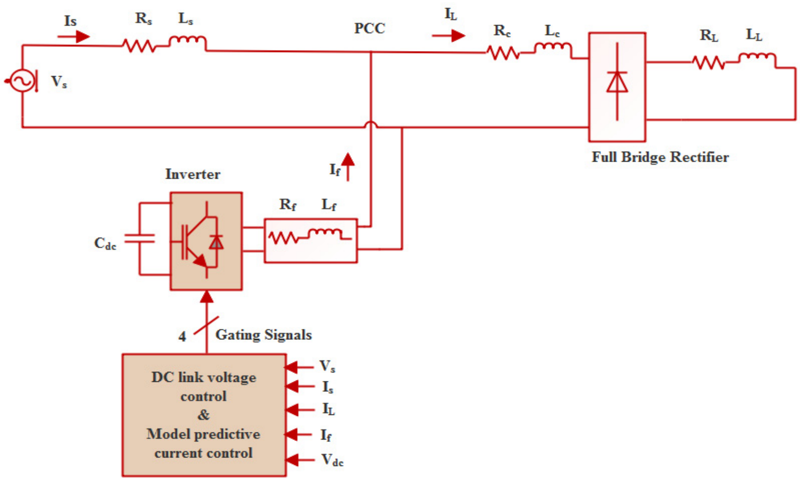


Figure 1. Configuration of the single-phase shunt active power filter.

In both simulation and real-time analysis, a single-phase uncontrolled bridge rectifier with RL load was considered as the NLL.

Typical supply voltage and current may be expressed as

$$v_s(t) = V_m \sin \omega t \tag{1}$$

$$i_s(t) = i_L(t) - i_f(t) \tag{2}$$

where V_m —magnitude of supply voltage

A nonsinusoidal current is drawn when a nonlinear load is linked to a single-phase supply. This can be stated in the following way:

$$i_L(t) = \sum_{n=1}^{\infty} I_n \sin(n\omega t + \theta_n)$$

$$i_L(t) = I_1 \sin(n\omega t + \theta_1) \sum_{n=2}^{\infty} I_n \sin(n\omega t + \theta_n) \tag{3}$$

where I_1 & I_n—peak value of load current with fundamental and nth harmonic components, and θ_1& θ_n—phase angle of load current.

The current SAPF compensation is then stated as

$$i_f(t) = i_L(t) - i_s(t) \tag{4}$$

The total instantaneous supply current, including losses after compensation, are then be stated as

$$i_s^*(t) = I_{sp} \sin \omega t \tag{5}$$

where I_{sp}—peak value of supply current. The supply current's peak value and phase angle must be established. The amplitude of the supply current is then computed using a standard proportional integral (PI) controller to evaluate the DC-link voltage error.

2.2. Model Predictive Current Control Algorithm

The block diagram of the proposed cost function-based MPCC algorithm in a single phase SAPF is shown in Figure 2. The two perditions are mainly used to improve the control performances [12]. With two-step prediction, the number of calculations and computational burdens are reduced, which is suitable for higher-power applications. It also improves load current control for various references and load circumstances [13].

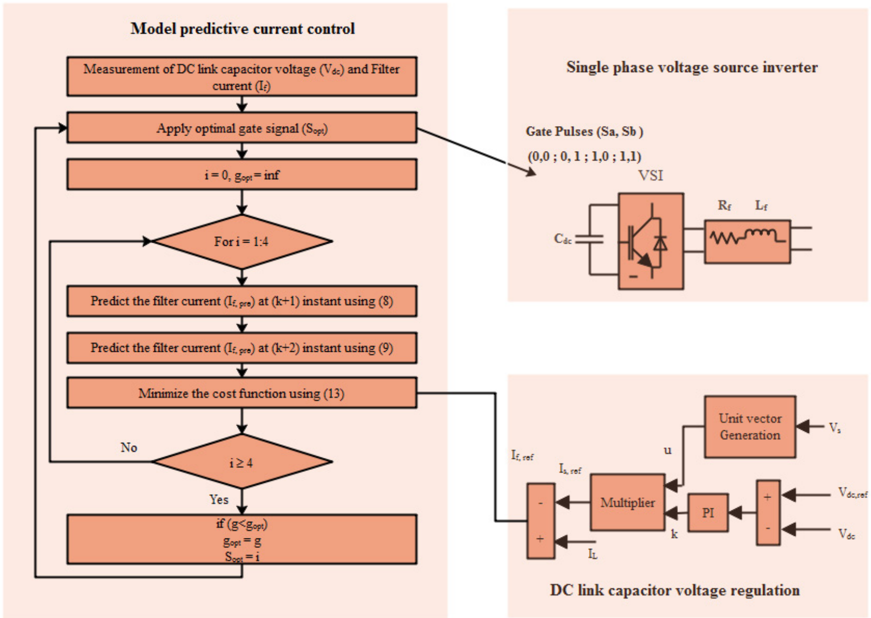


Figure 2. Model predictive current control algorithm and DC-link capacitor voltage regulation-based reference current extraction of single-phase SAPF.

The vector equation models of the SAPF filter current dynamics are expressed as

$$V_o = V_i - R_{eq} i_o - L_{eq} \frac{di_o}{dt} \tag{6}$$

Single-phase SAPF system equivalent resistance and inductance R_{eq}, L_{eq}, which may alternatively be written as

$$R_{eq} = R_f$$

and

$$L_{eq} = L_s + L_f$$

To estimate the filter current at the instant of k + 1 with a sample period T_s, the first-order approximation of the derivative is used.

$$\frac{di_o}{dt} = \frac{i_f(k+1) - i_f(k)}{T_S} \tag{7}$$

Then, 4 possible predicted filter current values of the single-phase VSI related to the inverter output voltage V_i can be attained from (6) and (7) as

$$i_{f,\ pre}(k+1) = \frac{T_s}{L_{eq}}(V_i(k) - V_s(k)) + \left(1 - \frac{R_{eq} T_s}{L_{eq}}\right) i_f(k) \tag{8}$$

where T_s is the sampling time, $i_{f,\ pre}$ and i_f, are the predicted filter currents at the next and present states, respectively. For one-step prediction (N = 1), the four switching states are used to predict the SAPF filter current, as presented in Figure 3a.

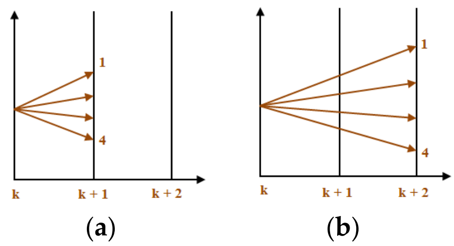


Figure 3. (**a**) Control variable of one-step prediction horizon, (**b**) control variable of two-step prediction horizon.

The four switching states are predicted at the sampling time (k + 2) for a two-step prediction horizon (N = 2) in Figure 3b.

To put it another way, the filter current may be extended to a two-step prediction horizon time as follows:

$$i_{f,\ pre}(k+2) = \frac{T_s}{L_{eq}}(V_i(k+1) - V_s(k+1)) + \left(1 - \frac{R_{eq}T_s}{L_{eq}}\right)i_f(k+1) \tag{9}$$

As a result, at the sampling instant (k), the control approach identifies a switching state that lowers the cost function in the sampling instant (k + 2). Table 1 shows the valid single-phase SAPF switching states.

Table 1. Switching states of single-phase SAPF.

S_a	S_b	V_i
1	0	V_{dc}
0	1	$-V_{dc}$
1	1	0
0	0	0

The suggested approaches' primary control goals are to improve reference current tracking and minimize switching frequency. The cost function might be stated as [5]:

$$g_1 = \left(i_{f,ref}(k+2) - i_{f,\ pre}(k+2)\right)^2 \tag{10}$$

$$g_2 = \lambda_{sw} \times n_c \tag{11}$$

where λ_{sw} is weighting factor for switching frequency reduction of the VSI; when $\lambda_{sw} > 0$, switching frequency minimization can be achieved. n_c is the number of commutations of the power semiconductors in VSI.

n_c can be expressed as follows:

$$n_c = \sum_{x=a,b} |S_x(k) - S_x, opt(k)| \tag{12}$$

where $S_x(k)$ is the predicted switching state and $S_x, opt(k)$ is the optimal switching state in the previous sample.

Usually, λ_{sw} is obtained using repetitive simulations to achieve optimal results for the control objective. λ_{sw} is evaluated using the switching frequency f_{sw} and source current Total Harmonic Distortion (THD).

The final cost function combining (10) and (11) is given as

$$g = g_1 + g_2 \tag{13}$$

The first-term focuses on the current tracking and the second-term focuses on the reduction in switching frequency.

The switching frequency (F_{sw}) is determined by counting the number of switching changes (n_{sw}) during a particular time interval $\left(T_f\right)$.

$$F_{sw} = \frac{n_{sw}}{T_f}$$

So the overall cost function aims to reduce the switching frequency and THD as much as possible. The detailed cost function based MPCC is demonstrated in Modified MPCC Algorithm (Algorithm 1).

The DC-link voltage should be kept constant in SAPF applications, and the source current reference is determined using the DC-link capacitor voltage regulation technique to compensate for the harmonic and reactive power provided by the non-linear load.

Algorithm 1. Cost Function-Based Model Predictive Current Control Algorithm

Input : $\left(i_f\right), \ (V_{dc})$
Output : $S_a, \ S_b$
Step 1: At the instant (k + 1) based on (8), predict the filter current $i_{f,\ pre}$
Step 2: At the instant (k + 2) based on (9), predict the filter current $i_{f,\ pre}$
Step 3: Calculate n_c for all switching states based on (12)
Step 4: Evaluate the cost function (g) based on (13)
Step 5: Choose the ideal switching state and apply to the SAPF. Return to Step 1

2.3. DC-Link Capacitor Voltage Control PI Control Scheme

The voltage of the DC-link capacitor is regulated using a traditional PI controller. To retain the DC-link capacitor voltage constant, compensate the total losses of the converter; to obtain the amplitude of source current reference, the PI control is used. The source current amplitude from the PI controller output is expressed as

The PI controller obtains the value of k, which can be stated as follows:

$$k = k_p\left(V_{dc,ref} - V_{dc}\right) + k_i \int V_{dc,ref} - V_{dc})dt \quad (14)$$

where k_p and k_i are the gain values of the PI controller, $V_{dc,ref}$ is the DC-link voltage reference, and V_{dc} is the measured DC-link voltage.

The PLL is used to generate the sine waveform. The output of the PI controller is multiplied by the sine waveform to generate the source current reference.

$$i_{s.ref} = k \times u = k \times \sin \omega t \quad (15)$$

The NLL current is then combined with the supply current reference to produce the filter reference current. Finally, the MPCC receives the filter reference current and actual filter current signals to generate SAPF gating signals. This PI controller employs optimal gain values (k_p,k_i).

3. Simulation Results

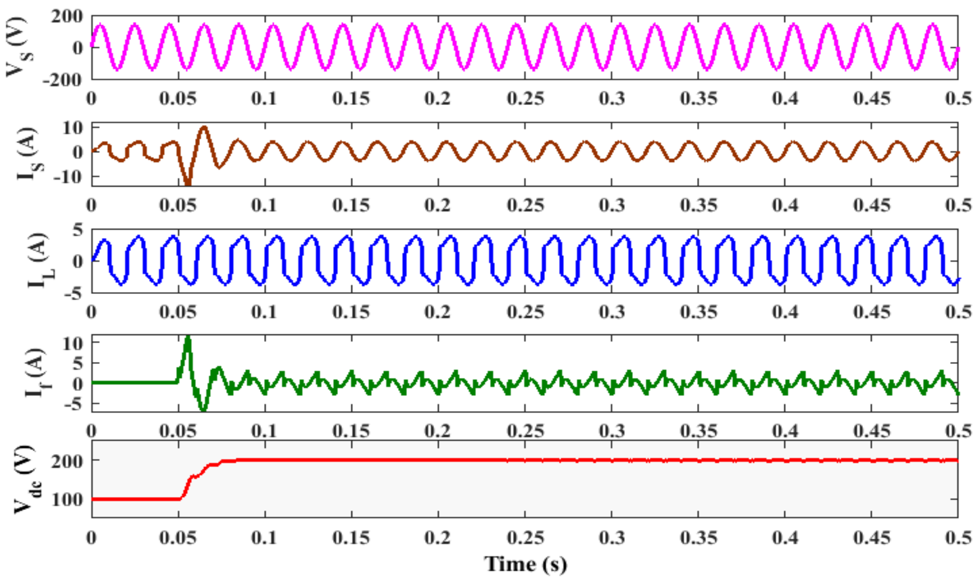
To validate the suggested control strategy, simulations were run in the MATLAB/ Simulink program with the parameters listed in Table 2. A two-step prediction horizon with a sampling time of T_s = 10 µs and cost function are indicated in Equation (4), where the switching frequency reduction term is considered. The execution times required for the one step and two-step prediction algorithms are 5 µs and 8 µs, respectively. With the developments in the microprocessor technology, it is easy to handle this higher computational requirement and also the easy inclusion of constraints and nonlinearities.

Table 2. Major components of single-phase SAPF.

S. No	Description	Components	Value
1	Supply voltage	V_s	100 V (rms)
2	DC-link capacitor voltage	V_{dc}	200 V
3	Supply frequency	F	50 Hz
4	Switching Frequency	F_{sw}	15 kHz
5	DC-link capacitance	Cdc	800 µF
6	Filter resistance and inductance	R_f and L_f	0.01 Ω and 5 mH
7	Source resistance and inductance	R_s and L_s	0.1 Ω and 1 mH
8	AC side resistance and inductance	R_c and L_c	
9	DC side resistance, inductance, and capacitance	RL_{Cdc}	28 Ω, 160 mH, and 100 µF
10	Voltage sensor	LEM-V	LV 25-p
11	Processor	Cyclone-IV EP4CE30F484 FPGA	-
12	Power-quality analyzer	Fluke 435	-
13	Mixed-signal oscilloscope	Agilent DSO-X 3014A	-

3.1. Performance Analysis with Resistive and Inductive (RL) Load Condition

The simulation results of the proposed control approach with resistive and inductive loads are shown in Figure 4. When the proposed algorithm-based SAPF was switched on at 0.1 s, with a power factor of one, the source current became sinusoidal.



(**a**)

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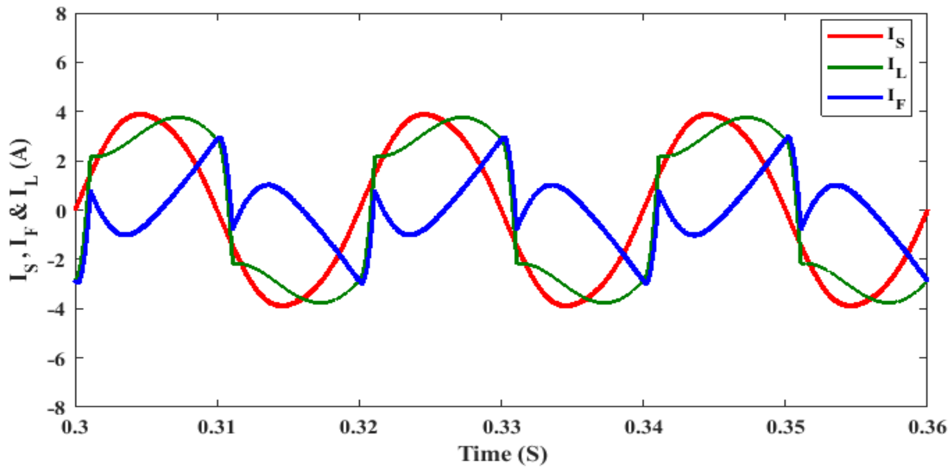

(**b**)

Figure 4. (**a**) Single-phase SAPF switch on response (**b**) source, load, and filter currents.

Weighting factor λ_{sw} in the control algorithm must be adjusted heuristically through simulations. By varying λ_{sw} from 0 to 0.35, the switching frequency was reduced from 15.071 to 7.284 kHz and the THD increased from 3.53 to 6.203%, as presented in Figure 5. The effect of λ_{sw} on the source current for different weight factors is presented in Figure 6. The THD level of the source current before filtering was 28.47%, and the matching harmonic spectrum is given in Figure 6A.

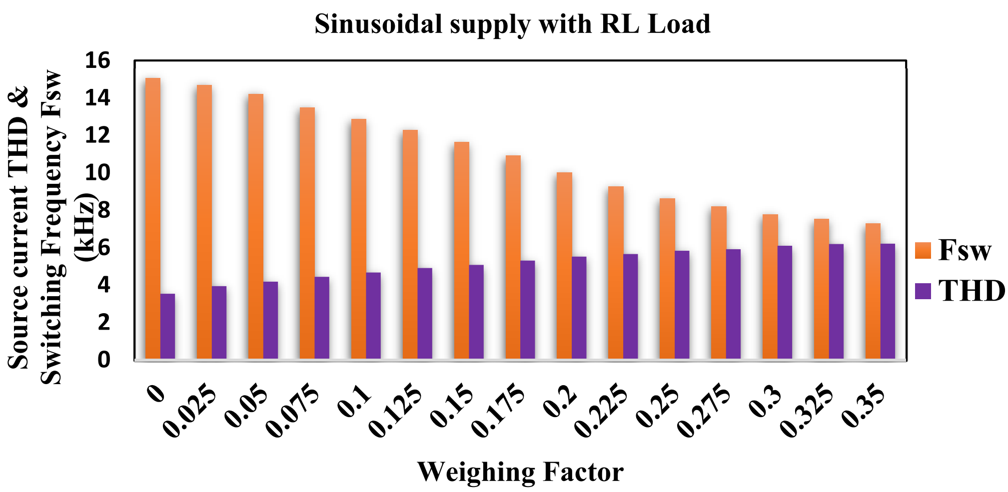

Figure 5. Variation effect of weighting factor λ on the supply current THD and switching frequency.

An acceptable value of λ_{sw} for the validation testing would be 0.1 since, with weight factor λ_{sw} = 0.1, the source current THD was determined to be 4.66% and the switching frequency was reduced from 15.071 to 12.866 kHz as shown in Figure 6B.

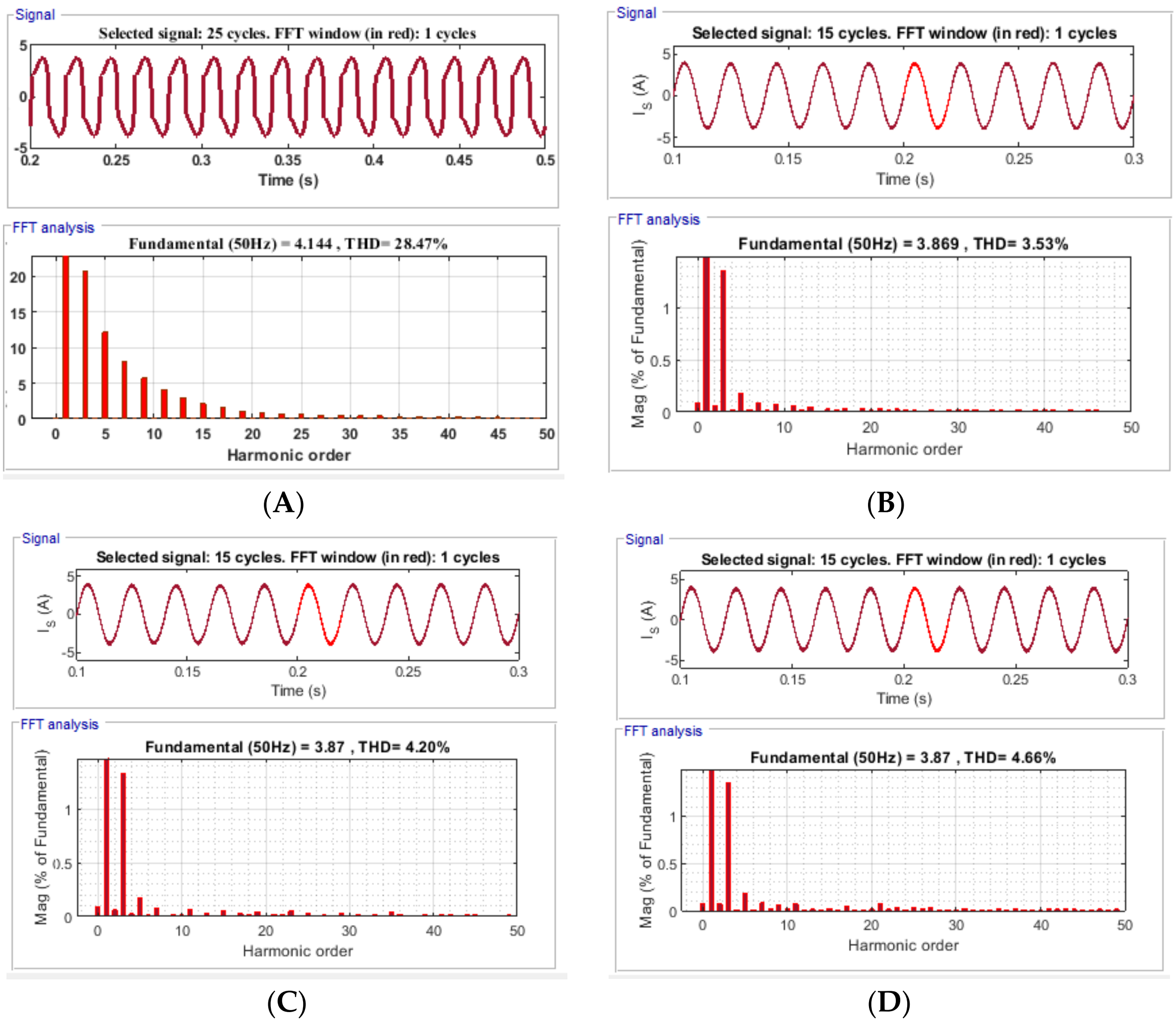

Figure 6. Simulation results of source current and harmonic spectrum: (**A**) source current (before compensation), (**B**) source current waveform ($\lambda = 0$), (**C**) source current waveform ($\lambda = 0.05$), (**D**) source current waveform ($\lambda = 0.1$).

3.2. Performance Analysis with Resistive and Capacitive (RC) Load

In this analysis, the SAPF system was analyzed with the RC load condition. The supply current THD before compensation was 35.36%. When SAPF was connected to the PCC at 0.05 s, the source current THD reduced from 35.36 to 3.97%.

The comparative analysis of the proposed controller with a conventional MPCC is shown in Table 3. From the results, it can be observed that the proposed MPCC offers a better performance in terms of reduced source current THD and switching frequency.

Table 3. Summary of the simulation test results for weighting factor-based MPCC of single-phase SAPF, including THD and switching frequency with RC load.

RC Load	Before Compensation	After Compensation	
		MPCC	Proposed MPCC (λ = 0.1)
Source Current THD (%)	35.36	3.58	3.97
F_{SW} (kHz)	-	14.307	12.620

4. Experimental Results

Figure 7 shows the complete assembly of a single-phase SAPF. VSI was developed using four IGBT switches with protection and control circuits from Mitsubishi Intelligent Power Modules (IPMs). A diode bridge rectifier with a series resistor and an inductor was also included. Load variation was achieved by connecting and disconnecting parallel loads. A current transformer (CT) detected the supply, load, and filter currents, whereas an LEM voltage transducer (LV25-P) detected the DC-link capacitor voltage and source voltage. The signal sensing and conditioning circuit are shown in Figure 8. A signal conditioning circuit feds the detected signals to the FPGA board's A/D converters. The single-phase SAPF was controlled in the digital platform based on Cyclone-IV EP4CE30F484 FPGA of the altera controller (Intel, Santa Clara, CA, USA), which is shown in Figure 9.

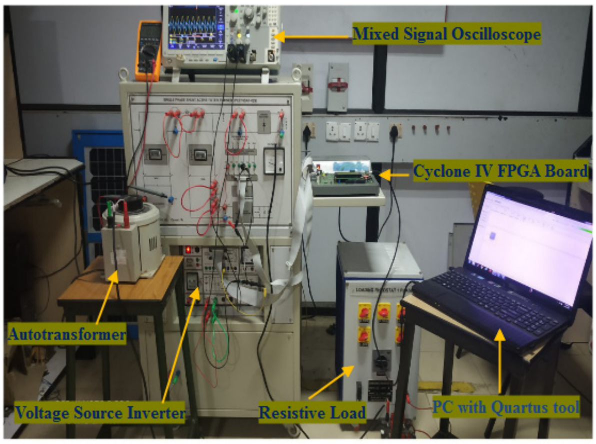

Figure 7. Complete assembly of single-phase SAPF.

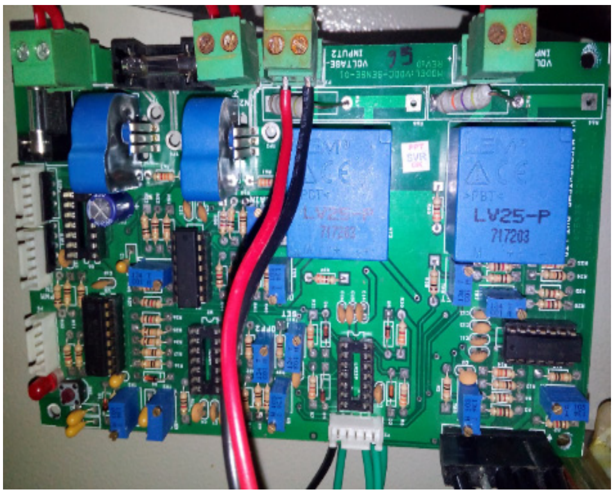

Figure 8. Signal sensing and conditioning circuit.

The design is done using Quartus II 15.0 software. The digital platform consisted of an FPGA and EPCS16 PROM devices, USB blaster, 4-channel 12-bit SPI bipolar ADC, 4-channel 12-bit SPI bipolar DAC, LCD, and on-board isolated RS232. Flash memory EPCS16 was used to configure the FPGA by connecting personal computers through a USB blaster. The VHDL code for the control of SAPF was verified, analyzed, and synthesized in the Quartus II 15.0 software platform. The JAM file was downloaded to the PROM device, which was used to configure the controller and experimental setup. The voltage and current signals were sampled using the ADC controller. Then, the controller read the signal from the ADC and generated the firing pulses to the SAPF.

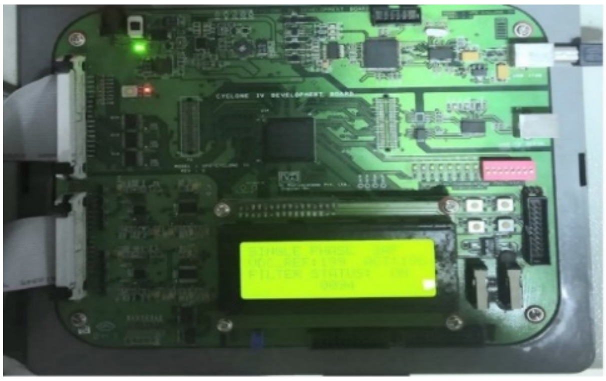

Figure 9. Cyclone-IV EP4CE30F484 FPGA controller.

The SAPF system settings were unchanged from the simulated test. The DC-link capacitor voltage was set at 200 V, while the root mean square and also the grid frequency remained at 100 V and 50 Hz, respectively. The sampling time for the proposed control scheme was 10 µs, which was suitable for high-speed FPGA processing. The suggested control technique's steady-state and switch-on responses were evaluated to ensure its practicality. The waveforms are shown in Figure 10a,b is the source voltage and the source current. Where the source current is not compensated. The supply current THD was found to be 24.9% before SAPF is connected to the PCC. It clearly showed the high harmonics of the supplying current waveform. During compensation, the supply current became harmonic-free, and the supply THD reduced from 24.9 to 3.7%. All of these waveforms were obtained using an Agilent DSO-X 3014A digital oscilloscope. Figure 10c–f illustrates the switch-on response and steady-state performance of SAPF. The harmonic current in the NLL was compensated by the operation of SAPF, so that the source current was sine in nature. The measure source current, SAPF current, and DC-link voltage are presented in Figure 10d–f, where the harmonics generated by the NLL are almost eliminated by the SAPF. The measured source voltage, filter current, and source current during switch-off conditions are exposed in Figure 10g. Figure 10h shows the PLL output. The test results show the ability to track the reference current very well and achieved source current in sinusoidal waveform with a power factor value of one. In the test, the switching frequency was nearly 15 kHz when not including the weighting factor in the cost function.

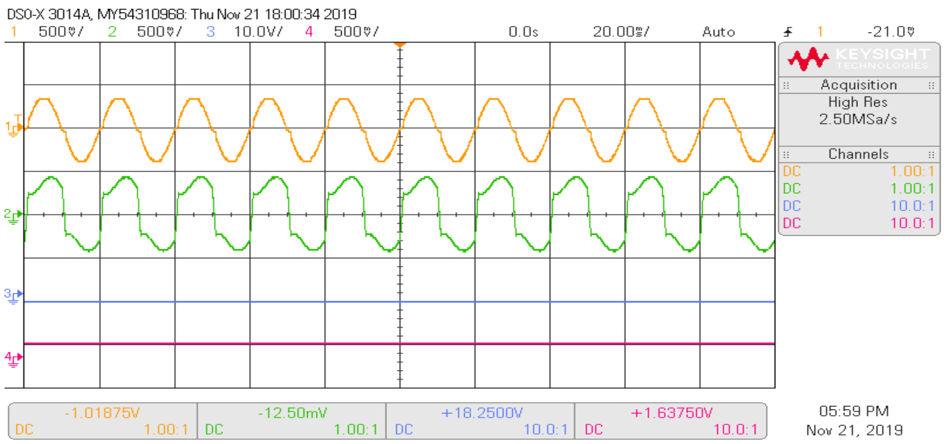

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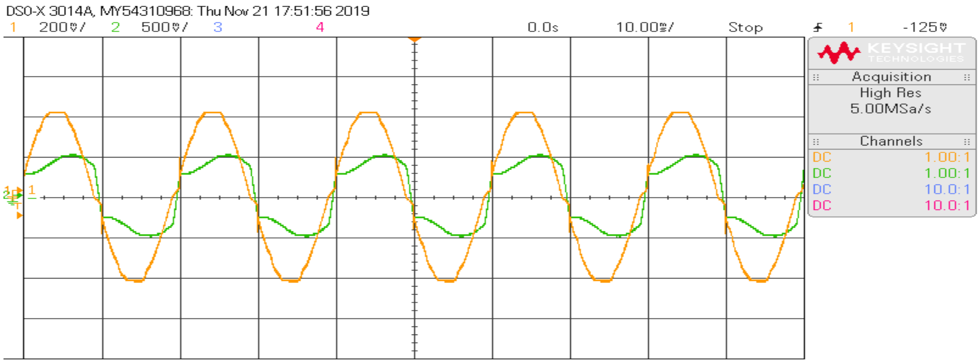
Figure 10. *Cont.*



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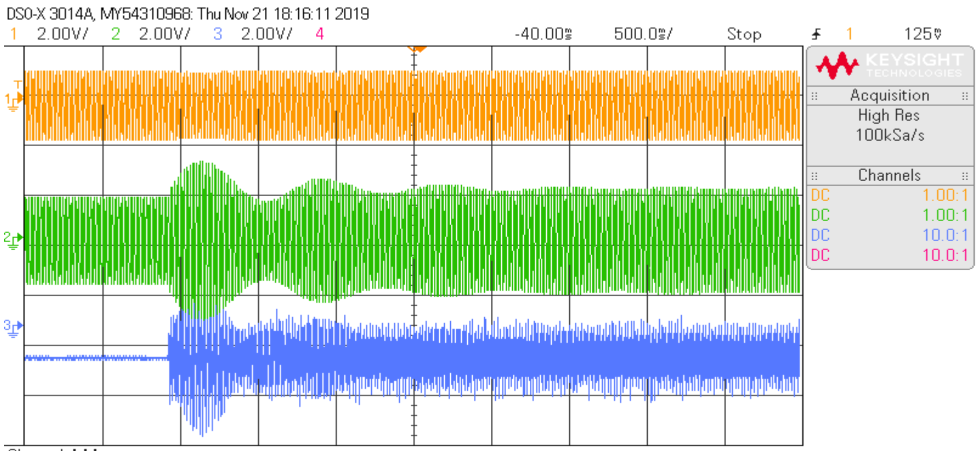

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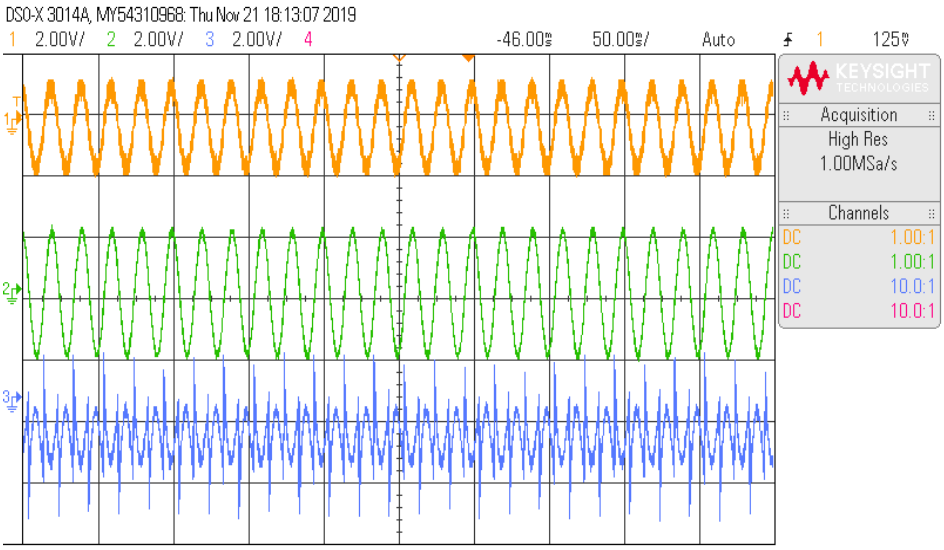

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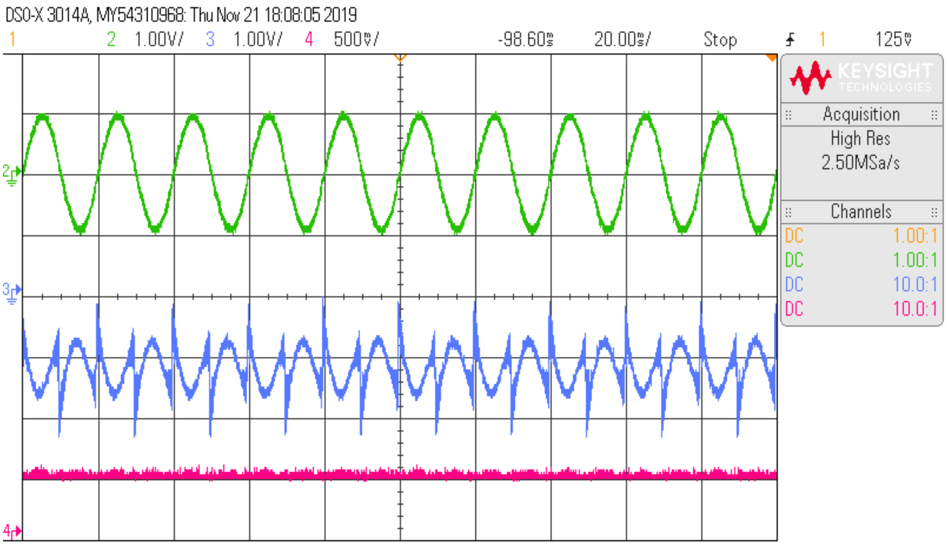

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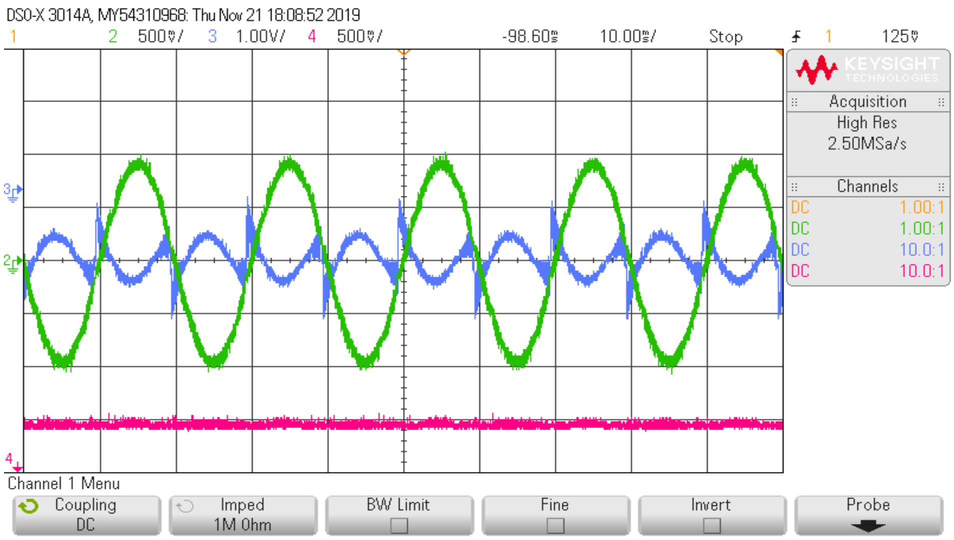

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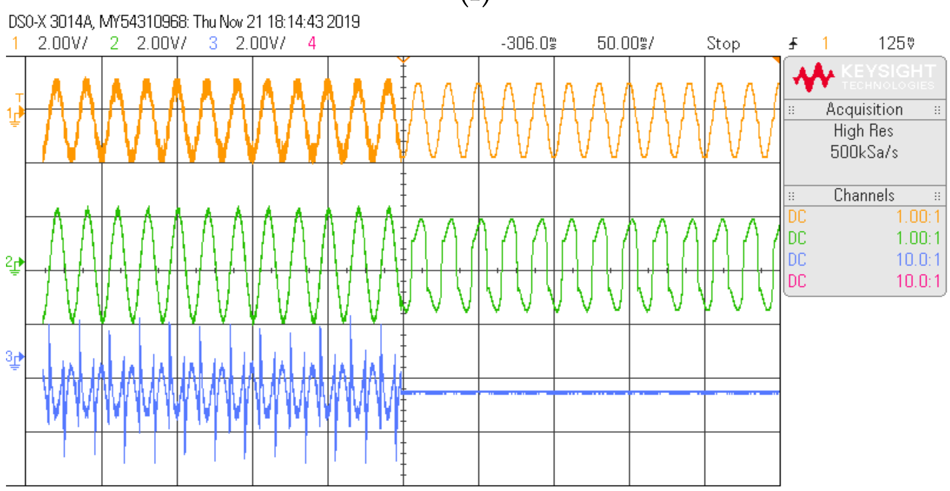

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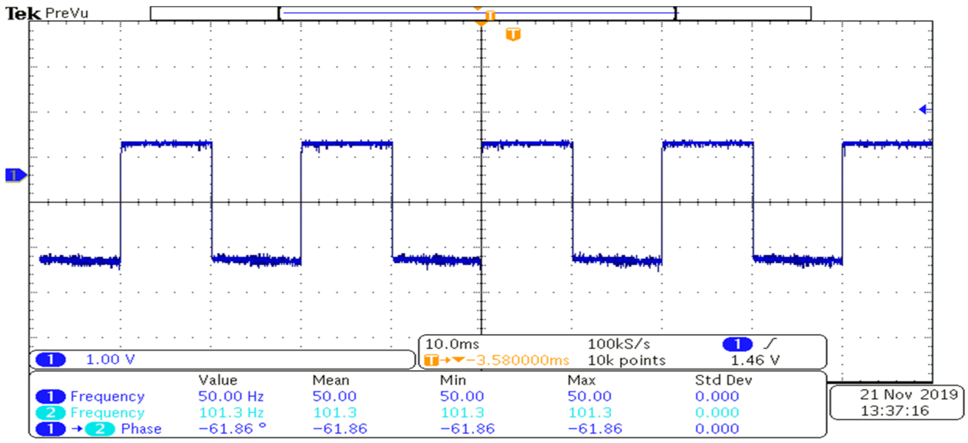

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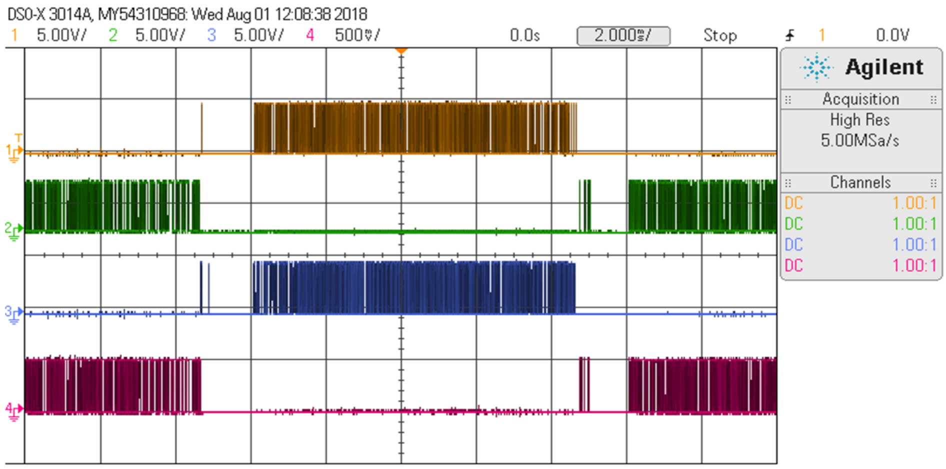
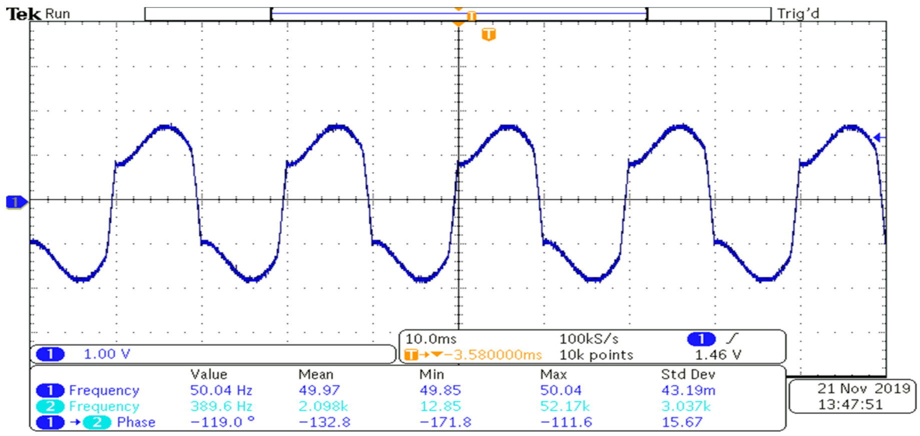


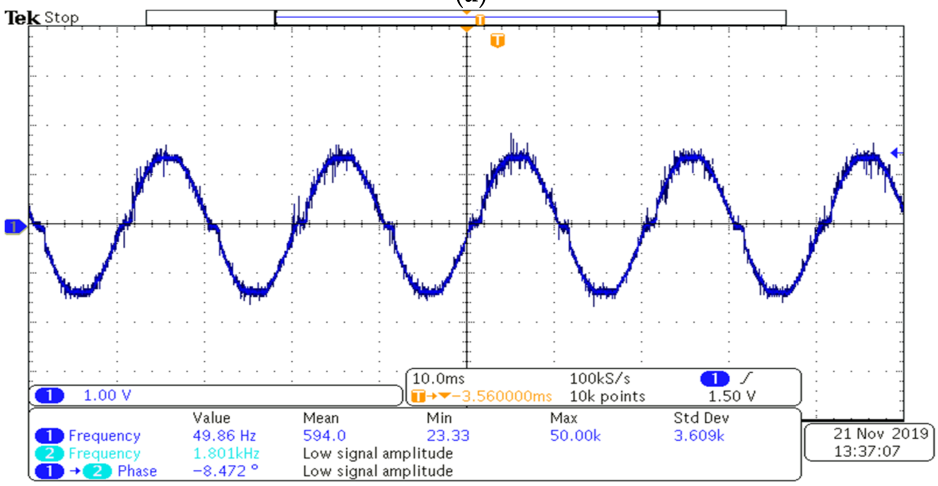
(**i**)

Figure 10. Experimental results of proposed SAPF (**a**) source voltage and current, load current, filter current (before compensation). (**b**) Source current and voltage. (**c**) Source voltage, source current, and filter current (switch-on condition). (**d**) Filter current, source voltage, and current. (**e**) Source current, filter current, and DC-link voltage. (**f**) Source current, filter current, and DC-link voltage. (**g**) Source voltage and current, filter current (switch-off condition). (**h**) PLL output. (**i**) Gating signals.

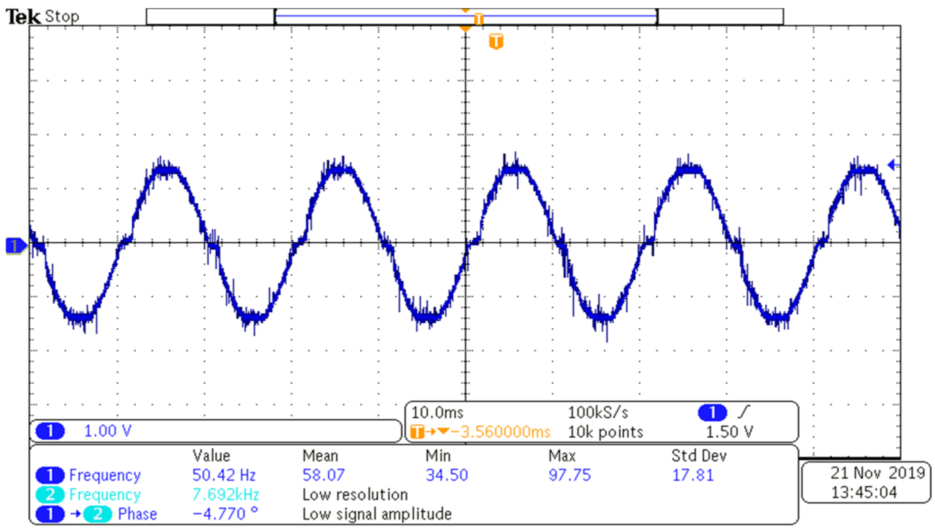
As shown in Figure 11a–d, the weighting factor is changed from 0 to 0.1, according to the change in the source current THD from 3.7 to 4.8%, and the switching frequency of VSI for the proposed control method decreases from 15.2 to 13.4 kHz in comparison to the conventional MPCC. Table 3 provides a comparison of the THD of the source current and switching frequency for the four dissimilar weighting factor values. Additionally, the comparison between various current controllers in the simulation and hardware based on source current THD is summarized in Table 4. As compared with hysteresis, predictive PWM, and conventional MPCC control methods, the cost function-based MPCC algorithm provides a lower switching frequency with an optimal source current THD value.



(**a**)

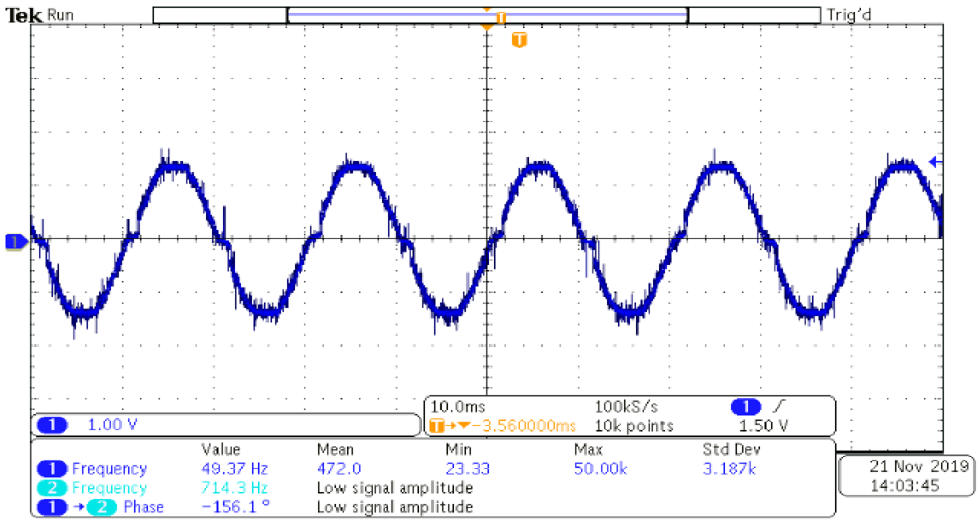


(**b**)



(**c**)

Figure 11. *Cont.*



(**d**)

Figure 11. Experimental outcomes: (**a**) source current (before compensation), (**b**) source current $\lambda = 0$, (**c**) source current $\lambda = 0.05$, (**d**) source current $\lambda = 0.1$.

Table 4. Summary of the simulation and practical test results for weighting factor-based MPCC of single-phase SAPF, including THD and switching frequency.

Source Current THD (%) (RL Load)	**Before Compensation**	**After Compensation**				
		Hysteresis Controller	**Predictive PWM Controller**	**(Weighting Factor-based MPCC)**		
				0	**0.05**	**0.1**
Simulation Results	28.47	3.82	4.5	3.53	4.20	4.66
Hardware Results	24.9	3.76	4.21	3.7	4.6	4.8
Switching Frequency (Fsw) in kHz	**Before Compensation**	**Hysteresis Controller**	**Predictive PWM Controller**	**After Compensation (Weighting Factor-based MPCC)**		
				0	**0.05**	**0.1**
Simulation Results	0	15.27	15	15.071	14.208	12.866
Hardware Results	0	15.13	15	15.200	14.600	13.400

As presented above the following conclusions have been ended from the experimental study.

- The NLL's current harmonics and reactive power were efficiently adjusted.
- The supply current took on a sine wave and aligned with the supply voltage.
- Under all working conditions, the DC-link capacitor voltage returned to its reference value. The suggested control approach also reduced supply current THD to far below 5% within the IEEE 519-2014 standard.
- When compared to traditional current control approaches, the MPCC algorithm based on a cost function provided a great trade-off between VSI switching frequency and harmonic performance. The results show that this technology is suited for both commercial and industrial applications.
- The proposed SAPF system was realized with the Cyclone-IV EP4CE30F484 FPGA controller. From the hardware outcomes, it can be seen that, during the load changing condition, the source current is sinusoidal in nature and in phase with the source voltage.

5. Conclusions

In this manuscript, a cost function-based MPCC was presented for reducing the switching frequency. The outcomes illustrate that the proposed system archives an excellent trade-off among the VSI switching frequency and harmonics performance. A comparison study indicates that the proposed technique achieves a reduced switching frequency of 13.4 kHz, and also decreases the THD of the supply current well below 5% within the IEEE 519-2014 limit. In addition, the simulation and experiment results show the effectiveness of the proposed method. The suggested approach is easy to calculate, and the simulation and experimental results show that it performs well in terms of dynamic features, operational efficiency, and output power quality. This approach is applicable to all types of converters for which power quality is a primary concern.

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