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Adaptive Charge-Compensation-Based Variable On-Time Control to Improve Input Current Distortion for CRM Boost PFC Converter

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Abstract: For boost power factor correction (PFC) converters operating in critical conduction mode (CRM), charge compensation strategies are utilized to improve input current distortion. However, since massive calculations are required under complex working conditions, it is difficult to achieve accurate charge compensation with limited real-time computing resources. To solve this issue, this paper proposes an adaptive charge-compensation-based variable on-time (ACVOT) control strategy. The ACVOT controller calculates the required switching on-time by adding a fundamental value and an extended on-time. The fundamental value is adjusted by the loop compensator in each half-line cycle to provide a basic bias. The extended on-time is calculated based on partial charge compensation equation in each switching cycle to reduce the distortion. Compared with conventional digital variable on-time (VOT) control, the proposed strategy improves the input current total harmonics distortion (THD) and reduces the LUT/register resources by 54%/43% in FPGA realization. To verify the effectiveness of the proposed strategy, a 200 W prototype is built using the GaN HEMT transistor, where the THD is reduced to 1.4% at full load.

Keywords: boost power factor correction (PFC); critical conduction mode (CRM); real time; total harmonics distortion (THD); variable on-time (VOT)

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1. Introduction

Power factor correction (PFC) is increasingly required in AC-DC converters to improve the total harmonics distortion (THD) and power factor (PF) [1–4]. As a classical choice, a boost PFC converter operating in the critical conduction mode (CRM) is preferred in medium- and low-power applications, owing to its simple control and high efficiency [5,6]. However, since CRM operation requires a reverse inductor current stage to achieve soft switching, the average inductor current is naturally less than the expected value under conventional constant on-time (COT) control, which causes serious input current distortion [7,8]. To reduce the input current distortion, analog and digital variable on-time (VOT) controls are proposed. These controls dynamically adjust the on-time to compensate the average inductor current, so that to reduce the THD as low as possible.

Analog-based VOT controls are developed in [9–14]. Since the distortion is closely related to the input, a feedforward from the input voltage to the on-time is implementable to reduce THD, while a constant feeding proportion is commonly used [9,10]. However, constant proportion cannot adapt to the input change; thus, dynamic proportion is an option to improve the THD [11]. Correspondingly, to improve the THD at different loads, the output power is sensed to adjust the on-time [12,13]. The above strategies do not

incorporate accurate online calculation that leads to limited performance. To further improve the THD, an accurate charge compensation model is built through Taylor series expansion, which is complex for analog implementation [14].

Comparatively, digital-based VOT controls provide more flexible solutions to reduce the THD [15–22]. These controls incorporate accurate relations among the average inductor current, the input voltage, and the load. They can be realized through either real-time calculations or look-up table (LUT) methods. For LUT realizations, the designers have to compromise among the simplicity, accuracy, and memory consumptions. In [16], LUT implementation only fit for PFC in the triangular current mode (TCM) is given. In [17], a general method that considers the input filter capacitor is proposed, which has complex tables to improve accuracy. The relationship between tables under different inputs and loads is further summarized in [18] and a method using a single table is proposed. However, the LUT building process is complex. Real-time strategies avoid the table-building process but consume unacceptable hardware resources with full-order calculation [19,20]. To save computing resources, a real-time current detector and an average current calculator using triangular approximation are applied [21]. The current distortion beyond input zero-crossing is neglected [22]. These existing strategies are relatively difficult to maintain accuracy while reducing complexity for implementation.

In this paper, an adaptive charge-compensation-based variable on-time (ACVOT) control is proposed. Different from directly calculating the required on-time, the ACVOT controller adds an extended time (T_{ext}) to a fundamental time ($T_{\text{on\_bias}}$) to calculate the switching on-time. The extended on-time is derived based on a full-order model of the inductor charge, which over-compensates the negative charge during valley switching (VS) or zero-voltage switching (ZVS), and is updated every switching cycle. The fundamental time is acquired through the output voltage feedback, which is updated every half-line cycle using PI compensation. Over-compensated extended time takes a simple form and contains a key component of accurate on-time. Moreover, the adjusted fundamental time supplements the required switching time. With a combination of online compensation and feedback adjustment, the proposed strategy maintains fairly low THD on effect and reduces the implementation complexity. Relevant simulations and experiments are conducted to verify the effectiveness of ACVOT control.

The rest of the paper is organized as follows. Section 2 discusses the operation analysis for CRM boost PFC converter, and explains the reasons for input current distortion. Then, the ACVOT control is proposed based on charge compensation equations. In Section 3, simulations are applied to verify the effectiveness and the adaptivity of the proposed control. Details of the control are also discussed in this section. Section 4 shows the experiment results and compares the results with other controls. Finally, a brief conclusion is given in Section 5.

2. Proposal of ACVOT Control

2.1. A General Analysis of CRM Boost PFC

The basic topology of a typical boost PFC converter is displayed in Figure 1, including the elements generally required, such as the EMI filter and the rectifier bridge. The GaN high-electron-mobility transistor (HEMT) and the SiC diode are used in this paper. The output junction capacitance C_{oss} of the GaN HEMT and the parallel capacitance C_d of the SiC diode are presented.

The vs. and ZVS are vital approaches for the CRM boost converter to improve the overall operation efficiency. The key waveforms of the converter when VS/ZVS is achieved are given in Figure 2a,b. As is shown, the v_{gs} turns high at the valley or the zero point of v_{ds}, which minimizes the switching-on loss of the power switch. In such cases, different operation stages are identified depending on the time intervals in Figure 2.

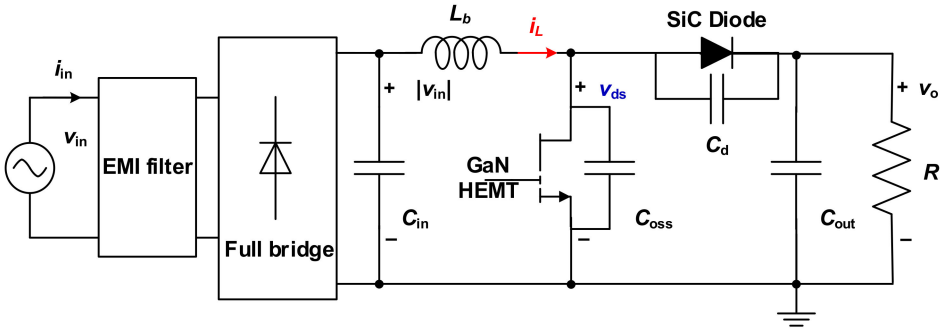

Figure 1. Boost PFC converter circuit with the GaN high-electron-mobility transistor (HEMT) and the SiC diode.

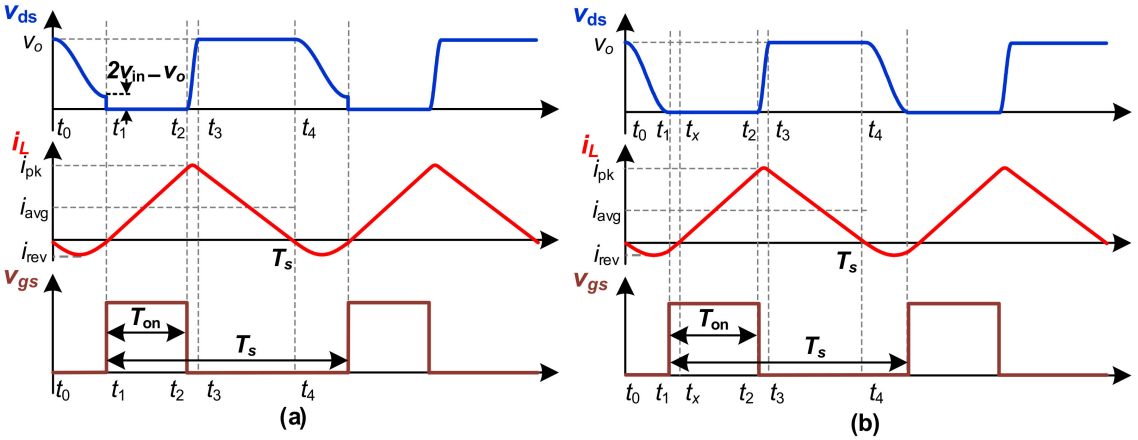

Figure 2. Key waveforms of CRM operations: (**a**) the vs. condition ($2v_{in} > v_o$); (**b**) the ZVS condition ($2v_{in} < v_o$).

For depicting topological states, the operating circuits of each stage are included in Figure 3, where the C_{in} and C are treated as constant voltage sources since their voltages change slightly during one switching cycle. Unspecified parasitic parameters are ignored to highlight the most concerning part.

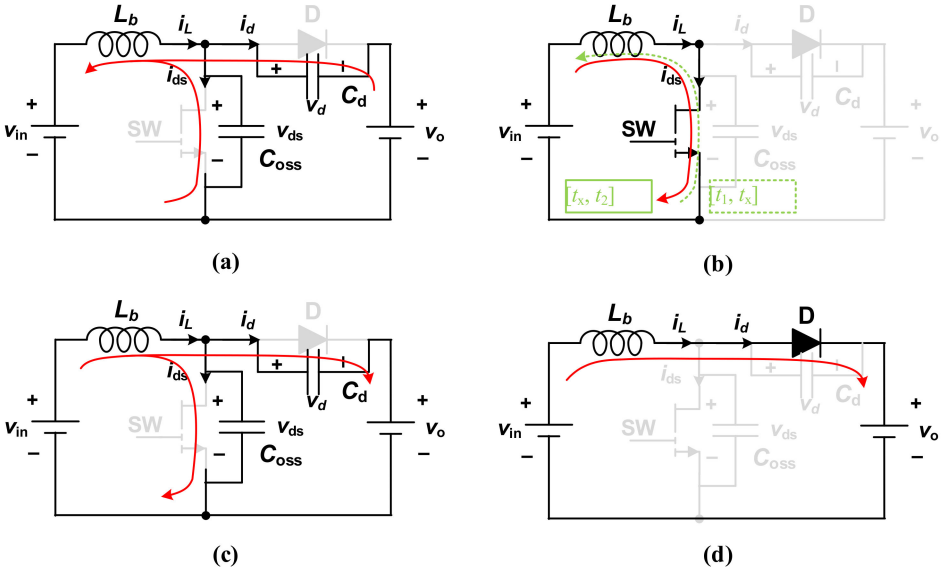

Figure 3. Operating circuits: (**a**) the reverse resonant period, i.e., $[t_0, t_1]$; (**b**) the switching-on period, i.e., $[t_1, t_2]$; (**c**) the forward resonant period, i.e., $[t_2, t_3]$; (**d**) the diode conduction period, i.e., $[t_3, t_4]$.

Firstly, the resonance process in Figure 3a,c is described by equations:

$$\begin{cases} v_{\mathrm{ds}} = v_{\mathrm{in}} - L_b \frac{di_L}{dt} \\ i_L = C_{oss} \frac{dv_{\mathrm{ds}}}{dt} + C_d \frac{dv_{\mathrm{d}}}{dt} \end{cases} \quad (1)$$

where the $v_{\mathrm{d}} = v_{\mathrm{ds}} - v_{\mathrm{o}}$. By solving Equation (1), the resonance stage satisfies:

$$\begin{cases} v_{\mathrm{ds}} = A_1 \cos(\omega_r t) + A_2 \sin(\omega_r t) + v_{\mathrm{in}} \\ i_L = -A_1 C_{\mathrm{eq}} \omega_r \sin(\omega_r t) + A_2 C_{\mathrm{eq}} \omega_r \cos(\omega_r t) \end{cases} \quad (2)$$

where the $C_{\mathrm{eq}} = C_{oss} + C_d$, ω_{r} = sqrt $(1/L_b C_{\mathrm{eq}})$, Z_r = sqrt (L_b/C_{eq}), and A_1 and A_2 are the undetermined coefficients. Since the initial state of v_{ds} is v_{o}, and the steady state of v_{ds} is v_{in}, the criteria $2v_{\mathrm{in}} - v_{\mathrm{o}}$ for whether the vs. or the ZVS condition is deduced. Next, different operation stages in both VS/ZVS conditions are described. The expressions for v_{ds} and i_L are listed in Table 1 depending on the time intervals.

Table 1. Expressions for v_{ds} and i_L depending on the time intervals.

Time Intervals	$v_{\mathrm{ds}}(t)$	$i_L(t)$
$[t_0, t_1]$	$v_{\mathrm{in}} - (v_{\mathrm{in}} - v_{\mathrm{o}}) \cos[\omega_r (t - t_0)]$	$\frac{v_{\mathrm{in}} - v_{\mathrm{o}}}{Z_r} \sin[\omega_r (t - t_0)]$
$[t_1, t_2]$	0	$\left(\text{For VS}, \frac{v_{\mathrm{in}}}{L_b}(t - t_1)\right)$ $\left(\text{For ZVS}, \begin{matrix} [t_1, t_x] \rightarrow i_L(t_1) + \frac{v_{\mathrm{in}}}{L_b}(t - t_1) \\ [t_x, t_2] \rightarrow \frac{v_{\mathrm{in}}}{L_b}(t - t_X) \end{matrix}\right)$
$[t_2, t_3]$	$v_{\mathrm{in}} - v_{\mathrm{in}} \cos[\omega_r (t - t_2)] + Z_r i_L(t_2) \sin[\omega_r (t - t_2)]$	$i_L(t_2) \cos[\omega_r (t - t_2)] + \frac{v_{\mathrm{in}}}{Z_r} \sin[\omega_r (t - t_2)]$
$[t_3, t_4]$	v_{o}	$i_L(t_3) - \frac{v_{\mathrm{o}} - v_{\mathrm{in}}}{L_b}(t - t_3)$

For the vs. condition ($2v_{\mathrm{in}} > v_{\mathrm{o}}$), there are four stages in one switching cycle.

Stage I: The reverse resonant period $[t_0, t_1]$. I_L is zero at t_0 instant and the initial value of v_{ds} is v_{o}. L_b starts resonating reversely with C_{eq}. *Stage II: The switching-on period* $[t_1, t_2]$. The gate drive signal v_{gs} stays high and i_L rises linearly from zero to its peak value i_{pk}. *Stage III: The forward resonant period* $[t_2, t_3]$. The power switch turn-off at t_2 and L_b starts resonating forwardly with C_{eq} in a short period of time. *Stage IV: The diode conduction period* $[t_3, t_4]$. The power switch is blocked and the diode is conductive. I_L decreases linearly to zero at the t_4 instant.

For the ZVS condition ($2v_{\mathrm{in}} < v_{\mathrm{o}}$), the expression of *Stage I*, *Stage III*, and *Stage IV* is the same as the expression in the vs. condition. The difference in *Stage II* is described by the following two segmented states: *Stage II-1: The switch-on period 1* $[t_1, t_{\mathrm{x}}]$. The power switch becomes conductive at t_1 instant and i_L starts rising linearly from the reverse peak value. *Stage II-2: The switch-on period 2* $[t_{\mathrm{x}}, t_2]$. The power switch stays conductive and i_L rises linearly from zero to its peak value i_{pk}.

Since the equations of i_L and v_{ds} are already given clearly in operation stages, the time intervals $t_{\mathrm{n}} - t_{\mathrm{n}-1}$ and the inductor charge Q_{n} during each stage are calculated by substituting numerical boundary conditions and by using step-by-step integration. The results in Tables 2 and 3 show a full-order model of the inductor charge.

Based on the above operation analysis, the reasons for input current distortion are now discussed.

As is known, the input current all passes through the inductor, and the average of the inductor current during the switching cycle is assumed to be $i_{\mathrm{L\_av}} = T_{\mathrm{on}}(v_{\mathrm{in}}/L_b)/2$ under COT control. Thus, with a constant T_{on}, the input current is in proportion to the sinusoidal

input voltage in assumption. However, with the full-order inductor charge model, the i_{L_av} is calculated as

$$i_{L\_av} = \frac{\Sigma Q_n}{\Sigma(t_n - t_{n-1})} \tag{3}$$

where the time intervals $t_n - t_{n-1}$ and the inductor charge Q_n are given in Tables 2 and 3. Because of the existence of the forward resonance stage and the reverse resonance stage, numerous nonlinear factors are introduced to the relation of i_{L_av} and T_{on}, which distorts the input current. The reverse resonance stage is focused to reduce the distortion, since the forward resonance stage is short and has negligible influence. On the one hand, the reverse resonance decreases the charge transferred during a switching cycle. On the other hand, it increases the length of the cycle. These two points result in the i_{L_av} being lower than expected.

Table 2. Lists of the time intervals during the switching cycle.

Stage	The ZVS Condition	The VS Condition
I	$t_1 - t_0 = \frac{1}{\omega_r}\left(\pi - \arccos\frac{v_{in}}{v_o - v_{in}}\right)$	$t_1 - t_0 = \frac{\pi}{\omega_r}$
II-1	$t_x - t_1 = \frac{1}{\omega_r v_{in}}\sqrt{v_o^2 - 2v_o v_{in}}$	$t_2 - t_1 = T_{on}$
II-2	$t_2 - t_x = T_{on} - \frac{1}{\omega_r v_{in}}\sqrt{v_o^2 - 2v_o v_{in}}$	
III	$t_3 - t_2 = \frac{1}{\omega_r}\left(\arcsin\frac{v_{in}}{\sqrt{v_{in}^2 + (Z_r i_L(t_2))^2}} + \arcsin\frac{v_o - v_{in}}{\sqrt{v_{in}^2 + (Z_r i_L(t_2))^2}}\right)$	
IV	$t_4 - t_3 = \frac{L_b}{v_o - v_{in}} i_L(t_3)$	

Table 3. Lists of the inductor charges during the cycle.

Stage	The ZVS Condition	The VS Condition
I	$Q_1 = -C_{eq} v_o$	$Q_1 = -2C_{eq}(v_o - v_{in})$
II-1	$Q_{21} = -\frac{C_{eq} v_o}{2v_{in}}(v_o - 2v_{in})$	$Q_2 = \frac{v_{in}}{2L_b} T_{on}^2$
II-2	$Q_{22} = \frac{v_{in}}{2L_b}\left(T_{on} - \frac{1}{\omega_r v_{in}}\sqrt{v_o^2 - 2v_o v_{in}}\right)^2$	
III	$Q_3 = C_{eq} v_o$	$Q_3 = C_{eq} v_o$
IV	$Q_4 = \frac{v_{in}^2}{2L(v_o - v_{in})}\left(\left(T_{on} - \frac{\sqrt{v_o(v_o - v_{in})}}{\omega_r v_{in}}\right)^2 - \frac{v_o(v_o - 2v_{in})}{\omega_r^2 v_{in}^2}\right)$	

Reviewing the operation of boost PFC, it is worth noting that energy is stored in the inductor L_b during the switching-on period and is transferred to the output during the diode conduction period, as shown in Figure 3b,d. However, when the energy stored in L_b is not enough to charge the C_{oss} and discharge the C_d to let $v_{ds} > v_o + v_{diode}$ (v_{cond_diode} is the conduction voltage of D), diode D cannot be turned on. The circuit enters a non-power transfer period, at which time resonance occurs, as shown in Figure 4. During this period, the energy is confined and dissipated in the tank circuit, which is composed of C_{in}, L_b, and C_{eq}.

Under COT control, the length of the switching-on period is regarded as constant. Thus, when the line voltage Vac is low near the zero-crossings, the switching-on period cannot supply sufficient energy to L_b. Non-power transfer occurs as described above. During this interval, the voltage drop rate of C_{in} is slow, which is determined by the relatively small loss in the resonant tank and the relatively large value of C_{in}. On the contrary, the line voltage decreases at a faster rate. Thus, the bridge rectifier cannot be turned on until the line voltage rises high again in the next half-line cycle. The line current i_{ac} forms a flat region during this interval, as illustrated in Figure 4b [11].

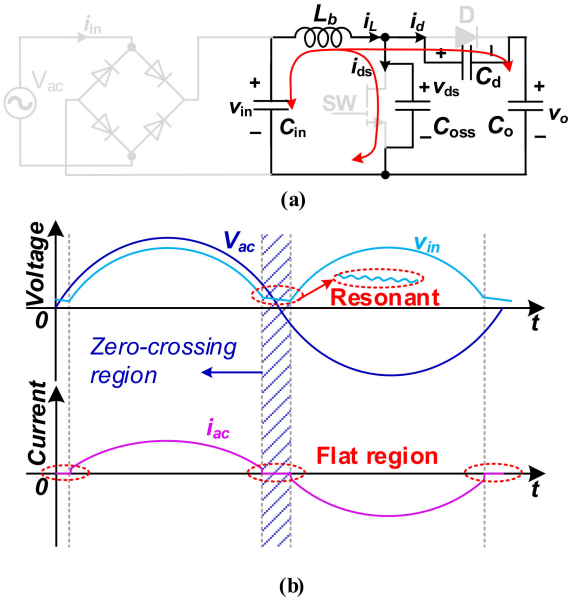

Figure 4. Typical operating circuit and waveforms in the crossover distortion phenomenon: (**a**) operating circuit during the non-power transfer period; (**b**) line voltage and current waveforms of the crossover distortion phenomenon.

This phenomenon is called "crossover distortion". If the energy charged during the switching-on period is described as a function of the input current, the criteria for the zero-crossing region are expressed as:

$$\frac{1}{2}Li_{ac}^2 \le \frac{1}{2}C_{eq}(v_o + v_{cond\_diode})^2 \tag{4}$$

Since the $i_{ac} = I_{ac\_rms} \cdot \sin\theta \approx P_o / V_{ac\_rms} \cdot \sin\theta$, the θ satisfying Equation (4) is expected to increase as P_o / V_{ac_rms} decreases, which extends the zero-crossing region. Thus, serious crossover distortion occurs under COT control in case of the high input voltage with light load. Comparatively, if the VOT method is adopted to extend the switching-on period in the zero-crossing region, the distortion is expected to be significantly reduced [14].

Moreover, the input filter also affects the input current distortion. Because of the feature of the PFC, the input impedance is equivalent to a resistance when discussing the effect of the input filter. Since a capacitor C_{in} is commonly used, a phase leading angle ϕ_1 can exist between the input current and the input voltage. It is easy to estimate ϕ_1 as

$$\begin{cases} i_{in} = \left(j2\pi f_{line} C_{in} + \frac{1}{R_{in}}\right) v_{in} \\ \tan\phi_1 = 2\pi f_{line} C_{in} \frac{V_{in\_rms}^2}{P_o} \end{cases} \tag{5}$$

where the $R_{in} = P_o / V_{in\_rms}^2$ is the input equivalent resistance, f_{line} is the line frequency, V_{in_rms} is the RMS value of the input voltage, and P_o is the output power of the PFC converter. The current distortion caused by C_{in} can be reduced by introducing a phase lag into the control [23]. Since the C_{in} is designed small and has low effects on the input current distortion compared with the reverse resonance, C_{in} is ignored when considering the main method of distortion compensation for simplicity. Except for the reasons above, the errors in control, the nonlinearity, the parasitic parameters of the devices, and the voltage ripple on C_{in} and C_{out} inevitably affect the input current. However, they are negligible for the analysis.

2.2. The Proposal of ACVOT Control

In order to eliminate input current distortion, the average inductor current of switching cycle should be controlled as the expected value. Assuming that the converter efficiency is η and the output power is P_o, the expected input current is expressed as

$$i_{in\_expected} = \frac{\sqrt{2}P_o}{\eta V_{in\_rms}} \sin(\omega t) \tag{6}$$

Therefore, the objective $T_{on\_obj}(t)$ curve that guarantees the i_{L_av} being sinusoidal can be calculated by letting the $i_{in\_expected} = i_{L\_av}$, where i_{L_av} is obtained with the full-order inductor charge model for accuracy. The $T_{on\_obj}(t)$ is derived as

$$T_{on\_obj}(t) = \sqrt{\left(\frac{L}{R}\right)^2 + LC\frac{v_o(v_o - 2V_{in\_rms}\sin(\omega t))}{(V_{in\_rms}\sin(\omega t))^2} + \sqrt{LC}\frac{L}{R}\frac{2(v_o - V_{in\_rms}\sin(\omega t))}{V_{out}}\left(\pi - a\cos\frac{V_{in\_rms}\sin(\omega t)}{v_o - V_{in\_rms}\sin(\omega t)} + \sqrt{\left(\frac{v_o}{V_{in\_rms}\sin(\omega t)}\right)^2 - 2\frac{v_o}{V_{in\_rms}\sin(\omega t)}}\right)} + \frac{L}{R} + \sqrt{LC}\sqrt{\frac{v_o(v_o - 2V_{in\_rms}\sin(\omega t))}{(V_{in\_rms}\sin(\omega t))^2}} \tag{7}$$

It is obvious that the $T_{on\_obj}(t)$ is too complex to directly calculate. Figure 5a shows the calculated $T_{on\_obj}(t)$ curve with certain circuit parameters: P_o = 200 W, V_{in_rms} = 220 V, v_o = 400 V, L_b = 200μH, C_{eq} = 120 pF, η = 100%, and f_{line} = 50 Hz. It is noticed that the $T_{on\_obj}(t)$ curve can be treated as its shape part is superimposed on a fundamental part.

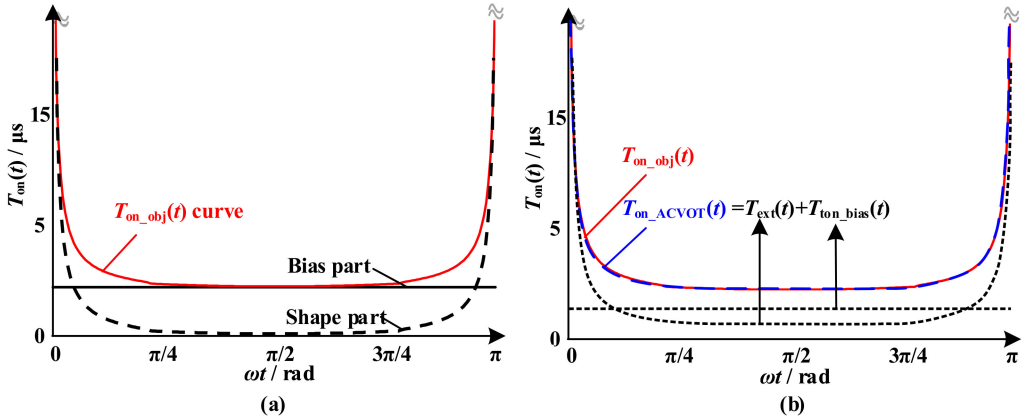

Figure 5. $T_{on}(t)$ curve with certain circuit parameters: (**a**) objective on-time curve, (**b**) calculated on-time curve under ACVOT control.

To simplify the calculation of $T_{on\_obj}(t)$, these two parts are considered to be acquired separately. Since the bias part is linear, utilizing feedback adjustment is suitable to avoid calculation. In addition, if the bias is adjusted by feedback, the shape curve is allowed to shift up and down as long as its shape is correct. This means that it is possible to simply obtain the shape curve using an over-compensation algorithm.

The generation of objective on-time under ACVOT control is divided into two parts accordingly. As shown in Figures 5b and 6, the ACVOT controller obtains an extended on-time T_{ext} with correct curve shape using a real-time calculator while obtaining a bias on-time curve with correct amplitude using the PI compensator in each half-line cycle. The combination of T_{ext} and T_{on_bias} easily generate the desired on-time curve. The detailed control strategy is proposed as follows.

Since the main reason for the input current distortion is the reverse resonance in previous discussion, it is reasonable to build the T_{ext} curve based on the influence of the reverse resonance part. From the view of charge, the negative charge caused by the reverse inductor current stage needs to be compensated. Figure 7 labels the related charge during a switching cycle. The extended on-time T_{ext} is derived by building partial charge compensation in both VS/ZVS conditions.

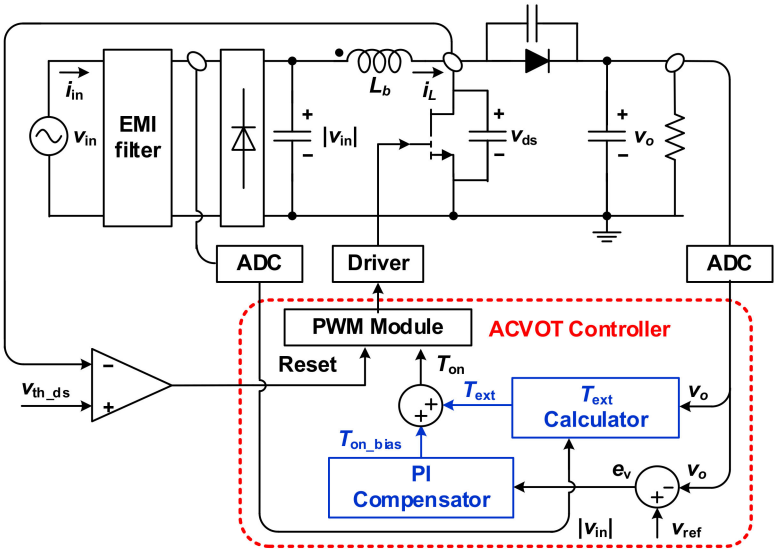

Figure 6. Implementation of the proposed control.

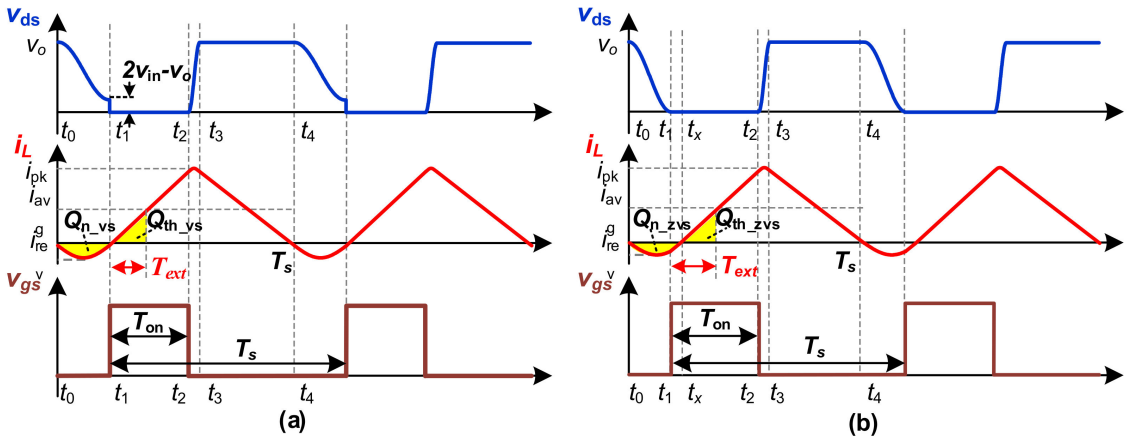

Figure 7. Diagram of the key inductor charge and the extended time of the ACVOT control: (**a**) the vs. condition ($2v_{in} > v_o$); the (**b**) ZVS condition ($2v_{in} < v_o$).

When the vs. condition is achieved, two parts of the inductor charge are shown in Figure 7a, where the charge Q_{n_vs} represents the level of the current distortion. To compensate Q_{n_vs}, an extra conduction time T_{ext} is extended and Q_{th_vs} represents the level of compensated charge by T_{ext}.

Q_{n_vs} is Q_1 in the vs. condition, as shown in Table 3. Therefore, Q_{n_vs} is obtained by

$$Q_{n\_vs} = 2C_{eq}(v_o - v_{in}), \tag{8}$$

where $t_1 = T_r/2 = \pi$ sqrt(L_bC_{eq}) is the valley switching point of the resonance.

The inductor current keeps rising with the almost constant slope $K = v_{in}/L_b$ during the time interval $[t_1, t_2]$. Thus, Q_{th_vs} is given by

$$Q_{th\_vs} = \frac{v_{in}T_{ext}^2}{2L_b} \tag{9}$$

Let $Q_{th\_vs} = Q_{n\_vs}$. The extended conduction time for the vs. condition is derived as

$$T_{ext\_vs} = \frac{2}{\omega_r}\sqrt{\frac{(v_o - v_{in})}{v_{in}}} \tag{10}$$

When the ZVS condition is achieved, two parts of the inductor charge are shown in Figure 7b, where the charge Q_{n_zvs} during [t_0, t_x] represents the level of the current distortion, and Q_{th_zvs} represents the level of the compensated charge introduced by T_{ext}.

Like with the vs. condition, Q_{n_zvs} is the sum of Q_1 and Q_{21} of the ZVS column in Table 3. Q_1 is obtained first in Table 2, which is expressed as

$$Q_1 = v_o C_{eq}. \tag{11}$$

To derive Q_{21}, the peak value of the reverse inductor current is given as $i_L(t_1) = -\sqrt{v_o^2 - 2v_o v_{in}}/Z_r$ according to the expression of $i_L(t)$ in Table 1, where t_1 is derived by setting $v_{ds}(t_1) = 0$ in expression of $v_{ds}(t)$ in *Stage I*, and the time interval $t_x - t_1$ is given in Table 2 by setting $i_L(t_x) = 0$ in expression of $i_L(t)$ in *Stage II-1*. With the initial condition and the integration time, Q_{21} is calculated as

$$Q_{21} = \frac{C_{eq}\left(v_o^2 - 2v_o v_{in}\right)}{2v_{in}} \tag{12}$$

With Q_1 and Q_{21}, Q_{n_zvs} is obtained. Thus, Q_{n_zvs} and Q_{th_zvs} are briefly expressed as

$$\begin{cases} Q_{n\_zvs} = \frac{C_{eq} v_o^2}{2v_{in}} \\ Q_{th\_zvs} = \frac{v_{in}(T_{ext} - (t_x - t_1))^2}{2L_b} \end{cases} \tag{13}$$

Let $Q_{th\_zvs} = Q_{n\_zvs}$. The extended conduction time for the ZVS condition is derived as

$$T_{ext\_ZVS} = \frac{v_o}{\omega_r v_{in}}\sqrt{1 - \frac{2v_{in}}{v_o}} + \frac{v_o}{\omega_r v_{in}} \tag{14}$$

The charge compensation relation $Q_{th\_vs} = Q_{n\_vs}/Q_{th\_zvs} = Q_{n\_zvs}$ generates the required $T_{ext}(t)$ of each cycle in both VS/ZVS conditions. Therefore, the final form of the extended on-time is established as

$$T_{ext} = \begin{cases} \frac{2}{\omega_r}\sqrt{\frac{(v_o - v_{in})}{v_{in}}}, v_{in} > 0.5v_o \ \text{ VS} \\ \frac{v_o}{\omega_r v_{in}}\sqrt{1 - \frac{2v_{in}}{v_o}} + \frac{v_o}{\omega_r v_{in}}, v_{in} < 0.5v_o \ \text{ ZVS} \end{cases} \tag{15}$$

Then, the initial bias on-time is estimated as

$$T_{on\_bias}(t) = \frac{2L_b}{v_{in}(t)} i_{in\_expected}(t) \tag{16}$$

Finally, the complete on-time form of ACVOT control is expressed as

$$T_{on\_ACVOT}(t) = T_{on\_bias}(t) + T_{ext}(t) \tag{17}$$

In order to obtain a good compensation effect, the $T_{on\_ACVOT}(t)$ curve should accord with the $T_{on\_obj}(t)$ curve. After adjusting the $T_{on\_bias}(t)$, the $T_{on\_ACVOT}(t)$ curve under the ACVOT control is plotted in Figure 5b with the same circuit parameters. It is obvious that the on-time curve under the proposed control and the $T_{on\_obj}(t)$ curve have good consistency. Further research about the ACVOT control is given in the following section.

3. Simulations and Details of the ACVOT Control

3.1. Mathematical Simulations for the ACVOT Control

In order to research the compensation effectiveness of the proposed control intuitively, close-loop mathematical simulations are applied based on the following steps:

1. Under arbitrary P_o and V_{in_rms}, the reference inductor current is given by Equation (6), the bias conduction time is given by Equation (16), and the extended on-time is

determined by Equation (15). Then, the on-time $T_{on\_ACVOT}(t)$ curve is calculated by Equation (17).

2. With the $T_{on\_ACVOT}(t)$, the average inductor current curve is estimated by Equation (3). Further, the input power P_{in_cal} is calculated by integration in each half-line cycle. Since the feedback loop keeps adjusting the amplitude of the expected input current I_{in_exp} to match the output power, an adjusting process is applied as follows: when $P_{in\_cal} - P_o > 0$, the loop shifts I_{in_exp} downward. When $P_{in\_cal} - P_o < 0$, the loop shifts I_{in_exp} upward. Thus, the P_{in_cal} can be regulated to match the P_o. After several iterations, the stable state of the closed-loop ACVOT controller is obtained.
3. The above two steps are repeated to obtain data in full input and load range. For comparison, the simulations about the COT control are also applied by the same steps.

The input current waveforms under the COT control and the ACVOT control are illustrated in Figure 8 with the simulated data, which has 200 W full load and the same circuit parameters as the previous section. It is observed that the input current waveform is significantly rectified using the ACVOT control.

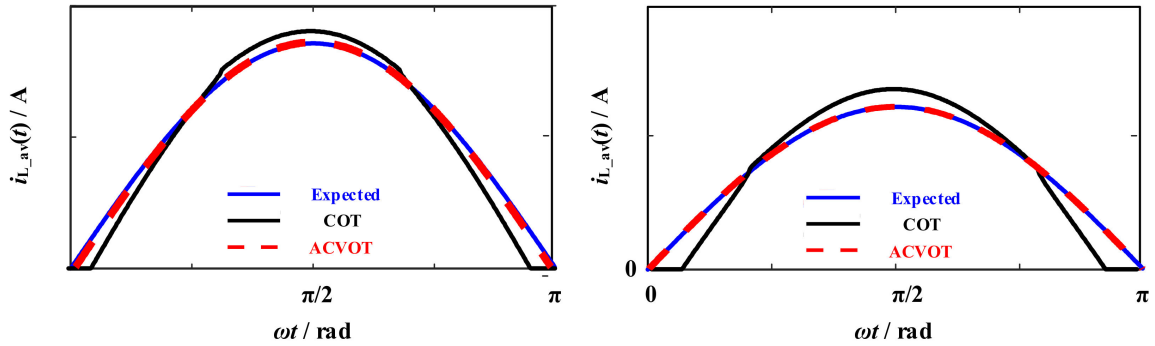

Figure 8. The simulated input current waveforms with full load under the COT control and the ACVOT control.

Although the input current waveforms in the above cases show good effectiveness of the ACVOT control, it is worth considering that the working conditions of PFC are complex and the control parameters have deviations in real implementations. Further research is conducted to verify the adaptivity of ACVOT control.

To show the feasibility of the ACVOT control in a wide input and load range, quantitative analysis of current distortion is established using PF and THD calculations. For a list of stable states at different P_o and V_{in_rms} conditions, the PF and THD values are estimated by

$$\begin{cases} PF = \dfrac{P_{in}}{V_{in\_rms} I_{rms}} = \dfrac{1}{\pi} \dfrac{\int_0^{\pi} v_{in}(t) i_{in}(t) d\omega t}{V_{in\_rms} \sqrt{\frac{1}{\pi} \int_0^{\pi} i_{in}^2(t) d\omega t}} \\ \mathrm{THD} = \sqrt{(\cos\theta / PF)^2 - 1} \end{cases} \tag{18}$$

where θ is the angle between the v_{in} and the fundamental component of i_{in}. θ is equal to 1 in calculation because the input filter is ignored.

The close-loop THD mapping under ACVOT control is shown in Figure 9b. For contrast, the THD mapping under COT control is plotted in Figure 9a. It is obvious that the ACVOT control is expected to effectively reduce the current distortion in a wide input and load range.

It is important to verify the sensitivity of values of L_b and C_{eq} under the ACVOT control, since they have large tolerance and the C_{eq} varies according to the variation of the drain–source voltage. Thus, the simulation is carried out with ±20% tolerance of the values of L_b and C_{eq}. The simulated PF and THD surfaces against different L_b and C_{eq} values with full load are shown in Figures 10 and 11. Limited by the article length, surfaces under different load conditions are not plotted but they have the same trend as Figures 10 and 11. It is observed that the ACVOT control slightly changes the THD and PF values under the

variation range of L_b and C_{eq}. Moreover, better THD and PF occurs when the negative L_b and positive C_{eq} variations are achieved. Thus, a small L_b value and a large C_{eq} value are recommended to set.

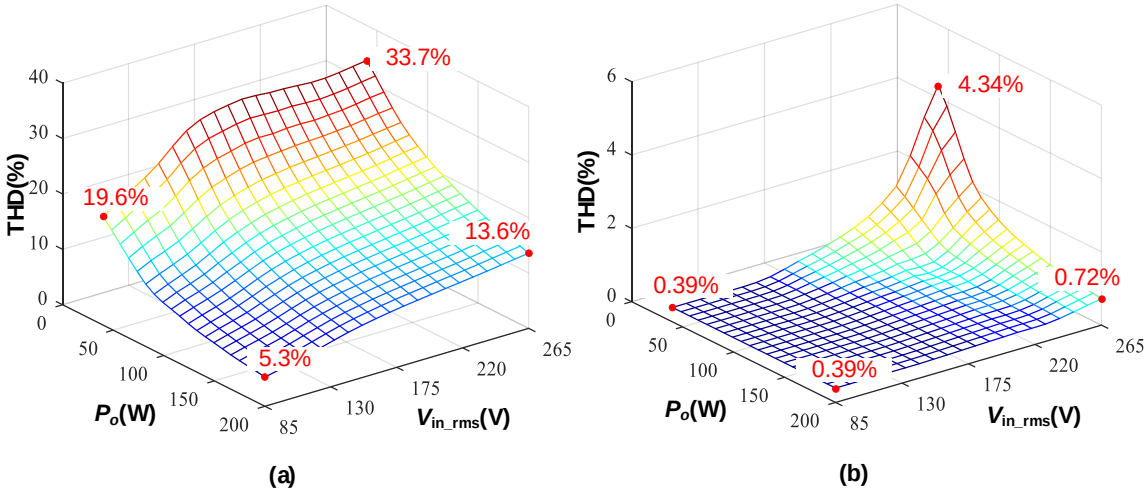

Figure 9. The close-loop THD mappings: (**a**) the COT control; (**b**) the ACVOT control.

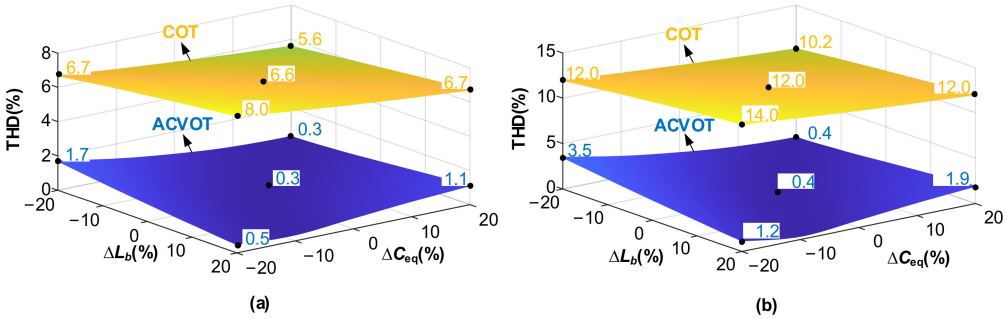

Figure 10. The THD surfaces with L_b and C_{eq} deviations: (**a**) 110 Vac; (**b**) 220 Vac.

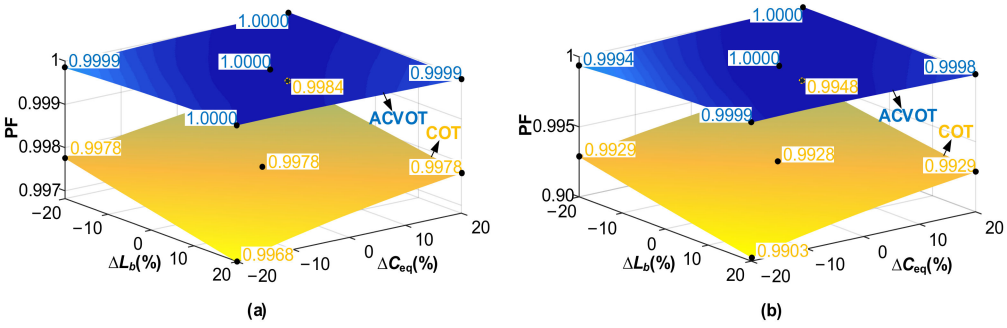

Figure 11. The PF surfaces with L_b and C_{eq} deviations: (**a**) 110 Vac; (**b**) 220 Vac.

3.2. Implementation Problems of ACVOT Control

Figure 6 illustrates the implementation of the proposed control, which is further discussed here.

In practical terms, the proposed control can be implemented based on a prior COT system, which mainly includes an input/output sampler, a voltage loop compensator, a PWM generator, and a valley/zero-voltage switching optimizer. In general, only an additional T_{ext} calculator is required for the proposed solution. This calculator uses the input, the output, the inductor value L_b, and the parasitic capacitance value C_{eq} to calculate Equation (15). Furthermore, its output is added to the output of voltage compensator, as shown in Figure 6, which is similar to a current loop compensator. The calculator

consumed resources are discussed in Section 3.3. Without other required operations, the proposed solution is easy to implement. Moreover, the calculation of T_{ext} is feasible for common digital processors and chips. The proposed solution is flexible to be realized by DSP or ARM.

Furthermore, considering the practical problems of the ACVOT control, some essential details require explanation.

Firstly, input voltage sampling before the rectifier bridge is recommended, since it avoids the residual voltage of C_{in} near the input zero-crossing point. Otherwise, the additional phase lock model is required to obtain the sinusoidal input voltage.

Secondly, it is important to realize the detection of the VS/ZVS point. As illustrated in Figure 6, voltage-based detection is adopted in this paper. If the $v_{ds\_th} = \max(2v_{in} - v_o, 0)$ is set, the RESET signal flips at the valley or zero-voltage point of v_{ds} according to the operation condition. In addition, a small offset is added to v_{ds_th} to ensure the comparator be trigged ahead of time, which also compensates for the detection delay.

Thirdly, the consideration of C_{eq} is simple under ACVOT control. Although the variations of C_{eq} are difficult to solve under different drain–source voltage curves and the piecewise equivalent method in [24] is more precise, using a constant C_{eq} is enough under ACVOT control in most implementations because C_{eq} is not sensitive under ACVOT control.

In addition, although the analytical solution of $T_{ext}(t)$ is continuous at the boundary of VS/ZVS conditions, it is better to make minor boundary adjustments to ensure a smooth $T_{ext}(t)$ curve when boundary error exists in implementation.

3.3. Features of ACVOT Control

The ACVOT control has the advantage of achieving both high performance and easy implementation. Related features are summarized as the following aspects:

1. Only a simple and fixed calculation is required to realize the compensation within the universal ac input and entire load range. There is no need to detect the maximum value of input voltage or calculate the phase of input voltage, and any pre-calculation procedure is avoided for designers.
2. The longest chain length of total calculation is six and they are basic operations except for one square root operation. To evaluate the resource consumption, an FPGA controller (EP4CE22F17C8N with ALTFP calculation IP cores) is used, the time and space consumption is reflected by the required clock-cycles, and the LUTs/registers resource is used. Table 4 compares the computing consumption between the ACVOT control and the control in [22], since [22] has the lowest operations consumption among the referenced digital methods that are not LUT-based (explained in Appendix A). As shown in Table 4, the ACVOT control consumes 54%/43% less LUTs/registers resources than the previous control.
3. Moreover, the input current distortion can be significantly reduced. According to Fourier analysis, the total harmonic component is less than 1% of the fundamental waveform at the condition in Figure 8. The fault tolerance of L_b and C_{eq} is sufficient, which guarantees the robustness of the ACVOT control. The experiments in the next section further verify the performance of the ACVOT control. In general, it is a real-time method with minimal cost but remarkable performance among the VOT controls.

Table 4. Computing consumption of the proposed method and the method in [22].

	Proposed		[22]	
	VS	**ZVS**	**VS**	**ZVS**
Counts of SQRT	1	1	1	2
Counts of DIV	1	2	2	2
Counts of MUL	1	3	5	7
Counts of ADD	1	2	4	6
Clock-cycles	62		70	
LUTs/Registers	1126/5512		2443/9738	

4. Experimental Results and Discussions

A 200 W boost PFC prototype is used to verify the effectiveness of the ACVOT control, which has main specifications in Table 5. Figure 12 gives a photograph of the experimental boost PFC prototype. The control implementation diagram is the same as Figure 6. The core material of the inductor L_b is PQ20/16-3F36 from FERROXCUBE. The C_{eq} is derived by the C_{oss} and C_d capacitance given in datasheets, based on a time-related equivalent model.

Table 5. The main specifications of the prototype.

Items	**Values**	**Items**	**Values**
Input voltage	90–245 Vac	L_b	287 µH
Output voltage	400 Vdc	C_{oss}	142 pF
Rated power	200 W	C_d	38 pF
Power switch	GS66508T	C_{eq} (C_{oss} + C_d)	180 pF
Power diode	STPSC8H065	C_{in}	220 nF
Rectifier bridge	GBU6J	C_{out}	180 µF

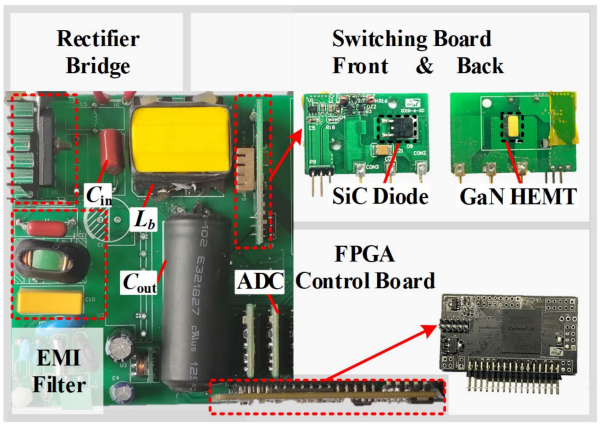

Figure 12. The experimental boost PFC prototype.

The board is modularity-based. The control module uses an FPGA chip Cyclone IV EP4CE22F17C8N from INTEL. The ADC modules use LTC2314-14 chips from TI and two ADC modules are used in the prototype. A 220nF CBB capacitor is adopted for filtering near the input. An 180 µF electrolytic capacitor is adopted near the output. The high-speed comparator TLV3501 is used to generate the RESET signal.

The experimental waveforms of v_{in}, i_{in}, and i_L at 110/220 Vac with 20%/100% load are shown in Figures 13 and 14 (measured with oscilloscope MDO3054 and current probe CPA300A). It is observed that there is serious input current distortion near the zero-crossing

point of the input voltage under the COT control, while the distortion is obviously reduced under the ACVOT control.

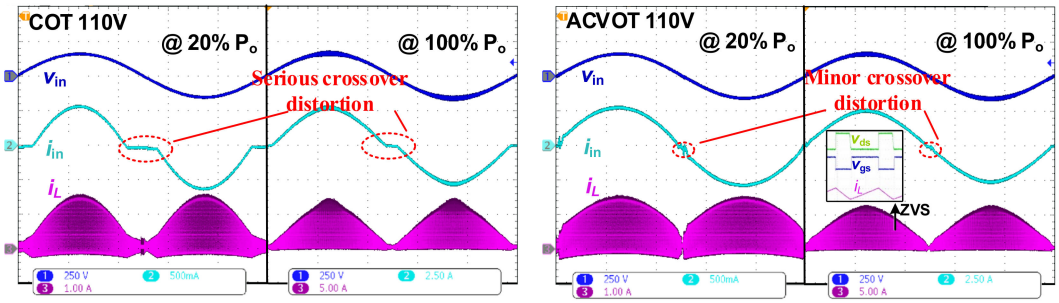

Figure 13. Waveforms at 110 Vac with 20%/100% load: (**a**) under the COT control; (**b**) under the ACVOT control.

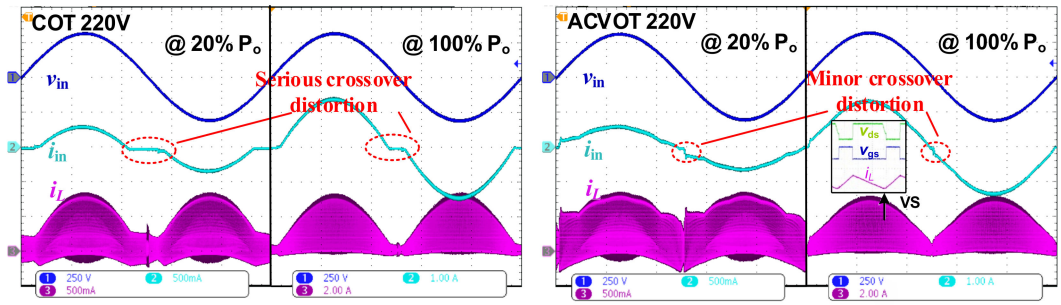

Figure 14. Waveforms at 220 Vac with 20%/100% load: (**a**) under the COT control; (**b**) under the ACVOT control.

It is noteworthy that the maximum value of $T_{on\_ACVOT}(t)$ is limited to 25 µs near the zero-crossing point for safety in experiments. Thus, the experiment results are slightly limited at the light load, at which time C_{in} also has a bigger effect. However, the light load condition is not necessary for PFC function, and the experimental results are acceptable and convincing for proving the improvement in the input current distortion.

Figure 15 gives the measured efficiency of the boost PFC prototype, and Figure 16a,b give the PF and THD charts at 110 Vac/220 Vac input with full load under the ACVOT control and the COT control (measured using the high-precision-power analyzer PA5000H). It is observed that the THD and PF are improved greatly within the entire load range at different AC input voltages under the proposed control. From Figure 16a, the input current THD is reduced to 1.4% at 110 Vac input with full load and 1.7% at 220 Vac input with full load.

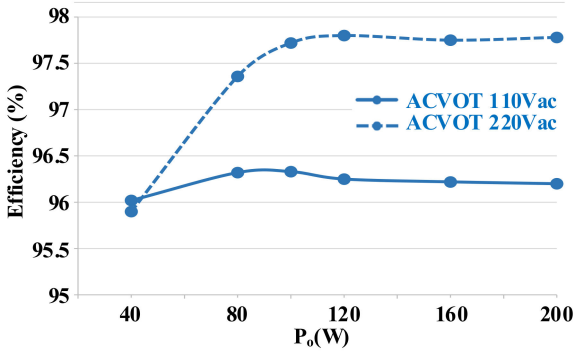

Figure 15. Measured efficiency of the prototype under the ACVOT control.

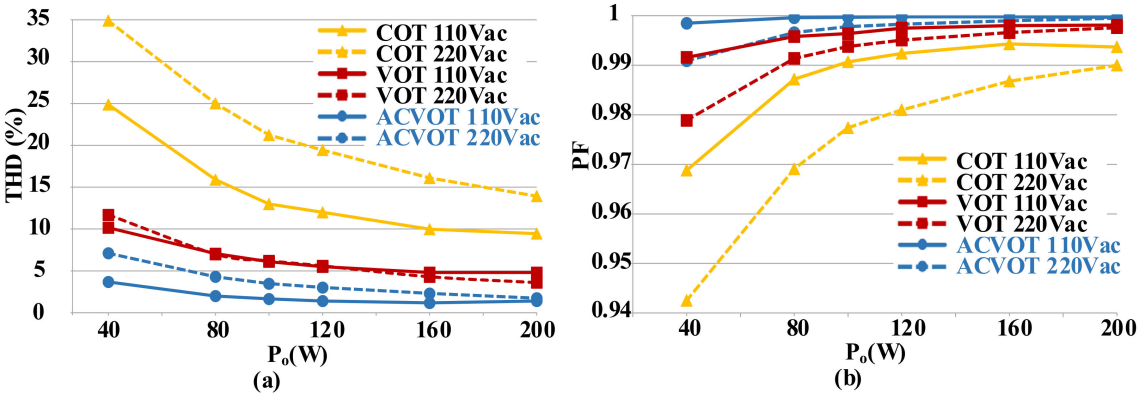

Figure 16. Measured input current PF and THD comparison: (**a**) THD; (**b**) PF.

Table 6 shows the comparison between the ACVOT control strategy and the previous VOT control strategies. Since [18] had relatively low THD data in the table, we also repeated the VOT control process in [18] at our board and showed the results in Figure 16a,b. Some of the differences shown between the data in Figure 16a and Table 6 are due to different prototypes used. In comparison, the proposed method achieves lower THD than other real-time control methods and achieves low THD levels close to reference [18]. It is noticed that [18] is based on a look-up table method. The difference between LUT implementation and real-time implementation can be explained. Method in [18] is roughly realized by:

1. Establishing a MATLAB file to estimate the average inductance current i_{L_av} (according to all fifteen equations in Tables 1 and 2);
2. Building an iterative model to acquire a table with right on-time values, which finally fits specific sinusoidal i_{L_av} curve;
3. Converting the table into a suitable storage file (satisfy different controllers of small power converter);
4. Adding storage units and accessing logic to the controller;
5. Adding accurate input phase detection to help table look-up.

Table 6. Comparison of the different control strategies.

Controls	ACVOT	[15]	[18]	[20]	[22]	[25]
Input line voltage	90–240 Vac	90–240 Vac	90–264 Vac	N/A	90–230 Vac	N/A
Output voltage	400 V	400 V	400 V	400 V	380 V	400 V
Rated power	200 W	200 W	160 W	30 W	200 W	100 W
Efficiency (max)	97.8%	N/A	98.35%	91.6%	97.35%	N/A
Input current THD (at rated power)	1.4% at 110 Vac 1.7% at 220 Vac	3.9% at 110 Vac Lack of data	0.97% at 110 Vac 2.9% at 220 Vac	Lack of data 5.6% at 220 Vac	4.3% at 90 Vac 9.8% at 230 Vac	3.74% at 110 Vac 5.5% at 220 Vac
Control method	*CRM*, digital Real-time	*CRM*/*DCM*, analog	*CRM*, digital LUT-based	*CRM*, digital Real-time	*CRM*, digital Real-time	*CRM*, digital Real-time

The method in this article is realized by:

1. Adding a several lines of the computing code (according to Equations (15) and (17)) in the prior control program).

As noted above, the easy implementation of the proposed method should be considered as a significant advantage for engineering. In summary, the ACVOT control is remarkable for its performance and easy implementation.

5. Conclusions

This paper proposes an adaptive charge-compensation-based control strategy for CRM boost PFC. The control strategy is established using the partial charge compensation algorithm and the feedback loop. A bias on-time is generated using the feedback loop. Furthermore, an extended on-time is calculated online using an algorithm to compensate the charge during the reverse inductor current stage. The above two times are added up to obtain the objective on-time, which avoids the need for numerous computing resources to directly obtain the accurate on-time. The proposed strategy improves the THD and reduces the LUT/register resources by 54%/43% in FPGA realization. Good adaptivity and robustness are shown in simulations and experiments. The input current THD is only 1.4% at the 110 Vac input with the full load and 1.7% at the 220 Vac input with the full load, supported by the 200 W prototype.

Author Contributions: Conceptualization and methodology, D.Z. and W.W.; resources, F.Z.; software and validation, N.L.; writing—review and editing, X.L.; supervision and project administration, J.Y. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare that they have no conflict of interest.

Appendix A

To explain why [22] has the lowest operations consumption among the referenced digital methods, as opposed to being LUT = based. Authors briefly list the key equations required for mentioned referenced methods in Table A1 [20,22,25], which correspond to Table 6. Moreover, Ref. [19] is excluded because it is used for totem-pole PFC, and Ref. [21] is excluded because it lacks specific calculations.

To simplify this information, symbols in the original equations are replaced by symbols with the same meaning in this paper, and complicated values which can be calculated in advance are replaced by constant symbols G_1, G_2, ... The readers should note the differences introduced by conversion of the expression styles.

Table A1. The key equations required for mentioned referenced methods.

Controls	Equations for the ZVS Condition	Equations for the vs. Condition
[20]	$M = \frac{v_o}{v_{in}}$ $T_{on} = G_1 + (M-1)G_2$ $k_1 = \frac{G_3 v_{in} + i_L(t_3)}{G_4 v_{in} + G_5 v_o + G_6 i_L(t_3)}$ $k_2 = \sqrt{G_7 \frac{M}{M-1}}$ $T_s = T_{on} + k_1 + k_2$	
[22]	$M = \frac{v_{in}}{v_o}, M\prime = \frac{v_o}{v_{in}}$ $k_1 = (1-M)T_{on}G_8 + G_9(M^2-4)$ $T_{on} = \sqrt{k_1} + G_{10}\sqrt{(M\prime-1)^2-1}$	$M = \frac{v_{in}}{v_o}, M\prime = \frac{v_o}{v_{in}}$ $k_1 = (1-M)T_{on}G_8 + G_9(3M\prime + 4M - 8)$ $T_{on} = \sqrt{k_1}$
[25]	$M = \frac{v_o}{v_{in}}$ $k_1 = G_{11}(G_{12} + (M-1)\sin G_{12})$ $T_{on} = \frac{G_{13} + \sqrt{G_{13}^2 + 4(M-1)\left(G_{13} + \frac{k_1}{\pi^2}M^2\right)k_1}}{2}$	$M = \frac{v_o}{v_{in}}$ $k_1 = G_{14}(G_{12} + G_{15}(M-1))$ $T_{on} = \frac{G_{13} + \sqrt{G_{13}^2 + 4\frac{(M-1)}{M}k_1}}{2}$

The required basic arithmetic units can be counted using the equations with consistent form in Table A1. This table shows that the equations in [22] have relatively few required computation consumptions.

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