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Space Vector Modulation (SVM)-Based Common-Mode Current (CMC) Reduction Method of H8 Inverter for Permanent Magnet Synchronous Motor (PMSM) Drives

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Abstract: This paper proposes a space vector modulation (SVM)-based common-mode (CM) currents reduction method of an H8 inverter for permanent magnet synchronous motor (PMSM) drives. There are power quality issues in the PMSM drive systems, such as current distortions and CM electromagnetic interference (EMI) due to the fast-switching operation of the inverter. These issues are related to CM voltage (CMV) and CM current (CMC). Although several studies have been conducted to reduce the CMV and CMC, some CMV variations and CMCs are still generated in the real implementation. Unlike conventional methods, the proposed method selects the voltage vectors with similar CMV levels and arranges them considering the series-connected switch operation of the H8 inverter in a voltage vector modulation sequence. At a low modulation index (MI), the proposed method synthesizes the reference voltage vector differently, depending on the position of the reference vector, to reduce both current distortions and CMCs. The validity of the proposed method is verified through simulations and experimental results.

Keywords: common-mode voltage; common-mode current; two-level voltage source inverter; permanent magnet synchronous motor

1. Introduction

With advancements in power switching devices, pulse-width modulated inverters are now able to operate with high switching frequencies. Operation at a high switching frequency makes the inverter more compact, efficient, and attractive. However, as the switching frequency increases, common-mode voltage (CMV) issues become significant [1]. In permanent magnet synchronous motor (PMSM) drive systems, CMVs cause common-mode currents (CMCs) flowing through the parasitic capacitors. These CMCs lead to problems in the PMSM drive system, such as the breakdown of winding insulation, electromagnetic interference (EMI) emission, and communication errors [2–4]. Thus, CMV issues are major concerns, which should be resolved before realizing the high-frequency switching operation of an inverter in real-world applications.

One way to alleviate the CMVs is to adopt a passive filter at the inverter input or output side [5,6]. However, an optimal design method of a passive filter is complex and requires trial and error. In addition, as the switching frequency of the inverter increases, the filter becomes larger and heavier [7], which makes these filter-based solutions unattractive in high-frequency switching operations.

On the other hand, the CMVs can be reduced without a passive filter by modifying the modulation schemes of the inverter. In a three-phase two-level inverter, the highest CMV is



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Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). generated at a zero-voltage vector (V_0 or V_7), as shown in Table 1. Therefore, conventional modulation schemes usually exclude the use of zero voltage vectors. Pulse-width modulation (PWM)-based CMV reduction methods are classified into three categories: active zero state PWM (AZSPWM) [8,9], near state PWM (NSPWM) [10], and remote state PWM (RSPWM) [11–14]. The AZSPWM selects the active voltage vectors (V_1-V_6) in the same way as the standard space vector modulation (SVM), but the zero vector is replaced with two active vectors [8,9]. Because two alternative active vectors have opposite directions with the same magnitude, the average magnitude of the modulated voltage vector becomes zero. In contrast, the NSPWM selects three active vectors to synthesize the reference voltage vector: an active vector closest to the reference vector and its two neighboring active vectors [10]. In both the AZSPWM and NSPWM, the reference voltage vector can be synthesized without using the zero vector, thus ideally restricting the CMV magnitude to $V_{dc}/6$. However, as the active vectors have different CMV levels (+ $V_{dc}/6$ or $-V_{dc}/6$) that are selected in a modulation sequence, there are several CMV variations between $+V_{dc}/6$ and $-V_{dc}/6$ in a sampling period. Since a pulsed CMC results from a high dv/dt in CMV, both variation and magnitude in CMV should be reduced.

Table 1. CMVs in a traditional three-phase two-level inverter.

Voltage Vector	Switching State (S_a , S_b , S_c) ¹	CMV Level ²
V_0	(0, 0, 0)	$-V_{dc}/2$
V_1	(1, 0, 0)	$-V_{dc}/6$
V_2	(1, 1, 0)	$+V_{dc}/6$
V_3	(0, 1, 0)	$-V_{dc}/6$
V_4	(0, 1, 1)	$+V_{dc}/6$
V_5	(0, 0, 1)	$-V_{dc}/6$
V_6	(1, 0, 1)	$+V_{dc}/6$
V_7	(1, 1, 1)	$+V_{dc}/2$

¹ $S_x (x_{a-a,b,c})$ indicates switching state in a leg of *x*: if $S_a = 1$, upper switch turns on and lower switch turns off in *a*-leg, whereas if $S_a = 0$, upper switch turns off and lower switch turns on. ² V_{dc} is DC-link voltage of inverter.

Among the PWM-based CMV reduction method, the RSPWM can effectively reduce pulsed CMCs [11]. To synthesize the reference voltage vector, the RSPWM selects only odd vectors (V_1 , V_3 , and V_5) or even vectors (V_2 , V_4 , and V_6) based on the position of the reference voltage vector. As shown in Table 1, since the odd (even) vectors have the same CMV level of $-V_{dc}/6$ (+ $V_{dc}/6$), the CMV variations can be minimized within a modulation period. Unfortunately, [11] does not consider the dead-time interval, where an unexpected CMV spike of $+V_{dc}/2$ or $-V_{dc}/2$ can be generated. Considering the dead-time interval, [12] proposed a modified RSPWM (MRSPWM) which selects odd or even vectors based on the position of the current vector. However, the MRSPWM causes several CMV variations between $+V_{dc}/6$ and $-V_{dc}/6$ whenever the load current passes its zero-crossing point. Furthermore, it is difficult to utilize the RSPWM-based methods for high-speed PMSM drive systems because of their limited modulation range within the triangular areas consisting of odd- or even-vector combinations (named RSPWM area in this paper). Although a specific overmodulation technique reported in [13] can maximally utilize the DC-link voltage, three-phase load currents are largely distorted due to a significant difference between the reference and modulated voltage vectors. A hybrid method of MRSPWM and SVPWM (HMSPWM) in [14] can reduce the current distortions in a high modulation range, but many CMV variations still appear during the SVM.

On the other hand, researchers have tried to improve the inverter topologies so as to utilize zero vectors with reduced CMVs [15–20]. Among them, the H8 inverter-based topologies, where two additional switches are employed in the traditional H6 inverter, have attracted significant attention [17–20]. A simple H8 inverter with an optional antiparallel Zener diode was proposed in [17]. The CMV can be reduced from $+V_{dc}/2$ to $+V_{dc}/4$ at V_7 and from $-V_{dc}/2$ to $-V_{dc}/4$ at V_0 by properly operating additional switches. Furthermore, to achieve near-zero CMV variation between the active and zero vectors (i.e., between V_0

and odd vectors or between V_7 and even vectors), H8 inverters were modified in [18–20]. These H8 inverter topologies can effectively reduce the peak CMVs at zero vectors, which enables the use of zero vectors in a modulation process. However, these approaches do not consider the advanced control strategies of the H8 inverter in detail. In other words, most previous works have focused only on the operation of the H8 inverter at zero vectors, even though the CMV spike of $+V_{dc}/2$ or $-V_{dc}/2$ can be generated during the dead-time interval between two active vectors. Although a dedicated modulation method for the H8 inverter considering the dead-time interval was developed in [19,20], its modulation range is still limited to the RSPWM range.

In this paper, an advanced modulation method for an H8 inverter is proposed to completely eliminate the CMV spikes even at the dead-time interval and to ultimately reduce CMCs in an entire modulation range. The concept of the proposed method in a low modulation range was proposed in [21], and it is extended to a six-step operation in this study. Depending on the position of the reference voltage vector, the proposed method selects three voltage vectors: two odd or even vectors and one zero vector. The selected zero vector is allocated not only at the beginning and end of a modulation sequence but also between two active vectors. Then, the series-connected switch of the H8 inverter is turned off during the zero-vector including the dead-time interval. Therefore, there is no CMV spike of $+V_{dc}/2$ or $-V_{dc}/2$, even at the dead-time interval. In addition, since the proposed method utilizes zero vectors, the current total harmonic distortions (THDs) and current ripples can be significantly reduced in the PMSM drive systems. Furthermore, in a high modulation range, the proposed method maintains the modulation manner of odd or even vector combination, but a two-sampling period-based vector synthesis method is adopted for the reference voltage vector far from the RSPWM area. As a result, at a high modulation range, the proposed method can improve the current THDs compared with [13], while reducing the CMV variations and CMCs compared with HMSPWM. In summary, the main contributions of this paper are as follows:

- (1). An advanced modulation method for an H8 inverter is proposed to minimize the CMV variations between $+V_{dc}/6$ and $-V_{dc}/6$;
- (2). Proper switching operation of the series-connected switch in the H8 inverter is considered during the modulation sequence to completely eliminate the highest CMV of $+V_{dc}/2$ or $-V_{dc}/2$ even at the dead time interval;
- (3). At a high modulation range, a novel vector synthesis method is proposed, which is based on two sampling periods but in the same modulation manner;
- (4). As a result, both the CMCs and current THDs can be improved over the entire modulation range, compared with the conventional methods.

The effectiveness of the proposed method is verified by simulation and experiment.

The remainder of this paper is organized as follows. Section 2 reviews the conventional CMC reduction methods, such as RSPWM-based methods for an H6 inverter and a basic operation for an H8 inverter in detail. The proposed method in both low and high modulation ranges is presented in Section 3. To verify the effectiveness of the proposed method, the simulation results and experimental results are presented in Sections 4 and 5, respectively. Finally, Section 6 concludes this paper.

2. Review of Conventional Strategies

This section reviews RSPWM, [11] MRSPWM [12,13], and HMSPWM [14] in detail. Besides, the basic operations of the H8 inverter are presented.

2.1. RSPWM, MRSPWM, and HMSPWM

To synthesize the reference voltage vector, the RSPWM combines three active voltage vectors with the same CMV level, thus minimizing the CMV variations during a modulation period. In an ideal case, the RSPWM restricts the CMV variations into six times during a reference rotational period. However, in real-world applications, the dead-time interval, which should be inserted between the gate signals of two switches in a leg, can cause



$$v_{CM} = (v_{an} + v_{bn} + v_{cn})/3$$
(1)

Figure 1. Circuit configuration and operation of H6 inverter: (a) Circuit configuration; (b) Circuit operation when voltage vector changes from V_1 to V_3 .

In Figure 1b, at V_1 , switches S_1 , S_6 , and S_2 turn on and switches S_4 , S_3 , and S_5 turn off; therefore, $v_{an} = +V_{dc}/2$ and $v_{bn} = v_{cn} = -V_{dc}/2$ and the CMV becomes $-V_{dc}/6$. In order to change vector state from V_1 to V_3 , S_1 and S_6 turn off during the dead-time interval. In this case, because all switches in *a*-phase leg turn off and current i_a flows to the load, the antiparallel diode of S_4 starts conducting. Accordingly, $v_{an} = v_{bn} = v_{cn} = -V_{dc}/2$ and the CMV spike of $-V_{dc}/2$ is generated during the dead-time interval. Subsequently, S_4 and S_3 turn on at V_3 and the CMV becomes $-V_{dc}/6$. In this way, the occurrence of the CMV spike during the dead-time interval is determined by the switching states and load current directions.

To completely eliminate the CMV spikes even at the dead-time interval, the MR-SPWM selects three active vectors based on the position of current vector I^* , as shown in Figure 2a [12]. However, several CMV variations between $+V_{dc}/6$ and $-V_{dc}/6$ are generated by misrecognizing the current sector around the zero-crossing point of the load current, due to PWM current ripples. Furthermore, the utilization of the DC-link voltage is poor without a special overmodulation method. When modulation index (MI) is defined as follows:

$$\mathrm{MI} = V_{s1} / (2V_{dc}/\pi) \tag{2}$$

where V_{s1} is a fundamental component of the inverter output voltage, the maximum MI of the MRSPWM is 0.604. An overmodulation method for the MRSPWM was proposed in [13] to extend the modulation range to a six-step operation. If the reference voltage vector is located at the overmodulation area in Figure 2b, this method synthesizes the approximate voltage vector within the RSPWM area. However, a significant difference between the reference and approximate voltage vectors results in high current distortions and high current ripples. Although the HMSPWM can reduce current distortions by adopting a standard SVPWM for several areas, as shown in Figure 2c [14], the CMV issues again become severe during the SVPWM.

2.2. Basic Operation of H8 Inverter

Figure 3 shows the circuit configuration of the H8 inverter and its equivalent circuits at zero voltage vectors. In Figure 3a, additional switches S_7 and S_8 are connected in series between the DC-link and H6 inverter. By appropriately operating S_7 and S_8 , the highest CMVs of $+V_{dc}/2$ and $-V_{dc}/2$ can be reduced. When active vectors are applied to the H8 inverter, S_7 and S_8 maintain the on-state for powering or regenerating operations, whereas S_7 or S_8 turns off during zero vector to reduce the magnitude of the peak CMV. As shown in

Figure 3b, S_8 turns off at V_0 ; therefore, $v_{an} = v_{bn} = v_{cn} = -V_{dc}/4$ based on Kirchhoff's current and voltage laws and the CMV becomes $-V_{dc}/4$ [18]. Similarly, S_7 turns off at V_7 ; therefore, $v_{an} = v_{bn} = v_{cn} = +V_{dc}/4$ and the CMV becomes $+V_{dc}/4$, as shown in Figure 3c. Compared with the CMV of the H6 inverter at zero vectors, the magnitude of the CMV is reduced by half in the H8 inverter. This allows the use of zero vectors in a modulation process. In [19,20], a dedicated modulation method for an H8 inverter was proposed to reduce the CMV variations and CMCs; however, its modulation area, which is defined based on the inscribed circle of a triangle, strictly limits MI to 0.524 ($V_{s1} = V_{dc}/3$) to maintain the CMV level at a constant value during a modulation process. In addition, at a high MI range, two CMV variations between $+V_{dc}/6$ and $-V_{dc}/6$ are generated for every sampling period, increasing the CMCs.



Figure 2. Conventional CMC reduction methods: (**a**) MRSPWM; (**b**) MRSPWM with overmodulation method; (**c**) HMSPWM.



Figure 3. Circuit configuration and operation of H8 inverter: (a) Circuit configuration; (b) Circuit operation at V_0 ; (c) Circuit operation at V_7 .

3. Proposed SVM-Based CMC Reduction Method

This paper proposes an SVM-based CMC reduction method for an H8 inverter. The proposed method is described through two parts based on the modulation range: low modulation range (MI \leq 0.604) and high modulation range (0.604 < MI \leq 1.0). To eliminate the peak CMVs over the entire modulation range, the operations of S_7 and S_8 were considered in both modulation ranges.

3.1. Low Modulation Range ($MI \le 0.604$)

3.1.1. Selection of Voltage Vector

The voltage vector diagram of the proposed method when MI is smaller than 0.604 is shown in Figure 4. Unlike the MRSPWM, which selects three active vectors, the proposed

method selects two active and one zero vectors. For example, as shown in Figure 4, the reference voltage vector in sector 1 is synthesized using two odd vectors V_1 and V_3 and one zero vector V_0 . Compared with the MRSPWM, the proposed method can greatly improve the current THDs and current ripples owing to the use of the zero vector. Considering the different combinations of voltage vectors, in the proposed method, the vector diagram is divided into 12 sectors; however, as each odd or even sector has the same CMV level, the number of CMV variations can be restricted to six times during a reference rotational period.



Figure 4. Voltage vector diagram of proposed method at $MI \le 0.604$.

The triangular area consisting of odd or even vectors means that the reference vector within that area can be synthesized by using the vector combinations, as shown in Figure 4. Therefore, the linear MI range of the proposed method is up to 0.604 (i.e., the linear modulation area becomes the inscribed circle of the star composed of two triangles). Compared with the conventional methods in [19,20], the proposed method further extends the MI range while maintaining the CMV level constant during a sampling period.

3.1.2. Modulation Sequence

In the modulation sequence of the proposed method, zero vector acts as a connector between two active vectors. As previously mentioned, the CMV spikes can be generated during the dead-time interval between two odd or even vectors. In order to prevent the generation of CMV spikes, zero vector is allocated between two odd or even vectors. Furthermore, to eliminate the CMV spikes when the reference vector position suddenly changes from a sector to another sector, zero vector is also allocated at the beginning and end of the modulation sequence. For example, Figure 5 shows the modulation sequences of the proposed method when the reference vector is located at sectors 1 and 2, respectively. As shown in Figure 5, the modulation sequence has a symmetric structure consisting of an open sequence and a close sequence during sampling period T_s . In sector 1, voltage vectors V_1 , V_3 , and V_0 are selected. V_0 is divided into four parts and allocated not only between V_1 and V_3 but also at the beginning and end of the modulation sequence. Therefore, there is no direct vector transition between V_1 and V_3 , which can cause CMV spikes. In this case, the turning-on and turning-off timings of S_8 is important. As shown in Figure 5a, S_8 turns off during V_0 including both side dead-time intervals regardless of whether or not the CMV spikes are generated. Based on the operation of S_8 , the peak CMV of $-V_{dc}/2$ can be completely reduced.



Figure 5. Modulation sequences of proposed method when G_1 – G_8 denote gate signals of switches S_1 – S_8 , respectively: (a) Sector 1; (b) Sector 2.

Similarly, Figure 5b shows the modulation sequence in sector 2, where voltage vectors V_2 , V_6 , and V_7 are selected. Unlike in operation in sector 1, S_7 should be turned off during V_7 , including both side dead-time interval. The modulation sequence with the operation of S_7 eliminates the peak CMV of $+V_{dc}/2$. It is worth noting that the proposed modulation method does not require information on the load current direction, unlike the MRSPWM; therefore, there are no CMV variations around the zero-crossing point of the current.

When the reference vector V^* is located in sector 1, the following relationship is satisfied:

$$\int_{0}^{T_{s}} V^{*} dt = \int_{0}^{T_{1}} V_{1} dt + \int_{0}^{T_{2}} V_{3} dt + \int_{0}^{T_{0}} V_{0} dt$$
(3)

where T_1 , T_2 , and T_0 are the modulation times of the first, second, and third vectors (V_1 , V_2 , and V_0 in the case of sector 1, as shown in Figure 4). Assuming that V^* and the DC-link voltage do not change during T_s , (3) can be rewritten as follows:

$$T_s \cdot V^* = T_1 \cdot V_1 + T_2 \cdot V_3 + T_0 \cdot V_0 = T_1 \cdot V_1 + T_2 \cdot V_3 \tag{4}$$

Based on (4), each modulation time can be calculated as follows:

$$T_1 = \frac{|V^*| \cdot \sin(2\pi/3 - \alpha)}{(2V_{dc}/3) \cdot \sin(2\pi/3)} \cdot T_s$$
(5)

$$T_2 = \frac{|V^*| \cdot \sin(\alpha)}{(2V_{dc}/3) \cdot \sin(2\pi/3)} \cdot T_s$$
(6)

$$T_0 = T_s - T_1 - T_2 \tag{7}$$

where $|V^*|$ is the magnitude of V^* and α is the modulation angle. To calculate the modulation times using the same equation forms in (5)–(7) in different sectors, α should be modified as follows:

$$\alpha = \begin{cases}
\theta & (\text{Sector } 1: 0 \le \theta < \pi/6) \\
\pi/3 - \theta & (\text{Sector } 2: \pi/6 \le \theta < 2\pi/6) \\
\pi/3 + \theta & (\text{Sector } 3: 2\pi/6 \le \theta < 3\pi/6) \\
2\pi/3 - \theta & (\text{Sector } 4: 3\pi/6 \le \theta < 4\pi/6) \\
2\pi/3 + \theta & (\text{Sector } 5: 4\pi/6 \le \theta < 5\pi/6) \\
\pi - \theta & (\text{Sector } 6: 5\pi/6 \le \theta < 6\pi/6) \\
\pi + \theta & (\text{Sector } 7: 6\pi/6 \le \theta < 7\pi/6) \\
4\pi/3 - \theta & (\text{Sector } 8: 7\pi/6 \le \theta < 8\pi/6) \\
4\pi/3 + \theta & (\text{Sector } 9: 8\pi/6 \le \theta < 9\pi/6) \\
5\pi/3 - \theta & (\text{Sector } 10: 9\pi/6 \le \theta < 10\pi/6) \\
5\pi/3 + \theta & (\text{Sector } 11: 10\pi/6 \le \theta < 12\pi/6)
\end{cases}$$
(8)

where θ is the angle of V^* as shown in Figure 4.

The voltage vector synthesis process when V^* is located in sector 1 is shown in Figure 6. Neglecting the allocation of V_0 in the modulation sequence in Figure 5a, V_1 among the selected active vectors is first applied during $T_1/2$. Therefore, the instantaneously modulated voltage vector is the same as that shown in Figure 6a. V_3 is then applied during T_2 over both the open and close sequences. In this case, the modulated vector intersects V^* , as shown in Figure 6b. Finally, by applying V_1 again during its remaining modulation time $T_1/2$, the modulated voltage vector is the same as V^* , as shown in Figure 6c.



Figure 6. Process of synthesizing reference voltage vector in sector 1: (a) During first half of T_1 ; (b) During T_2 ; (c) During second half of T_1 .

3.2. *High Modulation Range* $(0.604 < MI \le 1)$

3.2.1. Modulation Method Depending on Sub-Sectors

In [13], the overmodulation method of MRSPWM was proposed to maximally utilize the DC-link voltage. However, there are large current distortions because of the significant difference between the reference and modulated voltage vectors. Although [14] proposed the HMSPWM to reduce current distortions, the CMV variations increased during the SVPWM areas. To reduce both the CMV variations and current distortions at a high modulation range, an advanced modulation method for the H8 inverter is presented herein. The voltage vector diagram for high modulation range in the proposed method is shown in Figure 7a, and a magnified view of sectors 1 and 2 is shown in Figure 7b. As shown, when the range of MI is higher than 0.604, the area in sector 1 is subdivided into three parts: the RSPWM area, vector approximation (VA) area, and vector synthesis (VS) area.



The proposed method synthesizes the reference vector in different ways depending on the subsectors, as described in the following sections.

Figure 7. Voltage vector diagram of proposed method at MI > 0.604: (**a**) Overall diagram; (**b**) Subsectors in sector 1.

Sub-Sector 1: RSPWM Area

As previously mentioned, the reference voltage vector in the RSPWM area can be synthesized using the vector combinations in Figure 7a. For example, the reference vector in the RSPWM area of sector 1 can be synthesized using V_1 , V_3 , and V_0 with the same modulation sequence as that shown in Figure 5a. Figure 7b shows that the RSPWM area becomes narrow with increasing MI.

Sub-Sector 2: VA Area

The vector combinations in Figure 7a cannot completely synthesize the reference voltage vector located in the VA area; therefore, the proposed method approximates the reference vector to one at the boundary of the RSPWM area. Figure 8 shows the approximate method for the reference vector in the VA area of sectors 1 and 2, respectively. V_{App}^* and θ_{App} denote the approximate reference vector and its modulation angle, respectively. Figure 8 shows that the standard axis of θ_{App} changes depending on sectors; for example, the standard axis becomes V_1 in sector 1 and V_2 in sector 2, respectively. At a steady state, V^* may rotate in the voltage vector diagram while drawing a circle with a radius of $|V^*|$. V_{App}^* is always located at the same circumference as V^* in the same sector. Accordingly, $|V_{App}^*|$ is the same as $|V^*|$. θ_{App} whose radian range is [0, 0.19) becomes a function of $|V^*|$ as follows:

$$\theta_{App} = \frac{\pi}{3} - \cos^{-1}\left(\frac{V_{dc}}{3 \cdot |V^*|}\right) \tag{9}$$

Therefore, when V^* is located in the VA area, the proposed method can synthesize V^*_{App} using $|V^*|$. Compared with the overmodulation method in [13], VA area, in which the current THD and current ripples increase, becomes narrow because the proposed method additionally adopts vs. area, as explained in the following section.



Figure 8. Approximate method for reference voltage vector in VA area: (a) Sector 1; (b) Sector 2.

Sub-Sector 3: Vs. Area

In the vs. area, a two-sampling period-based vector synthesis method is proposed to reduce both current distortions and CMCs. When V^* is located in the vs. area, the proposed method synthesizes two voltage vectors: one is located at the boundary of the RSPWM area of the odd sector, whereas the other is located at the boundary of the RSPWM area of the even sector. By combining two vectors during two sampling periods, the proposed method can completely synthesize the reference vector located in the vs. area. For example, Figure 9 shows the vector synthesis method for the reference vector in the vs. area of sector 1. As can be seen, the vector synthesis method is divided into two vector modulation sequences: the odd-even vector sequence and even-odd vector sequence. In the odd-even vector sequence, the reference vector in the odd sector (V_{Odd}^*) is synthesized during T_s ; subsequently, the reference vector in the even sector (V_{Even}^*) is synthesized following T_s . In contrast, V_{Even}^* is first synthesized during T_s , and then V_{Odd}^* is synthesized during following T_s in the even-odd vector sequence. The proposed method alternates the order of odd-even and even-odd vector sequences sequences the order of odd-even and even-odd vector sequences every two sampling periods so as to reduce the CMV variations, and ultimately to reduce the CMCs.

"VS area" denotes an area in which V^* can be synthesized using both V^*_{Odd} and V^*_{Even} based on two sampling periods. As shown in Figure 10, the vs. area widens with increasing $|V^*|$ in the range of $(2V_{dc}/3\sqrt{3}, \sqrt{7V_{dc}}/3\sqrt{3}]$, whereas it shrinks with increasing $|V^*|$ in the range of $(\sqrt{7V_{dc}}/3\sqrt{3}, V_{dc}/\sqrt{3}]$. Therefore, the range of the vs. area can be divided into two ranges as follows:

$$VS \text{ Area in Sector1} = \begin{cases} \frac{\pi}{3} - \cos^{-1}\left(\frac{V_{dc}}{3|V^*|}\right) < \theta \le \cos^{-1}\left(\frac{V_{dc}}{3|V^*|}\right) & \text{for } \frac{2V_{dc}}{3\sqrt{3}} < |V^*| \le \frac{\sqrt{7}V_{dc}}{3\sqrt{3}} \\ \cos^{-1}\left(\frac{V_{dc}}{2|V^*|}\right) < \theta \le \frac{\pi}{3} - \cos^{-1}\left(\frac{V_{dc}}{2|V^*|}\right) & \text{for } \frac{\sqrt{7}V_{dc}}{3\sqrt{3}} < |V^*| \le \frac{V_{dc}}{\sqrt{3}} \end{cases}$$
(10)



Figure 9. Vector synthesis method for reference voltage vector in vs. area of sector 1: (a) Odd-even vector modulation sequence; (b) Even-odd vector modulation sequence.



Figure 10. Range of vs. area of sectors 1 and 2.

In addition, the vs. area in other sectors can be obtained by adjusting θ ; for example,

by replacing θ in (10) with $\theta - \pi/3$ in the vs. area in sectors 3 and 4. To obtain V_{Odd}^* and V_{Even}^* in the vs. area, the relation between V^* and V_{Odd}^* can be calculated as follows:

$$V^* |\cos \theta = \frac{1}{2} |V_{Odd}^*| \cos \theta_{Odd} + \frac{1}{6} V_{dc}$$
(11)

where $|V_{Odd}^*|$ and θ_{Odd} are the magnitude and modulation angle of V_{Odd}^* , respectively. As V_{Odd}^* is always located at the boundary of the RSPWM area, the relation between $|V_{Odd}^*|$ and θ_{Odd} can be calculated as follows:

$$|V_{Odd}^{*}| = \frac{V_{dc}/3}{\cos(\frac{\pi}{3} - \theta_{Odd})}$$
(12)

where the radian range of θ_{Odd} is $[0, \pi/6]$. By substituting (12) into (11), θ_{Odd} can be expressed using $|V^*|$ and θ as follows:

$$\theta_{Odd} = \tan^{-1} \left(\frac{\sqrt{3} \cdot (V_{dc} - 2|V^*|\cos\theta)}{6|V^*|\cos\theta - V_{dc}} \right)$$
(13)

Therefore, when $|V^*|$ and θ are given from V^* in vs. area, V^*_{Odd} can be calculated using (12) and (13). Subsequently, V^*_{Even} can be obtained as follows:

$$V_{Even}^* = 2V^* - V_{Odd}^*$$
(14)

Both odd-even and even-odd vector sequences can be realized by adjusting the application order of V_{Odd}^* and V_{Even}^* : V_{Odd}^* is first and V_{Even}^* is second in the odd-even vector sequence, whereas V_{Even}^* is first and V_{Odd}^* is second in the even-odd vector sequence.

For example, Figure 11 shows modulation sequences in vs. area of sector 1, where the odd-even vector sequence is first implemented, and the even-odd vector sequence is subsequently implemented. As can be seen in Figure 11, the CMV variation occurs every two sampling periods by alternating odd-even and even odd vector sequences; therefore, the CMCs can be significantly reduced compared with that of the standard SVPWM, while completely synthesizing the reference vector in the vs. area. Note that S_7 (S_8) turns off during the dead-time interval between even (odd) vectors to eliminate the CMV spikes.

L	Open So	equence	Close Se	equence	Open Se	equence	Close Se	equence	Open So	equence	Close Se	equence	Upen Se	equence	Close S	equence
Voltage Vector	$V_{1} \\ (1, 0, 0)$	V_{3} (0, 1, 0)	V_{3} (0, 1, 0)	$V_{I} (1, 0, 0)$	$V_{2} (1, 1, 0)$	V ₆ (1, 0, 1)	V ₆ (1, 0, 1)	$V_{2} (1, 1, 0)$	$V_{2} (1, 1, 0)$	V ₆ (1, 0, 1)	V ₆ (1, 0, 1)	$V_{2} (1, 1, 0)$	$V_{1} \\ (1, 0, 0)$	$V_{3} \\ (0, 1, 0)$	V_{3} (0, 1, 0)	$V_{1} \\ (1, 0, 0)$
$G_{\underline{I}}$	1	0	0	1	1	1	1	1	1	1	1	1	1	0	0	1
G_4	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0
$G_{\underline{3}}$	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
$G_{\underline{6}}$	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1
$G_{\underline{5}}$	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0
G_2	1	1	1	1	1	0	0	1	1	0	0	1	1	1	1	1
G_{Z}	1	1	1	1	1 07	1	1	1	1 07	1	1	1	1	1	1	1
G_8	1 ,	1	1	1	1	1	1	1	1	1	1	1	1 ,	1	1	1
CMV	0'			0		$+V_d$	_c /6			$+V_{d}$	_{tc} /6		0'			0
ji ji		$-V_{a}$	<u>c/6</u>											$-V_{a}$	6	
Time	$T_{l}/2$	$T_2/2$	$T_2/2$	$T_{1}/2$	$T_{I}/2$	$T_2/2$	$T_2/2$	$T_{l}/2$	$T_{l}/2$	$T_2/2$	$T_2/2$	$T_{l}/2$	$T_{I}/2$	$T_2/2$	$T_2/2$	$T_I/2$
	T_s T_s					T_s T_s										
į	$2 \cdot T_s$					$2 \cdot T_s$										
	Udd-Even vector Sequence					Even-Odd Vector Sequence										

Figure 11. Modulation sequences of proposed method in vs. area of sector 1.

3.2.2. Six-Step Operation

The proposed method naturally enters a six-step operation based on the operation in the VA region. Figure 12 shows overmodulation of the proposed method in the MI range of (0.907, 1.0]. As can be seen, when MI is larger than 0.907, the proposed method operates only in the VA area. Because the RSPWM area shrinks with increasing MI, V_{App}^* is gradually closed to V_1 ; therefore, at MI = 1.0, the six-step operation is naturally implemented without a special operation mode change.



Figure 12. Overmodulation of proposed method in MI range of (0.907, 1.0].

In the PMSM drive systems, although the current distortions and current ripples will be increased due to a rare switching operation, the six-step operation is widely adopted to maximize the utilization of the DC-link voltage. Additionally, the six-step operation extends a constant torque region in a speed-torque capability curve and increases the rated speed. In the proposed method, S_7 and S_8 maintain the on-state during the six-step operation because there is no transition between odd (or even) vectors.

4. Simulation Results

The proposed SVM method was simulated using a surface mounted PMSM (SPMSM) drive system. The simulation parameters and operating conditions are listed in Table 2. The SPMSM was controlled in a torque control mode, whereas the load motor was controlled in a speed control mode. The proposed method was tested at both low and high MI ranges by adjusting the rotor speed of load motor. The conventional MRSPWM [12] and standard SVPWM were also simulated for performance comparisons.

Parameter	Description	Value	Unit
V _{dc}	DC-Link Voltage	70	V
T_s	Sampling Period	250	μs
f_s	Sampling Frequency	8	kHz
T_d	Dead-Time Interval	4	μs
P_{rate}	Rated Power of SPMSM	750	Ŵ
V _{dc rate}	Rated DC-Link Voltage	200	V
ω_{rate}^{-}	Rated Speed	3000	rpm
Irate	Rated Current	4.4	Ā
T_{rate}	Rated Torque	2.39	Nm
р	Number of Poles	10	-
\dot{R}_s	Stator Resistance	0.6333	Ω
L_{S}	Stator Inductance	2.08	mH
V _{vk} /krpm	Peak Line-to-Line Back EMF Constant	45	V/krpm

Table 2. Simulation parameters and operating condition.

4.1. Low Modulation Range ($MI \le 0.604$)

Comparisons of the simulation results of three-phase current (i_a , i_b , and i_c), CMV, and CMC between the standard SVPWM, MRSPWM, and proposed method are shown in Figure 13 at a rated load current and rotor speed of 500 rpm (MI = 0.4). As shown in Figure 13a, the standard SVPWM has a superior load current THD as 1.71% in i_a , compared with the results of the other methods; however, severe CMV variations between $+V_{dc}/2$ and $-V_{dc}/2$ are generated, which significantly increase CMCs. The root mean square (RMS) CMC of the standard SVPWM is 10.7 μ A. On the other hand, in Figure 13b, the RMS CMC in MRSPWM can be reduced to 1.37 μ A by reduce both the magnitude and variation in the CMV. However, not only the current THD of i_a increases to 4.81% due to the absence of zero vector, but also several CMV variations between $+V_{dc}/6$ and $-V_{dc}/6$ are generated whenever load current passes through its zero-crossing point. The proposed method shown in Figure 13c, improves current THD of i_a to 2.64%, compared with that of the MRSPWM. In addition, the CMV variations between $+V_{dc}/6$ and $-V_{dc}/6$ are completely restricted to six times during a reference rotational period. Accordingly, there are only six pulsed CMCs during a reference period, and its RMS value is the lowest at 0.982 μ A.

The detailed switching operations of the proposed method in sectors 1 and 2 are shown in Figure 14, respectively. As shown in Figure 14a, there are no switching operations in *c*-phase (S_2 and S_5) because only V_1 , V_3 , and V_0 are used in modulation sequence in sector 1. In addition, the CMV spike of $-V_{dc}/2$ can be completely eliminated by turning off S_8 at V_0 considering dead-time interval. Similarly, in Figure 14b, switching states in *a*-phase (S_1 and S_4) do not change during modulation sequence because only V_2 , V_6 , and V_7 are selected to modulate V^* located in sector 2. Accordingly, S_7 turns off at V_7 including dead-time interval and the CMV spike of $+V_{dc}/2$ can be completely eliminated. Although the vector diagram of the proposed method is divided into 12 sectors, there are only six CMV variations between $+V_{dc}/6$ and $-V_{dc}/6$ during a reference rotational period, because odd (even) sectors have the same CMV level of $-V_{dc}/6$ ($+V_{dc}/6$). In addition, there are no unexpected CMV variations when load current passes through its zero-crossing points because the proposed does not rely on polarities of load currents, unlike MRSPWM.

4.2. High Modulation Range (MI > 0.604)

The performance of the proposed method at a high MI (>0.604) is also verified through a simulation. Simulation results of three-phase current (i_a , i_b , and i_c), CMV, and CMC are shown in Figure 15. When MI is larger than 0.604, V^* starts to pass through the vs. area where V^*_{Odd} and V^*_{Even} are synthesized. As shown in Figure 15a, additional CMV variations between $+V_{dc}/6$ and $-V_{dc}/6$ are generated at a rotor speed of 1000 rpm (MI = 0.7); i.e., the number of CMV variation is not restricted to six times during a reference period due to the vs. area. However, the vs. area allows V^* to be appropriately synthesized based on two



sampling periods. As a result, the proposed method maintains low current THDs as 3.48% (i_a) , 3.51% (i_b) , and 3.59% (i_c) at the expense of a few CMV variations.

Figure 13. Comparison of simulation results of three-phase current, CMV, and CMC at rated load current and rotor speed of 500 rpm (MI = 0.4): (a) Standard SVPWM; (b) MRSPWM; (c) Proposed method.

As shown in Figure 15b, when MI reaches to 0.9 by increasing the rotor speed from 1000 rpm to 1200 rpm, V^* passes through both the vs. and VA areas. The number of CMV variations is slightly increased compared with that at MI = 0.7, because current distortions increase due to VA area and the fluctuation of MI is also increased by PI current controllers. The fluctuation in MI can be reduced by adjusting the gains of the PI controller. In addition, the number of CMV variations are still low, compared with that of the MRSPWM (See Figure 13b), because the proposed method does not cause unexpected CMV variations at the zero-crossing points of the load current. Even at a high MI of 0.9, the proposed method exhibits sinusoidal current waveforms by utilizing the RSPWM, VS, and VA areas.

The six-step operation of the proposed method is shown in Figure 15c. Except for additional CMV variations due to the fluctuation of MI, the overall performance is similar to that of a traditional six-step operation: i.e., current distortions increase due to a rare switching operation, but the DC-link voltage is maximally utilized (MI = 1.0).

Figure 16 shows traces of the modulated voltage vector when the proposed method is applied at high MI. As can be seen, the modulated voltage vectors are always located in the RSPWM areas and their magnitudes (distance between origin point and modulated voltage vector point in the vector diagram) increase with increasing MI. In addition, when the rotor speed increases to 1400 rpm, MI is close to 1.0 (six-step operation); that is, traces of the modulated voltage vector hexagon. We can know that the proposed method naturally enters the six-step operation as traces of the modulated voltage vectors follow suburbs of the RSPWM area.



Figure 14. Simulation results of gating signals in proposed method: (a) Sector 1; (b) Sector 2.

1.0 0.8 0.6 0.4 0.2 0.0

10

0 $-5 \\ -10$

40 20 0

-20 -40

 i_{a} i_{b} , i_{c} [A]

CMV [V]

CMC [µA]

ſſ

Af







Figure 15. Simulation results of proposed method at high MI: (a) At rotor speed of 1000 rpm (MI = 0.7); (b) At rotor speed of 1200 rpm (MI = 0.9); (c) At rotor speed of 1400 rpm (MI = 1.0).



Figure 16. Voltage vector traces of proposed method at high MI: (**a**) At rotor speed of 1000 rpm (MI = 0.7); (**b**) At rotor speed of 1200 rpm (MI = 0.9); (**c**) At rotor speed of 1400 rpm (MI = 1.0).

5. Experimental Results

To verify the performance of the proposed SVM method, an experiment was conducted using an SPMSM test bench, as shown in Figure 17. The experimental parameters are the same as the simulation parameters, as shown in Table 2. The control algorithm was implemented using a DSP board (TMS320F28335). To achieve a maximum torque per ampere (MTPA) control for the SPMSM, the *d* and *q*-axes reference currents were set to zero and 6.22 A, respectively, in order to generate the rated torque. The reference voltage vector was generated using the *d* and *q*-axes PI current controllers. Therefore, the SPMSM was operated in a torque control mode, whereas the load motor was controlled in a speed control mode similar to the operation in the simulation. By adjusting the rotor speed of the load motor, the proposed method was carried out at both low and high MI ranges.



Figure 17. Photo of SPMSM test bench.

5.1. Low Modulation Range ($MI \le 0.604$)

The operations of the series-connected switches in the H8 inverter are shown in Figure 18. As shown in Figure 18a, when V_0 is applied to the H8 inverter (i.e., G_1 , G_3 , and G_5 become a low level, whereas G_2 , G_4 , and G_8 become a high level), G_7 becomes a low level. Subsequently, S_7 turns off and the peak CMV of $-V_{dc}/2$ is reduced to $-V_{dc}/4$ at V_0 . This operation is shown in Figure 5a. Similarly, as shown in Figure 18b, when V_7 is applied to the H8 inverter (i.e., G_1 , G_3 , and G_5 become a high level, whereas G_2 , G_4 , and G_8 become a low level), G_8 becomes a low level to turn off S_8 and to reduce the peak CMV of $+V_{dc}/2$ to $+V_{dc}/4$. This operation is shown in Figure 5b.



Figure 18. Experimental results of operation of S_7 and S_8 : (**a**) G_1 , G_3 , G_5 , and G_8 ; (**b**) G_4 , G_6 , G_2 , and G_7 .

The experimental results of three-phase voltage and CMV at a rated load current and rotor speed of 500 rpm are shown in Figure 19. As the reference voltage vector rotates counterclockwise in the voltage vector diagram, the vector sector increases from sector 1 to sector 12. The CMV was calculated using the measured three-phase voltage based on (1). There is no peak CMV of $+V_{dc}/2$ or $-V_{dc}/2$, which causes severe pulsed CMCs. In addition, the CMV variations between $+V_{dc}/6$ and $-V_{dc}/6$ can be completely restricted to six times during a reference rotational period (24 ms at a rotor speed of 500 rpm). That is, the CMV variations between $+V_{dc}/6$ and $-V_{dc}/6$ are generated only when the vector sector is changed between the odd and even sectors. The CMV generated patterns are similar during the odd (or even) sectors. Furthermore, unlike the MRSPWM, as the proposed method selects the voltage vector based on the position of the reference voltage vector, the unexpected CMV variations between $+V_{dc}/6$ and $-V_{dc}/6$ are reduced when load currents pass their zero-crossing points.

Comparison of experimental results of *a*-phase current, three-phase pole voltage, and CMV at a rated load current and rotor speed of 500 rpm is shown in Figure 20. The experiment results are similar to the simulation results, shown in Figure 13. In Figure 20a, the current THD of the standard SVPWM is superior as 4.32% than these of the other methods. However, many peak CMVs of $+V_{dc}/2$ and $-V_{dc}/2$ are generated, which lead to severe CMCs. In Figure 20b, although the CMV variations can be reduced in the MRSPWM, the current THD significantly increases to 7.89% due to the absence of the use of the zero vector. In addition, several CMV variations are still generated. On the other hand, as shown in Figure 20c, the proposed method not only improves the current THD as 5.85% compared with that of the MRSPWM but also completely restricts the number of CMV variations to six times.



Figure 19. Experimental results of vector sector, three-phase pole voltage, and CMV at rated load current and rotor speed of 500 rpm.



Figure 20. Comparison of experimental results of *a*-phase current, three-phase pole voltage, and CMV at rated load current and rotor speed of 500 rpm: (**a**) Standard SVPWM; (**b**) MRSPWM; (**c**) Proposed method.

5.2. High Modulation Range (MI > 0.604)

The proposed method was also implemented at high MI by increasing the rotor speed of the load motor. Figure 21 shows the experimental results of *a*-phase current, three-phase voltage, and CMV at a rated load current and rotor speed of 1200 rpm. Accordingly, as shown in Figure 21a, the peak value and frequency of *a*-phase current (*i_a*) is 6.22 A and 100 Hz, respectively. As can be seen, the peak CMV of $+V_{dc}/2$ or $-V_{dc}/2$ is eliminated by appropriately operating the series-connected switches, even at high MI. Unlike in the CMV-generated patterns at low MI, there are several CMV variations between $+V_{dc}/6$ and $-V_{dc}/6$ when the voltage vector sector is changed between odd and even sectors. This is because the proposed method modulates V^* , which is located in the vs. area, using V_{Odd}^* and V_{Even}^* based on two sampling periods. Figure 21b shows the magnified waveforms of Figure 21a. As can be seen, the CMV variations between $+V_{dc}/6$ and $-V_{dc}/6$ are generated only between odd and even voltage sectors. In addition, the occurrence of CMV variation between $+V_{dc}/6$ and $-V_{dc}/6$ is independent of the zero-crossing points of the load current.



Figure 21. Experimental results of *a*-phase current, three-phase pole voltage, and CMV at rated load current and rotor speed of 1200 rpm: (a) i_a , v_a , v_b , v_c , and CMV; (b) Magnified waveforms of (a).

Similarly, Figure 22 shows the experimental results of *a*-phase current, three-phase voltage, and CMV at a rated load current and rotor speed of 1500 rpm. When the rotor speed of SPMSM is 1500 rpm, MI is close to 1.0. As shown in Figure 22, the current waveform of i_a is similar to that of six-step operation; that is, the distortion of i_a increases because of the rare switching operation. Even at MI close to 1.0, the peak CMV of $+V_{dc}/2$ or $-V_{dc}/2$ is eliminated. Similar to the operation at a rotor speed of 1200 rpm, there are several CMV variations between $+V_{dc}/6$ and $-V_{dc}/6$ in the vs. area.

The experimental results of three-phase current at a rated load current and rotor speeds of 1000 rpm and 1500 rpm are shown in Figure 23, respectively. As can be seen, the current distortions of the proposed method increase with increasing rotor speed, similar to the traditional six-step operation. However, the proposed method not only eliminates the peak CMV of $+V_{dc}/2$ or $-V_{dc}/2$, but also reduces the CMV variations between $+V_{dc}/6$ and $-V_{dc}/6$. The experimental results of *a*-phase current, three-phase pole voltage, and CMV when load torque is changed are shown in Figure 24. As can be seen, the proposed method completely eliminates the peak CMV of $+V_{dc}/2$ or $-V_{dc}/2$ even at the load torque variations. Figure 25 shows a comparison of the current THD of i_a between the MRSPWM and proposed method depending on the rotor speed. The current THDs of the proposed method are lower than these of the MRSPWM over the entire rotor speed range; in particular, the proposed method reduces the current THD by up to 4.87% at 1200 rpm, compared with the MRSPWM.



Figure 22. Experimental results of *a*-phase current, three-phase pole voltage, and CMV at rated load current and rotor speed of 1500 rpm.



Figure 23. Experimental results of three-phase current at rated load current: (**a**) At rotor speed of 1000 rpm; (**b**) At rotor speed of 1500 rpm.



Figure 24. Experimental results at load torque variations: (**a**) Increase of load torque; (**b**) Decrease of load torque.



Figure 25. Comparison of current THD between MRSPWM and proposed method.

6. Conclusions

This study proposes an advanced SVM method of an H8 inverter for PMSM drives to reduce current distortions and CMCs over a wide MI range. In a modulation sequence, the proposed method selects the voltage vector with the same CMV level based on the vector diagram divided into 12 sectors. In addition, the appropriate operation of the seriesconnected switches of the H8 inverter, considering the dead-time interval, is proposed. The proposed method not only completely eliminates the peak CMV of $+V_{dc}/2$ or $-V_{dc}/2$, but also restricts the CMV variations between $+V_{dc}/6$ and $-V_{dc}/6$ into six times at a low MI. At a high MI, the proposed method maintains the modulation manner of the odd or even vector combination, but a two-sampling period-based vector synthesis method is adopted to improve current THDs. Because the modulated voltage vector follows the suburbs of the RSPWM area with increasing MI, the proposed method allows a natural transition into a six-step operation. The performance of the proposed method may be a good solution for reducing both current THD and CMC in the PMSM drive systems where a wide modulation range is required. Author Contributions: Conceptualization, W.-S.J.; methodology, W.-S.J., Y.-S.L. and J.-H.L.; software, W.-S.J.; validation, W.-S.J. and Y.-S.L.; formal analysis, W.-S.J.; investigation, W.-S.J., Y.-S.L. and J.-H.L.; resources, C.-H.L.; data curation, W.-S.J. and Y.-S.L.; writing—original draft preparation, W.-S.J. and Y.-S.L.; writing—review and editing, W.-S.J. and Y.-S.L.; visualization, W.-S.J.; supervision, C.-Y.W.; funding acquisition, C.-H.L. and C.-Y.W.. All authors have read and agreed to the published version of the manuscript.

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