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Novel Single-Phase Grid-Tied NPC Five-Level Converter with an Inherent DC-Link Voltage Balancing Strategy for Power Quality Improvement

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Abstract: This paper presents a novel single-phase grid-tied neutral-point-clamped (NPC) five-level converter (SPFLC). Unlike the literature on five-level NPC topologies, the proposed one is capable of inherently balancing the voltage of the DC-link split capacitors. For this purpose, a simple Multicarrier Phase Disposition (MPD) Pulse Width Modulation (PWM) technique is used, thus avoiding both complex modifications to the Space Vector Modulation (SVM) and offset voltage injections into the carrier based (CB) PWM, as commonly done in most conventional balancing algorithms. Bearing in mind that the proposed balancing strategy only requires measuring the capacitors' voltages and the sign of the converter output current, it has a very low complexity. The developed strategy is not only straightforwardly implemented but is also very effective for obtaining symmetrical and undistorted voltage levels from the proposed multilevel converter, as well as for significantly improving the power quality of the SPFLC output voltage and, in turn, of the grid current. The simulation results obtained with MATLAB-SimPowerSystems as well as the experimental results obtained with the prototype built in the laboratory validate the topology of the proposed NPC five-level converter and the voltage balancing strategy, by showing a good performance under step-changes and exhaustive operating test conditions.

Keywords: single-phase multilevel converter; NPC topology; grid-tied; capacitor voltage balancing; vector control; power quality

Citation: Lara, J.; Masisi, L.; Hernandez, C.; Arjona, M.A.; Chandra, A. Novel Single-Phase Grid-Tied NPC Five-Level Converter with an Inherent DC-Link Voltage Balancing Strategy for Power Quality Improvement. *Energies* **2021**, *14*, 2644. https://doi.org/10.3390/en14092644

Academic Editor: Ramkrishan Maheshwari

Received: 24 March 2021
Accepted: 19 April 2021
Published: 5 May 2021

1. Introduction

Voltage source converters (VSCs) are the core of modern power electronics, which allow modifying the frequency, magnitude and phase of the input voltage with the aim of plant controlling or for electric energy flow regulation purposes. The multilevel VSCs (MC) require more complex modulation techniques than conventional two-level converters. However, they present several advantages such as lower total harmonic distortion (THD) of the output waveform, lower dv/dt stress of the power devices and lower electromagnetic interference (EMI) [1,2]. They can also achieve a high control performance with lower switching frequencies, which represent a significant reduction of the volume and cost of the required output passive filter, as well as lower losses equivalent to an overall higher efficiency [3].

Over the past years, various topologies of MC have been proposed, e.g., NPC [4–6] flying capacitor (FC) [7] and cascaded H-bridge (CHB) [8]. The NPC type is very attractive because all its output voltage levels are obtained from a single DC source, whereas the CHB topology has the drawback of requiring an isolated DC source per cell [9]. In contrast

with FC, NPC does not have a limitation for operating at low switching frequencies and does not need precharging of the capacitors. Nevertheless, the NPC topology requires special techniques for compensating the inherent DC-link split capacitors' unbalancing problem [10–12]. In single-phase five-level NPC converters, this issue can be avoided by using two isolated DC voltage sources instead of capacitors, but such a solution requires more components, which implies a higher cost and a bigger system complexity [13,14].

The simplified bridge five-level NPC topology (SBFLC) [15], hereinafter named conventional topology, consists of two legs; the first leg comes from a two-level converter and the second one from a three-level NPC converter [16,17]. This simplification advantageously reduces the number of components, but inconveniently eliminates the switching combinations of the redundant vectors, thus becoming incapable of compensating the inevitable voltage unbalancing phenomenon. Its effect can be reduced by fairly increasing the capacitance of the DC-link split capacitors, but at the expense of their larger size and cost [18].

Unlike the SBFLC topology, the full-bridge five-level NPC topology (FBFLC) is capable of balancing the split capacitors' voltage [19,20]. For such purpose, different methods have been developed. In [21], the balancing strategy is based on injecting an offset voltage (OVI) into the carrier-based PWM, whereas [22] adopts a modified SVPWM algorithm and [23] utilizes an SVPWM segment-based modulation strategy. With the same aim, some other algorithms have been proposed, e.g., a nonlinear control technique [24], a neutral point current prediction [25] or varying the hybrid discontinuous PWM ratio with a PI controller [26].

In the present work, the authors propose a novel single-phase NPC five-level converter (SPFLC) based on a topology capable of inherently balancing the voltage of the DC-link split capacitors. Unlike [21,22], the proposed balancing strategy does not require either modifying the SVM or injecting offset voltages into the CBPWM; it uses a simple MPDPWM modulation technique [27,28], thus properly merging simplicity with functionality. Furthermore, given that the proposed balancing technique only requires measuring the capacitors' voltages and the sign of the converter output current for selecting the appropriate compensating switching vector from a Look-Up Table (LUT), it has a much lower complexity than all of the strategies presented in [20–26]. It is also important to remark that, in contrast with [23], the appropriate switching vector selected for carrying out the balancing compensation remains the same during the whole switching period T_{sw}.

The developed balancing strategy not only is straightforwardly implemented; it is also very effective for significantly improving the power quality of the proposed NPC multilevel converter output voltage and, in turn, of the grid current.

This paper is organized as follows: Section 2 describes the topology details of the proposed SPFLC, its current flowing paths for all switching states as well as the voltage balancing strategy of the DC-link split capacitors. Section 3 presents the vector control in the dq reference frame of the proposed grid-tied SPFLC. Section 4 shows the simulation results obtained with MATLAB-SimPowerSystems, whereas the experimental results obtained in laboratory, including a detailed power quality analysis are presented in Section 5. Section 6 provides the discussion and future research directions. Finally, the conclusions and some important remarks are given in Section 7.

2. Proposed Single-Phase NPC Five-Level Converter

Figure 1 shows three different topologies of single-phase NPC five-level converters, i.e., the conventional simplified-bridge (SB), the full-bridge (FB) and the proposed one. It can be noted that the conventional topology consists of six switches, two neutral clamping diodes and two DC-link split capacitors, whereas the proposed topology has, in addition to these components, two more switches, i.e., it has a total of eight. However, with these two extra switches, the proposed converter advantageously becomes capable of inherently balancing the capacitors' voltage. In contrast with the FBFLC, the proposed converter has two less clamping diodes and its balancing strategy does not require neither modifying

the SVM or the CBPWM; nor does it depend on compensation closed loops or gain tuning. Table 1 shows a comparison of the three topologies in terms of the number of components and the voltage balancing characteristics.

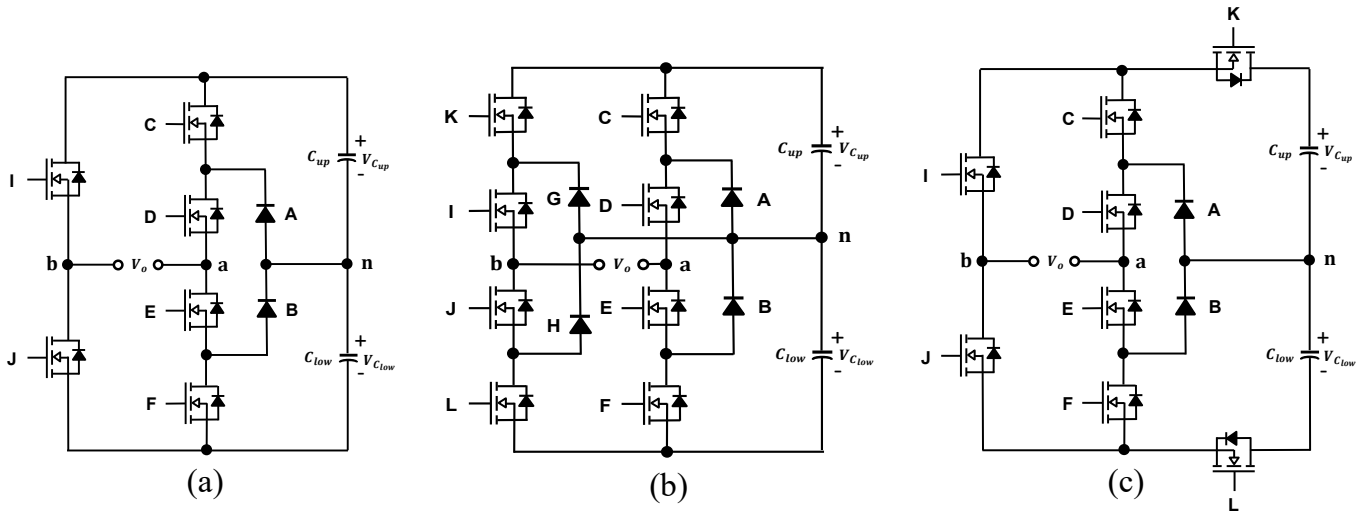

Figure 1. Single-phase NPC five-level converters; (**a**) conventional simplified-bridge topology [15–18], (**b**) full-bridge topology [20–26], and (**c**) proposed topology.

Table 1. Comparison of five-level NPC converters.

Feature	Number Of Components				Voltage Balancing	
Fl Npc Topology	**Capacitors**	**Switches**	**Diodes**	**Total**	**Capability**	**Complexity**
Simplified-Bridge (SB) [15–18]	2	6	2	8	NO	-
Full-Bridge (FB) [20–26]	2	8	4	12	YES	HIGH
Proposed	2	8	2	10	YES	LOW

On the other hand, for example, in the SB topology, only three switches stand with either half or even full DC bus voltage; this issue represents a serious inconvenience of the power devices' stress. Unlike this conventional topology [15–18] and the FB topology [20–26], the proposed one has an equivalent of four and six switches at each leg, respectively. According to the switching state, the full DC bus voltage is shared among five switches, whereas half of the DC bus voltage is shared among either four or at least three switches, depending on the active state for the voltage balancing purposes. It is important to remark that this feature inherently represents the advantage of having a lower stress on the switching devices, thus making more feasible the use of MOSFETs instead of IGBTs. The MOSFETs for high power applications are not only less costly than IGBTs but are also capable of working at higher frequencies and more efficiently [10].

Current Flowing Paths of Proposed SPFLC and Voltage Balancing Strategy of DC-Link Split Capacitors

Figure 2 shows the current flowing paths for the seven switching states of the proposed single-phase five-level converter. The state of the eight switches at each switching state, the resulting output as a function of the DC-link voltage as well as the voltage balancing strategy are summarized in Table 2. According to the power electronic circuits of Figure 2b,h, it can be observed that in the respective states 1 and 5, the neutral point n remains disconnected from the midpoint path of the clamping diodes, thus leaving C_{up} and C_{low} alone in series. Given that the same current flows through them, both are equally

charged/discharged and thus, in such cases, there is no voltage unbalance problem. In state 3 (Figure 2e), there is no current path with any of the capacitors, therefore, their initial voltages are kept the same and no charge/discharge occurs. For each of the remaining states, i.e., 2 U (Figure 2c), 2 L (Figure 2d), 4 U (Figure 2f) and 4 L (Figure 2g), there exists a current path that involves only one of the two capacitors. Given that it will be charged/discharged while the other one stays disconnected and keeps the same initial voltage, an unbalance arises between them. By taking into account the sign of the SPFLC output current i_{FLC} as well as the capacitors' unbalance voltage V defined as $V_{C_{up}} - V_{C_{low}}$ it is possible to maintain the voltage of both capacitors very close to each other. As described in Table 2, if the balancing algorithm is activated during the $+V_{dc}/2$ output voltage and $V \geq 0$ and $i_{FLC} \geq 0$, then the switching state 2 U has to be applied to the eight switches S_1, $S_2 \ldots S_8$, whereas if the balancing algorithm is deactivated or well-activated (it does not matter), but with a combination of V and i_{FLC} that is not greater than or equal to zero, then the switching state 2 L has to be selected. Similarly, for carrying out the voltage balancing during the $-V_{dc}/2$ output voltage, the algorithm chooses between the switching states 4 U and 4 L according to its activation/deactivation and also considering the conditions in which $V < 0$ and $i_{FLC} < 0$. By following Table 2, the proposed voltage balancing strategy for the split capacitors is capable of properly keeping the average neutral current around zero, even under step-changing conditions. Note that with the aim of contributing to reduce the switching losses during the voltage balancing, S_7 remains on in states 2 U/2 L, whereas S_8 remains on in states 4 U/4 L, respectively. Besides, irrespective of whether the balancing algorithm is active or not, both of these switches are always on in state 3.

Table 2. Switching states and voltage balancing strategy for the proposed five-level converter.

Switching State	State of Switches								Flc Output Voltage (V_{FLC})	Voltage Balancing Algorithm Activated	Capacitors Unbalance Voltage (ΔV)	Flc Output Current Sign (i_{FLC})
	S_1	S_3	S_5	S_7	S_2	S_4	S_6	S_8				
1	**0**	**1**	**1**	**1**	**1**	**0**	**0**	**1**	$+V_{dc}$			
2U	**0**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	$+V_{dc}$**/2**	**YES**	+	+
2L	**0**	**0**	**1**	**1**	**1**	**1**	**0**	**1**		**NO/YES**	**OTHERWISE**	
3	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**0**			
4U	**1**	**0**	**1**	**1**	**0**	**1**	**0**	**1**	$-V_{dc}$**/2**	**NO/YES**	**OTHERWISE**	
4L	**1**	**0**	**0**	**0**	**0**	**1**	**1**	**1**		**YES**	−	−
5	**1**	**0**	**0**	**1**	**0**	**1**	**1**	**1**	$-V_{dc}$			

Figure 3 shows the signals of the Multicarrier Phase Disposition PWM modulation strategy [27,28]. The reference or modulating signal and the triangular carrier signals, as well as the switching pattern and the resulting output voltage from the proposed SPFLC can be observed. This graph was obtained with the voltage balancing algorithm deactivated ($S_7 = S_8 = 1$) and without current flow.

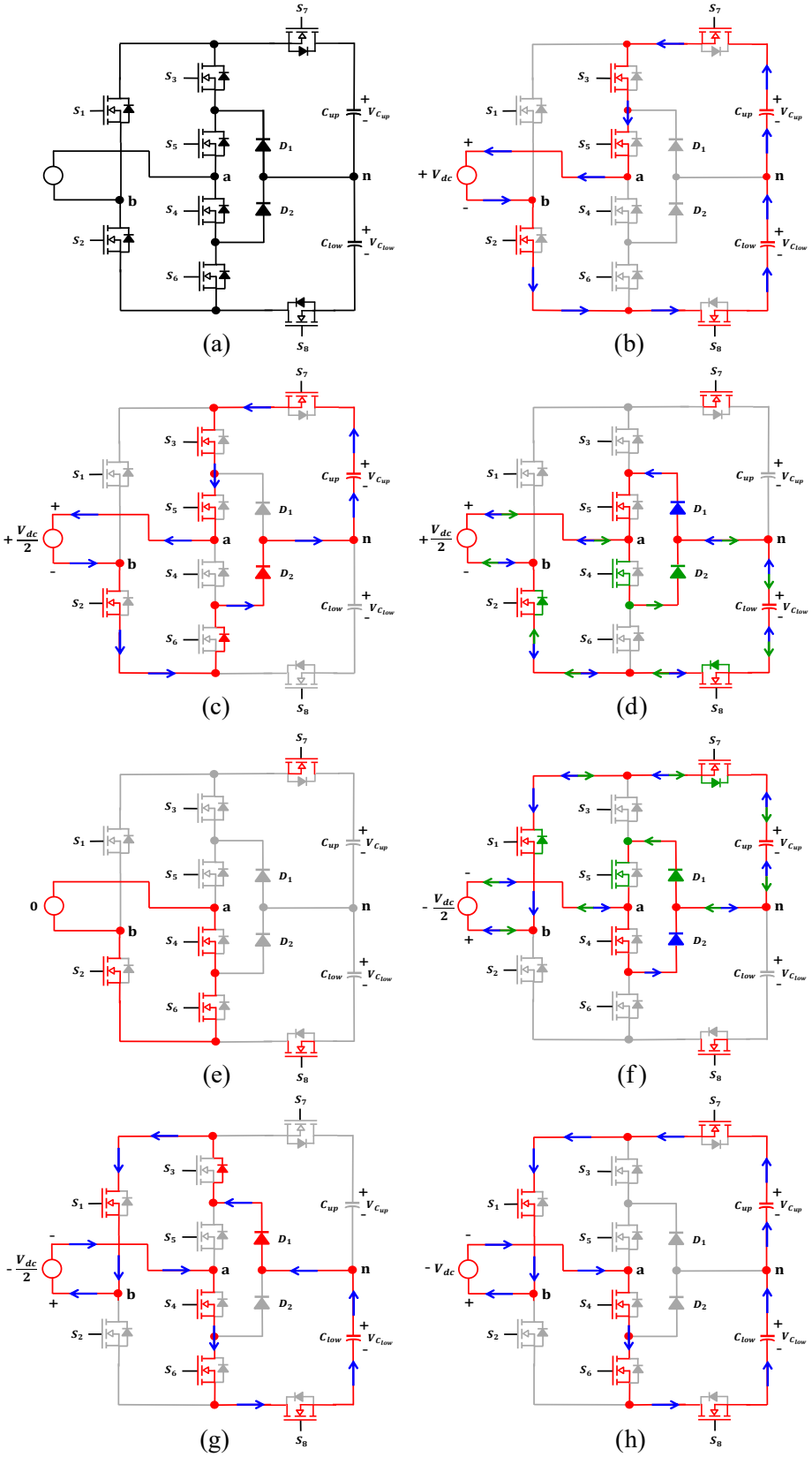

Figure 2. Current flowing paths for the seven switching states of the proposed SPFLC; (**a**) proposed topology; (**b**) State 1 $[+V_{dc}]$; (**c**) State 2 U $[+V_{dc}/2]$ from upper capacitor; (**d**) State 2 L $[+V_{dc}/2]$ from lower capacitor, (**e**) state 3 [0]; (**f**) state 4 U $[-V_{dc}/2]$ from upper capacitor; (**g**) state 4 L $[-V_{dc}/2]$ from lower capacitor; and (**h**) state 5 $[-V_{dc}]$.

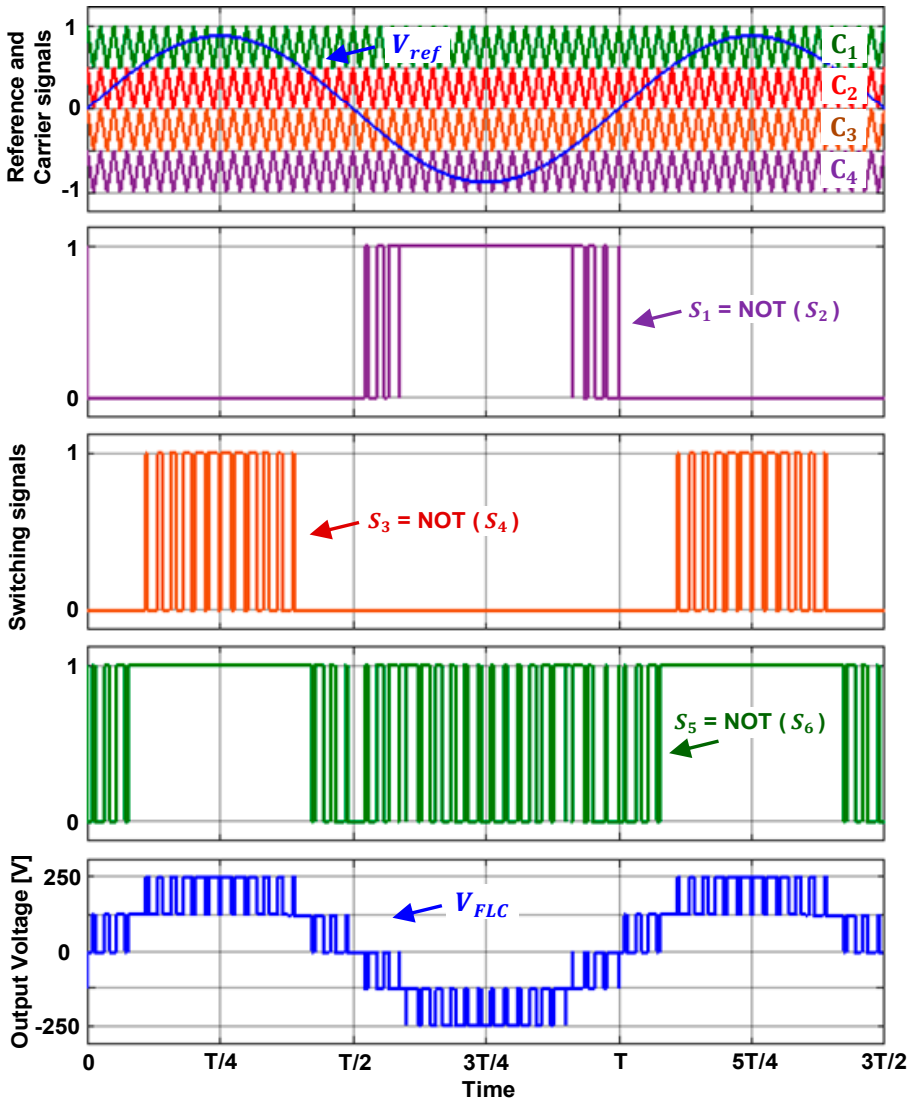

Figure 3. MPDPWM modulation strategy: reference and carrier signals, switching pattern and the resulting output voltage from the proposed SPFLC.

3. Vector Control of Proposed Grid-Tied SPFLC

Figure 4 shows the block diagram of the implemented current vector control strategy in the *dq* rotating coordinates for the proposed single-phase five-level converter connected to the grid through an *RL* line. It can be noted that the voltage component is the only control signal fed into the MPDPWM block, whereas the β component is simply disregarded [29]. Considering the equivalent three-phase representation from the one-line single-phase power system shown in Figure 4 and applying the Kirchhoff voltage law to the resulting circuit, the following equation in the *abc* stationary frame is obtained [29]:

$$L_L \frac{di_{abc}}{dt} + R_L i_{abc} + V_{FLC_{abc}} - V_{g_{abc}} = 0 \quad (1)$$

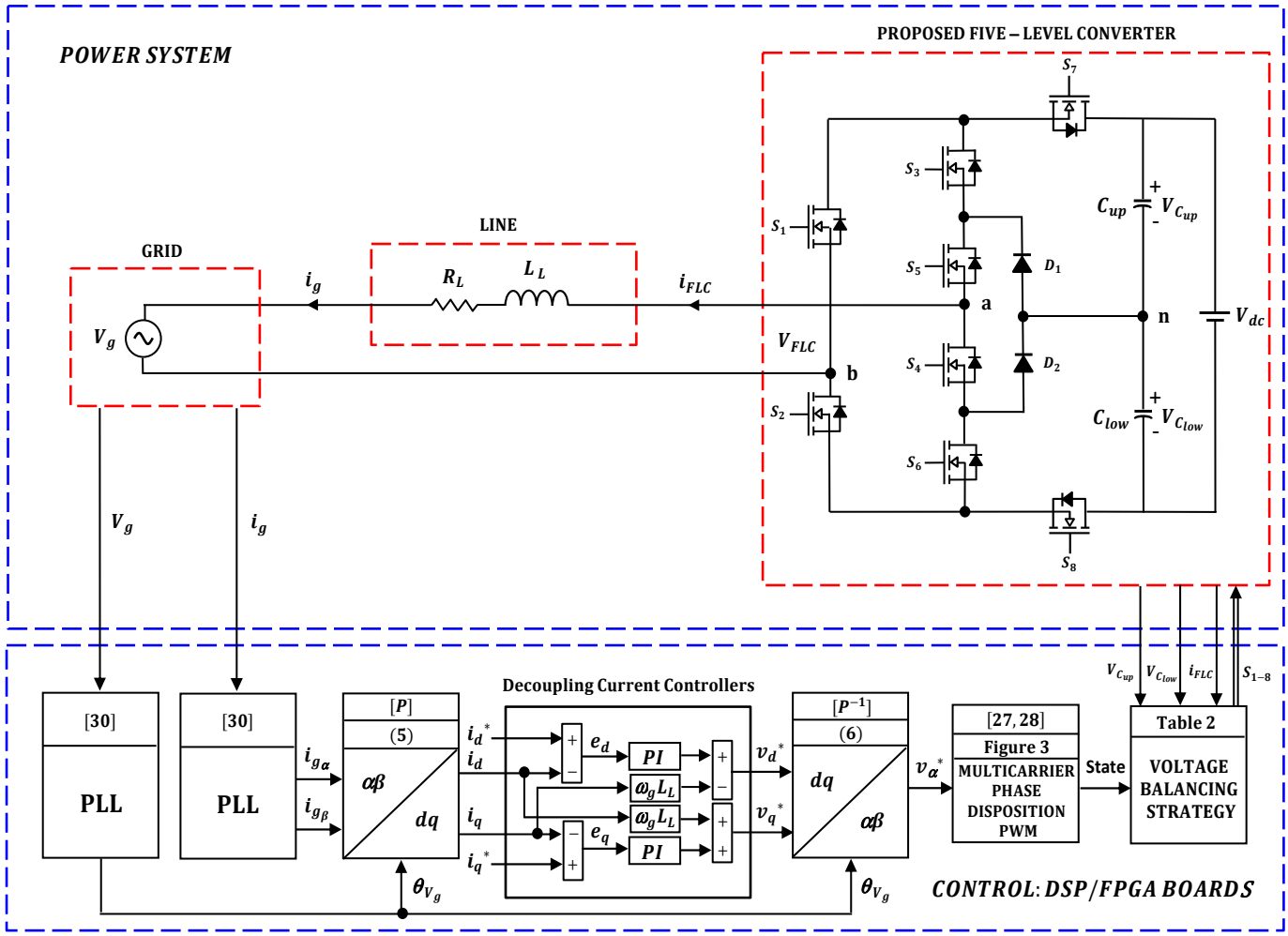

Figure 4. Block diagram of the proposed grid-tied SPFLC and its current vector control in the dq rotating coordinates.

In turn, the direct Clarke transformation allows representing (1) in the two phases of $\alpha\beta$ stationary frame as:

$$L_L \frac{di_{\alpha\beta}}{dt} + R_L i_{\alpha\beta} + V_{FLC_{\alpha\beta}} - V_{g_{\alpha\beta}} = 0 \tag{2}$$

where the three- and two-phase grid current vectors are $i_{abc} = [i_a\ i_b\ i_c]^T$ and $i_{\alpha\beta} = [i_\alpha\ i_\beta]^T$, respectively. After applying the direct Park transform (5) to (2), the expanded equations in the dq rotating reference frame are given by [29]:

$$L_L \frac{di_d}{dt} + R_L i_d - \omega_g L_L i_q + V_{FLC_d} - V_{g_d} = 0 \tag{3}$$

$$L_L \frac{di_q}{dt} + R_L i_q + {}_g L_L i_d + V_{FLC_q} - V_{g_q} = 0 \tag{4}$$

In order to decouple the d- and q-axis current controllers, the resulting coupling factors $\omega_g L_L i_q$ and $-\omega_g L_L i_d$ have to be subtracted in the control loops, as shown in Figure 4. The simulation results presented in Section 4 have been obtained with $k_p = 20$ and $k_i = 80$ for both d and q loops, whereas the experimental results presented in Section 5 have been obtained with $k_p = 3$ and $k_i = 125$, respectively. The details about the design procedure of the linear PI controllers, considering the current control loops and the resulting transfer functions, can be found in [29]. The vector control of the single-phase grid current is based on the space vector diagram shown in Figure 5.

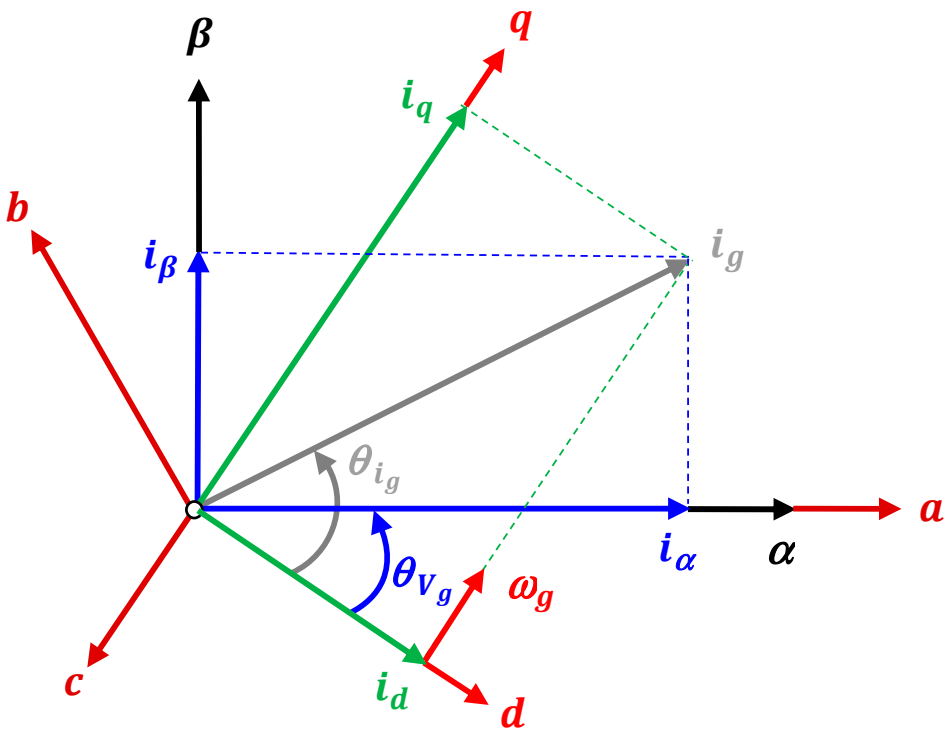

Figure 5. Space vector diagram of the stationary $abc/\alpha\beta$ reference frames and the rotating dq coordinates.

Besides, the direct P and inverse P^{-1} Park matrices used for transforming between the stationary coordinates $\alpha\beta$ and the rotating coordinates dq are defined as follows.

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = [P]\left[i_{\alpha\beta}\right] = \begin{bmatrix} cos(\theta_{Vg}) & -sin(\theta_{Vg}) \\ sin(\theta_{Vg}) & cos(\theta_{Vg}) \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{5}$$

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \left[P^{-1}\right]\left[i_{dq}\right] = \begin{bmatrix} cos(\theta_{Vg}) & sin(\theta_{Vg}) \\ -sin(\theta_{Vg}) & cos(\theta_{Vg}) \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{6}$$

where the product of these transformation matrices satisfies the property of giving the identity matrix I as

$$[P]\left[P^{-1}\right] = \left[P^{-1}\right][P] = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} = [I] \tag{7}$$

The grid voltage phase θ_{V_g} used in Park transforms and the beta grid current component i_{g_β} have been obtained by using the PLL, developed by Ziarani et al. [30].

4. Simulation Results

In order to validate the proposed grid-tied SPFLC, it was simulated in MATLAB-SimPowerSystems. Figures 6–10 show the results obtained from different tests under various operating conditions.

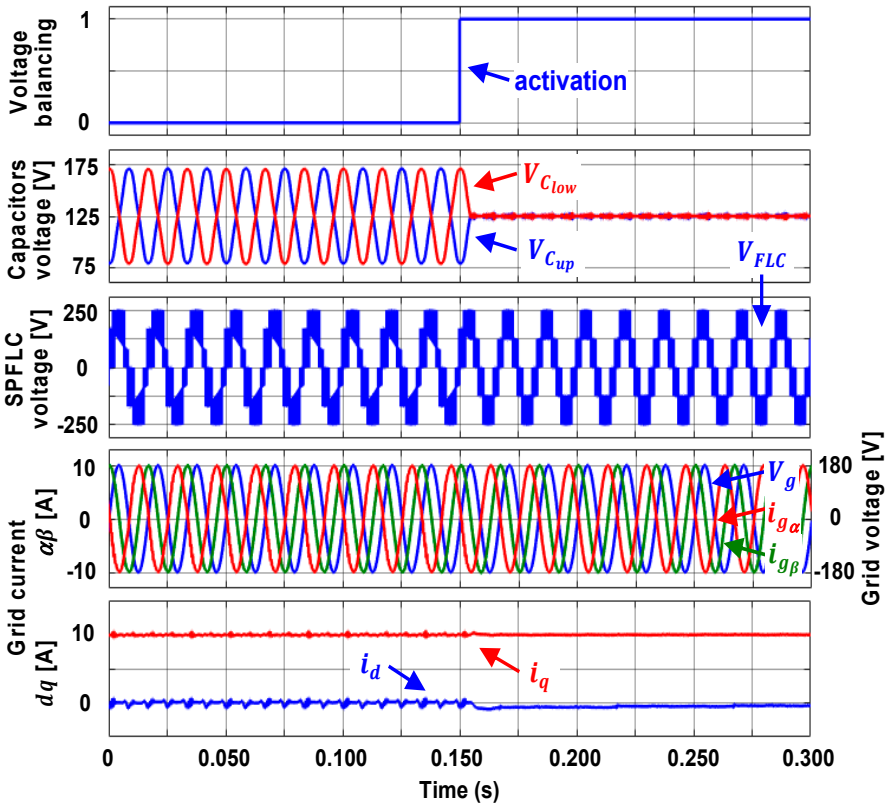

Figure 6. Performance of the voltage balancing strategy and the vector control for the proposed grid-tied SPFLC during steady state of the dq grid currents.

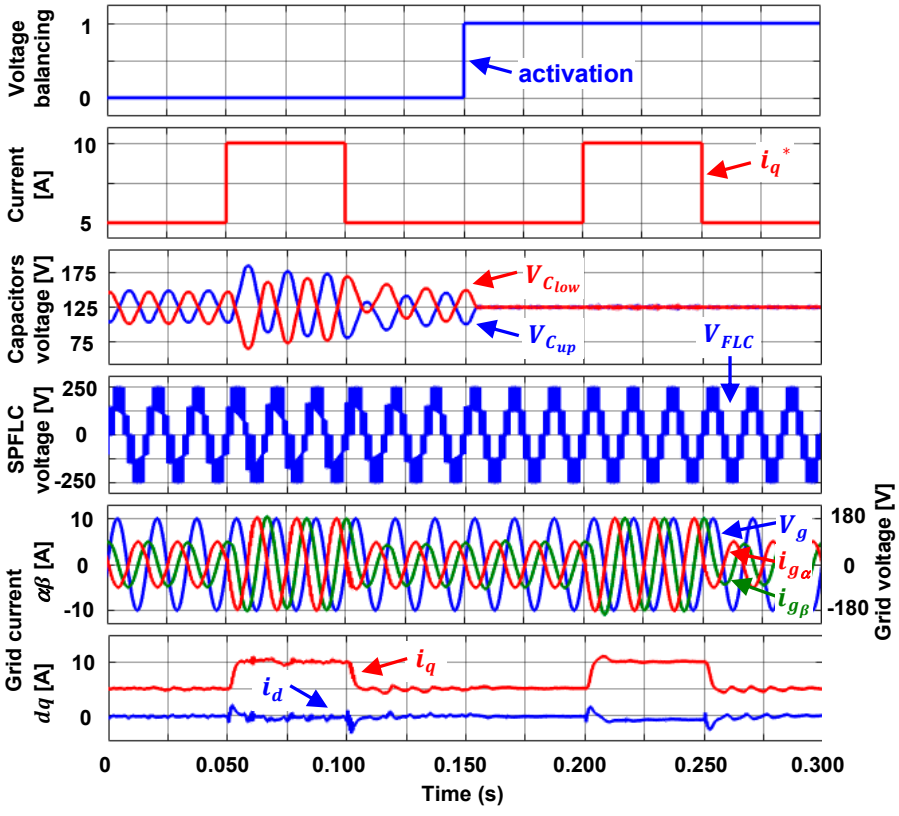

Figure 7. Performance of the voltage balancing strategy and the vector control for the proposed grid-tied SPFLC during a step-change in the q axis grid current.

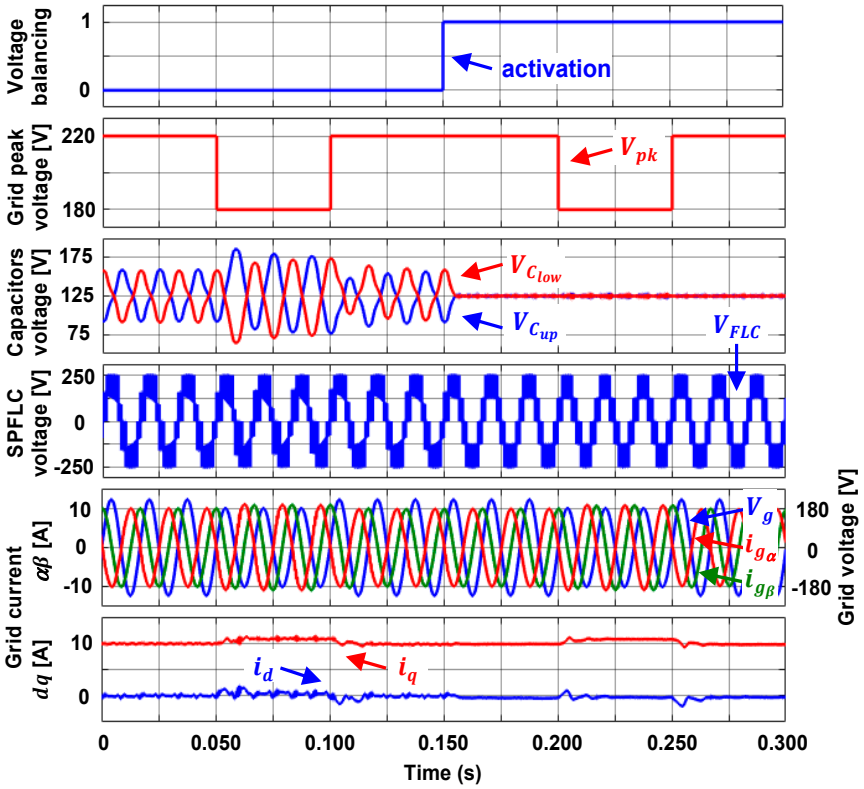

Figure 8. Performance of the voltage balancing strategy and the vector control for the proposed grid-tied SPFLC during a grid voltage sag/swell.

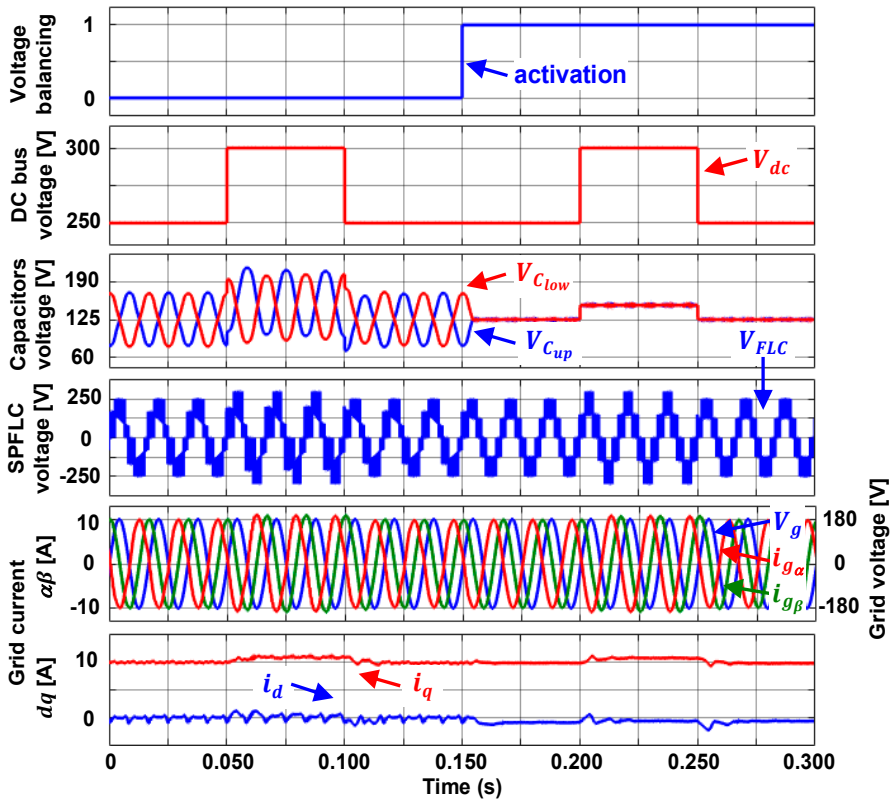

Figure 9. Performance of the voltage balancing strategy and the vector control for the proposed grid-tied SPFLC during a DC bus voltage step-change.

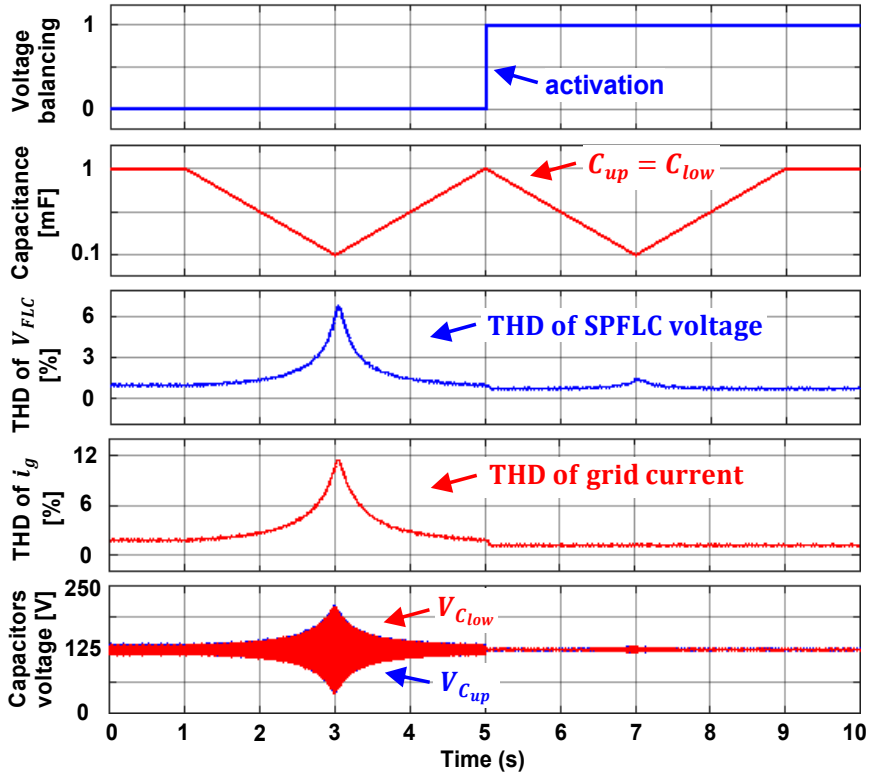

Figure 10. Dynamic response of the voltage balancing strategy and the vector control for the proposed grid-tied SPFLC during a sweep of the capacitance of the DC-link split capacitors.

In Figure 6, the response of the grid current control as well as of the strategy for balancing the voltage of the DC-link split capacitors in the proposed five-level converter, during steady state of the dq grid currents, can be observed. It is noteworthy how from half the time scale, i.e., t = 0.15 ns, when the voltage balancing is activated, the voltage unbalance of capacitors is fairly well compensated. In a very short-time, lower than 5 ms, the voltage of both capacitors practically achieves an overlapping at the constant level of $V_{dc}/2$. Note also how the negative slope at state 2 and the positive slope at state 4 of the SPFLC output voltage are properly corrected in a similar way, thus becoming a symmetrical and high-quality waveform. Figure 6 further shows the good performance of Ziarani's PLL for deriving the grid current β component and, in turn, of the resulting vector control for duly regulating the direct i_d and quadrature i_q currents to zero and 10 A, respectively. It is important to remark how the component i_{g_β} properly lags the i_{g_α} grid current by 90°, while it is accurately maintained out-of-phase with the grid voltage V_g. During this test, the capacitance of the upper and lower DC-link split capacitors has remained constant at $C_{up} = C_{low}$ = 200 μF.

Figure 7 shows the performance of the voltage balancing strategy and the vector control technique for the proposed grid-tied SPFLC during a step-change of the quadrature grid current component $i_q{}^*$ from 5 A to 10 A and then returned back to 5 A. Thanks to the decoupling of the dq current loops, the d axis current component properly remains at zero during all the simulation time, in spite of the step-changes carried out in the q axis. It can be observed how the voltage unbalance of the DC-link split capacitors increases with i_q. However, it is quite well-compensated after the activation of the balancing strategy at t = 0.15 s.

Figure 8 shows the performance of the voltage balancing strategy and the vector control for the proposed SPFLC during a grid voltage sag/swell. In this test, the peak value V_{pk} of the grid voltage was step-changed from 220 V to 180 V, thus representing a sag of 18%. After 50 ms, V_{pk} is returned back to 220 V, equivalent to a swell of around 22%. It can be observed that the voltage unbalance is inversely proportional with V_{pk}. However,

thanks to the balancing strategy activated at t = 0.15 s, the voltage unbalance is fairly well-regulated, thus accurately maintaining the voltage of split capacitors at 125 V from half the time scale. The good performance of the vector control for maintaining a constant and undisturbed grid current component during the step-changes of V_{pk} is noteworthy.

Figure 9 shows the performance of the voltage balancing strategy and the vector control technique for the proposed SPFLC during a DC bus voltage variation. At t = 0.05 s, the magnitude of V_{dc} was step-changed from 250 V to 300 V, thus representing an increment of 20%. Later, at t = 0.1 s, V_{dc} is returned to 250 V, equivalent to a decrement of around 17%. It can be observed that the voltage unbalance increases with V_{dc}. However, the voltage balancing strategy activated at half the time scale is capable of properly regulating the voltage of the split capacitors at $V_{dc}/2$. The negligible influence of the DC bus voltage changes on the dq current components is also noteworthy.

Figure 10 shows the dynamic response of the voltage balancing strategy and the vector control for the proposed grid-tied SPFLC during a sweep of the capacitance C_{up} and C_{low} of the DC-link split capacitors. In this test, $C_{up} = C_{low}$ was varied following a triangular waveform, with peak values of 1 mF and 100 µF. It can be observed how the voltage unbalance as well as the THD of the output voltage V_{FLC} from the SPFLC and, in turn, the THD of the grid current i_g increase nonlinearly with the linear reduction of such capacitance. Therefore, the maximum values of voltage unbalance and harmonic distortion occur at t = 3 s and t = 7 s, i.e., the points of minimum capacitance. It is noteworthy how after the activation of the voltage balancing strategy at half the time scale, i.e., t = 5 s, the voltage unbalance decreases from 125 V $\pm$ 85 V to only 125 V $\pm$ 7 V, whereas the maximum THD of V_{FLC} and i_g reduces from 6.9% and 11.4% to only 1.5% and 1.4%, respectively. This considerable reduction in the harmonic content of V_{FLC} and i_g clearly shows the significant power quality improvement achieved, thanks to the inherent capability of the proposed SPFLC for properly balancing the voltage of DC-link split capacitors. During this test, the direct and quadrature grid current components have been maintained constant at $i_d{}^*$ = 0 and $i_q{}^*$ = 10 A.

5. Experimental Results

In order to validate the voltage balancing strategy, the current vector control technique and the proposed grid-tied SPFLC, they have been implemented and evaluated exhaustively. Figure 11 shows a photo of the experimental setup built in the laboratory, whereas its main parameters are summarized in Table 3.

The proposed five-level converter was built with MOSFETs power switches IRF640, drivers IR2110 and high-speed optocouplers 6N137. The floating sources have been obtained from isolated transformers followed by diode-bridge rectifiers. The voltage and current transducers used in the sensing stage are LV 25-P and CSLA2CD, respectively. The monitoring, processing and control tasks have been performed with the FPGA Spartan-3 and DSP F28335 boards.

Table 3. Parameters of simulation and experimental grid-tied SPFLC.

Parameter	Symbol	Value		Units
		Simulation	Experimental	
Switching frequency	f_{sw}	**5**	**5**	**kHz**
Line resistance	R_L	**0.1**	**0.1**	**Ω**
Line inductance	L_L	**5**	**3**	**mH**
Grid voltage (peak)	V_g	**180**	**15**	**V**
Grid frequency	f	**60**	**60**	**Hz**
DC bus voltage	V_{dc}	**250**	**25**	**V**
Capacitance of split capacitors	C_{up}, C_{low}	**200**	**300**	**µF**
Sampling time/Time-step	T_s	**100**	**100**	**µs**

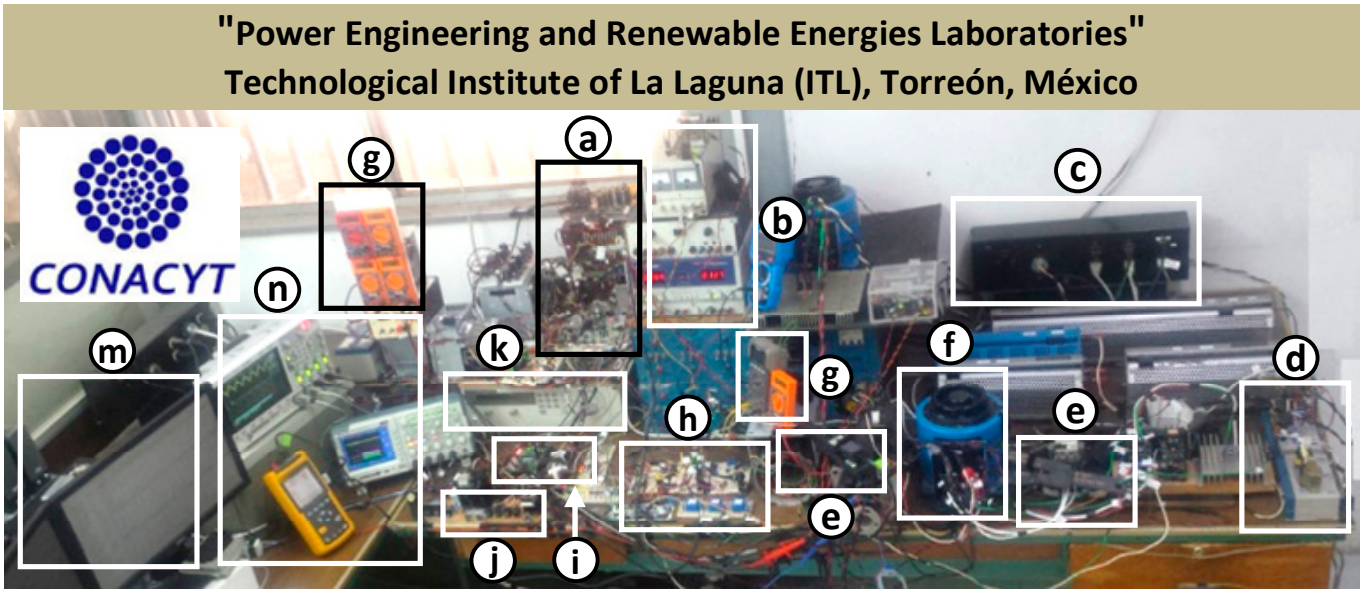

Figure 11. Experimental setup built in the laboratory; (**a**) novel single-phase five-level converter and its drivers; (**b**) auxiliary DC voltage sources; (**c**) grid connectors board; (**d**) line inductor; (**e**) Tektronix Hall current probes; (**f**) grid variable autotransformer; (**g**) multimeters; (**h**) voltage/current Hall sensors and signal conditioning stage; (**i**) DSP/FPGA-based control cards; (**j**) control dashboard; (**k**) Hewlett Packard programmable DC voltage source; (**m**) PC—Windows 10/i7/8 Gb RAM; and (**n**) Tektronix/Agilent digital scopes and Fluke 43B.

The same tests performed in simulation for getting the results of Figures 6–9 were also carried out experimentally. Figures 12–15 show the main waveforms obtained from these tests, i.e., (a) steady state of the dq grid current components with $i_d{}^* = 0$ and $i_q{}^* = 1.8$ A; (b) a step-change in the q axis grid current from zero to 1.8 A and back to zero; (c) a grid voltage sag/swell from 15 V_{pk} to 12 V_{pk} (20%) and back to 15 V_{pk} (25%); and (d) a DC bus voltage step-change from 25 V to 30 V (20%) and back to 25 V (17%). It is remarkable to observe how from half the time scale, when the voltage balancing strategy is activated, the voltage unbalance of split capacitors notably reduces, the asymmetry of the SPFLC output voltage V_{FLC} is properly corrected, the ripple of the direct current component i_d decreases and the distortion of the grid current $i_g = i_{g_\alpha}$ is fairly well-compensated while remaining accurately in quadrature with i_{g_β}; thus, notably enhancing the power quality in the grid-tied SPFLC system. In general, it is noteworthy how the experimental results accurately match the ones from simulation, thus validating the good dynamic and steady-state performance of the proposed grid-tied SPFLC and its voltage balancing strategy. Bearing in mind that, in all of the tests, the reference of the direct grid current component $i_d{}^*$ was set to zero and the electrical energy flowing direction was from the DC voltage source that feeds the bus of the SPFLC to the AC mains; hence, the grid current $i_{g_\alpha} = i_g$ always remains out-of-phase with the grid voltage V_g. The variables $V_{C_{low}}$, $V_{C_{up}}$, V_{FLC}, V_g and i_g shown in Figures 12–15 have been directly measured from the grid-tied SPFLC prototype, whereas the variables i_{g_α}, i_{g_β}, i_d and i_q have been output in real-time from the vector control algorithm embedded within the DSP. For this, PWM pins and analog low-pass filters have been used. Given that the PWM outputs only deal with a positive polarity, their zero reference in the scopes was set as one square per division, i.e., 1 A and 2 A, respectively. All of the measurements were sensed through differential voltage probes and Hall current probes by simultaneously using the four channels of the TPS2024B Tektronix scope as well as the four channels of the MSOX3054A Agilent scope.

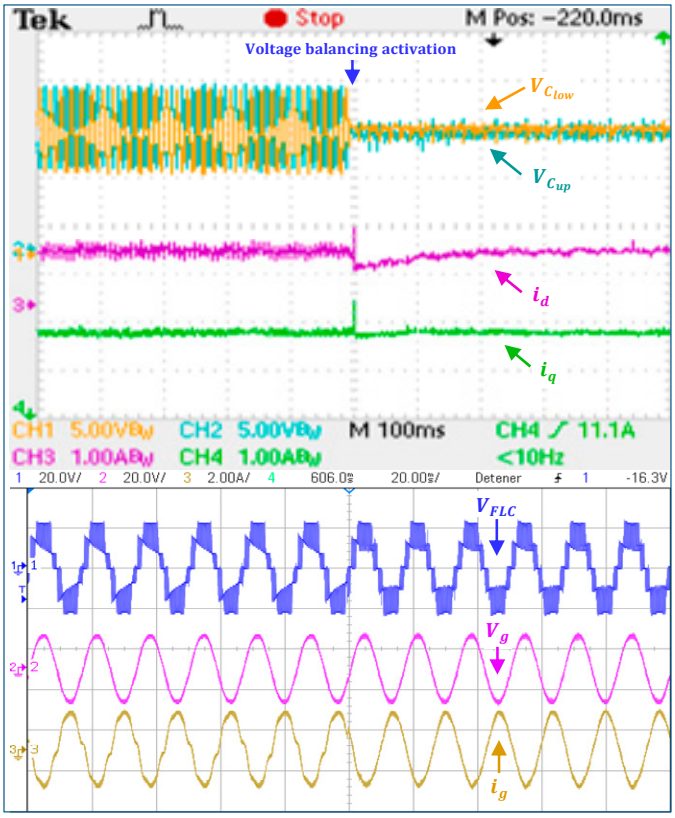

Figure 12. Performance of the voltage balancing strategy and the vector control for the proposed grid-tied SPFLC during steady state of the dq grid currents.

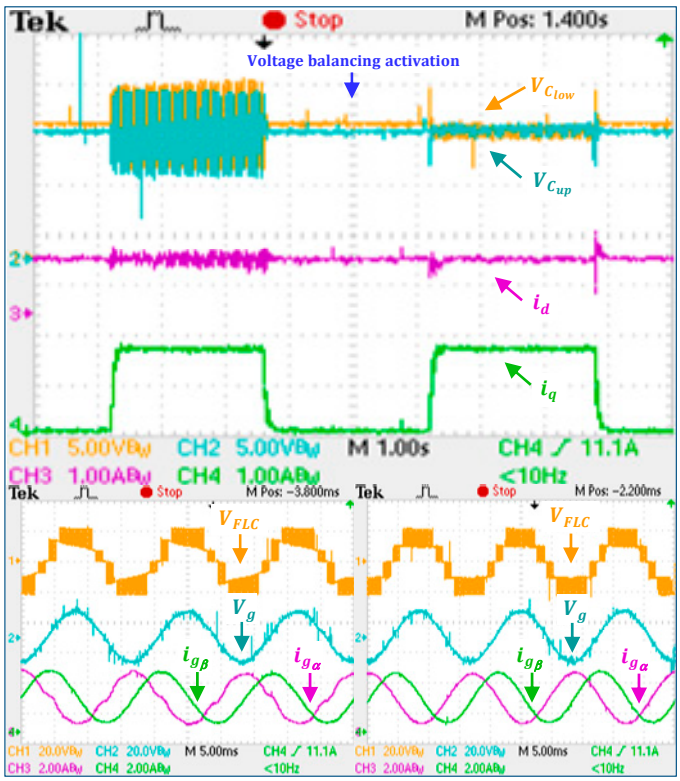

Figure 13. Performance of the voltage balancing strategy and the vector control for the proposed grid-tied SPFLC during a step-change in the q axis grid current.

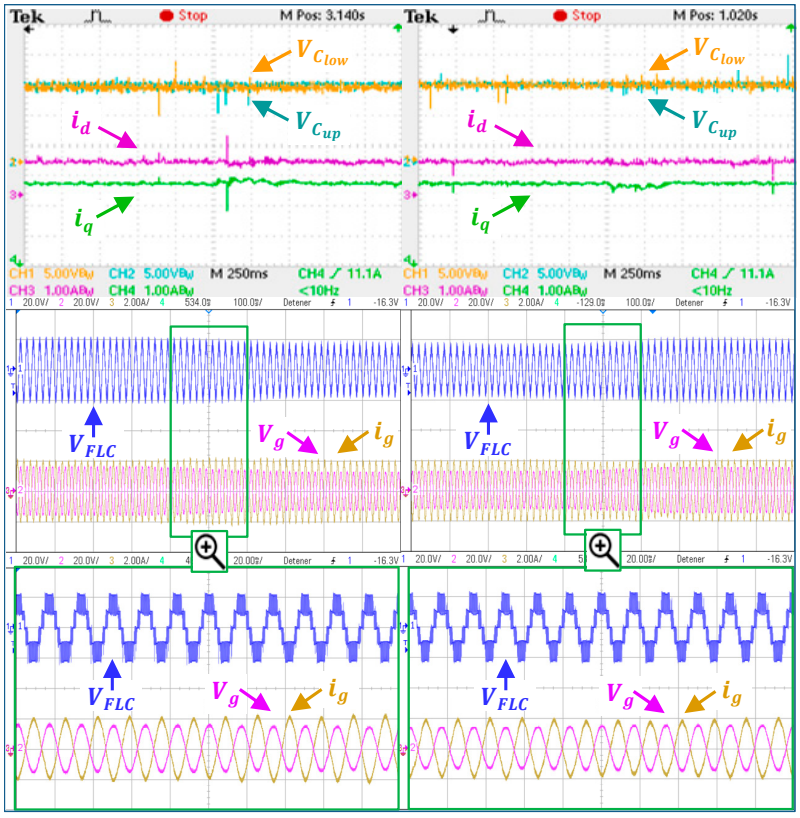

Figure 14. Performance of the voltage balancing strategy and the vector control for the proposed grid-tied SPFLC during a grid voltage sag/swell.

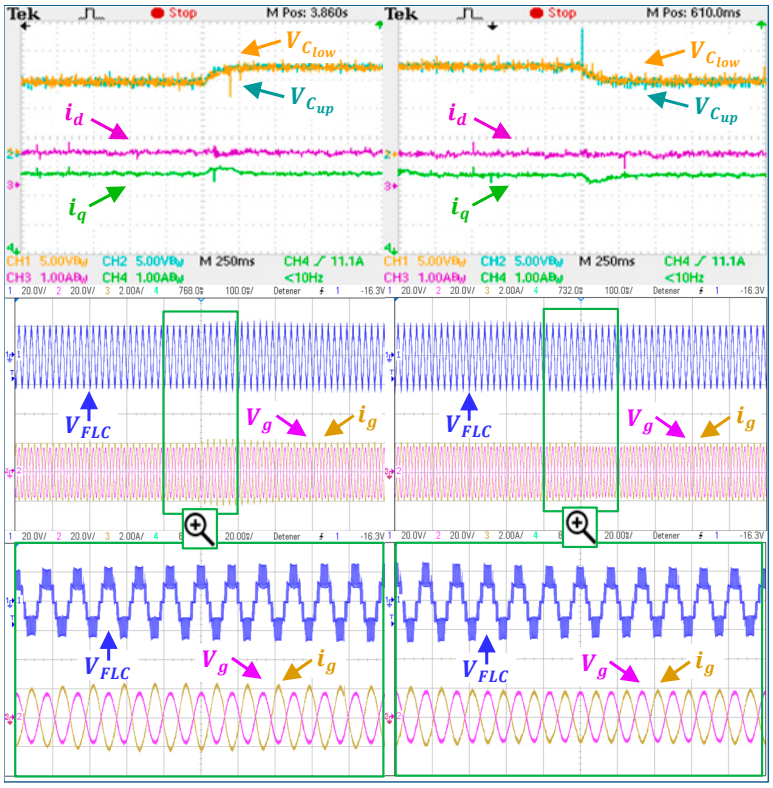

Figure 15. Performance of the voltage balancing strategy and the vector control for the proposed grid-tied SPFLC during a DC bus voltage step-change.

Figures 16 and 17 show the experimental results obtained from the power quality analysis of the SPFLC output voltage V_{FLC} and the grid current i_g both without and with the activation of the DC-link split capacitors voltage balancing strategy. It is noteworthy that when the balancing algorithm is activated, the THD of V_{FLC} and i_g reduces from 6.1% and 10.3% to only 2.7% and 1.9%, respectively. Furthermore, the performance of the vector control for regulating the direct current component i_d to zero alike enhances, thus maintaining i_g more accurately out-of-phase with the grid voltage V_g. Likewise, the balancing strategy also improves the power quality of the proposed grid-tied SPFLC, allowing it to achieve a unity power factor and a reactive power very close to zero, while the resulting grid current notably fulfills the standard *IEEE 519* by maintaining its harmonic content far below the 5% limit.

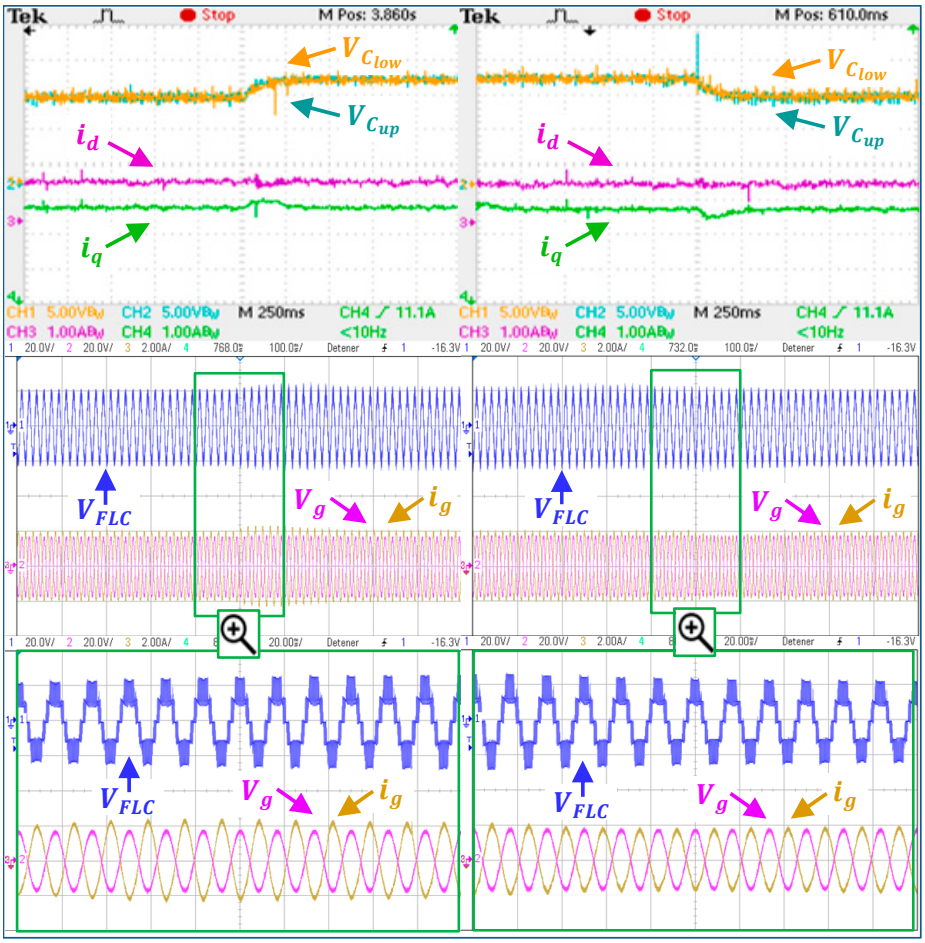

Figure 16. Fluke 43B-based power quality analysis of grid-tied SPFLC waveforms without the activation of the DC-link split capacitors' voltage balancing. (**a**) SPFLC output voltage V_{FLC} and the resulting grid current i_g from the vector control technique; (**b**) grid powers, grid factors, V_g and i_g; (**c**) spectrum of V_{FLC}; and (**d**) spectrum of i_g.

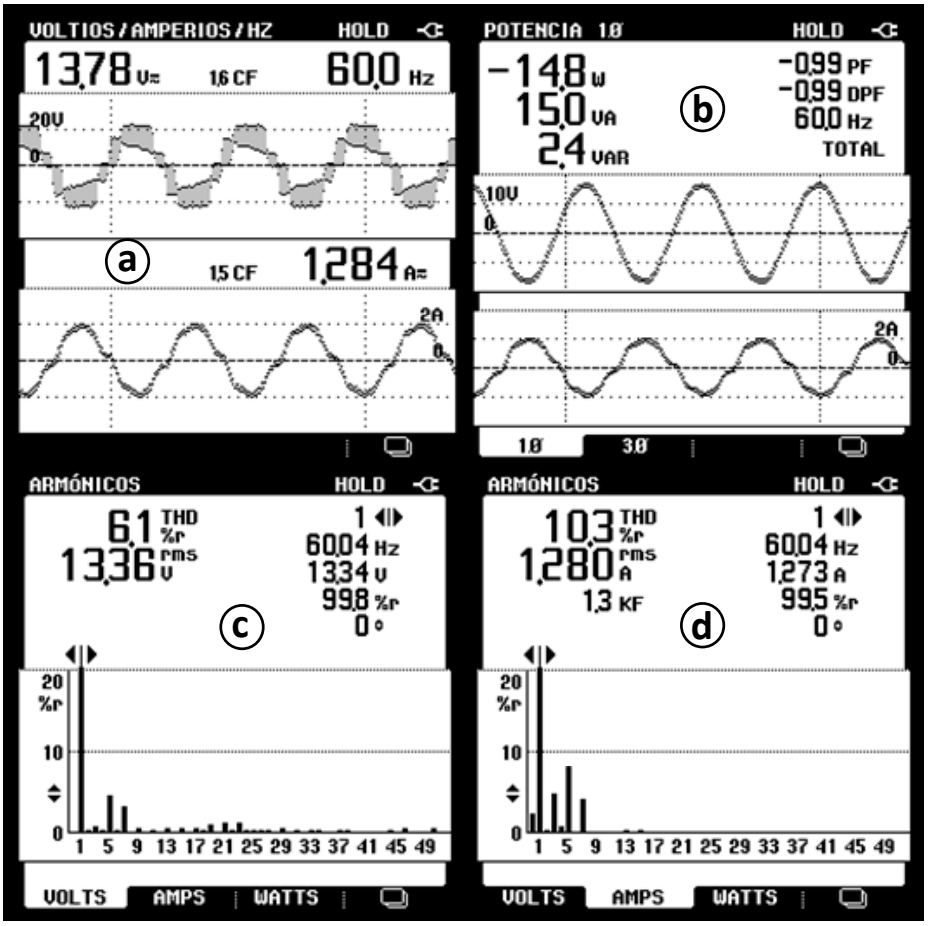

Figure 17. Fluke 43B-based power quality analysis of grid-tied SPFLC waveforms with the activation of the DC-link split capacitors' voltage balancing. (**a**) SPFLC output voltage V_{FLC} and the resulting grid current i_g from the vector control technique; (**b**) grid powers, grid factors, V_g and i_g; (**c**) spectrum of V_{FLC}; and (**d**) spectrum of i_g.

With the aim of properly comparing the three different single-phase NPC five-level converters under study, the power loss distribution and the maximum power transfer efficiency are used as figures of merit.

Figure 18 shows the first figure of merit based on the power losses distribution for three different single-phase five-level NPC converters, both with and without the voltage balancing of the DC-link split capacitors. In order to perform a fair and straightforward comparison, the magnitude of the power losses was normalized by considering all the results at once. Likewise, for ease of analysis, the cells' notation with the letters A–L in Figure 18 matches the description of the power devices within the topologies of Figure 1. The term cell denotes either the set of a switch with its antiparallel free-wheeling diode or a simple neutral clamping diode. Note that the cells G-H are only present in the full-bridge topology [20–26], whereas the cells K-L are only not present in the conventional simplified-bridge topology [15–18].

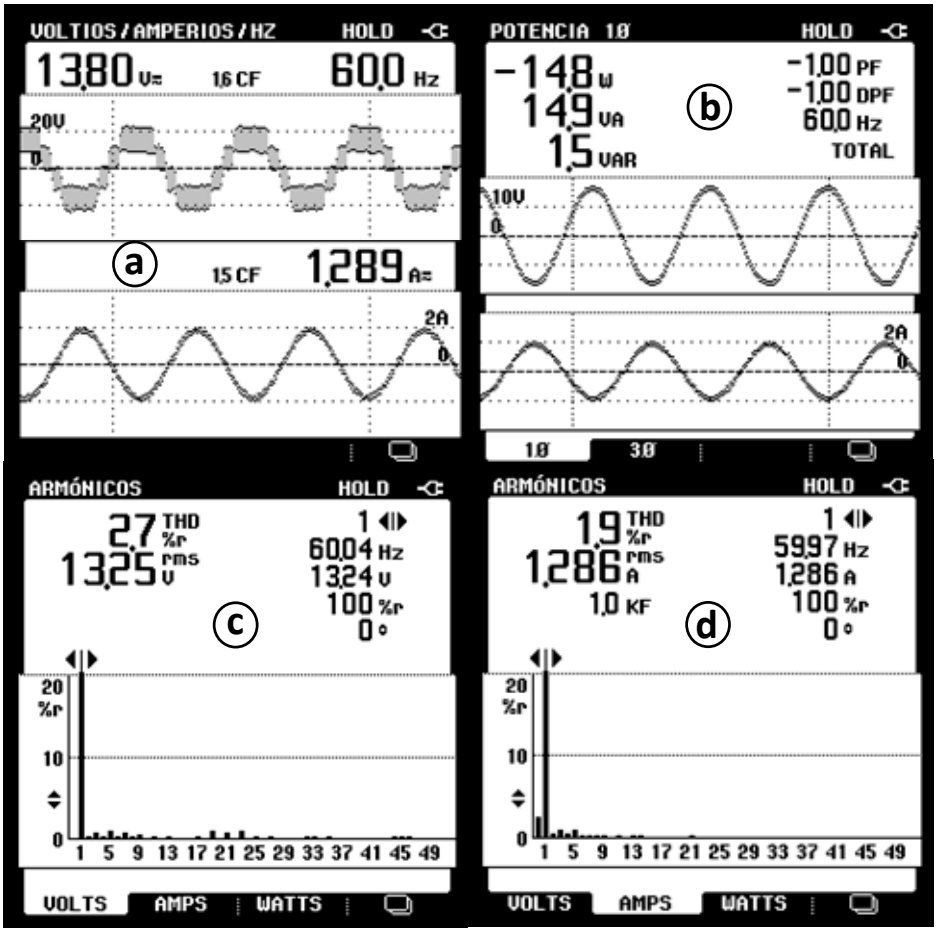

Figure 18. Figure of merit based on the power loss distribution for different five-level NPC converters with and without the voltage balancing of the DC-link split capacitors.

Table 4 shows the second figure of merit based on the maximum power transfer efficiency for three different five-level NPC converters, both with and without the voltage balancing of the DC-link split capacitors. It can be noted that the conventional simplified-bridge topology [15–18], having only six switches, is the most efficient, with 96.11%. Nevertheless, this configuration is inconveniently incapable of balancing the voltage of the split-capacitors. It is also noteworthy that the proposed topology is more efficient than the full-bridge topology [20–26] in both operation modes, i.e., with and without voltage balancing. Although this superiority in efficiency is quite small, the proposed topology also has the advantages of accounting for two less neutral clamping diodes and a voltage balancing strategy with a very low complexity.

Table 4. Figure of merit based on the efficiency of different five-level NPC converters with and without the voltage balancing of the DC-link split capacitors.

Five-Level Npc Converter	Efficiency (%)	
	Without Voltage Balancing	With Voltage Balancing
Simplified-bridge [15–18]	**96.11**	**-**
Full-bridge [20–26]	**95.26**	**95.13**
Proposed	**95.55**	**95.37**

6. Discussion

The experimental results shown in Section 5 properly validated the proposed SPFLC and its inherent DC-link voltage balancing strategy. Although the experimental setup is based on a low-power laboratory prototype, it can be seamlessly extended to a high-power system because the operating principle, theory and modeling behind the proposed topology and voltage balancing technique remain the same and are independent of the power level.

It is of significance to remark the different aspects that can affect the accuracy and validity of the experiments. The signal conditioning stage, built for interfacing the Hall-effect sensors that measure the voltage of the upper and lower split capacitors with the analog-to-digital converters of the DSP, is based on operational amplifiers and passive components such as resistors and capacitors. All the elements along this cascaded connection are inevitably prone to parameter variations due to temperature, thus affecting the gain and offset of the voltage measurements that are input to the control strategy for carrying out the voltage unbalancing compensation. Although the effect of an offset or a gain mismatch among the voltage sensors is only a constant DC unbalance bias, and even under these non-ideal conditions, the voltage ripple between the capacitors is completely compensated by the proposed balancing strategy, they have to be taken into account. Therefore, with the aim of guaranteeing the high accuracy and validity of the results, a digital calibration curve was implemented within the DSP. Furthermore, an automatic routine was also programmed for digitally removing the initial offset from the voltage sensors. To do this, before taking the initial voltage measurements, both of the split capacitors were discharged through a low-value resistor, and once the routine finished, the Hewlett Packard DC voltage source was connected to the terminals of the split capacitors.

The use of poor-quality measuring instruments as well as a weak grounding for the power system are other threats to the validity of experiments that can lead to biased and misleading results. However, in this work, a proper ground method was followed, which is in agreement with the literature. Moreover, accurate and high-performance instruments were used such as the power quality analyzer Fluke 43B, the scope Tektronix TPS2024B and the scope Agilent MSOX3054A.

The experimental results presented in Section 5 have been obtained at various times and in different days. Therefore, the repeatability of measurements as well as the good performance exhibited by the prototype under different conditions and scenarios can be interpreted as sufficient evidence for validating the setup. Bearing in mind that the experimental and simulation results presented throughout the paper agree, they thus mutually validate each other. Furthermore, the fact this study was properly compared to the already existing topologies in literature it gives us the reassurance that the obtained results are reliable.

On the other hand, it is also important to take notice that, even though the proposed topology is bidirectional, the voltage balancing strategy only applies for the inverter mode, i.e., when the energy flows from the DC source to the AC grid. Thus, the proposed topology is a good candidate for unidirectional applications such as photovoltaic, where the power always flows from the photovoltaic system to the grid or the load. Bearing in mind this situation, future research directions of the present work are the improvement of such five-level topology so that it becomes capable of balancing the voltage of split-capacitors in the rectifier mode too, i.e., when the energy flows from the AC grid to the DC side. The objective of future work on this matter is devising a multilevel NPC-converter with bidirectional voltage balancing capabilities, thereby expanding the fields and applications where it can be exploited.

7. Conclusions

A novel single-phase grid-tied neutral-point-clamped five-level converter with an inherent voltage balancing strategy that merges simplicity and effectivity was proposed and validated in this paper. The developed balancing strategy is based on a simple multicarrier

phase disposition PWM modulation and only requires measuring the capacitors' voltages and the sign of the converter output current for selecting the appropriate, compensating, switching vector from a LUT; thus, avoiding the complexity of conventional methodologies that modify the SVM or inject offset voltages into the CBPWM.

The obtained simulation and experimental results show a very good performance of the developed strategy for balancing the DC-link split capacitors in both steady state and transient conditions, e.g., a sudden variation in the q-axis grid current component, a grid voltage sag/swell and a DC bus voltage step-change. From the power quality analysis, it is noteworthy that the inherent balancing strategy of the implemented SPFLC makes possible obtaining straightforwardly a symmetrical five-level output voltage and a grid current with very low harmonic content, a more accurate vector control of the grid current and a better overall performance of the multilevel converter application.

A simple but effective voltage balancing strategy of the DC-link split capacitors, as the one presented in this paper, makes the proposed single-phase NPC five-level topology attractive and suitable for high-performance multilevel-based power applications such as the integration of photovoltaic energy to the grid, vehicle-to-grid V2G and standalone microgrids.

Author Contributions: All authors have equally contributed to the conceptualization, formal analysis, investigation, methodology, validation, and writing—review & editing of the paper. All authors have read and agreed to the published version of the manuscript.

Funding: This work was funded by the National Council of Science and Technology of Mexico (CONACYT) through its "Postdoctoral Fellowship Program" under grants 2019-000006-01NACV-00062 and 2020-000022-01NACV-00108.

Institutional Review Board Statement: Not Applicable.

Informed Consent Statement: Not Applicable.

Data Availability Statement: Not Applicable.

Acknowledgments: Authors would like to thank TNM Instituto Tecnológico de La Laguna for its partial support in this research.

Conflicts of Interest: Authors declare no conflict of interest.

Nomenclature

V_d, V_q	direct and quadrature grid voltage components
i_d, i_q	direct and quadrature grid current components
$\alpha\beta$, dq	stationary and rotating frames
X_β, X_ω	variable in the stationary frame
X_d, X_q	variable in the rotating frame
i_g, V_g	grid current and grid voltage
f_s, T_s	sampling frequency and sampling time
θ_{Vg}, θ_{ig}	phase of grid voltage and phase of grid current
ω_g	angular frequency of grid
V_{dc}	DC bus voltage of FLC
f_{sw}, T_{sw}	switching frequency and switching period
t, T	continuous time and fundamental period
T	transpose matrix
P, P^{-1}	direct and inverse Park matrices
k_p, k_i	proportional and integral gains of PI controllers

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