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Model Predictive Control for Paralleled Uninterruptible Power Supplies with an Additional Inverter Leg for Load-Side Neutral Connection

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Abstract: Uninterruptible Power Supplies (UPS) have been demonstrated to be the key technology in feeding either single- and three-phase loads in a wide range of critical applications, such as high-tier datacenters and medical facilities. To increase the overall system power capacity and resilience, UPS systems are usually connected in parallel. When UPS systems are parallel connected, a circulating current can rise, inhibiting correct system operation. Moreover, having a controlled load power distribution is another fundamental requirement in paralleled UPS systems. However, strategies to ensure these two topics have not been explored to date for UPS systems with a load-side neutral connection. This paper proposes an innovative Finite Control Set Model Predictive Control (FCS-MPC) strategy that ensures circulating current elimination and controlled load power distribution for paralleled UPS systems that use an additional inverter leg for load neutral point connection. Additionally, a system topology based on two parallel-connected UPS systems that can simultaneously supply single- and three-phase critical loads is proposed. Experimental results show the effectiveness and robustness of the proposed control techniques even when different types of loads are connected to the UPS systems.

Keywords: model predictive control; uninterruptible power supply; multilevel converters; zero sequence circulating current; power quality

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1. Introduction

Nowadays, Uninterruptible Power Supplies (UPS) represent a key technology feeding a wide range of highly sensitive and critical applications, which are increasingly growing in power grids. These systems are used in low-power applications, such as important domestic/business equipment and networks, as well as in high-power applications including industrial processes, high-tier datacenters, hospitals, and other medical facilities. In some of these applications, only Three-Phase Three-Wire (3P3W) loads are required to be supplied. In this case, no neutral wire in the UPS systems is required [1–3]. However, there are several applications in which both three-phase and single-phase loads need to be supplied [4–6]. Hence, for such applications, the used UPS systems must provide a neutral connection at the load-side terminals to feed all possible types of loads.

In the literature, there are two main solutions generally adopted in DC/AC converters of different applications. One of these solutions is characterized by the direct connection of the neutral point of the load to the mid-point of the DC bus [7,8]. The other possibility consists of using an extra leg in the inverter to which the neutral wire is connected [9–12]. One can immediately note that in the first solution, practically no additional hardware is required. This can, in some situations, be a significant advantage since, in terms of UPS configuration, only the connection of the neutral wire to the already-existing DC bus

capacitors' mid-point needs to be made, with no complicated changes in the hardware being required (e.g., rearranging a UPS that only supplies 3-phase loads into a UPS that can supply single-phase loads) and a lower cost.

However, with this solution, all load neutral current that comes from the load can flow into the DC bus capacitors. Hence, these capacitors can be subjected to an enormous amount of stress that tends to degrade the capacitors, changing their nominal capacitance and of course reducing their lifetime. Moreover, by connecting the neutral wire to the DC bus mid-point, the balancing of the DC bus capacitor voltage is even more difficult to achieve, which, for some converter configurations, is a very problematic situation. On the other hand, the second solution requires an additional converter leg with a more complicated control scheme design and execution. However, the disadvantages of additional capacitors' deterioration and DC bus capacitor voltage unbalancing are decreased, which typically leads to higher system performance and reliability compared to the first presented solution [11,13]. Hence, in this study, an additional leg is used in each of the UPS multilevel load-side converters to provide a neutral path for the circulation of the load neutral current.

Multilevel converters present several advantages in comparison with conventional 2-level converters [14]. Since they generate an output voltage with more levels, lower voltage and current Total Harmonic Distortion (THD) are typically achieved, as well as lower switching losses. Moreover, for the same DC bus voltage, the semiconductors are subjected to a lower voltage value. The 3-Level Neutral Point Clamped Converter (3LNPC) corresponds to a multilevel topology that has been largely used in the industry and significantly investigated by the scientific community in a wide range of applications, including UPS systems [2,3]. Thus, in this work, all used UPS converters consist of a 3LNPC topology.

UPS systems are connected in parallel basically due to two reasons: expansion of the installed power capacity (to meet the increase of critical load power in a facility) and increase in the global system resilience (to protect the critical load from possible internal UPS system failures). However, when power converters are parallel-connected an undesirable Zero Sequence Circulating Current (ZSCC) can appear and as shown in [3,15] this current highly distorts UPS systems phase currents, rises their magnitudes to dangerous values, and increases the global active power losses. Given that a fundamental requirement for the correct operation of paralleled UPS systems is the elimination of this current, the main strategies for circulating current elimination in paralleled UPS systems are mainly based on conventional PI control approaches, which typically use a dedicated control loop to eliminate the circulating current [16–18]. More recently, strategies for ZSCC suppression in complete three-phase paralleled UPS systems have been proposed using Model Predictive Control (MPC) [3,19]. However, in these works, only UPS systems with a 3-wire configuration at the load-side are studied. Hence, the study of the circulating current dynamics and the development of a strategy for its elimination in paralleled UPS systems with a neutral connection at the load-side are the contributions of this work.

The ability to distribute the load power is another important issue when UPS systems are paralleled-connected. The possibility of having a controlled distribution is considerably important since it can allow the optimization of the overall system efficiency [3]. Furthermore, if a UPS is not able to supply its power target (e.g., due to internal failure), then the other UPS systems can compensate with an increase in their target power. Nevertheless, load-sharing techniques that allow a controlled load power distribution between paralleled UPS systems with load-side neutral wire have not been explored to date.

Finite Control Set Model Predictive Control (FCS-MPC) has been considered a promising control strategy for power electronics applications [20,21]. Compared to more conventional control techniques (e.g., the use of a PI + PWM control scheme), the FCS-MPC theoretical concept is much more intuitive and simple. Moreover, this type of control typically presents a faster dynamic response [2,22,23] and allows an easier inclusion of system non-linearities and constraints in the control strategy design. Another important advantage is that in comparison to what is typically observed in the dynamic response of

a PI + PWM control scheme, with FCS-MPC, no overshoots or significant oscillations are observed [2,22].

Hence, despite presenting a higher computational burden, this type of predictive control has demonstrated to be a very promising control strategy for a wide range of power electronics applications, including those that present a multi-converter topology, such as paralleled DC/AC converters [24,25], standalone UPS systems [1,26] and paralleled UPS systems [3,15,27].

Hence, this paper has two main contributions:

- Proposal of a system topology that consists of two double-conversion paralleled UPS systems based on a multilevel topology, with a load-side neutral wire that allows the connection of multiple single/three-phase balanced/unbalanced loads;
- Proposal of an innovative control scheme that simultaneously ensures a high-quality load voltage waveform, circulating current suppression, and a controlled load power distribution between UPS systems.

Additionally, an analysis regarding the behavior of load-side converters neutral leg currents is provided, also representing a contribution of the work. This paper is organized as follows: Section 2 presents all converters' mathematical models and the circulating current dynamics; Section 3 demonstrates the control references calculation as well as the proposed predictive control strategy; experimental results are shown and discussed in Section 4; finally, in Section 5 the main conclusions of the work are presented.

2. UPS System Modelling and ZSCC Dynamics

Figure 1 illustrates the proposed system topology as well as relevant voltage and current signals. For simplicity, taking into account that the DC–DC converters and battery banks of both UPS systems do not affect the ZSCC dynamics, these two components are not considered in the present work. Thus, each UPS has two converters sharing a DC bus with two capacitors: a grid-side converter (GSC) and a load-side converter (LSC). The GSCs are connected to the mains using an inductor, whereas the LSCs are connected to the load using a second-order LC filter. These two converters are based on a 3LNPC topology, solely differing between them in the number of converter legs. Each GSC contains three legs and each of them is associated with a grid-side phase X. On the other hand, each LSC has four legs, and each of these legs is associated with the three load-side phases and the neutral point terminal. Hence, for a GSC, $X = \{R, S, T\}$, and for an LSC, $X = \{A, B, C, N\}$. All converter legs have four IGBTs with anti-parallel diodes as well as two clamping diodes. Hence, as Table 1 shows that for each leg, there are three possible switching states $S_X \in \{1, 0, -1\}$, which when applied lead to three different pole voltage values $v_{XM} \in \{v_{C1}, 0, -v_{C2}\}$, respectively. The pole voltage of phase X (v_{XM}) corresponds to the voltage between a terminal X and the M point, which is the middle terminal of the UPS DC bus. Given the configuration of each converter, each GSC and LSC has 27 and 81 possible switching states, respectively, which represent the mathematical model of these converters defined in Sections 2.1 and 2.2, respectively.

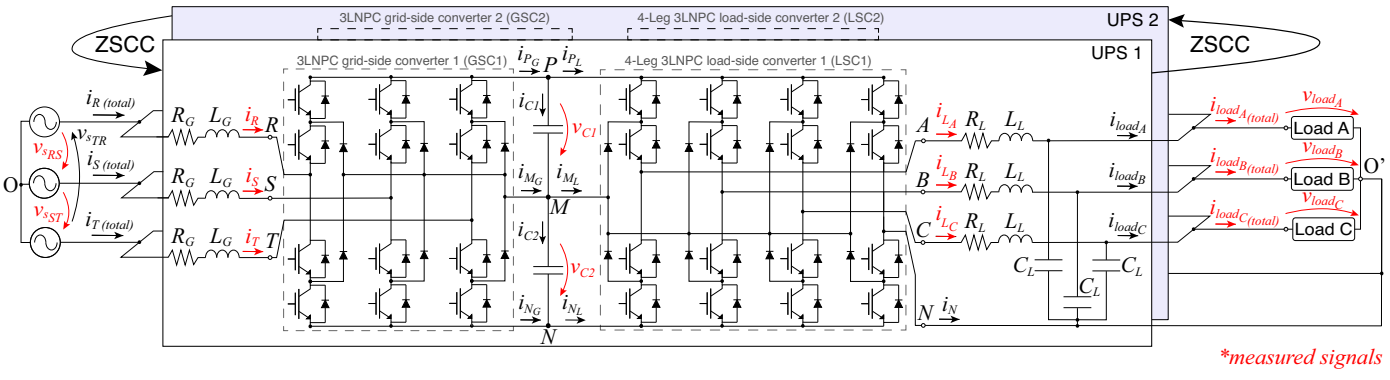


Figure 1. Circuit and main variable representation of the proposed paralleled UPS systems.

Table 1. GSC and LSC switching states in phase X.

GSC/LSC Switching State (S_X)	Active Switches	Generated Pole Voltage (v_{XM})
1	Upper two	v_{C1}
0	Middle two	0
-1	Lower two	$-v_{C2}$

2.1. Grid-Side Converter Mathematical Model

The generic mathematical model of the GSCs is presented here. Since the two UPS systems have the same configuration, the presented model is equal for the two GSCs, which is also valid for the LSCs. Regarding a GSC, from Figure 1, the following voltage equation is written:

$$v_{s_X} = L_G \frac{di_X}{dt} + R_G i_X + v_{XM} - v_{OM} \, . \tag{1}$$

In this equation, v_{s_X} denotes the grid phase voltage (obtained from the measured line-to-line voltages shown in red) and v_{OM} is the Common Mode Voltage (CMV) generated by the converter.

For simplicity, the GSC variables are transformed to space vector form by using the following transformation:

$$\overline{x} = \frac{2}{3} \cdot (x_R + a x_S + a^2 x_T) \tag{2}$$

where $a = e^{j\frac{2\pi}{3}}$ is the space rotation coefficient and $\overline{x}$ is the variable x in space vector form. Hence, in vector form, (1) is written as

$$\overline{v}_s = L_G \frac{d\bar{i}_g}{dt} + R_G \bar{i}_g + \overline{v}_g \, . \tag{3}$$

in which $\overline{v}_s$ corresponds to the grid voltage vector; the term $\bar{i}_g$ is the input UPS current vector and $\overline{v}_g$ the converter voltage vector. This equation allows one to obtain the converter current dynamics, which are given by

$$\frac{d\bar{i}_g}{dt} = \frac{\overline{v}_s}{L_G} - \frac{R_G}{L_G}\bar{i}_g - \frac{\overline{v}_g}{L_G} \, , \tag{4}$$

The DC bus capacitor voltage dynamics are given by

$$\frac{dv_{C1}}{dt} = \frac{1}{C_{DC}} i_{C1} \ , \tag{5}$$

$$\frac{dv_{C2}}{dt} = \frac{1}{C_{DC}} i_{C2} \ . \tag{6}$$

In these equations, the currents in the capacitors C_1 and C_2 are respectively given by

$$i_{C1} = i_{P_G} - i_{P_L} = i_{C2} - i_{M_G} + i_{M_L} \ , \tag{7}$$

$$i_{C2} = i_{N_L} - i_{N_G} = i_{C1} + i_{M_G} - i_{M_L} \ . \tag{8}$$

In these two equations $i_{P_G}, i_{M_G}, i_{N_G}$ corresponds to the currents supplied by the GSC to the DC bus, while $i_{P_L}, i_{M_L}, i_{N_L}$ denote the currents drawn from the DC bus by the LSC. The currents supplied by the GSC to the DC bus are obtained using the switching state applied to the converter and the converter phase currents:

$$i_{P_G} = i_R \cdot K_{P_R} + i_S \cdot K_{P_S} + i_T \cdot K_{P_T} \ , \tag{9}$$

$$i_{M_G} = i_R \cdot K_{M_R} + i_S \cdot K_{M_S} + i_T \cdot K_{M_T} \ , \tag{10}$$

$$i_{N_G} = i_R \cdot K_{N_R} + i_S \cdot K_{N_S} + i_T \cdot K_{N_T} \tag{11}$$

In these equations the coefficients K_{P_X}, K_{M_X}, K_{N_X} are equal to 1 if the switching state applied to leg X is $1, 0, -1$, respectively; otherwise, these coefficients are 0. The currents drawn from the DC bus by the LSC are obtained similarly and are defined in Section 2.2.

2.2. Load-Side Converter Mathematical Model

The mathematical model of the LSCs is analyzed here. As previously mentioned, the configuration of both UPS systems is exactly the same, meaning that the following equations are applicable for any LSC. Hence, from Figure 1 the following voltage equation is obtained:

$$v_{load_X} = -L_L \frac{di_{L_X}}{dt} - R_L i_{L_X} + v_{XM} - v_{O'M}\ , \tag{12}$$

with $X = \{A, B, C\}$. In this equation v_{load_X} corresponds to the measured load phase voltage; the term i_{L_X} denotes the LSC phase currents; and the term v_{XM} corresponds to the pole voltage of phase X and $v_{O'M}$ to the CMV generated by the converter, O' in this case being the neutral point of the load. Since the neutral leg of the converter connects the neutral load point to the mid-point of the DC bus, the LSC CMV directly corresponds to the neutral pole voltage v_{NM}, which is directly obtained from the DC bus capacitor voltage and the switching state applied to the neutral leg:

$$v_{O'M} = v_{NM} = \begin{cases} v_{C1}, & S_N = 1 \\ 0, & S_N = 0 \\ -v_{C2}, & S_N = -1 \end{cases}\ . \tag{13}$$

From Figure 1, the following current equation can also be written;

$$i_{L_X} = i_{load_X} + i_{C_{L_X}} = i_{load_X} + C_L \frac{dv_{load_X}}{dt}\ , \tag{14}$$

with $X = \{A, B, C\}$. In this equation, the term i_{load_X} corresponds to the phase X current after the UPS LC filter, C_L denotes the filter capacitance, and $i_{C_{L_X}}$ the current in the phase X filter capacitor. From Equations (12) and (14), the dynamics of the LSC current and load voltage are obtained, which are given by

$$\frac{di_{L_X}}{dt} = -\frac{1}{L_L} v_{load_X} - \frac{R_L}{L_L} i_{L_X} + \frac{1}{L_L} v_{XM} - \frac{1}{L_L} v_{O'M}\ , \tag{15}$$

$$\frac{dv_{load_X}}{dt} = \frac{1}{C_L} i_{L_X} - \frac{1}{C_L} i_{load_X}\ . \tag{16}$$

The currents drawn by the LSC from the DC bus are obtained using the switching state applied to the converter and the converter phase currents:

$$i_{P_L} = i_{L_A} \cdot K_{P_A} + i_{L_B} \cdot K_{P_B} + i_{L_C} \cdot K_{P_C} + i_N \cdot K_{P_N}\ , \tag{17}$$

$$i_{M_L} = i_{L_A} \cdot K_{M_A} + i_{L_B} \cdot K_{M_B} + i_{L_C} \cdot K_{M_C} + i_N \cdot K_{M_N}\ , \tag{18}$$

$$i_{N_L} = i_{L_A} \cdot K_{N_A} + i_{L_B} \cdot K_{N_B} + i_{L_C} \cdot K_{N_C} + i_N \cdot K_{N_N}\ . \tag{19}$$

In these equations the coefficients K_{P_X}, K_{M_X}, K_{N_X} are equal to 1 if the switching state applied to leg X is $1, 0, -1$ respectively; otherwise, these coefficients are 0. The LSC neutral current i_N is obtained (for the LSC1) using the following equation:

$$i_{R_1} + i_{S_1} + i_{T_1} = i_{L_{A_1}} + i_{L_{B_1}} + i_{L_{C_1}} + i_{N_1}\ , \tag{20}$$

which can be written for sample k as

$$i_{N_1}[k] = 3 \cdot i_0[k] - (i_{L_{A_1}}[k] + i_{L_{B_1}}[k] + i_{L_{C_1}}[k]) . \tag{21}$$

where the term $i_0[k]$ corresponds to the ZSCC at sample k, which is defined in Section 2.3. The LSC2 neutral current is calculated analogously using the ZSCC and respective LSC2 phase currents.

2.3. Zero-Sequence Circulating Current Modelling

As previously described, when UPS systems are parallel connected, a circulating current (ZSCC) can flow between the UPS systems. This current needs to be eliminated to ensure a correct system operation. In the case of the studied system, the ZSCC can be obtained by measuring the three grid-side phase currents of any UPS:

$$i_0 = \frac{i_{R_1} + i_{S_1} + i_{T_1}}{3} = -\frac{i_{R_2} + i_{S_2} + i_{T_2}}{3} . \tag{22}$$

This means that the circulating current will have an equal magnitude in both paralleled UPS systems but opposite polarity, considering the measurement conventions presented in Figure 1. In the equation, the subscripts 1 and 2 are used to differentiate between variables of UPS1 and UPS2. This notation is also adopted throughout the paper.

As demonstrated in [3] for two paralleled UPS systems (without load-side neutral wire connection), this current is generated due to the low impedance paths, which, depending on the switching states, can in the worst case be subjected to the two DC buses voltages. In the case of UPS systems without load-side neutral wire connection, this circulating current is limited by the impedance of the grid-side and load-side filters' inductors. However, in the presented studied system, in which the two DC buses can be directly connected through the neutral legs, only the grid-side filter impedance limits this current, as mathematically proven below. Hence, to obtain the dynamics of the ZSCC in paralleled UPS systems with a load-side neutral connection formed by an additional inverter leg, the following voltage equations are firstly written:

$$\begin{cases} L_{G_1}\frac{di_{R_1}}{dt} + R_{G_1} i_{R_1} + v_{RM_1} - v_{O'M_{L_1}} = L_{G_2}\frac{di_{R_2}}{dt} + R_{G_2} i_{R_2} + v_{RM_2} - v_{O'M_{L_2}} \\ L_{G_1}\frac{di_{S_1}}{dt} + R_{G_1} i_{S_1} + v_{SM_1} - v_{O'M_{L_1}} = L_{G_2}\frac{di_{S_2}}{dt} + R_{G_2} i_{S_2} + v_{SM_2} - v_{O'M_{L_2}} \\ L_{G_1}\frac{di_{T_1}}{dt} + R_{G_1} i_{T_1} + v_{TM_1} - v_{O'M_{L_1}} = L_{G_2}\frac{di_{T_2}}{dt} + R_{G_2} i_{T_2} + v_{TM_2} - v_{O'M_{L_2}} \end{cases} \tag{23}$$

From these equations, by isolating the terms i_{R_1}, i_{S_1} and i_{T_1} (or i_{R_2}, i_{S_2} and i_{T_2}) and by following substitution of the re-written equations in (22), the following dynamics are obtained for the ZSCC:

$$\frac{di_0}{dt} = \frac{(v_{Z_{G_2}} - v_{O'M_2} + v_{O'M_{L_1}} - v_{Z_{G_1}})}{(L_{G_1} + L_{G_2})} - \frac{i_0 \cdot (R_{G_1} + R_{G_2})}{(L_{G_1} + L_{G_2})} \tag{24}$$

In this equation, the terms R_{G_1}, R_{G_2}, and L_{G_1}, L_{G_2} are the resistance and inductance of each GSC, respectively. As for the terms $v_{O'M_{L_1}}$ and $v_{O'M_{L_2}}$, they denote the CMVs generated by LSC1 and LSC2, respectively. As previously mentioned, since the neutral leg connects the load neutral point to the middle point of the respective DC bus, the LSC CMVs are directly obtained using the neutral leg switching state and the DC bus capacitor voltages (13). On the other side, the terms $v_{Z_{G_1}}$ and $v_{Z_{G_2}}$ are obtained for the GSCs through the respective converter pole voltages, which are also obtained using the converter switching state and DC bus capacitor voltage. Hence, these terms are for a given GSC given by

$$v_{Z_G} = \frac{v_{RM} + v_{SM} + v_{TM}}{3} . \tag{25}$$

3. Proposed UPS Systems Controller

The control techniques developed for the paralleled UPS systems are described in this section. The control design is the same for both systems, meaning that the information presented in this section is valid for any UPS, except when indicated. Hence, as each UPS has the same control principle, to avoid redundancy, only the schematic representation of the UPS1 controller is demonstrated with detail in Figure 2.

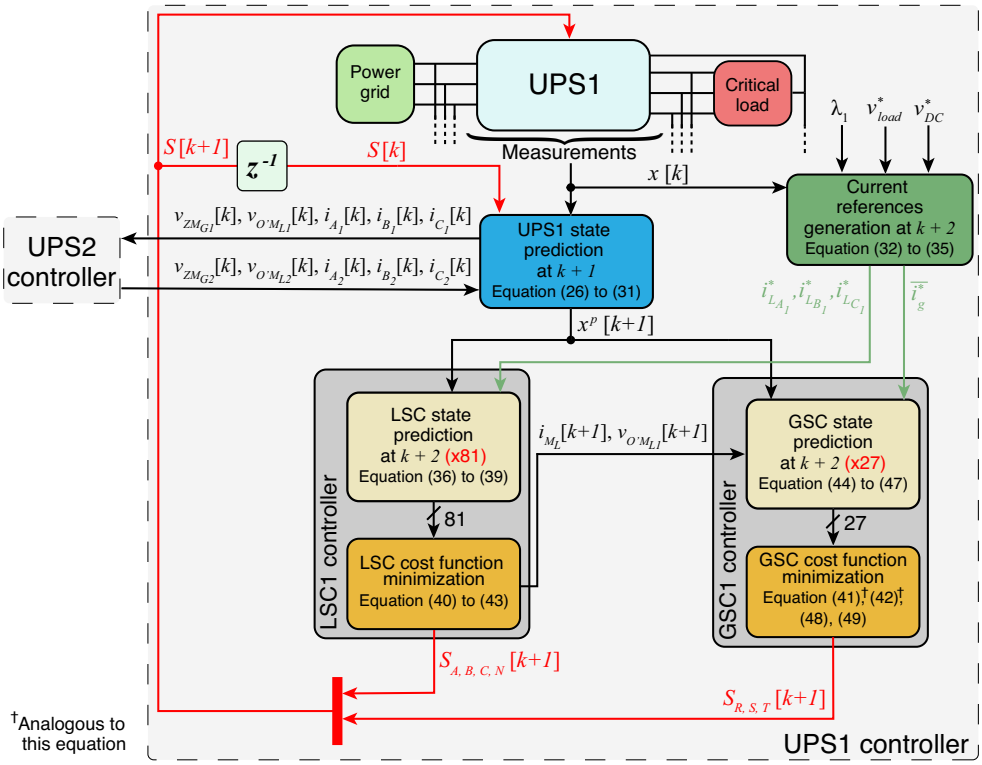


Figure 2. Schematic representation of the proposed UPS controller (UPS1).

This figure indicates the equations associated with the main stages of both UPS controllers: current references calculation, system state prediction at samples $k+1$ and $k+2$, and converter cost function minimization. As described in Section 3.1, a delay of one sample is considered between signal measurement and control actions. In this schematic, the variables that need to be shared between UPS1 and UPS2 controllers are also indicated.

To improve the overall system performance without a significant increase in the strategy computational burden, a cooperative principle similar to the proposed in [3] is adopted at two levels: within a UPS controller and between controllers of the two UPS systems. Within the controller of a UPS, the switching state to be applied on the respective LSC is the first to be selected. In this way, this selection is made, taking into consideration only its effect on the respective UPS. However, to select the control action for the GSC, the switching state already selected for the LSC is taken into account. As for the cooperation principle between the two UPS systems, it is used to increase the effectiveness of ZSCC elimination as demonstrated during the next sections.

In paralleled UPS systems, each UPS is usually controlled using an independent control platform. This typically poses several difficulties in achieving real-time communication between UPS controllers. Hence, in the proposed control schemes, this is taken into account, and only the required variables are shared between UPS controllers.

3.1. Controller Delay Compensation

As used in [2,3,26] a delay of one control sampling time is considered between measurements and converters switching state update. Hence, at sample k, all relevant signals

for UPS controllers are measured. Next, a set of required variables at sample $k+1$ is predicted, considering the present switching states that were applied to the converters at sample k. This $k+1$ system state prediction is necessary to evaluate the control variables associated with a given converter at $k+2$ for all possible converter switching states. The switching state that leads to the minimization of a converter cost function is chosen and applied to the respective converter at sample $k+1$, after which a new control cycle starts.

For $k+1$ prediction, the forward Euler approach is applied in the mathematical models previously described. Hence, from (4), (5), (15), (16) and (24), a UPS input-current space vector, DC capacitor voltage unbalance, LSC phase currents, load phase voltage, and ZSCC at $k+1$ are, respectively, predicted through the following equations:

$$\bar{i}_g^p[k+1] = \left(1 - \frac{R_G T_s}{L_G}\right)\bar{i}_g[k] + \frac{T_s}{L_G}\bar{v}_s[k] - \frac{T_s}{L_G}\bar{v}_g[k]\,, \tag{26}$$

$$\Delta v_C[k+1] = \Delta v_C[k] + \frac{T_s}{C_{DC}}(i_{M_L}[k] - i_{M_G}[k]), \tag{27}$$

$$i_{L_X}^p[k+1] = \left(1 - \frac{R_L T_s}{L_L}\right) i_{L_X}[k] - \frac{T_s}{L_L}\left(v_{load_X}[k] + v_{XM}[k] - v_{O'M}[k]\right), \tag{28}$$

$$v_{load_X}^p[k+1] = v_{load_X}[k] + \frac{T_s}{C_{eq}}(i_{L_{X_1}} + i_{L_{X_2}} - i_{load_{X_{(total)}}})[k], \tag{29}$$

$$i_0^p[k+1] = i_0[k] \cdot \left(1 + T_s \cdot \frac{R_{G_1} + R_{G_2}}{L_{G_1} + L_{G_2}}\right) + T_s \cdot \left(\frac{(v_{Z_{G2}} - v_{O'M_{L2}} + v_{O'M_{L1}} - v_{Z_{G1}})[k]}{L_{G_1} + L_{G_2}}\right). \tag{30}$$

In these equations, T_s denotes the control sampling time. Equations (28) and (29) are calculated for all load-side phases X, with $X = \{A, B, C\}$; the term C_{eq} denotes the equivalent load-side filter capacitance, defined in Section 3.2. For the GSCs controllers, the predicted grid voltage at sample $k+1$ is given by

$$\bar{v}_s^p[k+1] = \bar{v}_s[k] \cdot e^{j2\pi f_{grid} T_s}\,, \tag{31}$$

where f_{grid} corresponds to the grid voltage frequency.

3.2. LSC Current Reference Generation

The load-side converter references are generated, with the strategy proposed in [3] as the basis. This strategy considers an equivalent load-side filter capacitance, which, in the case of the two paralleled UPS systems, is given by

$$C_{eq} = C_{L_1} + C_{L_2}\,. \tag{32}$$

To ensure the load voltage, the current that is injected into this capacitor is controlled. In turn, since in terms of the load voltage only the total current in the capacitor is required to be ensured, distributing this current in a controlled fashion between UPS systems allows one to obtain a controlled load-sharing condition. Hence, from (16) and by using the backward Euler approach, the total current that the UPS systems need to inject into C_{eq} to track the voltage reference $v_{load_X}^*$ is given by

$$i_{L_{(total)_X}}^*[k+2] = i_{load_{(total)_X}}[k+2] + \frac{C_{eq}}{T_s}(v_{load_X}^*[k+2] - v_{load_X}^p[k+1])\,. \tag{33}$$

where $i_{L_{(total)_X}}^*[k+2]$ is the total current reference that needs to be injected in the equivalent capacitor and $i_{load_{(total)_X}}[k+2]$ denotes the load current absorbed by the phase X load. For simplicity, given that the load currents have a small variation during a sampling time, $d_{i_{load}}/dt \approx 0$, and the following simplification is made: $i_{load_{(total)_X}}[k+2] = i_{load_{(total)_X}}[k]$. The proportion of the total reference current that each UPS needs to supply to the load is

defined using the coefficients λ_1 and λ_2, respectively. Thus, λ_1 is the proportion of the total current reference that UPS1 should track, and λ_2 is the proportion of that current assigned to UPS2 ($\lambda_2 = 1 - \lambda_1$). In this way, the converter current references for each LSC ($i^*_{L_{1_X}}[k+2]$ and $i^*_{L_{2_X}}[k+2]$) are, respectively, calculated by multiplying λ_1 and λ_2 by $\bar{i}^*_{L_{(total)_X}}[k+2]$.

3.3. GSC Current References Generation

To obtain the GSC current references for both UPS systems, the active power balancing within the respective UPS system is firstly calculated. Hence, the power reference, denoted as P^*_{grid} is obtained by using the following equation:

$$P^*_{grid} = (P_{grid} - P_G) + P_L + P^*_{charge} \,. \tag{34}$$

where P_{grid} denotes the active power that flows from the grid into the respective GSC; the term P_G corresponds to the power that the DC bus absorbs from the GSC, whereas the term P_L denotes the power drawn from the DC bus by the LSC. The power losses in the GSC are represented by the difference $P_{grid} - P_G$. Finally, the term P^*_{charge} is the power that is needed to discharge/charge the DC bus voltage to the given reference value considering a time horizon of Nth samples [26].

After the calculation of P^*_{grid}, the GSC current references in $\alpha\beta$ reference frame are obtained through

$$\bar{i}^*_g[k+2] = \frac{2}{3} \cdot \frac{P^*_{grid}}{|\bar{v}_s|} \cdot e^{j(\angle \bar{v}_s + 2\pi \cdot 2 f_{grid} T_s)} \,. \tag{35}$$

In this equation $|\bar{v}_s|$ and $\angle \bar{v}_s$ are, respectively, the amplitude and phase of the grid voltage vector, obtained using a PLL that extracts information from the grid voltage of every control sampling time. Since the converters optimization is made for sample $k+2$, the term $\angle \bar{v}_s$ needs to be summed to $2\pi \cdot 2 f_{grid} T_s$ in order to obtain the GSC current references at sample $k+2$.

3.4. Load-Side Converter Controller

In the proposed control strategy, each LSC must fulfill a set of three objectives:

1. Tracking of the LSC current references (ensuring a high-quality load voltage waveform and load power distribution);
2. Elimination of the circulating current;
3. Balancing of the DC bus capacitor voltage.

For the first objective, the output converter current needs to be predicted at sample $k+2$. To achieve that, the following equation is used:

$$i^p_{L_X}[k+2] = \left(1 - \frac{R_L T_s}{L_L}\right) i_{L_X}[k+1] - \frac{T_s}{L_L}\left(v_{load_X}[k+1] + v_{XM}[k+1] - v_{O'M}[k+1]\right) \tag{36}$$

where $X \in \{A, B, C\}$. In this equation, $v_{XM}[k+1]$ and $v_{O'M}[k+1]$ correspond to the pole voltage of phase X and converter CMV at sample $k+1$, which are the variable terms in the equation. These terms directly depend on the switching state being evaluated to be applied to the converter at sample $k+1$.

The proposed control strategy was developed taking into account its implementation in independent control platforms. This means that a UPS controller only knows the switching states to be applied at $k+1$ in its UPS converters. Hence, despite the ZSCC dynamics at $k+2$ being dependent on the switching states of all UPS converters at sample $k+1$, the ZSCC prediction at $k+2$ within each UPS controller only takes into consideration the terms generated by the converters of the respective UPS. Moreover, since the LSC control action within a UPS controller is the first to be calculated, the predicted ZSCC by UPS1 and UPS2 controllers only contains the CMV terms of their LSCs. Thus, the predicted

ZSCCs considered to select the switching states for LSC1 and LSC2 are, respectively, given by

$$i^p_{0_{L1}}[k+2] = i_0[k+1] + T_s \frac{i_0[k+1](R_{G_1} + R_{G_2}) + v_{O'M_{L_1}}[k+1]}{L_{G_1} + L_{G_2}} \tag{37}$$

$$i^p_{0_{L2}}[k+2] = i_0[k+1] + T_s \frac{i_0[k+1](R_{G_1} + R_{G_2}) - v_{O'M_{L_2}}[k+1]}{L_{G_1} + L_{G_2}} \tag{38}$$

To achieve the third objective, the DC capacitor voltage unbalance at sample $k+2$ is predicted as follows:

$$\Delta v_C[k+2] = \Delta v_C[k+1] + \frac{T_s}{C_{DC}} i_{M_L}[k+1], \tag{39}$$

In this equation, it can be seen that since the LSC control action is the first to be computed, only the impact of the LSC is considered through the term $i_{M_L}[k+1]$.

With the FCS-MPC approach, for each converter objective, a partial cost function is defined. Hence, the objective function associated with LSC current references to tracking, ZSCC elimination, and DC bus capacitors' balancing are, respectively, given by

$$g_{i_L} = \sum_{X=A,B,C} |i^*_{L_X}[k+2] - i^p_{L_X}[k+2]|, \tag{40}$$

$$g_{z_L} = |i^p_{0_L}[k+2]|, \tag{41}$$

$$g_{bal_L} = |v^p_{C1}[k+2] - v^p_{C2}[k+2]|, \tag{42}$$

These three partial objective functions are combined in a global LSC cost function, which is given by

$$G_{LSC} = g_{i_L} \cdot W_{i_L} + g_{z_L} \cdot W_{z_L} + g_{bal_L} \cdot W_{bal_L}. \tag{43}$$

This equation combines each partial function with their respective weighting factor W_x that allows one to define the importance of the objectives and provide magnitude correction between the controlled variables. This global cost function is evaluated for the 81 possible LSC switching states, in each UPS controller.

3.5. Grid-Side Converter Controller

Each GSC must also fulfil three objectives, two of them being common to the LSCs. These objectives are as follows:

1. Tracking of converter current references so that the respective UPS absorbs the required power from the grid with low harmonic distortion and the approximate unit power factor;
2. Suppression of the circulating current;
3. Minimization of the unbalancing of the DC bus capacitor voltage.

To achieve the first objective, the input UPS current vector ($\alpha\beta$ components) is predicted at sample $k+2$ using the following equation:

$$\bar{i}^p_g[k+2] = \left(1 - \frac{R_G T_s}{L_G}\right) \bar{i}_g[k+1] + \frac{T_s}{L_G} \bar{v}_s[k+1] - \frac{T_s}{L_G} \bar{v}_g[k+1], \tag{44}$$

where $\bar{v}_g[k+1]$ corresponds to the GSC voltage vector, which is the unique variable term in the equation and directly dependent on the switching state being evaluated for application in the converter at sample $k+2$.

Regarding the ZSCC elimination objective, the predicted ZSCC by UPS1 and UPS2 controllers when evaluating the switching state to be applied to the respective GSC, are given by

$$i_{0_{G1}}^{p}[k+2] = i_0[k+1] + T_s \frac{i_0[k+1](R_{G_1} + R_{G_2}) + v_{O'M_{L_1}}[k+1] - v_{ZM_{G_1}}[k+1]}{L_{G_1} + L_{G_2}} \quad (45)$$

$$i_{0_{G2}}^{p}[k+2] = i_0[k+1] + T_s \frac{i_0[k+1](R_{G_1} + R_{G_2}) - v_{O'M_{L_2}}[k+1] + v_{ZM_{G_2}}[k+1]}{L_{G_1} + L_{G_2}} \quad (46)$$

In these two equations, it can be seen that for the GSC control action selection, the respective UPS controller takes into account the respective LSC CMV term that was previously calculated.

For the third objective, the DC bus capacitor voltage unbalance at sample $k+2$ is calculated by using

$$\Delta v_C[k+2] = \Delta v_C[k+1] + \frac{T_s}{C_{DC}}(i_{M_L}[k+1] - i_{M_G}[k+1]), \quad (47)$$

In this case, the effect of both converters on the DC bus capacitor voltage is considered by including the currents $i_{M_L}[k+1]$ and $i_{M_G}[k+1]$ in the prediction.

The partial cost function regarding the first GSCs objective is given by

$$g_{i_G} = |\vec{i}_g^{*}[k+2] - \vec{i}_g^{p}[k+2]| \quad (48)$$

For the second and third GSCs objectives, the partial cost functions are calculated analogously to (41) and (42), respectively.

The global objective function that combines each GSC partial function with its respective weighting factor W_x for a given GSC is given by

$$G_{GSC} = g_{i_G} \cdot W_{i_G} + g_{z_G} \cdot W_{z_G} + g_{bal_G} \cdot W_{bal_G}\ , \quad (49)$$

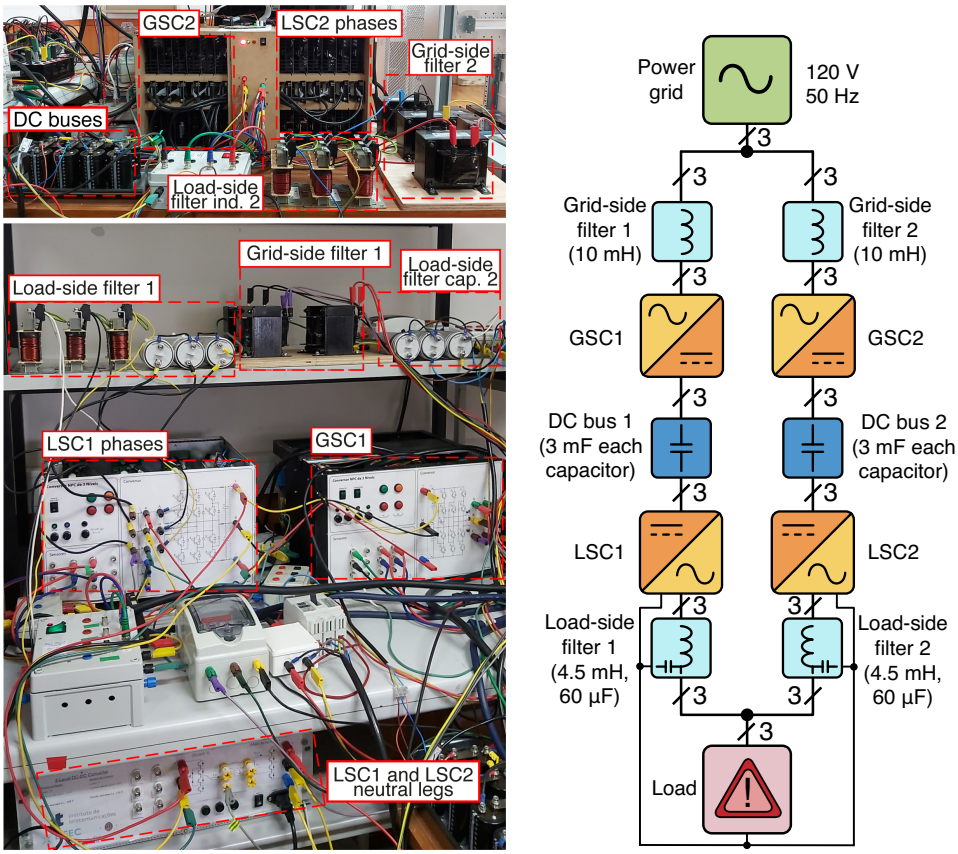
This equation is valid for both GSCs and is evaluated for the 27 possible switching states.

4. Experimental Results

In this section, the experimental results are shown. An analysis regarding the LSC neutral leg currents is firstly demonstrated in Section 4.1. Then, the effectiveness of the proposed control strategy in eliminating the undesired ZSCC is demonstrated in Section 4.2. The robustness of the control strategy in ensuring a high-quality load voltage waveform and distributing the load between the UPS systems is demonstrated in Section 4.3. A power quality analysis is provided in Section 4.4 in which the main power quality parameters are evaluated. An analysis regarding the system dynamics when the critical load changes is presented in Section 4.5, and, finally, in Section 4.6, the system is simulated when supplying high-power loads.

Figure 3a presents a labeled picture of the main experimental setup components, namely GSCs and LSCs as well as respective filters. Figure 3b presents an electrical block diagram of the proposed UPS systems, which can be seen as a simplified version of Figure 1. This representation also contains the per phase filter parameters and the capacitance of each DC bus capacitor, which are also indicated in Table 2.

The controllers are developed in Matlab/Simulink environment and executed in a dSpace MicroLabBox control platform, which is also used for data acquisition at the same sampling rate. This platform has a dual-core PPC microprocessor as well as an FPGA. For controller execution, only the dual-core PPC microprocessor is used with the control algorithm of each UPS being assigned to a core.



(**a**) (**b**)

Figure 3. Experimental setup: (**a**) Photograph of the used components; (**b**) electrical block diagram.

The electrical parameters of the experimental tests are listed in Table 2. As this table shows, for the inductive grid-side filters, an inductance of 10 mH is considered. Each DC bus has two capacitors with an equal capacitance of 3 mF. The second order LC load-side filters contain an inductance of 4.5 mH and capacitance of 60 µF.

Table 2. Electrical parameters of UPS systems.

Electrical Parameter	Value
RMS grid line-to-line voltage	120 V
GSC voltage frequency	50 Hz
GSC filters inductance	10 mH
Capacitance of each DC bus capacitor	3 mF
LSC filters inductance	4.5 mH
LSC filters capacitance	60 µF

The control references and weighting factors used in both UPS controllers are listed in Table 3. In order to select the control sampling time, a set of tests was made to select the minimum possible value, with which all algorithms can be executed without microprocessor overrun occurring. Hence, a sampling time of 90 µs was selected for UPS controllers. An RMS line-to-line voltage of 120 V was considered for the load-side reference voltage, whereas for the DC bus voltage, its reference was set to 220 V. All partial objective functions weighting factors were selected from empirical tests. For converter current tracking and ZSCC elimination, these values were set to 1, whereas for DC bus capacitor voltage balancing, they were set to 0.3.

For the experimental tests, different types of loads are used. For the LSC neutral leg current analysis presented in Section 4.1, a balanced linear load is used, which consists

of three resistors connected to each phase ($R \approx 33.3\,\Omega$ per phase). On the other hand, to test the robustness of the proposed techniques, in Sections 4.2 and 4.3, a highly unbalanced load consisting of three distinct single-phase loads is used: a full-bridge rectifier feeding an RC parallel circuit ($R = 20\,\Omega$ and $C = 180\,\mu F$) is connected to phase A; an RL load is linked to phase B ($R = 10\,\Omega$ and $L = 15\,mH$); and a resistor of $R = 25\,\Omega$ is connected to phase C. This load configuration was also used for the power quality analysis in Section 4.4. In Sections 4.5 and 4.6, different types of loads are used, which are explained in the respective sections.

Table 3. Control parameters used in both UPS controllers.

Control Parameter	Value
Control sampling time	90 µs
RMS load line-to-line voltage	120 V
Load voltage frequency	50 Hz
UPS1 and UPS2 DC bus voltage reference	220 V
W_{i_G}, W_{i_L}, W_{z_G} and W_{z_L}	1
W_{bal_G} and W_{bal_L}	0.3

4.1. LSC Neutral Leg Currents Analysis

This section provides an analysis of the LSC neutral leg currents in regard to the magnitude difference that can exist between these currents and other load-side currents, namely LSC phase currents and load neutral currents. In this test, a balanced set of three single-phase linear loads is used in order to generate a practically null load neutral current, with both UPS systems supplying half of the load power ($R \approx 33.3\,\Omega$ per phase).

Figure 4 illustrates the load voltage, the absorbed load phase currents, the load neutral current, the neutral leg current of each LSC, and the ZSCC.

Firstly, as Figure 4a shows, in these conditions, a high-quality load voltage waveform is obtained, with a THD of approximately 1.2%. With the balanced linear load connected, practically sinusoidal currents are absorbed from the UPS system with a peak value of approximately 2.5 A, as shown in Figure 4b. Hence, the load neutral current presented in Figure 4c is practically null.

Figure 4d,e show the LSC phase currents, which are directly controlled, in order to ensure the respective load phase voltage waveforms, as discussed in Section 3.4. As can be seen in these two subfigures, the LSC phase currents present a peak value of approximately 5 A, which corresponds to twice the load phase currents' peak.

Regarding the neutral leg current of a given LSC, as demonstrated in (21), it depends on the sum of the respective LSC phase currents as well as on the ZSCC that flows between the paralleled UPS systems. Thus, since each LSC phase current is directly controlled to ensure the respective load phase voltage waveform, there can be situations in which the sum of LSC phase currents results in a higher value than that of the peak of the LSC phase currents, significantly increasing the converter neutral leg current. Moreover, from (21), it can be observed that the ZSCC can also increase the LSC neutral leg currents even more. Hence, Figure 4f,g show that despite the balanced linear load being connected to the UPS systems, with the load neutral current being practically null, the currents that circulate in the neutral legs of both LSCs are significantly different from zero, clearly reaching peak values even higher than those seen in the LSC phase currents. In the tested conditions, as demonstrated in Figure 4h, the ZSCC is controlled, consisting of a ripple current around zero and, hence, having a small effect on the neutral legs' current values. However, when not controlled, the ZSCC can significantly increase the LSC neutral leg currents, as is demonstrated in Section 4.2.

These results show that even when supplying a balanced linear load that generates a load neutral current that is practically null, due to the required LSC control and ZSCC (21), the currents in the neutral legs of these converters can be significantly different from zero. Even though the RMS value of the neutral leg currents is significantly smaller than that of

the LSC phase currents, these can reach significantly higher peak values. This occurs even when the load power is equally divided between the UPS systems.

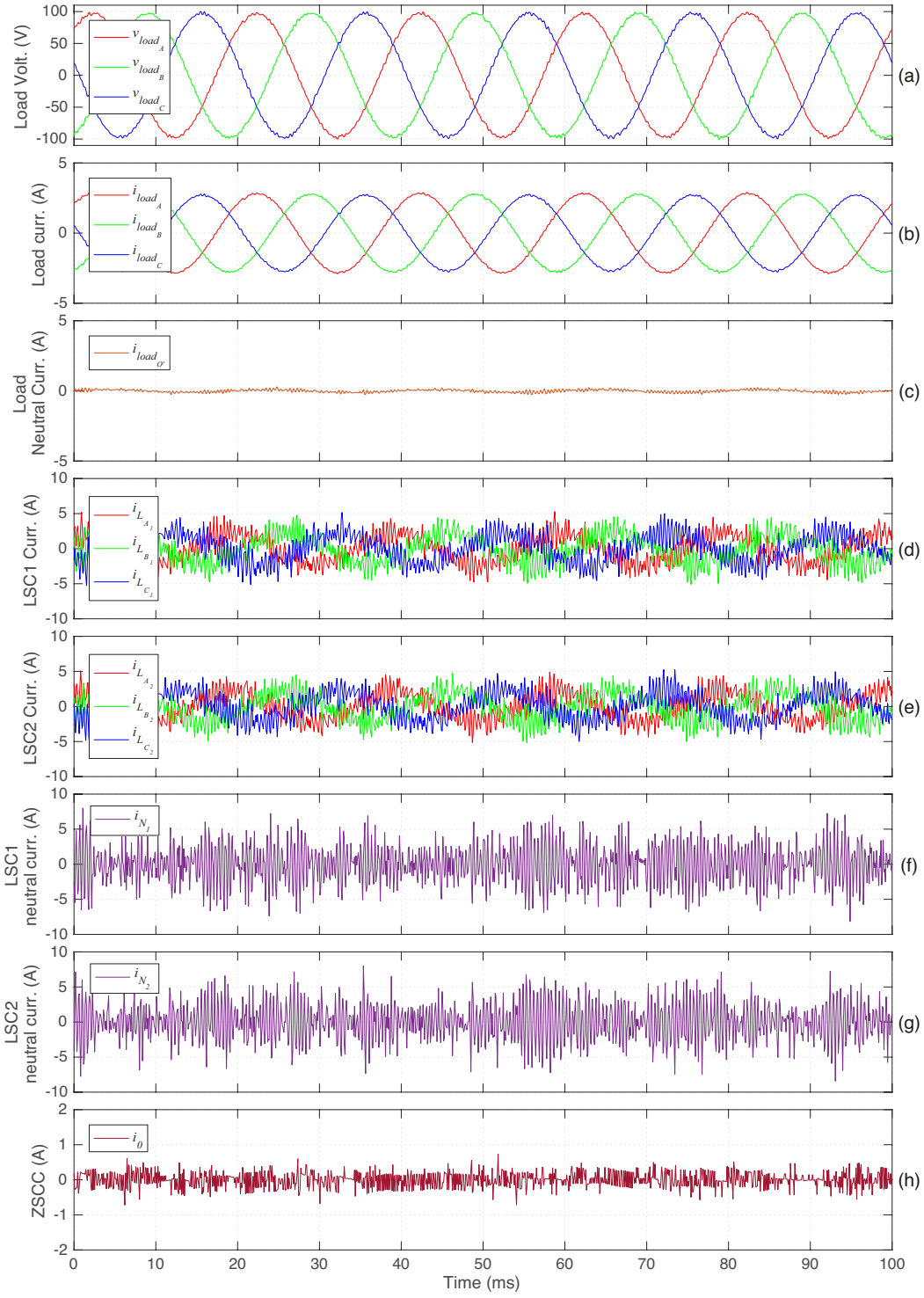


Figure 4. Neutral currents analysis with a balanced linear load connected to the UPS systems: (**a**) load voltage; (**b**) load phase currents; (**c**) load neutral current; (**d**) LSC1 phase currents; (**e**) LSC2 phase currents; (**f**) LSC1 neutral leg current; (**g**) LSC2 neutral leg current; (**h**) zero-sequence circulating current.

This analysis allows the conclusion that the semiconductors to be used in the neutral legs of the proposed paralleled UPS system topology must be able to support higher currents than the semiconductors of the LSC phase legs.

4.2. Zero-Sequence Circulating Current Elimination

Figure 5 shows the importance of ZSCC elimination as well as the effectiveness of the proposed strategy in suppressing this undesired circulating current. This figure shows the ZSCC, input UPS systems currents, LSC phase currents, LSC neutral leg currents, and the generated load voltage. In this test, the highly unbalanced non-linear load is used, with both UPS systems supplying half of the power to this load. Until $t \approx 36$ ms, the ZSCC suppression technique is active, and then it is deactivated. This means that the ZSCC is considered as a converter objective only until that instant, and after that, the elimination of this current is no longer a control objective ($W_{z_G} = W_{z_L} = 0$). Hence, from Figure 5a, it can be observed that after ZSCC suppression deactivation, the ZSCC starts to rise, reaching a maximum absolute value of roughly 7.5 A. Hence, as presented in Figure 5b,c both UPS input currents are significantly affected, becoming highly distorted and reaching higher values compared to those observed while the ZSCC elimination mechanism is active.

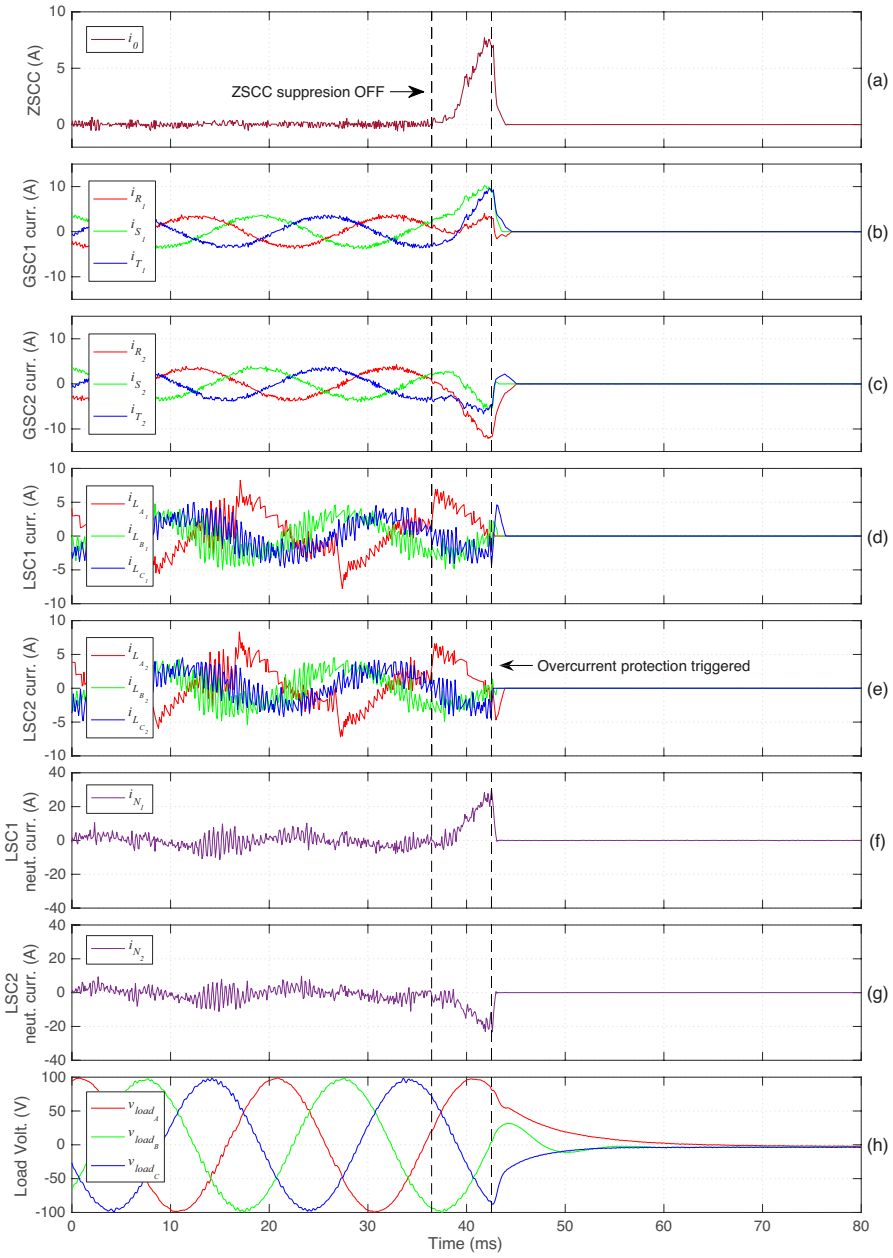


Figure 5. Effectiveness of the proposed ZSCC suppression technique: (**a**) Zero-Sequence Circulating Current (ZSCC); (**b**) UPS1 input current; (**c**) UPS2 input current; (**d**) UPS1 LSC current; (**e**) UPS2 LSC current; (**f**) LSC1 neutral current; (**g**) LSC2 neutral current; (**h**) load voltage.

Figure 5d,e demonstrate that the existence of a considerable circulating current has practically no impact on the LSC phase currents. However, by observing the neutral leg currents in both UPS systems, in Figure 5f,g, it can be seen that their magnitude is significantly increased. When the LSC1 neutral leg current reaches 30 A ($t \approx 43$ ms), the corresponding overcurrent protection is triggered (30 A is the predefined maximum admissible current at the converter neutral legs). It can be seen that this is a significantly higher value in comparison with the LSC neutral currents that were observed while ZSCC elimination was active.

To fully protect the prototype, when overcurrent protection is triggered, all converters of both UPS systems are switched off.

As Figure 5h shows, at $t \approx 43$ ms, all power converter IGBTs are deactivated, and as a consequence of this, the load voltage is no longer ensured. In an industrial or medical application, this would lead to a supply interruption of extremely important loads, which could result in negative social and economic consequences.

These results show the importance of ZSCC elimination as well as the effectiveness of the proposed control technique in its suppression.

4.3. System Analysis for Different Load-Sharing Conditions

The capability of the proposed control techniques in simultaneously ensuring a high-quality load voltage and distributing the load power between the two UPS systems, while keeping their overall stability, is shown in Figures 6 and 7.

The load used in this section is the same as the load used in the previous section: a full-bridge rectifier feeding an RC parallel circuit ($R = 20\,\Omega$ and $C = 180\,\mu$F) is connected to phase A, an RL load is linked to phase B ($R = 10\,\Omega$ and $L = 15\,$mH), and a resistor of $R = 25\,\Omega$ is connected to phase C.In these results, initially, UPS1 provides 75% of the load power, whereas UPS2 supplies the remaining 25%. Then, the percentage of the load power assigned to each UPS is determined to be 50%, and, finally, the power assigned to UPS1 is decreased to 25% with the UPS2 supplying the remaining 75%.

Figure 6 presents the generated load voltage, load phase currents, load neutral current, LSC phase currents, LSC neutral leg currents, and, finally, the average UPS system output power and total power, respectively.

Firstly, from Figure 6a, it is observed that a high-quality load voltage waveform is permanently ensured by the paralleled UPS systems during all different load-sharing conditions with a THD of approximately 1.2%. It is worth mentioning that this THD value is below the maximum value (8%) recommended by the IEC Standard 62040-3. The currents absorbed by the three-single phase loads connected to the UPS systems (full-bridge rectifier feeding an RC circuit + RL load + R load) are presented in Figure 6b. From this subfigure, it can be observed that for the different load power distributions, even when the load-sharing condition changes, the total current absorbed by the load remains practically unchanged.

The load neutral current, which corresponds to the sum of all load phase currents, is presented in Figure 6c. It can be seen that this current corresponds to a very irregular waveform with a peak value of approximately 7 A.

Figure 6d presents the LSC1 phase currents, whereas Figure 6e demonstrates the current in the neutral leg of this converter. From Figure 6d, it can be seen that the magnitudes of the LSC1 phase currents clearly change for the different tested load-sharing conditions. Similarly, from Figure 6e, it is observed that as the UPS1 supplies a lower value of power to the load, the current that flows in the converter neutral leg also decreases. In Figure 6f,g, a similar behavior is observed for the LSC2 phase and neutral leg currents. In this case, as the power supplied by UPS2 to the load is increased, the LSC2 phase currents become higher. In turn, the neutral leg current of this converter also increases, as demonstrated in Figure 6g.

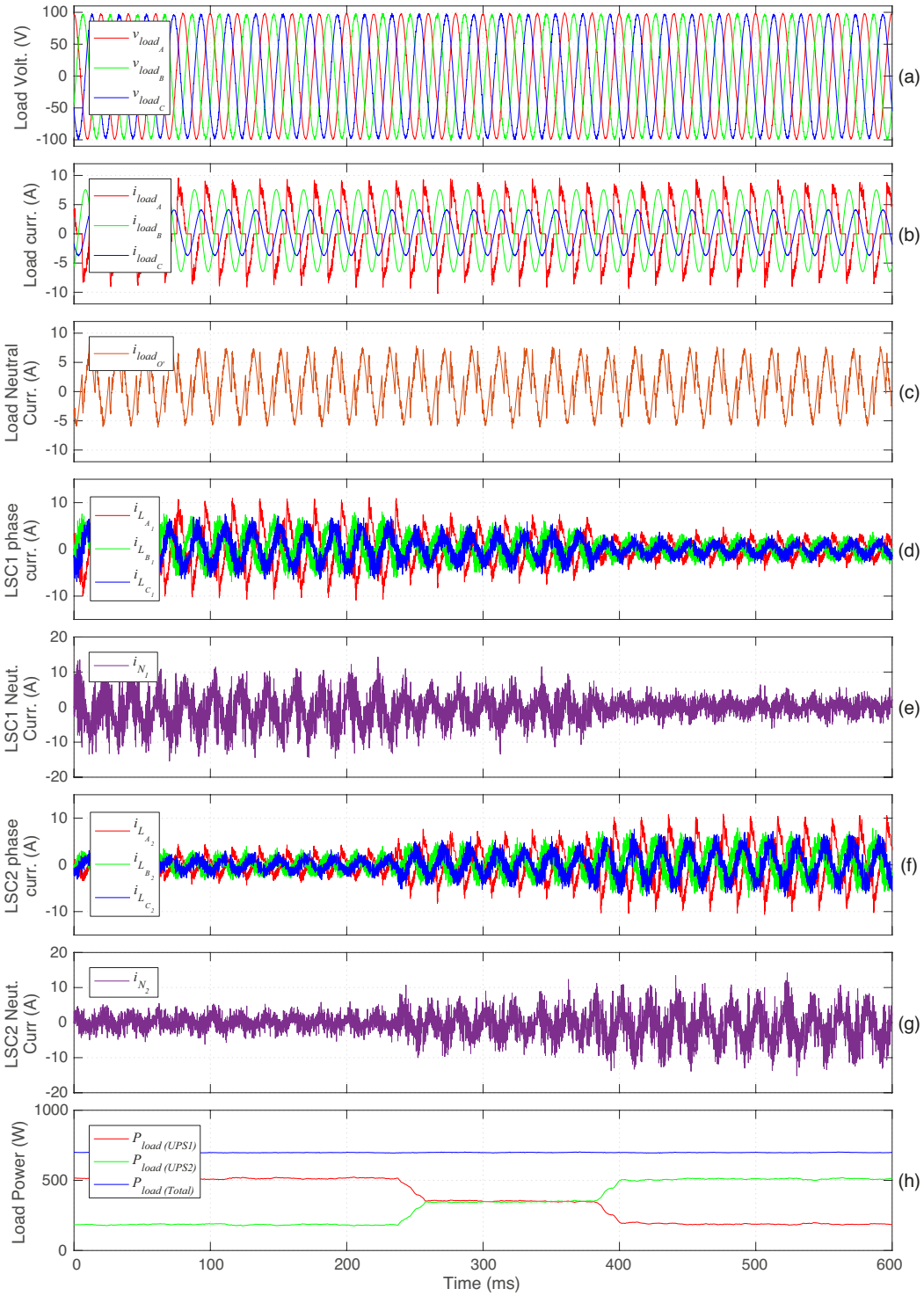


Figure 6. System response for different load-sharing conditions: (**a**) load voltage; (**b**) load phase currents; (**c**) load neutral current; (**d**) LSC1 phase currents; (**e**) LSC1 neutral leg current; (**f**) LSC2 phase currents; (**g**) LSC2 phase currents; (**h**) average UPS system output power and total load power.

Once again, from Figure 6e,g, it can be seen that the neutral leg currents reach higher peak values than the LSC phase current values. For example, note that when a given UPS supplies 75% of the load power, the peak value observed in the LSC phases is roughly 10 A. The peak value reached by each LSC neutral current is clearly higher than this value (≈15 A). This is also verified for the other load-sharing conditions, in which the neutral leg currents reach a higher value than the LSC phase current peak. Hence, these results show

that the LSC neutral leg current peaks are higher than the LSC phase current peaks, even for asymmetric load power distributions.

From Figure 6d,f it can be observed that the output power of each UPS rapidly changes to the new target value, with slower changes being observed in the calculated average powers presented in Figure 6h, only because a time horizon of one period (20 ms) is required in their calculation. Thus, after roughly only 20 ms, all presented average powers stabilize at the new value.

Figure 7 presents the ZSCC, the input currents of both UPS systems, and the DC buses capacitor voltage for the same load-sharing conditions presented in Figure 6.

Firstly, from Figure 7a, it is observed that the ZSCC is effectively suppressed, presenting a ripple near zero for any load-sharing condition. With the ZSCC eliminated, the UPS systems have correct operation. Hence, as shown in Figure 7b,c both UPS systems present near-sinusoidal input currents for the different load-sharing conditions, even supplying a highly unbalanced load.

During all these power distribution changes, as shown in Figure 7d,e, the DC bus capacitor voltage balancing is ensured in both UPS systems, which is also crucial for the correct UPS system operation. Moreover, even for different load-sharing conditions, the UPS controllers are able to maintain the voltage of both DC buses near the defined reference of 220 V.

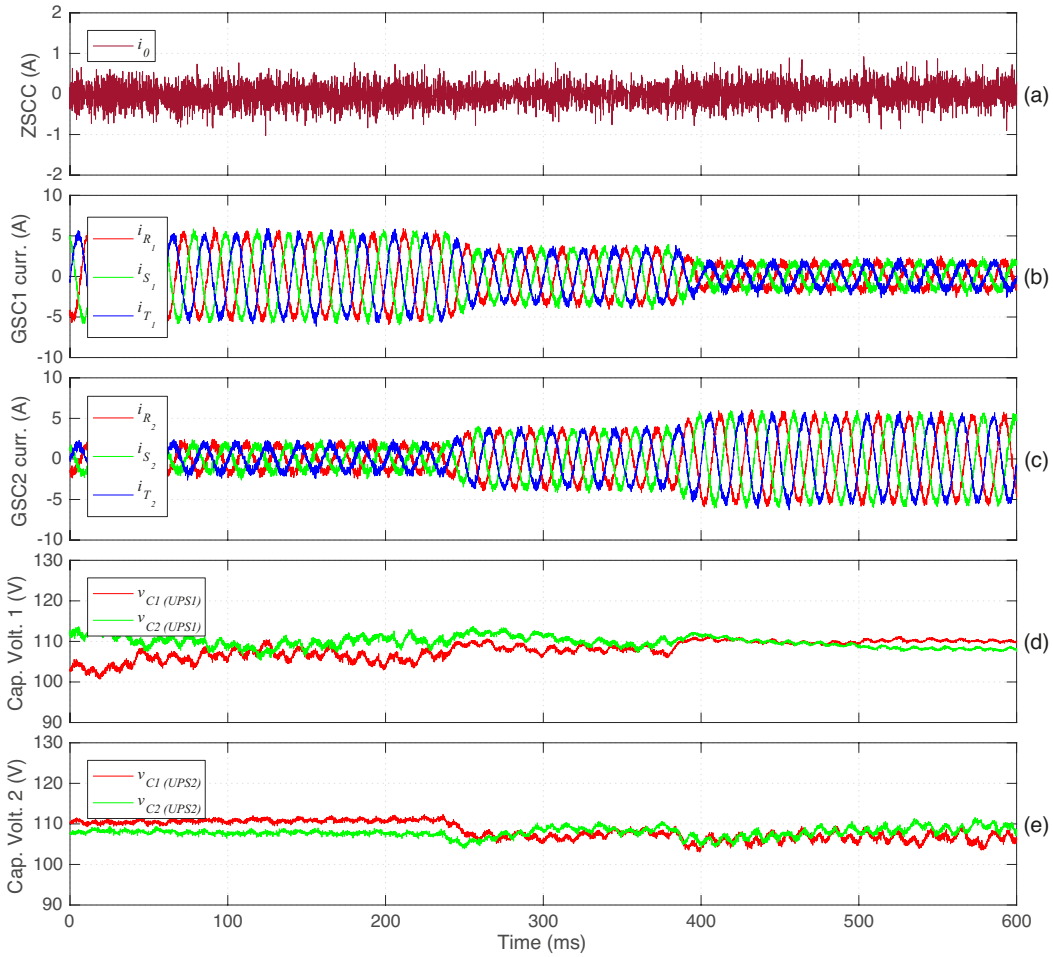


Figure 7. System response for different load-sharing conditions: (**a**) zero-sequence circulating current; (**b**) UPS1 input current; (**c**) UPS2 input currents; (**d**) UPS1 DC bus capacitor voltage; (**e**) UPS2 DC bus capacitor voltage (same time window shown in Figure 6).

These results show that the proposed techniques allow the UPS systems to simultaneously supply a highly unbalanced load, with the absorbed load power being distributed

between these systems, a high-quality voltage waveform being ensured, and the undesired ZSCC being effectively eliminated.

4.4. Power Quality Analysis

In this section, a power quality analysis is presented for the proposed system. When UPS systems are installed in a given facility, they must respect certain power quality requirements, namely regarding the harmonic distortion of the generated load voltage and current that the UPS absorbs from the power grid. Typically, the load voltage generated by a UPS system must present a maximum THD value lower than 8% as defined in the IEC Standard 62040-3. On the other hand, the absorbed grid current should have low harmonic distortion and therefore low THD value.

All presented results in this section were obtained using a YOKOGAWA WT3000 power analyzer. Figure 8 shows power analyzer results when both UPS systems supply half of the power to the load used in Sections 4.2 and 4.3. In the figure, the three generated load phase voltage waveforms (upper three), a grid line-to-line voltage, and a phase current waveform (lower two) are presented. Relevant measurements regarding these voltage and grid waveforms are also shown in this figure, including RMS and THD values.

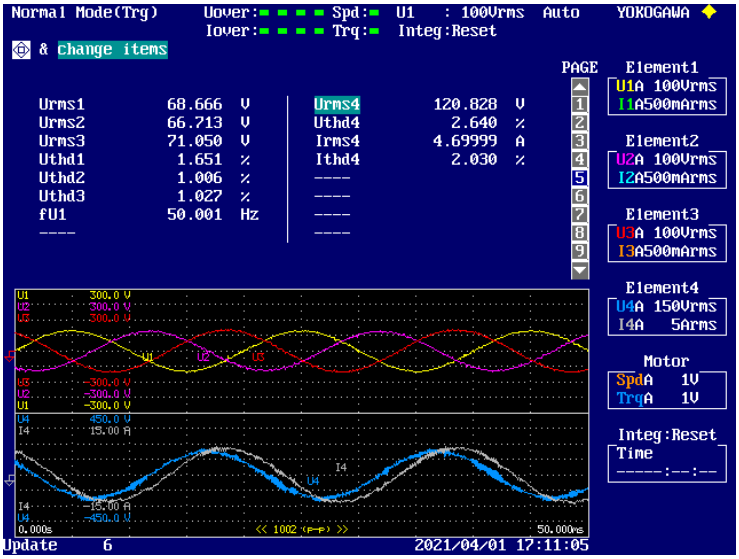


Figure 8. Power analyzer results: three load phase voltages, one line-to-line grid voltage, and one total grid phase current.

Regarding the RMS value of the generated voltages, as shown in Table 3, the line-to-line RMS voltage is set to 120 V, and, therefore, the RMS phase voltage reference is $120/\sqrt{3} \approx 69.28$ V. As seen in Figure 8, the RMS of the generated load phase voltages corresponds approximately to this reference, with a value of 68.67 V in phase A, 66.71 V in phase B, and 71.05 V in phase C, corresponding to deviations of -0.88%, -3.70%, and 2.55%, respectively. These small deviations are observed mainly due to the fact that a highly unbalanced load is connected to the UPS systems. As for the load voltage harmonic distortion, it can be seen that in all phases, a very low THD value is observed. The mean THD value is roughly 1.23%, which corresponds to a value well below the maximum limit of 8% recommended by the IEC Standard 62040-3.

As for the total absorbed grid current (phase *R*, grey waveform), for these test conditions, it has an RMS value of roughly 4.7 A with a low THD of approximately 2.03%. To avoid redundancy in the results, since the other two absorbed grid currents present similar waveform, RMS and THD values, only the phase *R* grid current is analyzed here.

In the following, an analysis is presented to evaluate if low THD values can be ensured even when wrong filter parameter values are considered in UPS controllers. Typically, this can occur for two main reasons: filter parameter deviation (e.g., due to component aging)

or wrong filter parameter characterization. Hence, there can be situations in which filter parameter values above or below the real values are wrongly considered in UPS controllers. These two situations were considered in the analysis.

The load voltage THD behavior was studied with UPS controllers considering a wrong load-side filter inductance or capacitance, while the grid current THD behavior was analyzed with UPS controllers considering wrong grid-side filter values. To evaluate the impact of each filter component, the same error was simultaneously considered in UPS1 and UPS2 controllers.

The influence that considering wrong load-side filter inductance values in UPS controllers has on the load voltage THD is demonstrated in Table 4. As shown in this table, when the actual inductance value (4.5 mH) is considered, a load voltage THD of roughly 1.2% is obtained. When an inductance 10% higher than the real parameter value is considered in UPS controllers, the load voltage THD increases to 1.5%. Similarly, by considering the load-side filter inductance 20% higher than its real value (5.4 mH), the THD increases even more, to 2.0%. When a value 30% above the real inductance value is considered in the controllers (5.85 mH), the load voltage THD corresponds to 2.6%. This THD value is more than twice the original, 1.2%. Nevertheless, this is a significantly lower value than the recommended maximum THD of 8%.

On the other hand, when controllers consider a lower inductance than their actual value, the load voltage THD remains practically unchanged, with a constant value of roughly 1.2%, as seen in Table 4. This THD value is observed even when a value 30% below the real inductance (3.15 mH) is considered in the UPS controllers. Hence, for the tested conditions, it can be seen that when the considered load-side filter inductance value in UPS controllers is below the real parameter value, no tangible impact is observed on the load voltage THD.

These results allow the conclusion that even for a significant error between the load-side filter inductance value considered in UPS controllers and its real value, a load voltage with low THD is generated, which is significantly below 8% for all conditions demonstrated in Table 4.

Table 4. Load voltage THD behavior when wrong load-side filter inductance values are considered in UPS controllers.

Error (%)	Considered Inductance (mH)	≈Load Volt. THD (%)
+30	5.85	2.6
+20	5.4	2.0
+10	4.95	1.5
0	4.5	1.2
−10	4.05	1.2
−20	3.6	1.2
−30	3.15	1.2

In Table 5, the impact of considering wrong load-side filter capacitance values on load voltage THD is shown. As demonstrated in this table, when the real capacitance value is considered in UPS controllers, a THD of approximately 1.2% is obtained. When the considered load-side filter capacitance is 10% above the real value (66 μF), the load voltage THD slightly increases to 1.3%. If the considered capacitance value is 20% higher than the real value (72 μF), then the THD increases even more to roughly 1.5%. Finally, with an error of 30%, the load voltage THD reaches 1.9%.

As for the observed load voltage THD behavior when a capacitance below the real parameter value is considered in the UPS controllers, a similar behavior to the previous presented analysis is observed regarding the load-side filter inductance. Thus, as demonstrated in Table 5, even when a capacitance 30% below the real capacitance is considered, the load voltage THD remains at 1.2%. Hence, it can be observed that for the tested condi-

tions, when the considered load-side filter capacitance value is below the real parameter, no impact is observed on the load voltage THD.

These results show that even when a significant error exists between the considered and real capacitance value, a high-quality load voltage waveform is generated with a THD significantly below 8%.

Table 5. Load voltage THD behavior when wrong load-side filter capacitance values are considered in UPS controllers.

Error (%)	Considered Capacitance (μF)	≈Load Volt. THD (%)
+30	78	1.9
+20	72	1.5
+10	66	1.3
0	60	1.2
−10	54	1.2
−20	48	1.2
−30	42	1.2

Finally, Table 6 shows the grid current THD behavior when wrong grid-side filter inductance values are considered in UPS controllers. As shown in this table, when the real inductance value (10 mH) is considered in UPS controllers, a grid-current THD of 1.9% is obtained. In this analysis, from Table 6, it can be seen that the grid current harmonic distortion increases when inductance values below the real are considered in the UPS controllers. In fact, for the tested conditions, when the considered grid-side inductance is higher than its actual value, slight decreases are observed in the THD. However, it was observed that in these cases, the overall system efficiency also slightly decreases.

The highest THD value (3.5%) is observed when an inductance value 30% below the real inductance is considered in UPS controllers. This THD value corresponds to almost twice the grid current THD value obtained with the real inductance value being considered; however, this is still an acceptable THD value.

Table 6. Grid current THD behavior when wrong grid-side filter inductance values are considered in UPS controllers.

Error (%)	Considered Inductance (mH)	≈Grid Curr. THD (%)
+30	13	1.6
+20	12	1.6
+10	11	1.7
0	10	1.9
−10	9	2.1
−20	8	2.5
−30	7	3.5

In sum, these results show that even when significant deviations exist between real and considered filter parameters values in UPS controllers, the proposed controllers and UPS systems absorb grid currents and ensure load voltage waveforms with low harmonic distortion.

4.5. System Dynamic Response under Load Changes

In this section, the dynamic response of the proposed controllers when an additional load is connected to the UPS systems in operation is demonstrated. Figures 9 and 10 present the behavior of the system when both UPSs are initially supplying a three-phase three-wire linear load and at a given instant a non-linear unbalanced load is connected to the UPS systems. In the tested conditions, UPS1 supplies 75% of the power to the load, and UPS2 supplies the remaining 25%. The linear load has a 100 Ω resistance per phase, whereas the second load consists of the rectifier + RC circuit in phase A and RL load in phase B, which is connected to the UPS systems at $t \approx 71$ ms. Figure 9 shows the generated load phase

voltage, load phase currents, LSC phase currents and average UPS system output power, and total load power.

From Figure 9a, it can be seen that even when the unbalanced non-linear load is connected to the UPS systems, a high-quality load voltage is permanently generated by both UPS controllers. Particularly, no disturbance is observed in the load voltage even with the behavior change in the load currents after connection of the second load (Figure 9b).

It can be seen that the LSC phase currents rapidly adapt in order to maintain a high-quality output voltage waveform, as shown in Figure 9c,d.

Figure 9e shows the behavior of UPS system output power and total load power. After the load connection, the UPS systems start to supply a higher power level, and, thus, the presented powers start to rise. As shown in this subfigure, the load-sharing condition is kept even after the connection of the rectifier + RC circuit in phase A and RL load in phase B is made.

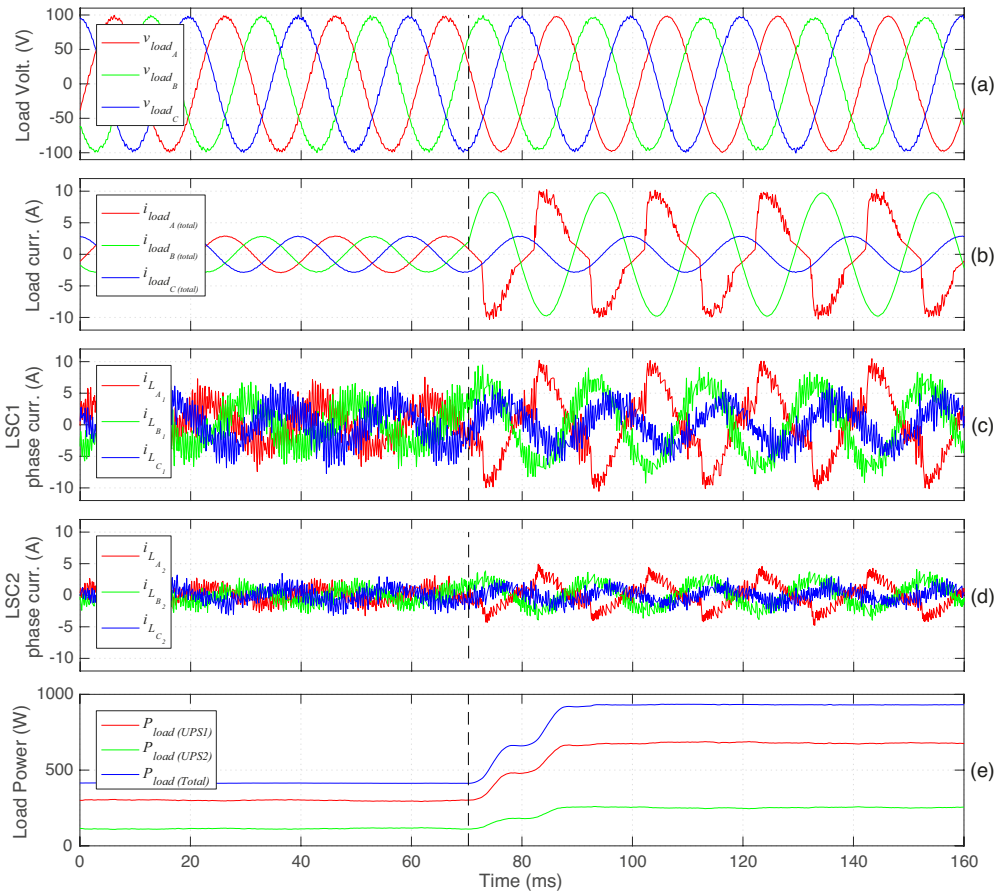


Figure 9. System response when different types of loads are connected to the UPS systems: (**a**) Load voltage; (**b**) load phase currents; (**c**) LSC1 phase currents; (**d**) LSC2 phase currents; (**e**) average UPS system output power and total load power.

Figure 10 shows the DC bus capacitor voltage, GSC1 and GSC2 phase currents, total currents absorbed from the grid, and the ZSCC during the same test.

Figure 10a,b demonstrate that the connection of the additional load has little impact on the DC bus of both UPS systems with the DC buses' capacitor voltage balancing being ensured even at the instant in which the second load is connected. On the other hand, the DC buses have a small voltage drop, which is rapidly compensated, with no overshoot. This voltage drop is observed because the GSC current references are not instantaneously updated since they are computed by considering the balancing of average active power in the UPS system instead of instantaneous active power.

The GSC1 and GSC2 currents are presented in Figure 10c,d, respectively. From these two subfigures, it can be seen that after the connection of the second load, the magnitude of both GSC1 and GSC2 clearly increases with the UPS systems absorbing a higher power value from the grid. Hence, as shown in Figure 10e, the total absorbed grid current magnitude also increases after the second load connection.

Finally, from Figure 10e, it is observed that the ZSCC is effectively eliminated. The connection of the additional load does not affect the suppression of this current, which is crucial for the overall stable operation of both UPS systems.

These results show that with the proposed control techniques, the UPS systems show an overall good dynamic response, even when abrupt changes in the behavior of the critical load occur.

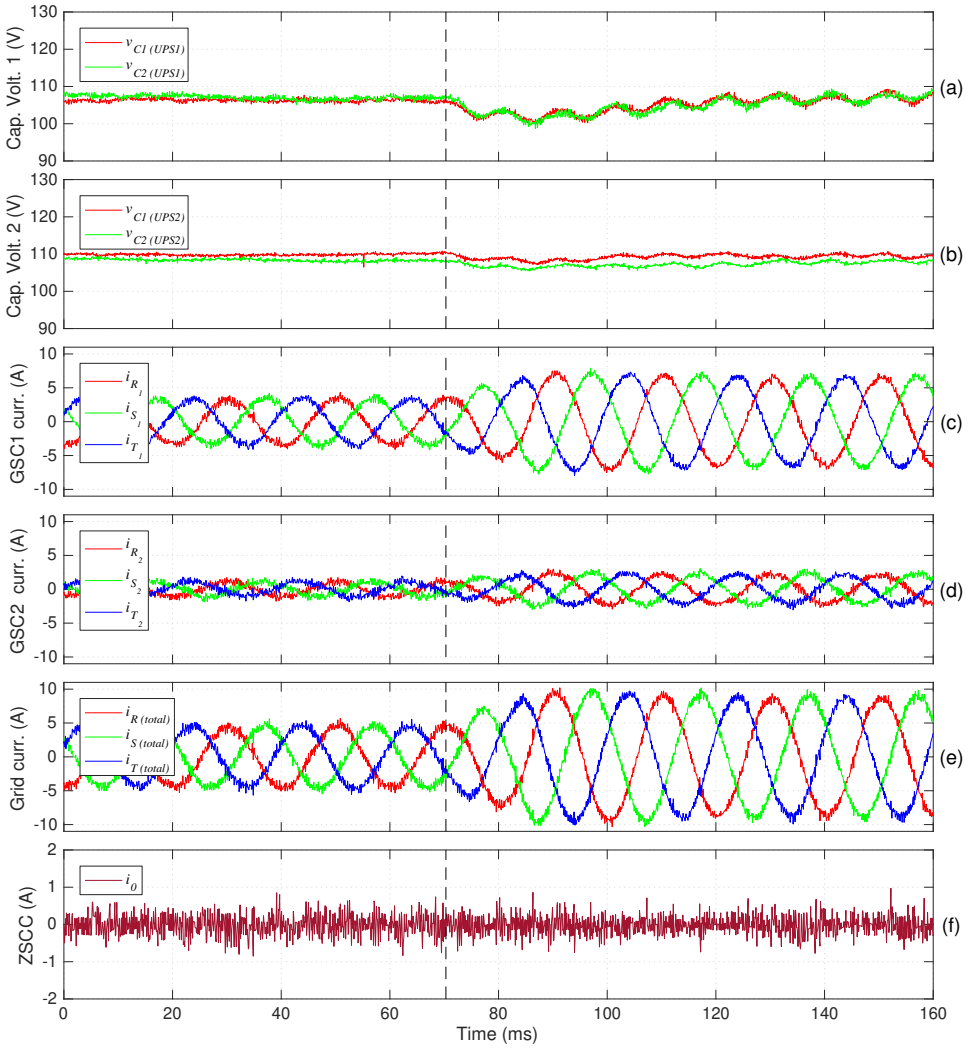


Figure 10. System response when different types of loads are connected to the UPS systems: (**a**) UPS1 DC bus capacitor voltage. (**b**) UPS2 DC bus capacitor voltage; (**c**) UPS1 input current; (**d**) UPS2 input current; (**e**) total current absorbed from the grid; (**f**) zero-sequence circulating current (same time window shown in Figure 9).

4.6. System Simulation for a High-Power Application

In the previous sections, experimental results were shown considering a low power lab-oriented prototype, which, in turn, is operated at low voltage due to safety and material protection reasons. However, UPS systems usually supply high-power loads with higher voltage and current levels than those previously considered. In this section, the operation of the proposed UPS systems feeding high-power loads at higher voltage and current levels

is demonstrated with simulation results. Hence, instead of considering an RMS grid and load voltages of 120 V as used in the previous sections, for the following results, a 400 V RMS value is considered for the line-to-line grid and load voltages. On the other hand, instead of considering a DC bus with 220 V, in this case, the DC bus voltage reference is 700 V. All filter parameters and control weighting factors are equal to the values presented in Tables 2 and 3.

Figure 11 shows the response of the system when both UPS systems supply half of the power to a three-phase resistor (R = 10 Ω per phase); at a given instant, a second load consisting of a single-phase rectifier + RC (R = 20 Ω and C = 200 μF) circuit is connected to phase A, and an RL (R = 10 Ω and L = 20 mH) load is connected to phase B.

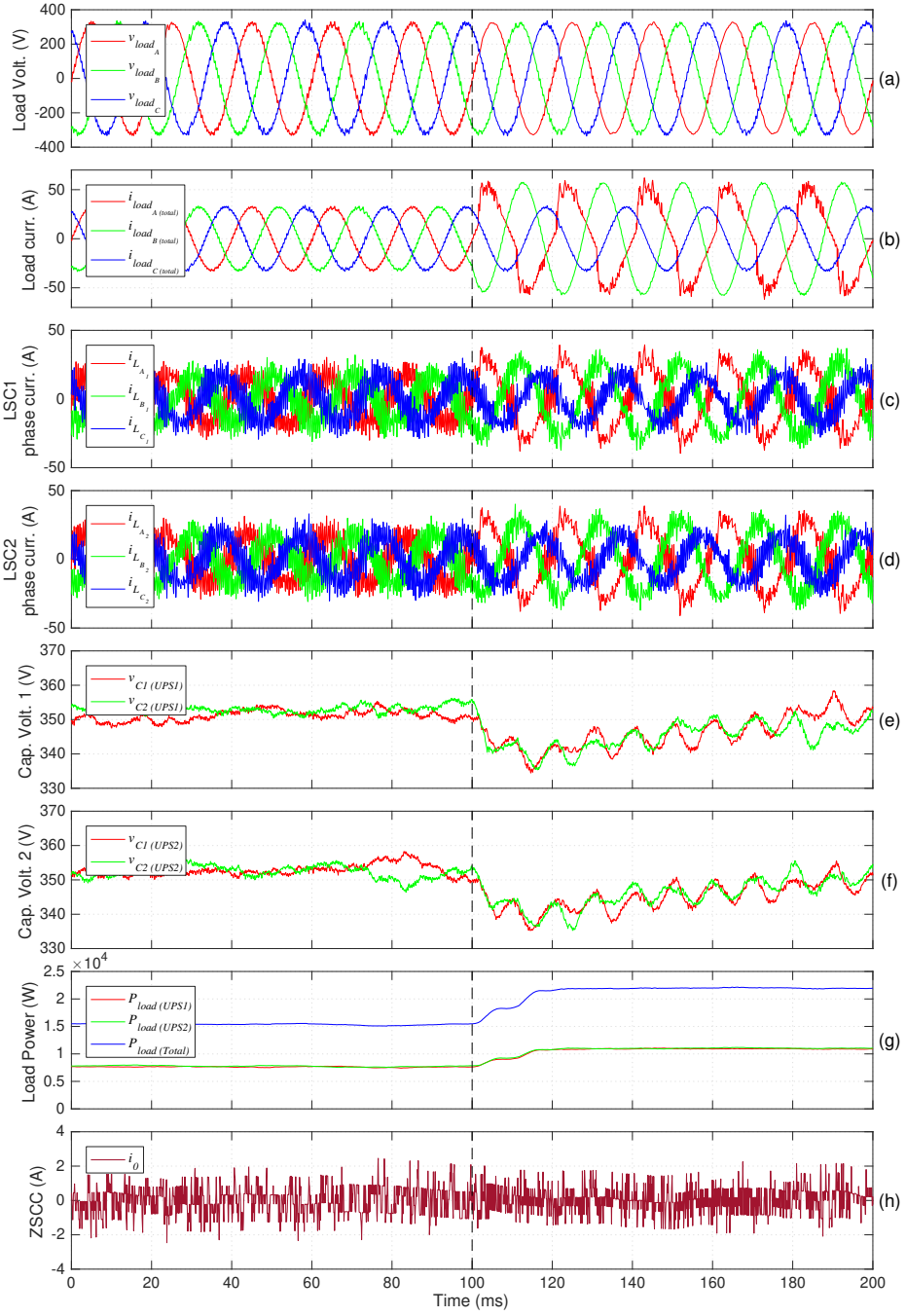


Figure 11. System simulation for a high-power application: (**a**) load voltage; (**b**) load current; (**c**) LSC1 phase currents; (**d**) LSC2 phase currents; (**e**) UPS1 DC bus capacitor voltage; (**f**) UPS2 DC bus capacitor voltage; (**g**) average UPS system output power and total load power; (**h**) ZSCC.

The figure presents the generated load phase voltage, load phase currents, LSC phase currents, DC bus capacitor voltages, average UPS system output power and total load power, and the circulating current.

As previously mentioned, for the presented conditions, the RMS line-to-line voltage reference is set to 400 V. Hence, the load phase voltages, which are presented in Figure 11a, should have an RMS voltage of $400/\sqrt{3}$ and a peak value of $400 \times \sqrt{2}/\sqrt{3} \approx 326.6$ V. As seen in this subfigure, the generated load voltage waveform has higher distortion in comparison to all previously presented results. However, as previously mentioned, for these simulation results, considering a high-power level, the filter parameters are the same as those used in the experimental results for lower power/voltage levels. This may suggest that for higher voltage/power levels, filter parameter redesign may have to be considered.Nevertheless, even by using the presented filter parameters, near-sinusoidal load voltages are still observed with a THD value of approximately 4% (well below the maximum limit of 8% defined in IEC Standard 62040-3). Note that this THD value is obtained even when supplying unbalanced and non-linear currents to the load, as demonstrated in Figure 11b.

The LSC phase currents are presented in Figure 11c,d, in which a higher ripple than in the previous sections can be seen. This is observed mainly because UPS systems are operating with high voltages at their output and DC buses, and, consequently, considerably high voltages can be applied in the load-side filter inductor, which leads to this high ripple in LSC currents. However, in comparison to the previous sections, a similar relation between the ripple and fundamental frequency magnitude of these currents is observed.

From Figure 11e,f it can be seen that each DC bus capacitor voltage is roughly 350 V, which indicates that these capacitor voltages are balanced and that the DC bus voltage is roughly 700 V, which corresponds to the defined reference value. These two subfigures also show that even in high-power applications, the connection of the additional load has little impact on the DC bus of both UPS systems, with the voltage drop being compensated with no overshot in DC buses.

Figure 11g shows the behavior of UPS system output power and total load power. The UPS systems supply an average active power slightly over 7.5 kW, which gives a total power supplied to the load of roughly 15 kW. After the connection of the additional load, the load-sharing condition is kept with the total power supplied, reaching roughly 22 kW.

Finally, from Figure 11h, it is observed that even when supplying high-power loads, the circulating current is effectively eliminated.

The importance of the elimination of this current is emphasized in Figure 12. This figure also demonstrates the effectiveness of the proposed ZSCC suppression mechanism in a high-power application. The undesired ZSCC effects on UPS systems operation phenomena were previously demonstrated in Section 4.2. Nevertheless, in simulation environment, since no overcurrent protections are considered for UPS systems protection, these undesired effects can be better demonstrated. The figure presents the ZSCC, GSC currents, LSC phase currents, LSC neutral leg currents, and the generated load voltage when the high-power unbalanced load previously described is supplied by the UPS systems. In this test, the ZSCC suppression mechanism is deactivated at $t = 100$ ms ($W_{z_G} = W_{z_L} = 0$).

As Figure 12a shows, after the deactivation, the ZSCC magnitude significantly rises, reaching a maximum absolute value of roughly 25 A. Hence, as presented in Figure 12b,c both UPS input currents are highly distorted and reach peak values that correspond to roughly twice the peak value observed in normal operation (ZSCC suppression ON).

The existence of ZSCC has practically no impact on the LSC phase currents, as seen in Figure 12d,e. However, similarly to the GSCs currents, the neutral leg currents in both LSCs rise to values roughly twice the peak value observed in normal operation, reaching values of 100 A.

Nevertheless, as seen in Figure 12h, the circulating current has no tangible impact on the total current absorbed from the the power grid. Even when a high ZSCC exists, near-sinusoidal currents are absorbed.

Finally, as Figure 12i demonstrates, the load voltage is also ensured by the UPS systems, even with a high circulating current. However, as seen in Section 4.2, in a real-world ap-

plication, the ZSCC can increase the current values of GSCs and neutral legs to hazardous values. This increases losses in the systems and causes additional stress to the components of the UPS, reducing their lifetime and possibly causing their failure. Additionally, overcurrent protections can be triggered, leading to the deactivation of the UPS system and consequently compromising the critical load.

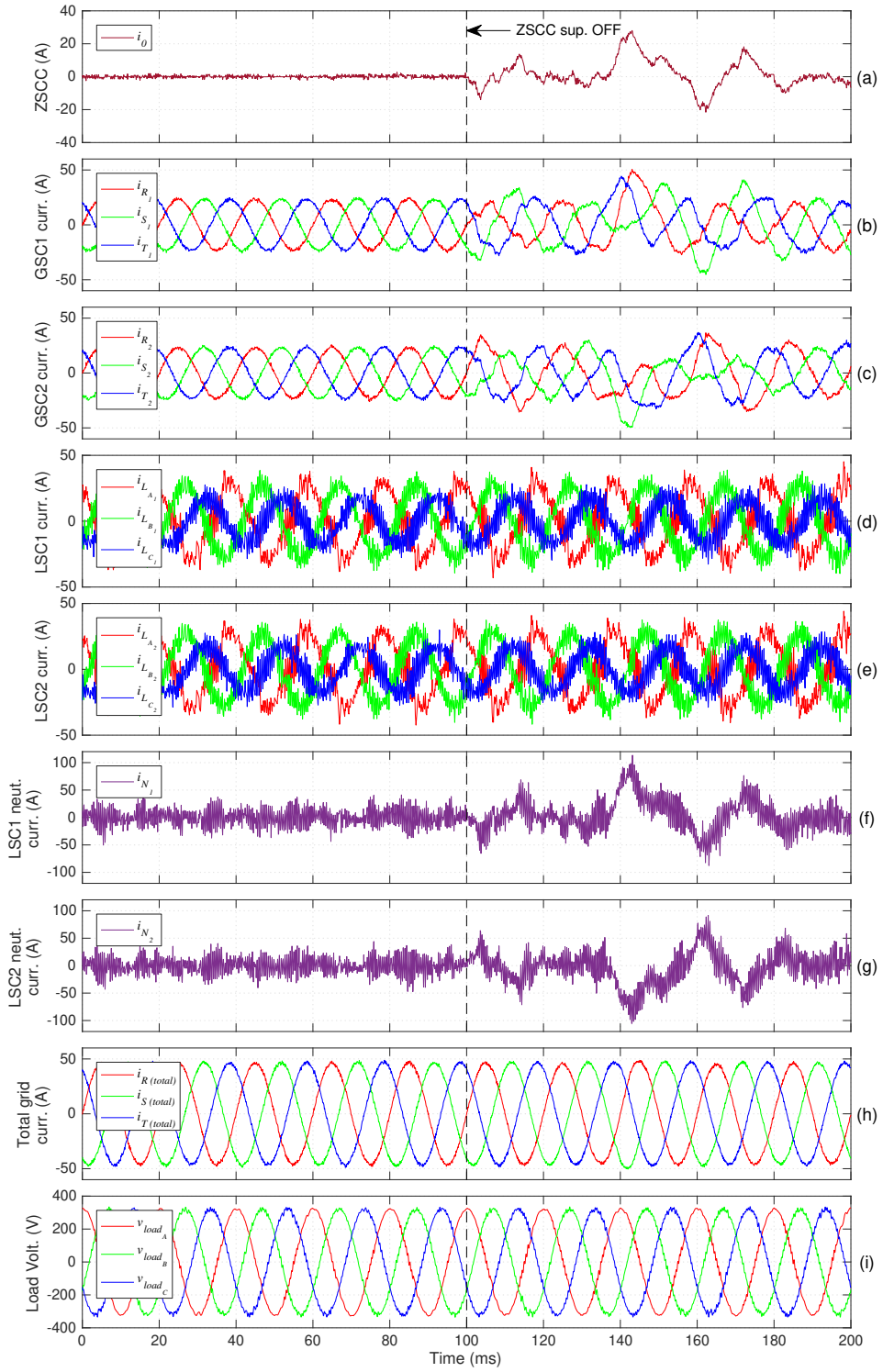


Figure 12. Effectiveness of the proposed ZSCC suppression technique in a high-power application [Simulation]: (**a**) Zero-Sequence Circulating Current (ZSCC); (**b**) UPS1 input current; (**c**) UPS2 input current; (**d**) UPS1 LSC current; (**e**) UPS2 LSC current; (**f**) LSC1 neutral current; (**g**) LSC2 neutral current; (**h**) Total absorbed grid current; (**i**) load voltage.

These simulation results show that with the proposed control techniques, the proposed UPS systems can be used to feed not only low-power critical loads but also high-power critical applications.

5. Conclusions

This paper presents a system topology based on two double-conversion paralleled UPS systems that use an additional leg in their load-side converters (LSC) to provide a connection in each UPS for the load-side neutral wire. The proposed system configuration enables multiple single/three-phase balanced/unbalanced loads to be fed, which given the variety of loads that typically exists in critical applications, such as medical facilities and high-tier datacenters, is a fundamental requirement. A new cooperative Finite Control Set Model Predictive Control (FCS-MPC) technique is also proposed to control all converters of the two paralleled UPS systems.

The dynamics of the undesirable Zero-Sequence Circulating Current (ZSCC) that can flow between both UPS systems, inhibiting a proper overall system operation, are analyzed in this work, and the importance of their suppression is demonstrated.

An analysis regarding the LSC neutral leg currents is also provided, in which it is demonstrated that the currents flowing in these legs can reach considerably higher values in comparison to the LSC phase currents and load currents. This suggests that the semiconductors to be used in the LSC neutral leg must present higher current ratings than those of the semiconductors to be used in the LSC phase legs.

The experimental results demonstrate that with the proposed control technique, the ZSCC is effectively eliminated, allowing correct operation of the parallel-connected UPS systems. A high-quality load voltage waveform is ensured even when the system supplies a highly unbalanced set of single-phase loads under different load-sharing conditions, with each UPS supplying different proportions of the power to the load. Moreover, the presented experimental results show that an overall fast dynamic response and stable steady-state conditions are obtained, even when additional loads are connected with the UPS systems in operation. Finally, the simulation results show that the proposed control techniques and paralleled UPS systems with load-side neutral connection can be used in high-power applications with industrial voltage levels.

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