

## Article

# New Sub-Module with Reverse Blocking IGBT for DC Fault Ride-Through in MMC-HVDC System

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**Abstract:** When integrating multi-grid renewable energy systems, modular multi-level converters (MMCs) are promising for high-voltage DC (HVDC) transmission. Because of the characteristics of the system, however, it is more difficult to prevent a fault at the DC terminal than at the AC terminal of the MMC. Accordingly, a fault ride-through (FRT) strategy for the operation of the MMC in the DC terminal is required for stable system operation. In this paper, a solution for closed-circuit overcurrent caused by a permanent line-to-line DC fault is proposed. This method is able to reduce the fault current through the adjustment of the slope of the total voltage in the system by operating a sub-module having lower switching losses and fewer passive devices compared with existing topologies. Additionally, through the equivalent circuit of the proposed scheme in a sub-module in case of a fault, the FRT mechanism for the fault current is explained. The feasibility of this proposed technique was verified through time-domain simulations implemented by Powersim, Inc.

**Keywords:** HVDC; FRT; MMC; sub-module; DC line-to-line fault; topology; DC transmission; reverse-blocking IGBT



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## 1. Introduction

Recently, the DC power transmission and distribution system has been employed in various studies of electric power construction in multi-grid systems through renewable energy resources such as wind and photovoltaic power generation. voltage source converters (VSC)-based high-voltage DC (HVDC), which began development in the 1940s, is able to transfer power based on a considerable size of cable with the development of new and renewable energy, installation and maintenance are relatively inexpensive, and the error rate is low [1]. Unlike conventional VSCs, HVDC systems, AC filters, and high-capacity capacitors are not needed in an MMC [2–4]. It is possible to implement a high-level voltage waveform accumulated at multiple levels using a cell known as a sub-module (SM), which has a combination of series-connected low-voltage switches. This cell has certain advantages, such as the fast and independent control of AC and DC systems and the reduction in harmonic distortion [5–7].

However, in case of a fault between DC terminals or a pole-to-ground fault [8], a conventional modular multi-level converter (MMC) system has a limitation on terminating the overcurrent through a freewheeling diode due to the topological structure of the half-bridge sub-module (HBSM). So, to stabilize the operation of the MMC system, there is a need to protect the switches from overcurrent and overvoltage. Additionally, a strategy either to immediately isolate the system from the DC side or to reduce the fault current should be designed in detail [9,10]. According to the literature on MMC-based HVDC DC transmission lines, fault ride-through (FRT) strategies using an arm inductor [11], a circuit breaker [12–15], and a fault current limiter (FCL) [16,17] are based on the phenomenon of voltage drop by high impedance in case of a DC fault. Another approach to blocking the

fault current involves decreasing the slope of voltage in the MMC by using reverse voltage created by sub-modules in case of a DC fault.

The DC circuit breaker is a simple and convenient technology providing many technological advances and upgrades so far, but its relatively high price and the difficulty of arc reduction are issues that need to be resolved [14].

The AC circuit breaker has a quick interruption function, but it takes relatively long to operate the circuit breaker, so there is the possibility of damage to the switch and to the device inside the converter. In 2011, a method was proposed of blocking the fault current by lowering the slope of the voltage by forming reverse voltage generated in the full bridge sub-module (FBSM) when a fault occurs [18,19]. However, in normal operation, this method is expensive when power loss deteriorates due to using double the number of passive devices compared with conventional HBSMs. Various studies have been conducted to reduce the number of passive elements in a cell, but for better FRT capability, the increase in both total device number and power loss is inevitable according to the previous studies. The more complex the topology needed, the more difficulties are encountered in balancing both voltage and operating a system [20–29]. Appendices A and B show the comparison and analysis of the voltage applied to each cell, the arrangement of passive devices, the normal state, and the state of the switch in case of a fault for the existing sub-module topology.

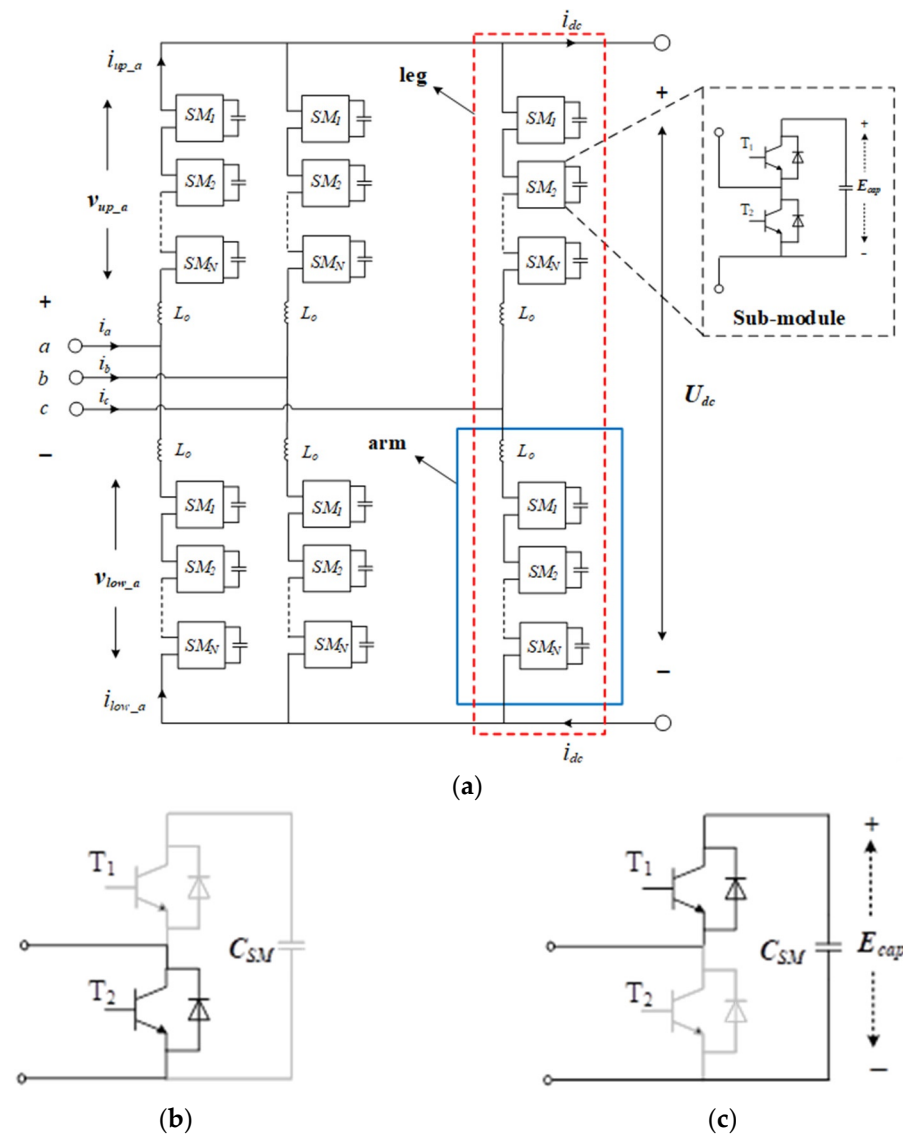
In this paper, a sub-module composed of an insulated-gate bipolar transistor (IGBT), a reverse blocking IGBT (RB-IGBT), and a thyristor is proposed. There is modularity in the proposed configuration since it operates just like a conventional HBSM in normal operation, but significantly fewer passive devices are required in the proposed sub-module compared with existing models with FRT capability. In the case of a DC fault, the module is operated by lowering the slope of the voltage in an MMC by means of the thyristor in the sub-modules. The RB-IGBT, which was first developed in Fuji, has fewer numbers of semiconductor devices compared with conventional IGBT as well as distinct merits such as low power loss and symmetrical voltage blocking. These features are suitable for a multi-level power system with a low switching frequency [30–32].

This paper is organized as follows: The second section explains the basic principle of the operation based on the topology of the proposed MMC system. In the following section, the proposed topology is analyzed according to the protection strategy provided in case of a DC fault. In the fourth section, the effect of the proposed circuit is verified in time-domain simulations by Powersim, Inc. Finally, the conclusions of this research are presented in the final section.

## 2. Topology and Operation

### 2.1. Basic Structure and Operation of MMC

Figure 1 shows a three-phase half-bridge sub-module MMC system in rectification mode. In a leg of phase, there are two upper and lower arms; in each, inductor  $L_o$  and  $N$  serially connected sub-modules are placed. At this time, the half-bridge sub-module consists of two IGBTs and one capacitor.



**Figure 1.** Modular multi-level converter (MMC) circuit diagram: (a) its topology; operation of a half-bridge sub-module under the normal condition of (b) zero voltage; (c) charge/discharge current path of  $C_{SM}$ .

Figure 1b shows the two switching conditions in the half-bridge sub-module. During normal operation, the left and right switching conditions are zero voltage and generation of capacitor voltage, respectively, depending on the charge and discharge in the capacitor in terms of current direction. Two current variables  $i_{up\_a}$  and  $i_{low\_a}$  in the upper and lower arms are determined by both AC phase current ( $i_a$ ) and DC current ( $i_{dc}$ ) as

$$i_{up\_a} = \frac{1}{3}I_{dc} + \frac{1}{2}i_a \quad (1)$$

$$i_{low\_a} = \frac{1}{3}I_{dc} - \frac{1}{2}i_a \quad (2)$$

The upper and lower arm voltages of the A phase in the MMC topology during normal operation are

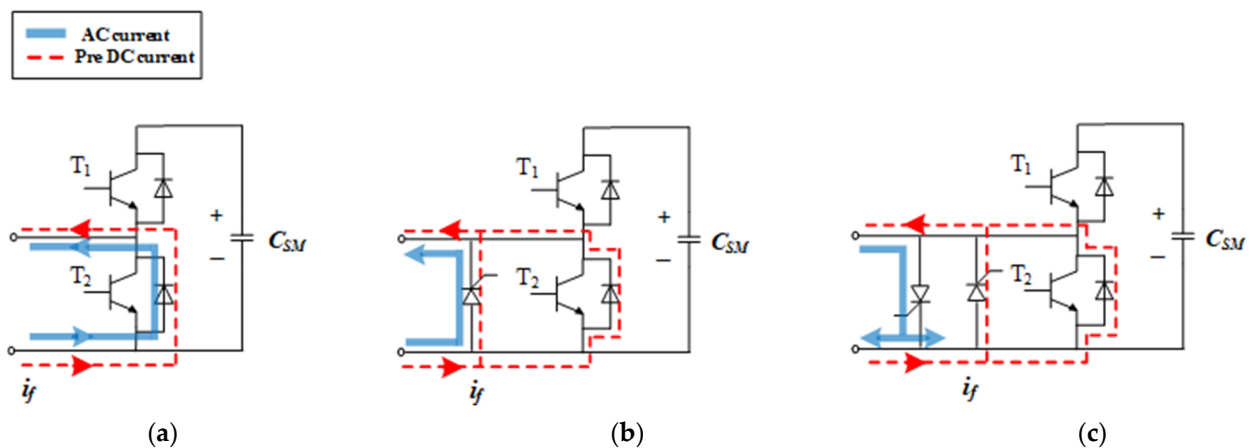
$$v_{up\_a} = u_a - \frac{1}{2}U_{dc} - L_o \frac{d}{dt}i_{up\_a} \quad (3)$$

$$v_{low\_a} = -\left[u_a + \frac{1}{2}U_{dc} + L_o \frac{d}{dt}i_{low\_a}\right] \quad (4)$$

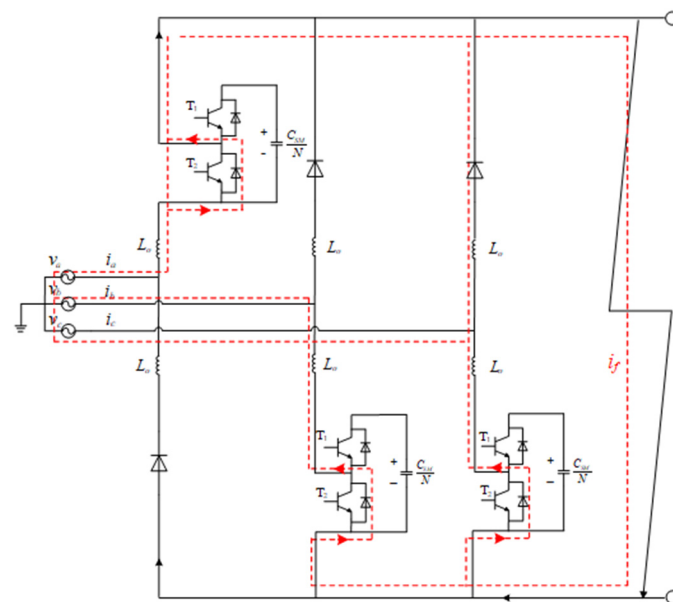
where  $u_a$  and  $U_{dc}$  are the AC voltage of phase A and the DC bus voltage of the same phase, respectively. The variables of the other two phases are named by following the same convention.

## 2.2. Analysis of Short Circuit during DC Fault

As shown in Figure 2a, in the case of a DC fault in a three-phase HBSM MMC, the switches in all sub-modules are turned off. Hence, the fault current in the short circuit flows through a freewheeling diode next to the lower IGBT, and the circuit is not controlled in rectification mode. In Figure 3, the current from the AC source and the discharge current from the capacitor form an overcurrent path along the short circuit.



**Figure 2.** Conventional half-bridge sub-module (HBSM) under the faulty condition ( $i_f < 0$ ), (a) an HBSM without a thyristor, (b) an HBSM with a single thyristor, and (c) an HBSM with double thyristors.



**Figure 3.** Equivalent MMC circuit after HBSMs being blocked under the faulty condition.

In Figure 2b, the HBSM topology is featured by one additional thyristor to protect a set of switches next to the thyristor in the sub-module under the faulty condition by bypassing the fault current through the thyristor [33].

The sub-module in Figure 2c limits the fault current by adding another thyristor in parallel to the existing thyristor in Figure 2b; hence, the mode of uncontrolled rectification is

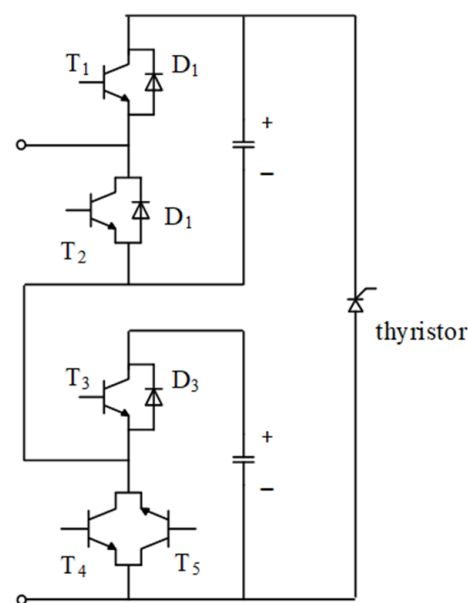


changed [34]. However, in this case, blocking overcurrent through the freewheeling diode is difficult, and FRT capability is not provided in the system.

### 3. Proposed FRT Strategy

#### 3.1. Proposed Circuit Topology

Figure 4 shows the sub-module configuration proposed in this paper. The basic structure is a reverse-parallel combination of diodes for the bypass route in the case of failure of two series-connected HBSMs, including an RB-IGBT. It consists of one RB-IGBT, three IGBTs, one diode, and two capacitors on a three-level sub-module voltage basis. In this case, the RB-IGBT is a low-power switching device capable of bi-directional reverse-voltage blocking capability, which is impossible with conventional IGBTs, and has lower conduction loss characteristics than conventional IGBTs shown as Appendices A and B. It is expected to be used more in high-power systems in the future [35–37].

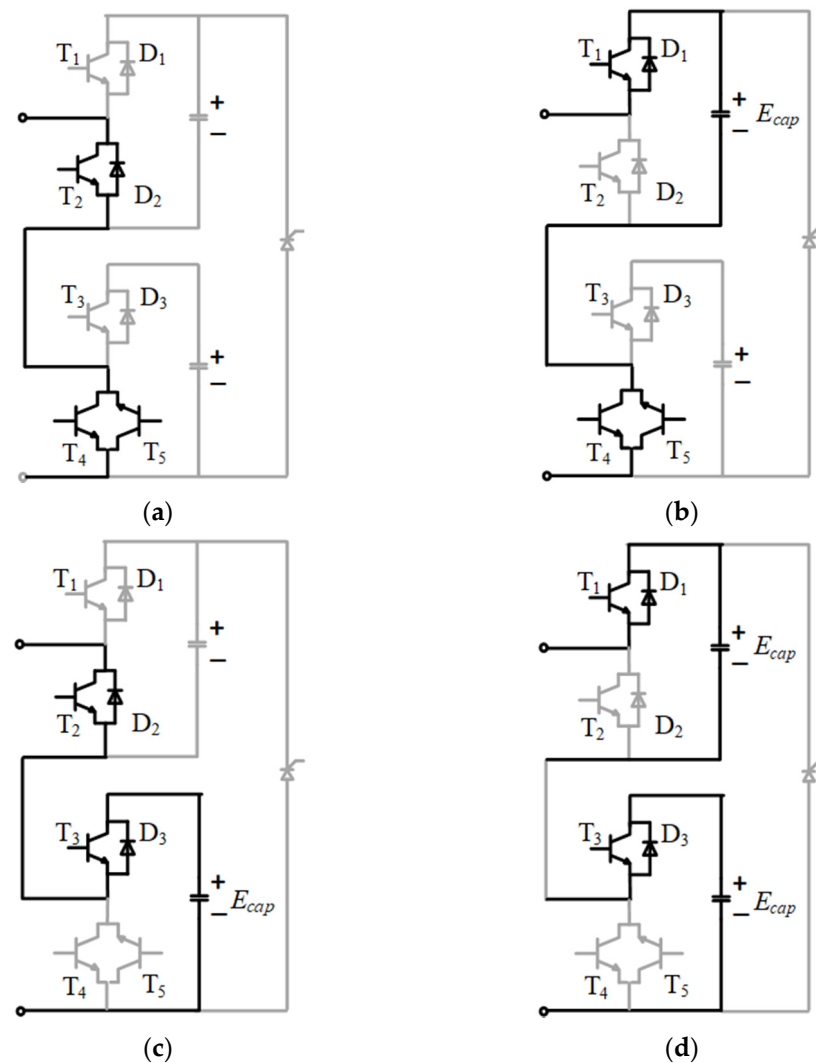


**Figure 4.** Proposed sub-module topology: bridged half-bridge sub-module (BHBSM).

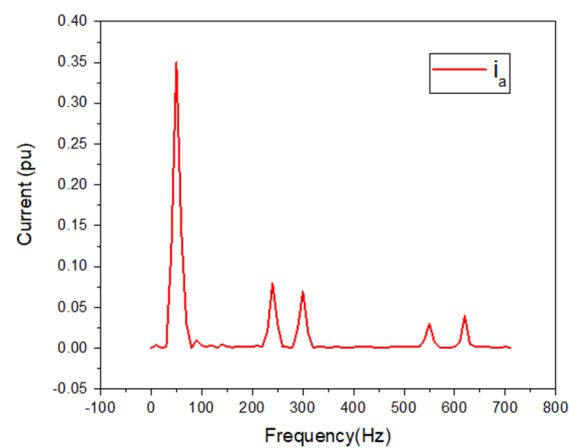
Figure 5a–c shows the operation state of the proposed sub-module that generates a voltage of 0 to 2 times of sub-module voltage ( $E_{cap}$ ) during normal operation in Table 1. When current  $i_{SM}$  flow through the sub-module,  $T_5$  keeps the on-state at all times as it acts as an anti-parallel diode in the conventional IGBT and operates  $T_3$  and  $T_4$  complementarily under RB-IGBT operation, basically operating in a similar manner as an HBSM. Figure 6 depicts the result of the fast Fourier transformation (FFT) of the grid current  $i_a$  waveforms.

**Table 1.** Switch mode of the BHBSM.

Voltage Level		$i_{SM} > 0$	$i_{SM} < 0$
Normal state	0 (V)	$T_2, T_4, T_5$	
	$E_{cap}$ (V)	$T_1, T_4, T_5 / T_2, T_3, T_5$	
	$2E_{cap}$ (V)	$T_1, T_3, T_5$	
Fault state	$2E_{cap}$ (V)	$D_1, D_3$	-
	$-E_{cap}$ (V)	-	$D_2, \text{Thyristor}$



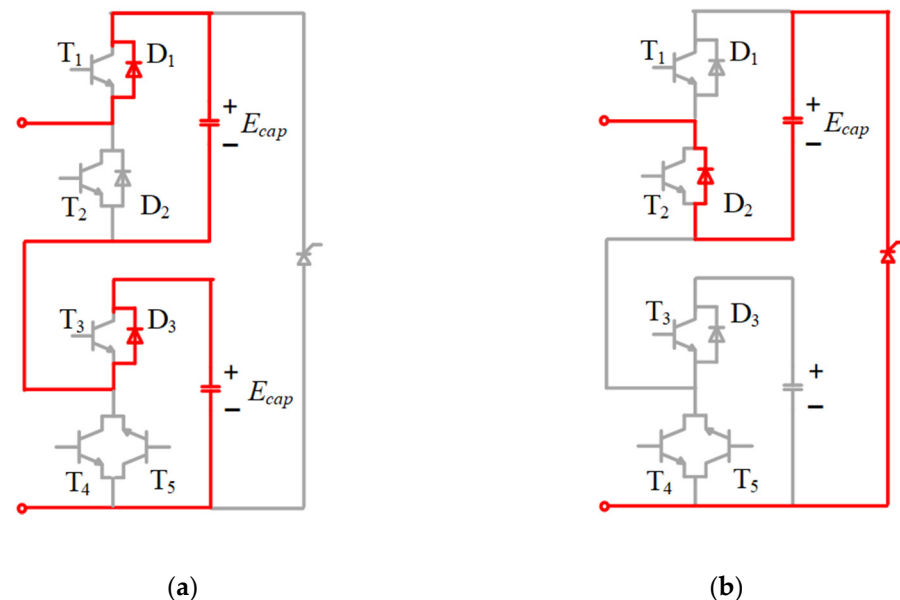
**Figure 5.** Operation of the BHBSM during the normal state (a) 0 [V], (b,c)  $1E_{cap}$  [V], and (d)  $2E_{cap}$  [V] per cell.



**Figure 6.** Fast Fourier transformation (FFT) analysis of the grid current.

Figure 7 shows the operation status of the sub-module when a DC fault occurs and, as shown in Figure 7a,b, all switches, including the RB-IGBT, are turned off in Table 1. At this time, in case the fault current is negative, as shown in Figure 7b, with the RB-IGBT being turned off, as shown in Figure 7b, the existing freewheeling effect changes to enable the

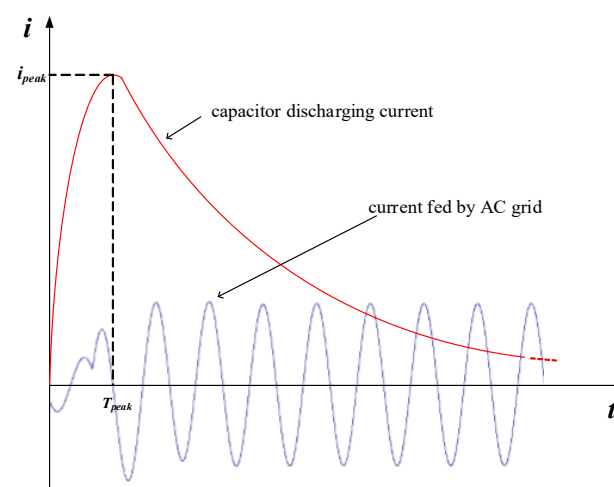
formation of a fault current path to the thyristor. Thereby, it forms a current flow along the anti-parallel diode  $D_2$  and forms  $-E_{cap}$  reverse voltage using the three-level voltage cell. The BHBSM is composed of a relatively small number of semiconductors compared with the existing three-level sub-module with fault ride-through capability. Consequently, one thyristor is exposed to twice the rated voltage. Importantly, the operating principle of the HBSM is applied during normal operation.



**Figure 7.** Operation of the BHBSM during the fault state according to the direction of a fault current: (a)  $i_f > 0$  and (b)  $i_f < 0$ .

### 3.2. DC Fault Analysis with the Proposed Design

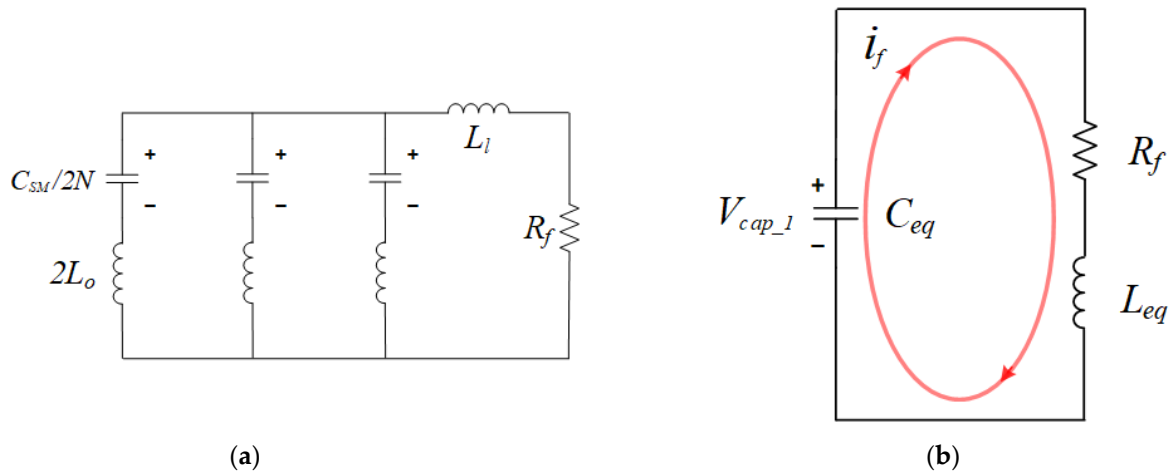
The process of dealing with short-circuit overcurrent after a DC fault in the MMC system is analyzed in a time-sequential manner following a given control strategy. Figure 8 shows the current from the capacitor discharge and the current flowing in the AC grid due to a short-circuit fault. Specifically, at first, the status where current is predominantly influenced by capacitor discharge is analyzed before all sub-modules are turned off. Then, the influence of AC grid current after turning off all sub-modules is investigated.



**Figure 8.** Decomposition of a short-circuit current after a DC-side fault without fault ride-through (FRT).

Figure 9 shows the equivalent circuit of the proposed design when the circuit is shorted due to a DC fault. It is a natural response circuit considering only the capacitor discharge, which is the most important factor in the increase in fault current before all the sub-modules are turned off. The characteristic of voltage in the three-phase balanced system is given by

$$V_{cap\_1} = \frac{1}{3} \sum_{i=a,b,c} (v_{up\_i} + v_{low\_i}) = R_f i_f + L_{eq} \frac{di_f}{dt} \quad (5)$$



**Figure 9.** Equivalent circuit of the MMC before sub-modules are turned off in case of (a) three phases; (b) a simplified circuit.

From (5), the secondary circuit equation is given as

$$\frac{d^2 i_f}{dt^2} + \frac{R_{eq}}{L_{eq}} \frac{di_f}{dt} + \frac{1}{L_{eq} C_{eq}} i_f = 0 \quad (6)$$

Equivalent inductance and equivalent capacitance in the circuit are expressed as

$$L_{eq} = \frac{2}{3} L_o + L_l, \quad C_{eq} = \frac{3}{2N} C_{SM} \quad (7)$$

where  $V_{cap\_1}$  is the total voltage value formed by the capacitance in the equivalent circuit,  $R_f$  denotes the resistance component expected at the time of failure,  $L_o$  represents the inductance of the arm inductor, and  $L_l$  is the inductance component of the line.

With the initial value  $i_f(0) = 0$ ,  $V_{cap\_1}(0) = U_{dc}$  and the following condition

$$\delta = \frac{R_{eq}}{2L_{eq}}, \quad \omega_d = \sqrt{\omega_o^2 - \delta^2}, \quad \omega_o = \frac{1}{\sqrt{L_{eq} C_{eq}}}$$

from the R, L, C series circuit in Figure 8, fault current in the time domain and the total voltage in the sub-module capacitor are calculated using Equations (8) and (9), respectively [38,39].

$$i_f(t) = X e^{-\delta t} \sin Yt \quad (8)$$

$$V_{cap\_1}(t) = U_{dc} e^{-\delta t} \cos Yt + X R_{eq} e^{-\delta t} \sin Yt \quad (9)$$

The variables X and Y are as follows

$$X = \frac{U_{dc}}{Y L_{eq}} = \frac{2 U_{dc} C_{eq}}{\sqrt{4 L_{eq} C_{eq} - R_{eq}^2 C_{eq}^2}} \quad (10)$$

$$Y = \omega_d = \frac{\sqrt{4L_{eq}C_{eq} - R_{eq}^2C_{eq}^2}}{2L_{eq}C_{eq}} \quad (11)$$

Peak values of the fault current occur at the point of a curve, which is  $di_f/dt = 0$ , due to the discharge energy during the DC fault period, as depicted in Figure 8. At this time, the peak current values  $i_{peak}$  are formed at  $T_{peak}$ , as presented in (13).

$$T_{peak} = \frac{1}{Y} \tan^{-1} Y\tau \quad (12)$$

$$i_{peak}(t) = i_f(T_{peak}) = X e^{-\delta t} \sin(\tan^{-1} Y\tau) \quad (13)$$

From (10) and (13), the magnitude of the arm inductance affects the peak of the fault current.

Figure 10 shows the analysis of a circuit in which the polarity of the AC-grid voltage is changed by operating thyristors and turning off the switch of the IGBTs, as depicted in Figure 7. The capacitor voltage in the circuit is applied to each sub-module after the thyristors in the proposed sub-modules are turned on through a control strategy. In its equivalent circuit in Figure 11, the polarity of AC-grid voltage is flipped in the direction opposite to the total sub-module voltage across the converter. The sub-module total voltage is represented by  $V_{cap\_2}$ . Based on the equivalent circuit, the relationship between the AC grid voltage and the total capacitor voltage  $V_{cap\_2}$  in the converter is presented as follows:

$$V_{cap\_2} = 2N \cdot v_{SM} \quad (14)$$

$$V_{ab} - V_{cap\_2} - L_{eq} \frac{di_f}{dt} - R_{eq} i_f \leq 0 \quad (15)$$

where  $V_{ab}$  is the line-to-line voltage between the A phase and B phase. The fault current is limited by the offset effect of the sub-module total capacitor voltage concerning the AC grid voltage in Equation (15).

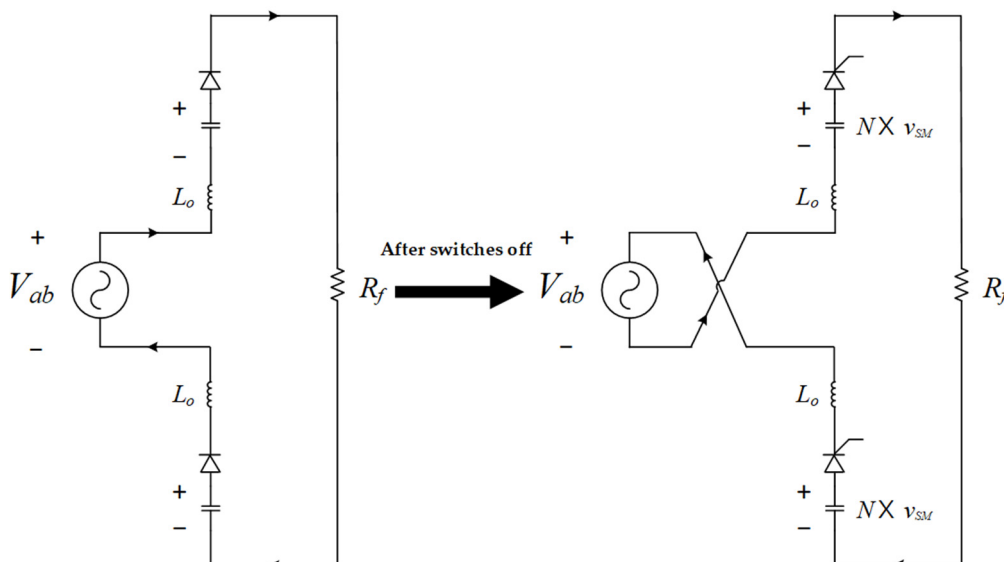
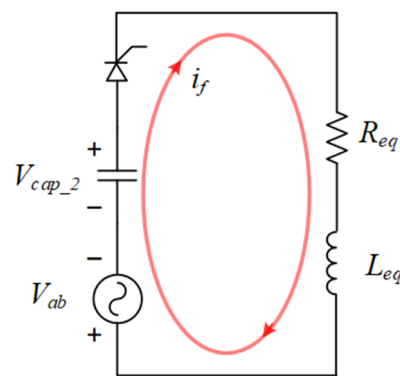
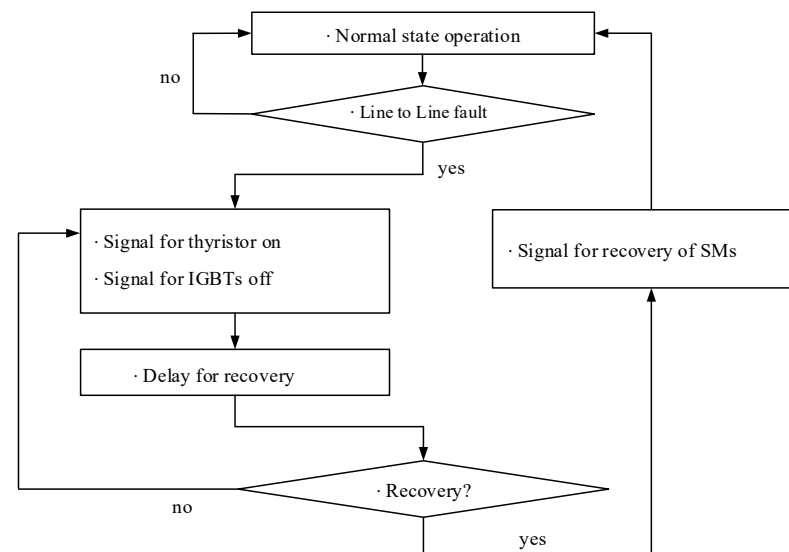


Figure 10. Circuit analysis when operating the proposed sub-modules in accordance with an FRT strategy.



**Figure 11.** Simplified equivalent circuit of an MMC after operating the proposed thyristor in the sub-modules.

Figure 12 shows a control algorithm used to prevent fault current from the event of a permanent DC line-to-line fault in the MMC system. In case of a short-circuit overcurrent due to a DC fault in a normal state of MMC operation, the system turns off all sub-module transistors and activates all thyristors if the system detects arm current that exceeds an initial allowable value. The initial allowable current value is set to two to three times the original value.



**Figure 12.** FRT strategy diagram for DC fault clearance.

The signal for thyristor is sent to induce the voltage clamp down in the circuit by changing the polarity of the AC voltage source in the AC terminal. Then, after the cause of the DC fault is resolved, the system is restored to its original state if the measured value of the fault current is reduced to within tolerance after a certain recovery time.

#### 4. Simulation

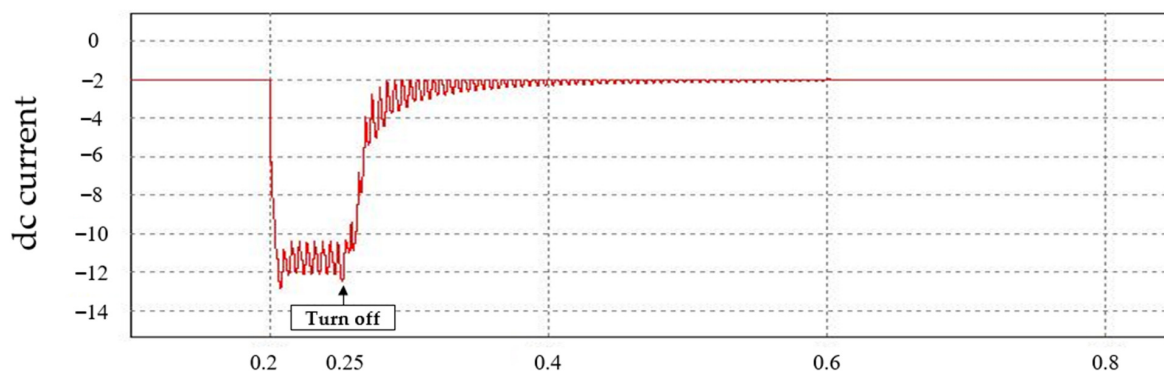
Since this paper mainly concerns FRT capability based on the operation of new topologies in an MMC, the simulation circuit model based on the minimum numbers of sub-modules was employed. The parameters for the simulation are listed in Table 2. First, the verification process started with a permanent DC line-to-line fault occurring at 0.2 s during normal operation. Then, after operation for the FRT strategy based on the proposed sub-module at 0.25 s, the system was restored to the original status at 0.6 s. The control operation included a series process of turning off all IGBTs and RB-IGBTs of the sub-modules,

and turning on all the thyristors in the event of a DC fault. All waveforms were converted into per unit (PU) values.

**Table 2.** Circuit parameters for simulation.

Parameter	Values (Unit)
Rated AC grid voltage	120 kV
AC grid frequency	60 Hz
Rated active power	150 MW
Rated DC voltage	$\pm 120$ kV
Transformer ratio (star delta: Y/D)	1.732
Arm inductance/Line inductance	5 mH/1 mH
Arm resistance	1 $\Omega$
Sub-module capacitance	800 $\mu$ F
Fault resistance	0.1 $\Omega$

Figure 13 depicts the current waveforms on the DC side of the system. During normal operation, when the equilibrium of the three-phase converter is maintained, a potential difference occurs in the DC side line due to a potential difference between the upper and lower arms after the DC fault event. Since the MMC operates in rectifier mode immediately after the switch is turned off, the DC-link current is not immediately attenuated. After the MMC is switched off at 0.25 s, the DC arc starts to attenuate due to the formation of reverse voltage according to the FRT of the sub-module. In addition, an overcurrent is generated on the DC side because of the summed current from the discharge energy and the AC source. However, owing to the sub-modules in the converter at 0.25 s, the fault current in the DC side line also decreases.



**Figure 13.** Simulation results of the DC side of an MMC.

Figure 14 shows the waveform of the AC grid, the arm current in the converter, as well as the sub-module thyristor current. After the DC fault at 0.2 s, the short circuit current is significantly increased owing to the current from discharge energy in the sub-modules and the current flowing continuously from the AC source. However, after 0.05 s, the operation of the thyristor causes the polarity of the voltage in the sub-module to be opposite to that of the AC source voltage. Consequently, the total voltage in the MMC is attenuated, and the magnitude of the current is reduced to a value close to zero.

Figure 14c,d shows the waveforms of the upper and lower arm currents, respectively. The same principle as the AC is applied to the arm current in the short circuit, with the total voltage value in a closed loop being clamped to zero according to the control operation at approximately 0.25 s after the current rises, which decreases the arm current accordingly. The control operation starts with the operation signal of the thyristor. Figure 14e shows the waveform of the thyristor. The current path through the sub-module flows through the thyristor while forming capacitor voltage in all the sub-modules. The internal device of the sub-module is protected by the path bypassing the transistor switch.



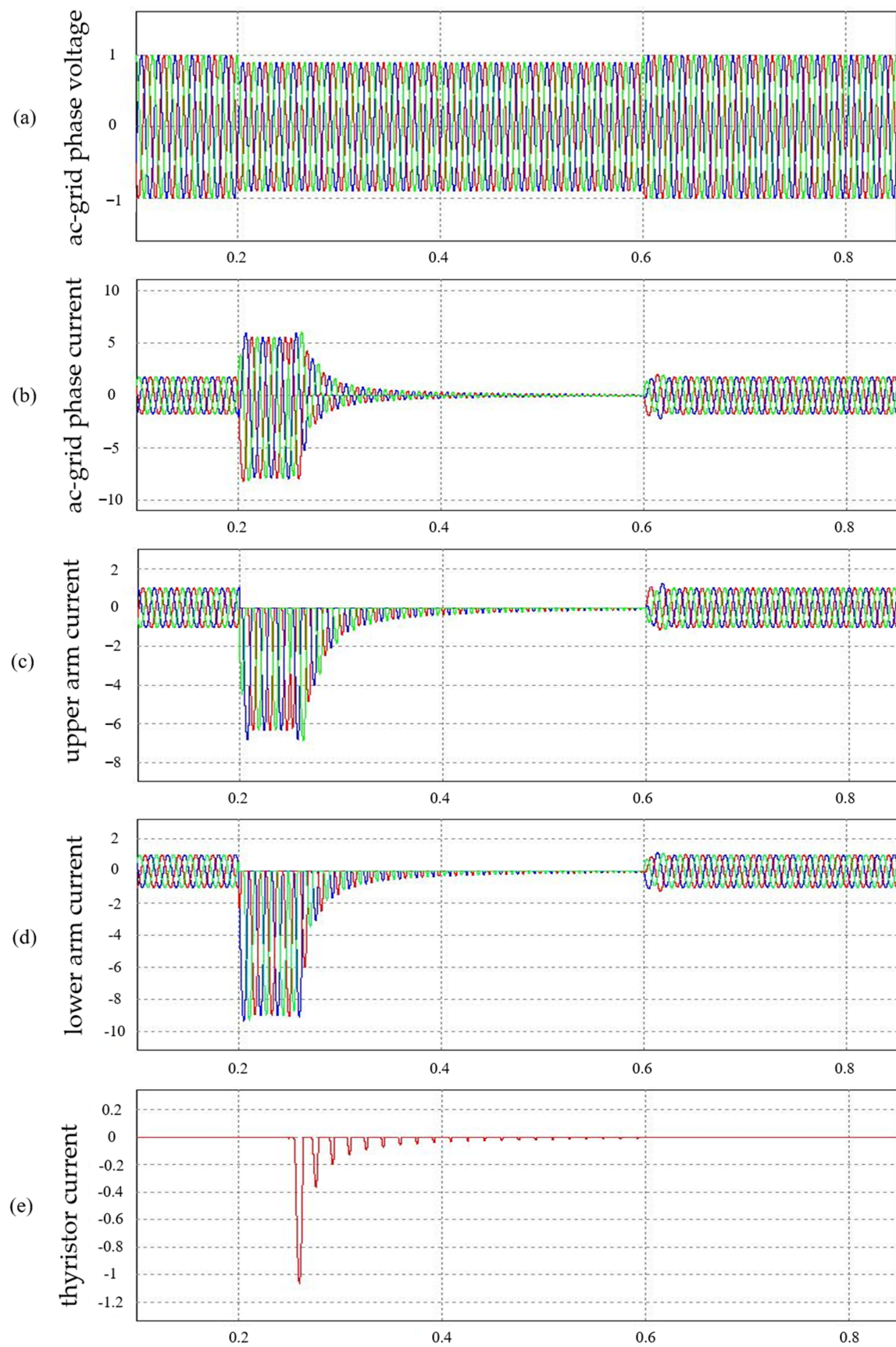


Figure 14. Simulation results of an MMC with the proposed sub-module.

Figure 15a–d shows the waveform of the AC depending on the capacitance magnitude of the sub-module. The sub-module capacitance does not have a significant effect on the peak value of the fault current; nevertheless, it affects the clearance and recovery times depending on its magnitude. That is, as the capacitance gradually increases, the clearance and recovery times of the current in the AC and DC side are relatively increased after the FRT control operation is performed.

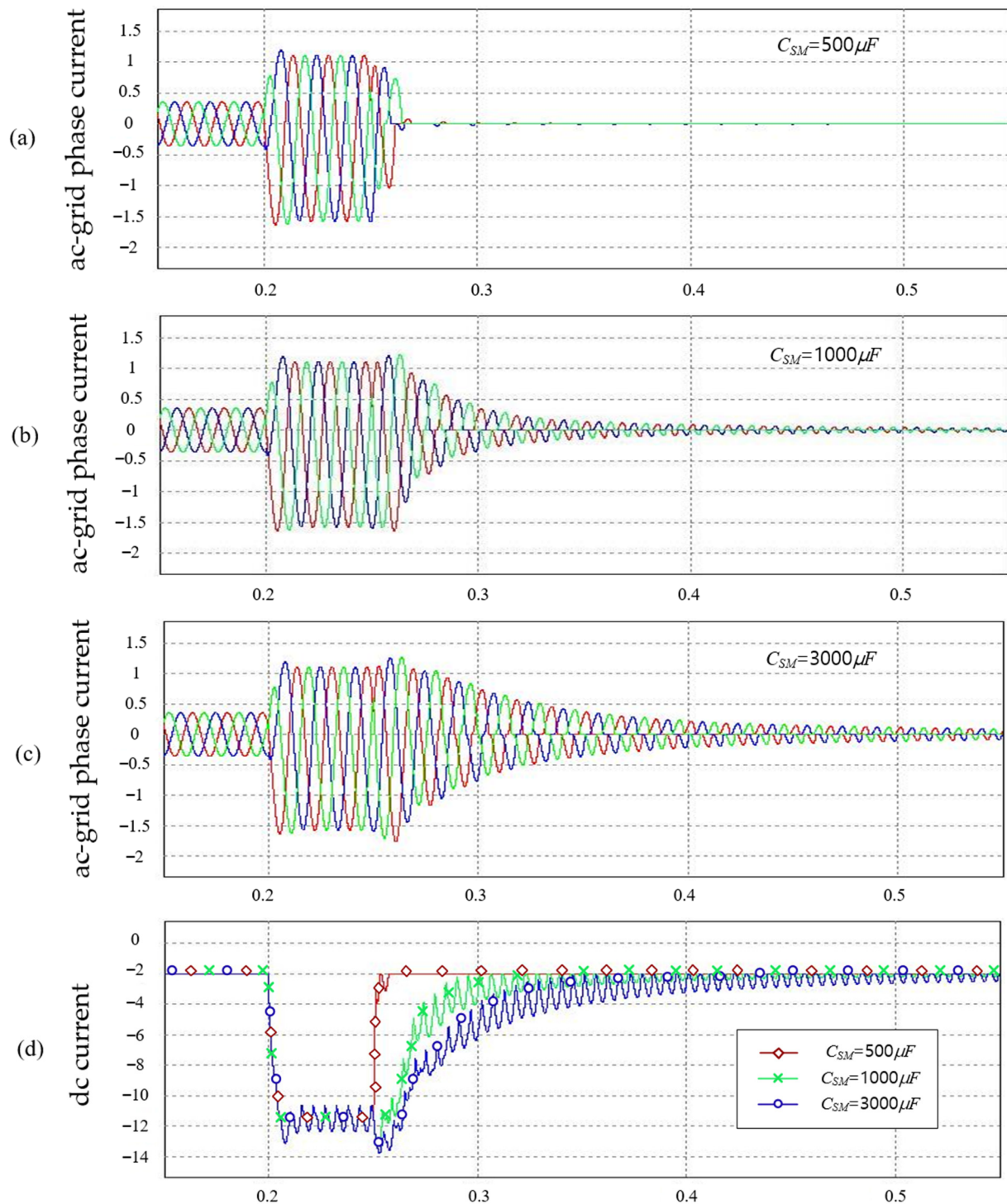


Figure 15. AC and DC current under different sub-module capacitance.

Figure 16 shows the relationship of the DC current magnitude depending on the arm inductance magnitude. In the relationship between the value of the arm inductance and the peak value of the fault current, the current peak value decreases as the inductance value increases, according to (10) and (13). Furthermore, the simulation results in Figure 16 demonstrate the relationship between the magnitude of the arm inductance value and the current peak during a fault situation.

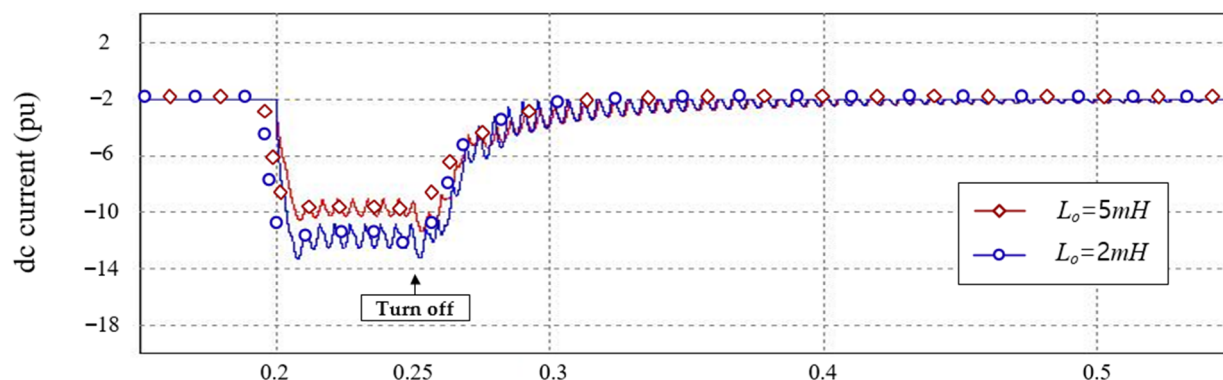


Figure 16. DC current under different arm inductance.

## 5. Conclusions

This paper proposed a method to prevent overcurrent in a converter in case of a short circuit produced by a permanent fault in the DC transmission line of an MMC-based HVDC system. Overcurrent is avoided by adjusting the slope of the total voltage in the short circuit using interacting sub-modules. The proposed sub-module maintains the same modularity of the switching pattern like an HBSM in normal operation, and a reduced number of devices is used in the proposed topology, unlike conventional sub-modules with FRT capability. Additionally, it is capable of generating three voltage levels per cell in normal operation. This shows that it enables a composition with fewer devices and lower power loss sub-modules than conventional topologies by using a new semiconductor switch device.

**Author Contributions:** Conceptualization, U.-J.K. and S.-G.O.; methodology, U.-J.K.; software, U.-J.K.; validation, U.-J.K.; formal analysis, U.-J.K.; investigation, U.-J.K.; resources, U.-J.K.; data curation, U.-J.K.; writing—original draft preparation, U.-J.K.; writing—review and editing, U.-J.K. and S.-G.O.; visualization, U.-J.K.; All authors have read and agreed to the published version of the manuscript.

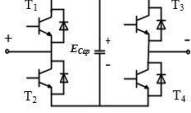
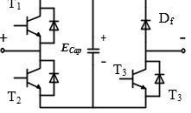
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**Conflicts of Interest:** The authors declare no conflict of interest.

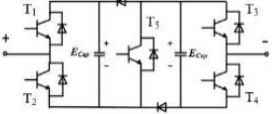
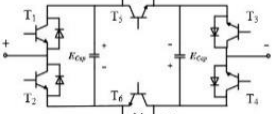
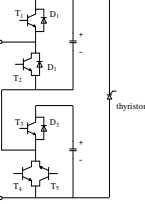
## Appendix A

**Table A1.** Comparison between conventional sub-module topologies with FRT capability (two-level cell).

Sub Module	Full Bridge	Modified Full Bridge
		
0 [V]	T <sub>2</sub> , T <sub>4</sub>	T <sub>2</sub> , T <sub>3</sub>
1E <sub>cap</sub> [V]	T <sub>1</sub> , T <sub>4</sub>	T <sub>1</sub> , T <sub>3</sub>
2E <sub>cap</sub> [V]	-	-
2 times device rated voltage	-	-
Cell voltage per cell (I <sub>f</sub> > 0)	D <sub>1</sub> , D <sub>4</sub> :E <sub>cap</sub>	D <sub>1</sub> , D <sub>3</sub> :E <sub>cap</sub>
Cell voltage per cell (I <sub>f</sub> < 0)	D <sub>2</sub> , D <sub>3</sub> :−E <sub>cap</sub>	D <sub>f</sub> , D <sub>2</sub> :−E <sub>cap</sub>
No. of capacitors per cell	1	1
No. of IGBTs per cell	4	3
No. of extra diodes per cell	-	1
No. of RB-IGBTs per cell	-	-
No. of thyristors per cell	-	-

## Appendix B

**Table A2.** Comparison between conventional sub-module topologies with FRT capability (three-level cell).

Sub Module	Clamp Double	Five Level cross Connected	BHBSM
			
0 [V]	T <sub>2</sub> , T <sub>3</sub> , T <sub>5</sub>	T <sub>1</sub> , T <sub>3</sub> , T <sub>5</sub>	T <sub>2</sub> , T <sub>4</sub> , T <sub>5</sub>
1E <sub>cap</sub> [V]	T <sub>1</sub> , T <sub>3</sub> , T <sub>5</sub>	T <sub>2</sub> , T <sub>4</sub> , T <sub>6</sub>	T <sub>1</sub> , T <sub>4</sub> , T <sub>5</sub>
2E <sub>cap</sub> [V]	T <sub>2</sub> , T <sub>4</sub> , T <sub>5</sub>	T <sub>1</sub> , T <sub>4</sub> , T <sub>6</sub>	T <sub>2</sub> , T <sub>3</sub> , T <sub>5</sub>
2 times of device rated voltage	T <sub>1</sub> , T <sub>3</sub> , T <sub>6</sub>	T <sub>2</sub> , T <sub>3</sub> , T <sub>6</sub>	T <sub>1</sub> , T <sub>3</sub> , T <sub>5</sub>
Cell voltage per cell (I <sub>f</sub> < 0)	-	2ea IGBTs	-
No. of capacitors per cell	(T <sub>5</sub> , D <sub>5</sub> , T <sub>6</sub> , D <sub>6</sub> )	D <sub>2</sub> , D <sub>3</sub> , D <sub>5</sub> :−E <sub>cap</sub>	D <sub>2</sub> , D <sub>4</sub> , D <sub>f</sub> :−2E <sub>cap</sub>
No. of IGBTs per cell	D <sub>2</sub> , D <sub>4</sub> , D <sub>f</sub> :−E <sub>cap</sub>	2	2
No. of extra diodes per cell	5	6	3
No. of RB-IGBTs per cell	2	-	-
No. of thyristors per cell	-	-	1

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