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Generalized Behavioral Modelling Methodology of Switch-Diode Cell for Power Loss Prediction in Electromagnetic Transient Simulation

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Abstract: Modern wide-bandgap (WBG) devices, such as silicon carbide (SiC) or gallium nitride (GaN) based devices, have emerged and been increasingly used in power electronics (PE) applications due to their superior switching feature. The power losses of these devices become the key of system efficiency improvement, especially for high-frequency applications. In this paper, a generalized behavioral model of a switch-diode cell (SDC) is proposed for power loss estimation in the electromagnetic transient simulation. The proposed model is developed based on the circuit level switching process analysis, which considers the effects of parasitics, the operating temperature, and the interaction of diode and switch. In addition, the transient waveforms of the SDC are simulated by the proposed model using dependent voltage and current sources with passive components. Besides, the approaches of obtaining model parameters from the datasheets are given and the modelling method is applicable to various semiconductors such Si insulated-gate bipolar transistor (IGBT), Si/SiC metal–oxide–semiconductor field-effect transistor (MOSFET), and GaN devices. Further, a multi-dimensional power loss table in a wide range of operating conditions can be obtained with fast speed and reasonable accuracy. The proposed approach is implemented in PSCAD/ Electromagnetic Transients including DC, EMTDC, (v4.6, Winnipeg, MB, Canada) and further verified by the hardware setups including different daughter boards for different devices.

Keywords: semiconductor; model; power loss

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1. Introduction

A power electronics (PE) system plays a key role in the process of efficient energy control, conversion, and management. Power semiconductor devices are the core components in a PE system and have a significant impact on system efficiency, reliability, and cost [1]. For decades, silicon-based devices, such as insulated-gate bipolar transistors (IGBTs) [2], metal-oxide-semiconductor field-effect transistors (MOSFETs) [3], are mainly and widely used in various modern PE applications (e.g., Photovoltaics (PV) [4], Power Factor Correction (PFC) [5], power supply [6], and other power converters [7,8]). However, the PE system performance and efficiency are hindered by Si-based devices due to the fundamental material limits. Recently, wide-bandgap (WBG) devices [9–11], such as silicon carbide (SiC) MOSFETs [12], enhancement-mode gallium nitride (eGaN) high-electron-mobility transistors (HEMTs) [13,14], have emerged and gained great popularity due to the superior features of fast switching speed and low switching loss. Thereby, the switching frequency can be further increased bringing the merits of size reduction for magnetic components, high power density, and high efficiency. Whereas the increased power losses of semiconductors are typically the main contributor to total loss especially for high-frequency (HF) applications, and the generated heat energy during switching transition may lead to fatigue failure and affect the reliability [15]. Hence, an accurate power loss model, which

is applicable for different semiconductors and provides a deep insight into the switching process, is highly desirable for device selection and PE system optimization.

Currently, the ideal switch or two-state resistances model is typically adopted in most electromagnetic transient (EMT) simulators such as PSCAD/EMTDC and MATLAB/Simulink [16]. This simple model is mainly used to evaluate the overall system response and control strategy, and only the conduction loss is roughly considered. The conduction loss can be directly determined by the output curves in the datasheet, while the switching loss is more complicated and can be measured in the double-pulse test (DPT) [17]. Although DPT is widely used and can achieve high accuracy, it typically involves expensive probes and much peripheral bulky equipment such as a high voltage power supply. Designing a testing board with low parasitics is challenging and also significant for WBG devices due to the fast switching. Recently, several physic-based semiconductor models [18–21], such as simulation program with integrated circuit emphasis (SPICE) models [22,23], have been proposed to accurately describe the transient behaviors of the devices. However, the geometrical parameters for the model are often not available in the datasheet and thus the applicability of the model is limited. Another type of model (i.e., behavioral model [24,25]) has been developed, which focuses more on the external behaviors of the devices instead of the internal physics. As a result, the complexity is reduced and fast simulation speed can be achieved. It is adequate and widely used for system-level study, but more detailed transient concerns are needed to accurately evaluate the switching performance and estimate the power losses.

To have a better description of the switching transients, a lot of analytical loss models have been proposed [26,27]. Piecewise linearizing the switching process of the device is a commonly used method which enables simple and rapid loss estimation [28]. Whereas, the accuracy is still limited due to the ignorance of the parasitics. To improve it, more comprehensive loss models are developed considering various factors, such as temperature-dependent parameters [29,30], interactions between diode and switch [31], cross-talk issue [32], displacement current [33,34], and non-flat miller plateau [35]. Thereby, the switching loss can be obtained by solving the equivalent circuit for each switching sub-stage. Further, the entire switching process of eGaN HEMT in synchronous buck converter application is presented in [36,37] considering the third quadrant operation with the help of the 2-dimensional electron gas (2DEG). However, these methods are complicated involving huge computational burdens, not to mention the convergence issue. The measurement techniques and loss distribution including the capacitive losses for eGaN HEMT are illustrated in [38,39] and the scalable loss estimation method is further proposed based on the measurements. However, the measured data in the datasheet is typically under specific conditions, which limits the applicability and accuracy.

In a PE system, a power switch is typically paired with a diode as a switch-diode cell (SDC) to provide current commutation [40]. This basic commutation cell as shown in Figure 1a is widely used in PE applications and it consists of the active power switch (S), diode (D), equivalent circuit voltage (V_{dd}) and load current (I_{L}) [41]. Note that, four configurations of S, namely Si/SiC MOSFET, Si IGBT and eGaN HEMT, are taken into account in this paper and D can be a single positive-intrinsic-negative (PIN) diode, a Schottky barrier diode (SBD), the body diode of MOSFET or the equivalent diode of eGaN HEMT. During switching transition, power loss is resulted mainly from the switching and conduction losses of S as well as the conduction loss and reverse recovery loss of D. In order to estimate these power losses in a PE system, a generalized behavioral modelling method of switch-diode cell in electromagnetic transient simulation (EMT) is proposed and it is an extension of previous work [42–45]. There are three technical contributions in this paper comparing with the conventional methods.

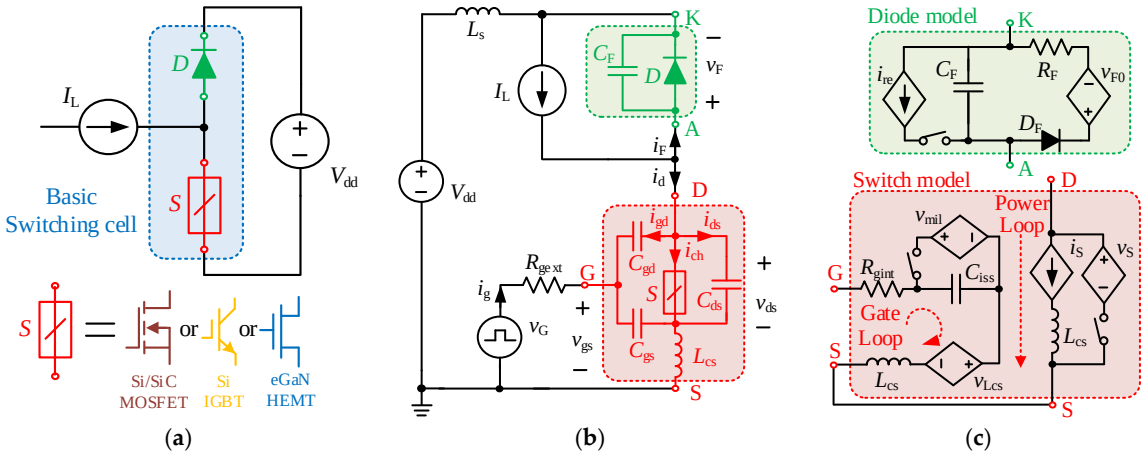


Figure 1. Schematic diagrams of (**a**) switch-diode cell circuit; (**b**) DPT circuit; (**c**) Proposed switch and diode models.

- A generalized behavioral model of SDC is proposed which is realized by dependent sources with passive components considering the impacts of parasitics, the temperature-dependent parameters, and the reverse recovery behavior of *D*. This model is not limited to a specific device and it is applicable to various devices including Si/SiC MOSFET, Si IGBT, and eGaN HEMT. In addition, most of the model parameters can be obtained from the device datasheets by the curve fitting method and no additional measurement is involved. Based on the specific requirement, the model can be modified and integrated into different simulators accordingly.
- The switching process of the switch-diode cell in a clamped inductive switching circuit is studied analytically based on the equivalent circuits for each switching sub-stage. Accordingly, the semiconductor model is developed and implemented in PSCAD/EMTDC. The switching analysis in this paper is more comprehensive considering the respective features of different devices such as the tail current of IGBT and the third quadrant operation of eGaN HEMT.
- A DPT setup was designed for experimental verification. To meets the different requirements of different semiconductors, three daughter boards were specifically designed incorporating with the main control board to characterize various devices and measure the corresponding power losses in a wide range of operating conditions. The simulated results are compared with the experimental results and show good agreements within 10% average error range.

2. Model Description

The simulation procedure of the proposed model is demonstrated in Figure 2. Initially, the device requirements for the desired PE application (e.g., voltage, current, temperature, and frequency) are determined. Based on those requirements, a specific semiconductor device is preliminarily selected for modelling and characterization. According to the device's datasheet, the key model parameters can be extracted by the curve fitting method. Afterwards, the model parameters together with the operating conditions are input to the proposed device model, and a DPT simulation using the proposed model is further carried out. Subsequently, the transient voltage and current waveforms can be obtained, and simultaneously the power loss of the device can be computed. If the simulated results, in terms of switching transient behaviors and power loss, meet the requirements within the acceptable range, then the semiconductor is eventually selected for this application. Otherwise, it is necessary to reselect another device and evaluate the performance until the design is optimized.

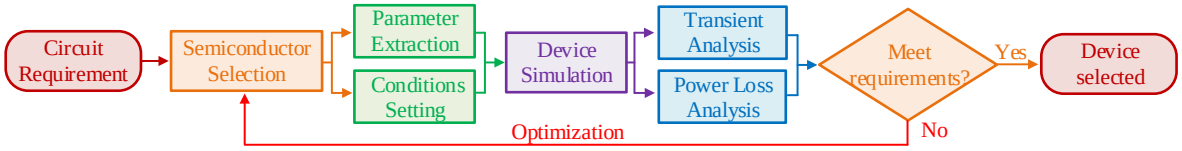


Figure 2. Flow chart of the proposed modelling procedure.

In order to understand the switching behaviors of the SDC, a diode-clamped inductive load circuit (i.e., DPT circuit) is taken as an example which is widely used for device characterization. As shown in Figure 1b, the basic commutation unit consists of two complementary switches, one operates as a freewheeling diode D and the other is an active switch S controlled by the gate drive voltage (v_G) through the external gate resistance R_{gext}. In a typical hard-switching PE system, S is identified by a positive drain current i_d (collector current i_c for IGBT) direction matching with the direction of I_L. Since the commutation time is sufficiently short, I_L and V_{dd} are hardly changing during switching transition and thus they are treated as constant current and voltage sources, respectively.

Note that, the crucial circuit parasitic elements are also included as shown in Figure 1b. All the stray inductances in the power loop including the printed circuit board (PCB) trace and device package inductance are lumped and represented by L_s, while the common source inductance (L_{cs}) of S is considered separately. In addition, the parasitic capacitances of S include gate-drain capacitance (C_{gd}), gate-source capacitance (C_{gs}) and drain-source capacitance (C_{ds}). Besides, the equivalent capacitance of D (C_F) denotes for junction capacitance of diode. It should be mentioned that when D is configured as the body diode of a switch rather than a single diode, C_F will be the corresponding parasitic capacitance of the switch. During a switching transition, I_L commutates between S and D. When a positive v_G is given, the gate-source voltage (v_{gs}) will increase to turn on S. Subsequently, i_d including the channel current (i_{ch}), the gate-drain current (i_{gd}) and the drain-source current (i_{ds}) starts rising, meanwhile the diode forward current (i_F) declines gradually. When S is fully turn on, the drain-source voltage (v_{ds}) decreases to the on-state voltage and the diode forward voltage (v_F) rises to V_{dd}. The behavioral models of a SDC as illustrated in Figure 1c are proposed to reproduce the switching behaviors of S and D, respectively. The details of the model descriptions including the active switch and diode model are presented as follows.

2.1. Active Switch Model

As shown in Figure 1c, the proposed active switch model consists of two parts, the gate loop and the power loop. It is noted that L_{cs} is shared by both loops and thus each loop includes one L_{cs} in order to decoupling both loops. Additionally, a dependent voltage source (v_{Lcs}) is added in the gate loop to reflect the interactive impact of the current source (i_S) on L_{cs} as expressed by,

$$v_{Lcs} = L_{cs} \cdot di_S/dt \quad (1)$$

- Gate Loop Part

The external v_G is typically flipped between V_{gon} (20 or 15 V) and V_{goff} (−5 or 0 V) based on the specific gate drive requirement of the switch. The device internal gate resistance (R_{gint}) is merged into R_{gext} as the total gate resistance (R_G). Furthermore, the gate related junction capacitances (i.e., C_{gd} and C_{gs}) are represented by the input capacitance (C_{iss}) and an additional dependent voltage source (v_{mil}). This equivalent v_{mil} becomes valid only when the miller plateau occurs on v_{gs} during switching transition and its value can be computed by

$$v_{mil} = v_{th} + i_{ch}/g_{fs} \quad (2)$$

where v_{th} and g_{fs} stand for threshold voltage and transconductance of a switch, respectively. Additionally, i_{ch} during miller plateau period typically equals to I_L which will be discussed in Section 2.3.

It is noted that the gate inductance is neglected here for simplicity although it can introduce a slight delay on v_{gs}. In fact, this delay is mainly resulted from L_{cs} and v_{Lcs} due to the fast change of i_d. Besides, the gate drive circuit is normally placed close to S in order to minimize the potential oscillation introduced by the gate inductance and thus this inductance is negligible.

- Power Loop Part

In this model, i_d is represented by i_S which is the sum of i_{ch}, i_{gd} and i_{ds}. Note that, most of the time, i_S is the same as i_{ch} except for the voltage transition period when a displacement current is introduced due to the process of charging and discharging of the parasitic capacitance. In order to reflect the voltage change during switching transition as well as the on-state voltage (v_{on}) of S, an equivalent dependent voltage source (v_S) is adopted here. The value of v_{on} can be determined by $R_{ds(on)}$ with I_L in (3) or the saturation voltage (v_{cesat}) for the case of IGBT.

$$v_{on} = R_{ds(on)} \cdot I_L. \tag{3}$$

Besides, L_{cs} is also included in the power loop part which is associated with L_s to influence the transient waveforms. Thereby, the gate loop and power loop parts are decoupled and their interaction is represented by the equivalent dependent sources instead of nonlinear junction capacitances resulting in a reduction of model complexity.

2.2. Diode Model

The static model of a diode typically can be represented by an ideal diode (D_F), a forward resistance (R_F) and a voltage source (v_{F0}) based on the forward characteristics in the device datasheet. Typically, v_F of the diode can be computed by,

$$v_F = R_F \cdot i_F + v_{F0}. \tag{4}$$

It should be mentioned that, for the case of eGaN HEMT as D, the diode behavior is realized by 2DEG and thus the calculation of v_F is based on the reverse conduction characteristic of the GaN device [44] which is highly affected by the gate drive voltage (v_{GF}) of GaN device as shown in (5),

$$v_F(\text{GaN}) = R_{Fr} \cdot i_F + v_{thF} - v_{GF} \tag{5}$$

where R_{Fr} and v_{thF} are on-resistance in the third quadrant and threshold voltage of a GaN device, respectively. Since negative v_{GF} is typically provided to avoid the cross-talk issue, higher v_F is thus resulted which will increase the conduction loss of D. Notice that, if a positive v_{GF} is provided enabling the channel fully on, the on-state resistance will be the same value in the first quadrant.

Moreover, the dynamic characteristic of D is described by C_F in parallel with an equivalent dependent current source (i_{re}) for the reverse recovery behavior of D. When D switches from forwarding conduction to off-state, i_F cannot be eliminated immediately and it takes a while to extinguish the excess carriers, this time is called reverse recovery time (t_{rr}). The reverse recovery process occurs as soon as i_F becomes negative, i_{re} can be expressed by [45],

$$i_{re} = \begin{cases} di_F/dt \cdot t, \ t < t_{rm} \\ I_{rm} \cdot \exp((t - t_{rm})/\tau_{re}), \ t \geq t_{rm} \end{cases}, \tag{6}$$

where τ_{re} denotes decay time constant and i_{re} reaches the peak current (I_{rm}) at time t_{rm}. In addition, the slew rate of diode current (di_F/dt) typically keeps the same as the turn-off slew rate of S. It needs to notice that, this reverse recovery behavior commonly exists in PIN diode and body diode of S, while the reverse recovery loss is eliminated for the case of SBD or eGaN HEMT and thus i_{re} can be neglected for simplicity. In fact, in these cases,

the effect of C_F is the main concern which can introduce displacement current resulting in capacitive loss during switching transition.

2.3. Switching Transient Modelling

The switching process of the SDC in the DPT circuit is thoroughly analyzed based on the switching waveforms and the equivalent circuits as follows.

- Turn-on transition ($t_0 - t_3$)

The typical turn-on waveforms along with power loss information are illustrated in Figure 3 considering the case of PIN or body diode as well as the case of SBD or eGaN HEMT. The equivalent circuits during this period are also provided in Figure 4.

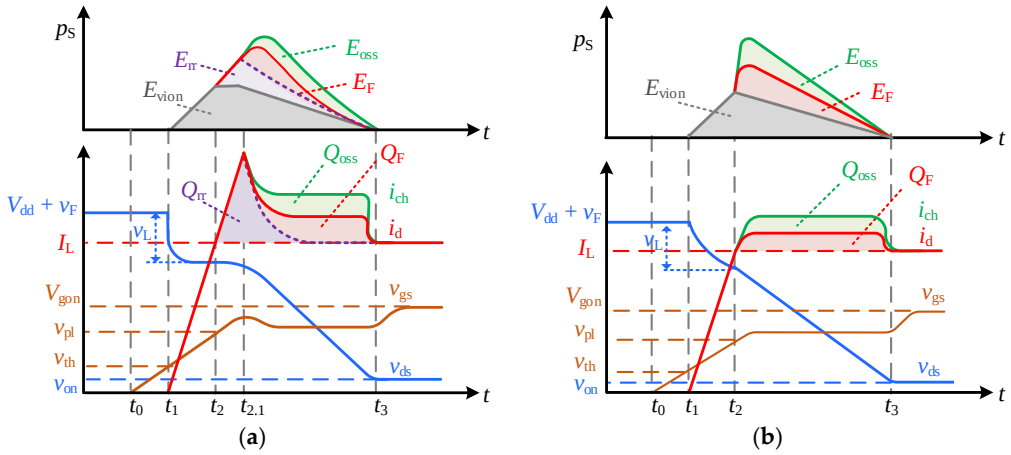


Figure 3. Typical turn on waveforms for S with D (**a**) PIN or body diode; (**b**) SBD or eGaN HEMT.

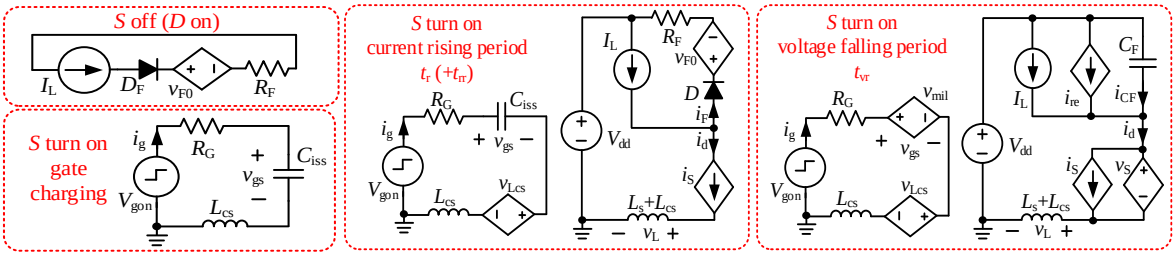


Figure 4. Simplified equivalent circuits during S turn on transition.

Initially, S is in the off-state, and all the I_L flows through D. The corresponding v_F can be estimated by (5). At t_0, the gate charging period begins with a positive V_{gon} applying to v_G and C_{iss} is charged up through R_G. Subsequently, v_{gs} will increase accordingly with the time constant ($\tau_{iss} = R_G \cdot C_{iss}$). Note that L_{cs} in the gate loop will prolong the turn-on time causing more power losses.

The current rising period begins when v_{gs} goes beyond v_{th}. During this interval, the conductive channel of S is forming and i_S starts rising from zero to I_L which can be expressed by

$$i_S = g_{fs} \cdot (v_{gs} - v_{th}). \quad (7)$$

The fast change of i_S on one hand, will introduce a negative feedback v_{Lcs} from power loop to gate loop due to L_{cs} to further delay the turn-on process. On the other hand, it will result in a total voltage drop (v_L) on L_s and L_{cs}. Simultaneously, v_{ds} decreased by v_L as shown in Figure 3.

As I_L commutates from D to S, i_S reaches I_L at t_2 and v_{gs} will be clamped at v_{mil}. At the same time, i_F decreases to zero and D enters into the reverse recovery as shown in Figure 3a. This additional i_{re} will add to i_S (= I_L + i_{re}) resulting a current spike and thus

a bump in v_{gs} according to (2). When i_{re} reaches I_{rm}, it starts declining and the voltage falling period begins. Subsequently, v_{ds} starts decreasing which is controlled by v_S and the corresponding slew rate can be determined by,

$$dv_{ds}/dt = dv_S/dt = -\left(V_{gon} - v_{mil} - v_{Lcs}\right)/\left(C_{gd}{\cdot}R_G\right). \tag{8}$$

As v_{ds} keeps decreasing and v_F increases simultaneously, the output capacitance (C_{oss}) of S and C_F of D is discharged and charged, respectively. Since the voltage of C_{oss} and C_F are clamped to V_{dd}, they share the same absolute value of voltage change. The resultant capacitive displacement current for C_{oss} (i_{oss}) can be expressed by (9). Additionally, this i_{oss} along with the counterpart for C_F ($i_{CF} = -C_F{\cdot}dv_{ds}/dt$) will affect i_d as can be seen in Figure 3. By applying Kirchhoff's law, i_d can be determined by (10) and i_S is modified accordingly to consider these displacement currents.

$$i_{oss} = i_{gd} + i_{ds} = C_{oss}{\cdot}dv_{ds}/dt \tag{9}$$

$$i_d = i_S = I_L + i_{re} - C_F{\cdot}dv_{ds}/dt \tag{10}$$

Based on Figure 1b along with the above equations, i_{ch} can be further obtained,

$$i_{ch} = i_d - i_{oss} = I_L + i_{re} - (C_{oss} + C_F){\cdot}dv_{ds}/dt \tag{11}$$

Consequently, during this period, i_d includes I_L, i_{re} and i_{CF}, while the additional i_{oss} is further added to i_{ch} as shown in Figure 3. As a result, v_{mil} will also change according to (2). This period ends when v_{ds} drop to v_{on} at t_3. Thereafter, v_{gs} will continue climbing until reaches V_{gon}.

Furthermore, the turn-on waveforms for the case of SBD or eGaN HEMT are presented in Figure 3b. Since the reverse recovery behavior is neglected for these cases as mentioned previously, i_{re} keeps zero and the voltage falling period starts right after i_S reaches I_L. Apart from that, the turn-on modelling and analysis are the same as the case of the PIN diode.

- Turn-off transition ($t_4 - t_7$)

The turn-off process can be considered as the opposite of turn-on transition and the typical transient waveforms are illustrated in Figure 5. In order to turn off S, V_{gon} is replaced by a negative gate drive signal V_{goff} and thus C_{iss} is discharged through R_G resulting the reduction of v_{gs}. As v_{gs} drops to v_{mil}, C_{gd} absorbs nearly all the i_g and thus v_{ds} begins to rise which again causes a current decline of i_d. When v_{ds} reaches V_{dd}, the miller plateau disappears and i_d begins decreasing with v_{gs} which results an additional v_L on v_{ds} as shown in Figure 5a.

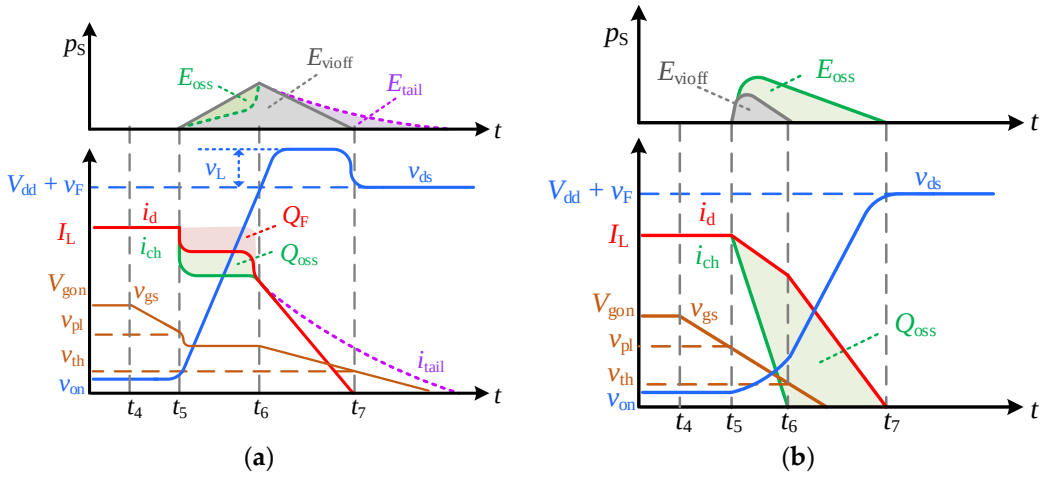


Figure 5. Typical turn off waveforms for S as (**a**) Si IGBT or Si/SiC MOSFETs; (**b**) Typical eGaN HEMT.

As v_{gs} drops below v_{th}, i_d becomes zero and S turns off completely. However, for the case of Si IGBT, the tail current (i_{tail}) is considered due to the recombination of the excess carriers. This i_{tail} will prolong the turn off time and can be modelled by the exponential function [42],

$$i_{tail} = I_{tail0} \cdot \exp(-(t - t_{tail0})/\tau_{tail}) \quad (12)$$

where τ_{tail} stands for carrier transit time and the tailing period starts at t_{tail0} with the initial value of I_{tail0}. These parameters can be estimated from the turn-off current waveform.

As can be seen from Figure 5b, a notable difference for the case of eGaN HEMT is v_{gs} does not typically plateau due to the much smaller capacitance and it keeps decreasing until reaches V_{goff}. As a result, i_{ch} quickly declines synchronized with v_{gs} based on (7), meanwhile v_{ds} rises slightly and the slew rate is limited by the relatively high C_{oss} at low v_{ds}. In fact, the channel turns off completely before v_{ds} is significantly rising. However, i_d does not follow the fast decreasing i_{ch} since its changing rate is limited by the inductances in the power loop. Additionally, C_{oss} is charged by the current difference between i_d and i_{ch} resulting a slight increase of v_{ds} which can be expressed as

$$dv_{ds}/dt = dv_S/dt = (i_d - i_{ch})/C_{oss} \quad (13)$$

Meanwhile, C_F is discharged resulting in a reduction of v_F. Additionally, i_d thus can be obtained by

$$i_d = i_S = I_L - C_F \cdot dv_F/dt \quad (14)$$

Once v_{gs} drops below v_{th}, namely i_{ch} becomes zero, the channel shuts down and I_L is shared by C_{oss} and C_F. During this period, v_{ds} keeps rising according to (14). When v_{ds} rises to V_{dd}, I_L starts commuting to D and the S turn-off transition finishes. Note that if very high R_G is used for eGaN HEMT, the turn-off analysis will be the same as the case of MOSFET as shown in Figure 5a.

Based on the above analysis v_S can be considered as an open circuit except for voltage rising/falling periods and S on-state. During the voltage transition period, v_s is modelled as a dependent voltage source with a voltage slew rate as mentioned previously. In addition, the key expressions of i_S for different conditions can be summarized in Table 1. It is noted that when v_{gs} is less than v_{th}, the conduction channel is not established and theoretically, no current is flowing through the device. As a result, i_S is modelled with zero ampere under this condition in PSCAD/EMTDC which can be considered as open circuit. In this paper, all analytical equations for v_s and i_s are implemented and programmed with conditions in the custom programming modules in PSCAD. In this way, it is feasible and convenient to make any modifications as necessary.

Table 1. Key expressions for i_S in the proposed model.

i_S	Condition	$v_{gs}<v_{th}$	$i_d<I_L$	$i_d>I_L$	Tail Period for IGBT	Turn-off for eGaN HEMT
	Expression	0	(7)	(10)	(12)	(14)

3. Power Loss Analysis and Parameter Extraction

In general, the power losses of SDC mainly include conduction loss and switching loss. Typically the conduction losses of S and D can be calculated directly as the product of operating current (i.e., I_L) and the on-state voltage drop based on (3–5). In addition, the reverse recovery loss of D can be estimated based on the reverse recovery charge (Q_{rr}) and v_F from the device datasheet and the switching loss of S is analyzed as follows.

3.1. Turn on Loss(E_{on})

The instantaneous power of S (p_S) along with E_{on} are presented in Figure 3. Basically, E_{on} consists of the turn-on V-I overlap loss (E_{vion}), the reverse recovery related loss (E_{rr}) and the capacitive losses (E_{oss} and E_F) for C_{oss} and C_F, respectively. E_{vion} graphically can

be divided into two parts, the i_d rising period and v_{ds} decreasing period. Hence, E_{vion} can be expressed as

$$E_{vion} = \int_{t_1}^{t_2} v_{ds} \cdot i_d dt + I_L \cdot \int_{t_2}^{t_3} v_{ds} d \tag{15}$$

Since reverse recovery behavior of D and the displacement current of C_{oss} already have been considered in the modelling of i_S, therefore the sum of E_{vion}, E_{rr} and E_{oss}, which is actually the measured turn-on loss (E_{onm}), can be directly obtained by integrating i_d and v_{ds}. This significantly reduces the complexity comparing with the analytical loss model by computing the switching time for each sub-stages. Moreover, according to (11), both the discharging current of C_{oss} and charging current of C_F are flowing through the channel of S and thus these capacitive energy losses (i.e., E_{oss}, E_F) are dissipated into the channel. Based on the capacitance curves, E_{oss} can be expressed as

$$E_{oss} = \int_0^{V_{dd}} v_{ds} \cdot C_{oss} dv_{ds} \tag{16}$$

Since the charging current of C_F is provided by V_{dd} and part of the energy is stored in C_F, thus the energy loss dissipated in the channel (i.e., E_F) can be derived based on the charge of C_F (Q_F),

$$E_F = V_{dd} \cdot Q_F - \int_0^{V_{dd}} v_F \cdot C_F dv_F = \int_0^{V_{dd}} (V_{dd} - v_F) \cdot C_F dv_F \tag{17}$$

Consequently, E_F theoretically should also be included in E_{on} which can be expressed as,

$$E_{on} = E_{onm} + E_F = \int_{t_1}^{t_3} i_d \cdot v_{ds} dt + E_F \tag{18}$$

3.2. Turn off Loss(E_{off})

Generally, the power loss during turn-off transition occurs from t_5 to t_7 which includes the turn-off V-I overlap loss (E_{vioff}), E_{oss} and the tailing loss for the case of IGBT (E_{tail}). The analysis of E_{vioff} is significantly different for the slow-switching scenario in Figure 5a and the typical fast-switching for eGaN HEMT in Figure 5b. As for the former case, v_{gs} is fixed at v_{mil} and thus i_d is relatively constant throughout the voltage rising period. Thereafter, i_d decreases significantly meanwhile v_{ds} keeps relatively constant. Hence, E_{vioff} for this case can be graphically calculated as

$$E_{vioff} = \int_{t_5}^{t_6} v_{ds} \cdot i_d dt + \int_{t_6}^{t_7} (V_{dd} + v_L) \cdot i_d d \tag{19}$$

Similarly, the sum of E_{vioff} and E_{tail}, namely the measured turn-off loss (E_{offm}), is typically an integral of i_d and v_{ds}. It is noticed that, C_F is discharged and the energy is transferred to the inductive load during the voltage rising period resulting in a reduction of i_d, while C_{oss} is charged and the corresponding energy (i.e., E_{oss}) is stored which will be dissipated in the next turn-on transition. Therefore, E_{oss} should be theoretically excluded from E_{off} which can be expressed as

$$E_{off} = E_{offm} - E_{oss} = \int_{t_5}^{t_7} v_{ds} \cdot i_d dt - E_{oss} \tag{20}$$

As for the typical eGaN HEMT scenario, v_{gs} skips the plateau and the channel turns off quickly before v_{ds} rises significantly as discussed previously. Afterwards, the energy is commutating between the inductive load and the two capacitances (i.e., C_F and C_{oss}) which is almost lossless. Since the resistive overlap loss only occurs as long as the channel is on, it is significantly reduced for this case due to the relatively low v_{ds} during this time. Nevertheless, E_{off} still can be calculated by (20).

3.3. Parameter Extraction

The key model parameters can be directly extracted from the corresponding curves provided in the device datasheet by the curve fitting method [46–48], to avoid the supplementary experiments which are usually not practical. This method is adopted in this paper since it is applicable to different semiconductor devices and provides a relatively balanced tradeoff between accuracy and practicability. As an example, different types of semiconductors from different manufacturers as listed in Table 2 are selected for modelling and validation of the proposed method. The extracting sequence is discussed in detail as follows.

Table 2. Semiconductor devices selected for modelling and validation.

Device Type	Si IGBT	SiC MOSFET	Si MOSFET	eGaN HEMT	SiC SBD
Part Number	IKW40T120	SCT2080KE	NVHL072N65S3	GS66506T	SCS220KG
Manufacturer	Infineon	Rohm	On Semiconductor	GaN System	ROHM

- Static characteristic

In order to reproduce the switching behavior of S, two key parameters (i.e., v_{th} and g_{fs}) are considered first. Since v_{th} typically is a temperature-dependent parameter rather than a constant value, it can be fitted by the 2nd order polynomial of junction temperature (T_{j}) from the corresponding curve in the datasheet. Likewise, the transfer characteristic of S can be fitted by the quadratic function of v_{gs} and subsequently g_{fs} can be further determined based on v_{th} and (7) as

$$g_{\mathrm{fs}} = i_{\mathrm{s}} \cdot \sqrt{k_{\mathrm{ga}} / \left(i_{\mathrm{s}} - k_{\mathrm{gb}}\right)} \cdot k_{\mathrm{gTa}} \cdot \left(T_{\mathrm{j}} / T_{\mathrm{a}}\right)^{k_{\mathrm{gTb}}} \tag{21}$$

where k_{ga}, k_{gb}, k_{gTa}, and k_{gTb} are fitting constants. T_{a} is room temperature which is considered as 25 °C here. In this way, g_{fs} under the given T_{j} in datasheet can be obtained. The fitted results of transfer characteristics are compared and shown in good agreement with the datasheet in Figure 6. It is also found that there is a positive correlation between T_{j} and g_{fs} for Si IGBT and Si/SiC MOSFET while it shows a negative correlation for the case of eGaN HEMT.

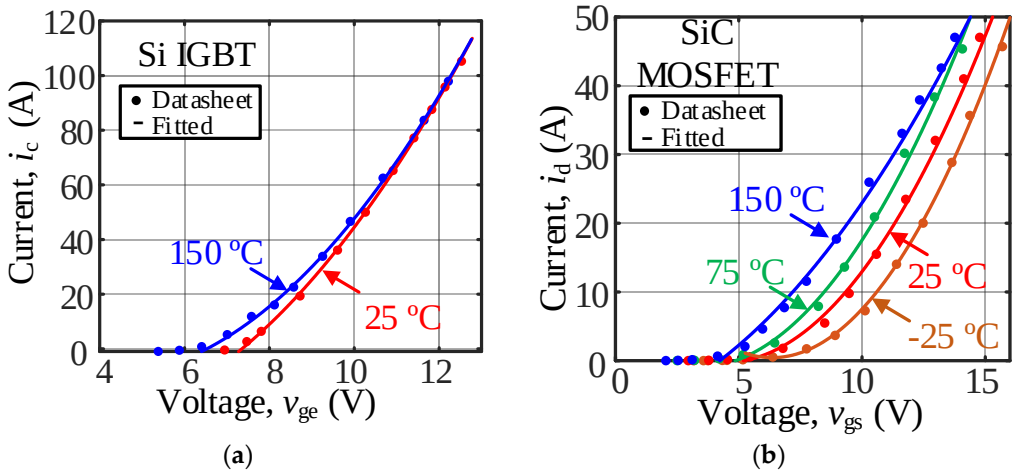


Figure 6. *Cont.*

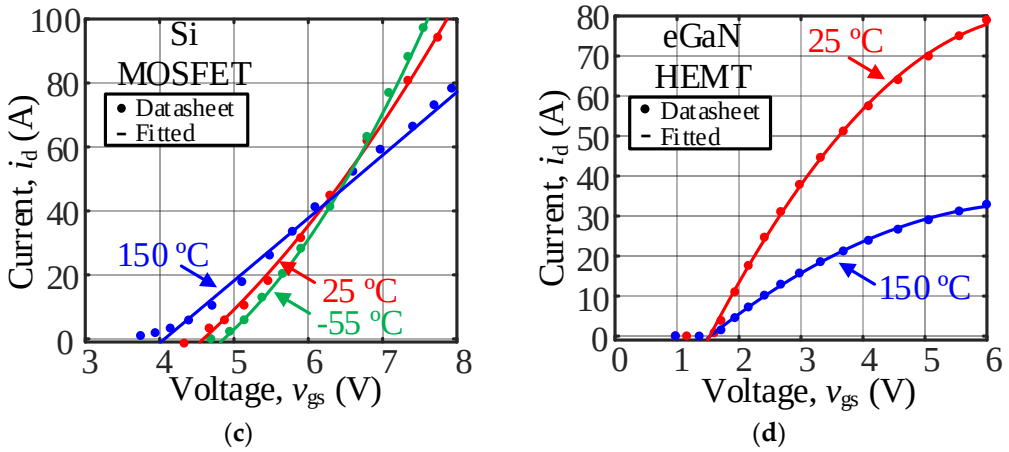


Figure 6. Fitted results of transfer curves for (**a**) Si IGBT; (**b**) SiC MOSFET; (**c**) Si MOSFET; (**d**) eGaN HEMT.

Furthermore, in order to represent the on-state characteristic of S as expressed in (3), the parameter v_{cesat} for IGBT or $R_{\mathrm{ds(on)}}$ for other cases is needed to be extracted. Typically, both of v_{cesat} and $R_{\mathrm{ds(on)}}$ are affected by T_{j} and i_{S} according to the curves in the datasheet. Therefore, v_{cesat} can be obtained by the following Equation (22).

$$v_{\mathrm{cesat}} = (k_{\mathrm{cea}} + r_{\mathrm{cea}} \cdot i_{\mathrm{S}}) + (k_{\mathrm{ceb}} + r_{\mathrm{ceb}} \cdot i_{\mathrm{S}}) \cdot (T_{\mathrm{j}} - T_{\mathrm{a}}) \tag{22}$$

where k_{cea}, r_{cea}, k_{ceb} and r_{ceb} are fitting coefficients. Note that the gate voltage is assumed as constant in the parameter extraction for simplicity.

Likewise, $R_{\mathrm{ds(on)}}$ for the cases of MOSFET and eGaN HEMT can be extracted by

$$R_{\mathrm{ds(on)}} = (k_{\mathrm{ona}} + r_{\mathrm{ona}} \cdot i_{\mathrm{S}}) + (k_{\mathrm{onb}} + r_{\mathrm{onb}} \cdot i_{\mathrm{S}}) \cdot (T_{\mathrm{j}} - T_{\mathrm{a}}) \tag{23}$$

where k_{ona}, r_{ona}, k_{onb} and r_{onb} are fitting coefficients. Based on the above equations, the key parameters for different semiconductors in this paper can be extracted and illustrated in Table 3.

Table 3. Key fitting coefficients parameters of different semiconductors.

Parameter	k_{ga}	k_{gb}	k_{gTa}	k_{gTb}	k_{cea},k_{ona}	r_{cea},r_{ona}	k_{ceb},k_{onb}	r_{ceb},r_{onb}
Si IGBT	2.05	−6.96	14.2	−0.012	−0.001	$1{\cdot}10^{-4}$	0.972	0.0215
SiC MOSFET	0.42	−0.35	2.96	−0.086	$4.1{\cdot}10^{-4}$	$1.12{\cdot}10^{-6}$	0.073	$5.1{\cdot}10^{-4}$
Si MOSFET	3.72	−19.2	13	−0.57	0.048	$2.87{\cdot}10^{-3}$	0.034	0.0012
eGaN HEMT	0.23	−776.9	0.51	−0.31	0.067	$7.2{\cdot}10^{-5}$	$8.4{\cdot}10^{-4}$	$4{\cdot}10^{-6}$

- Parasitic capacitance and inductance

It is a fact that nonlinear capacitances are the key to the dynamic characteristic of the device. Typically, the capacitance curves provided in the datasheet is in the form of C_{iss}, C_{oss} and reverse capacitance (C_{rss}) which can be mathematically converted to junction capacitances. Generally, these capacitances are voltage-dependent and can be extracted by fitting the curves as

$$C(v) = f(v), \tag{24}$$

where f is a general fitting function for extraction of capacitance. In this paper, various f are used for different devices to fit the corresponding curves as shown in Figure 7. Notice that the nonlinear capacitance curves vary from different devices and thus it is reasonable to change f accordingly.

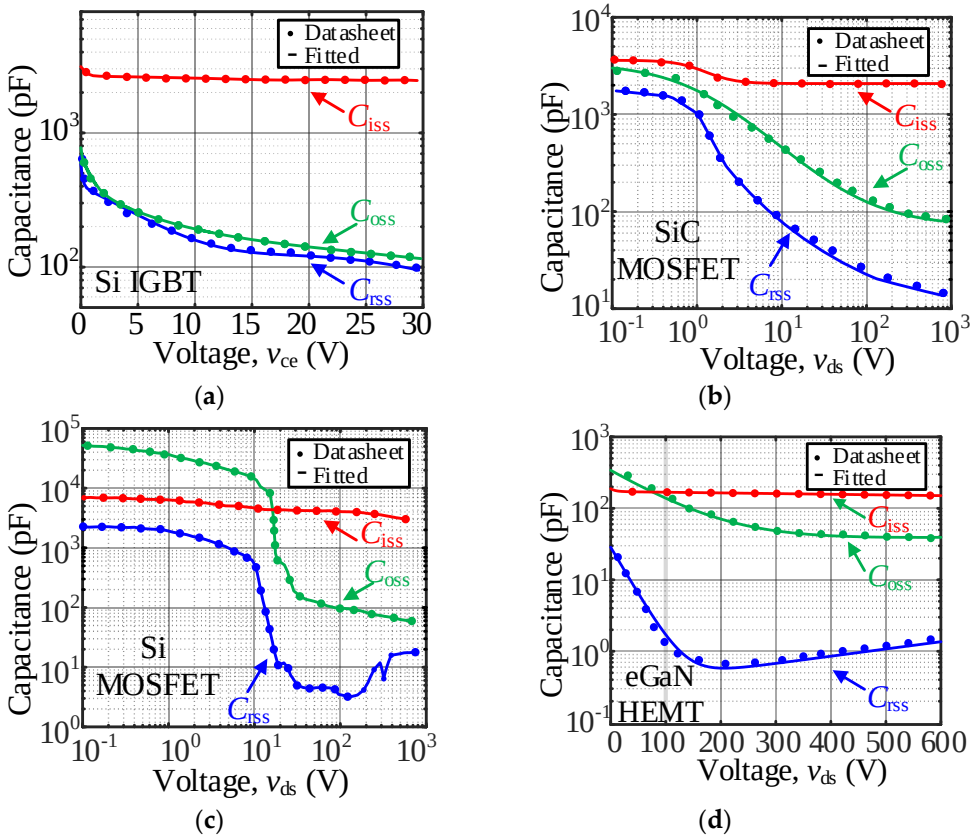


Figure 7. Parasitic capacitance extraction with the methods of (**a**) 5th order Gauss function; (**b**) Analytical equation [49]; (**c**) Interpolating look-up table (LUT); (**d**) 3rd order exponential function.

As for the parasitic inductance, only the internal inductance of the device is normally provided in the datasheet, while the stray parasitic inductance is highly related to the specific device package and PCB design. There are two widely used methods for inductance extraction, namely calculation method and experimental method. Based on the PCB and device package specification, the corresponding inductance can be computationally obtained with the help of calculation tools such as the Ansys Q3D Extractor software (v1.0, Canonsburg, PA, USA). According to (1), it also can be extracted from the slew rate of current along with v_L during S turn on transition or from the resonant frequency of the power loop in the experimental results. In this paper, the parasitic inductances are initially estimated based on the PCB trace length of the power loop and the gate loop [50] as well as the device package (e.g., 2–5 nH for TO-247 [51]) and further calibrated from the switching waveforms.

- Diode parameters

According to (4), R_F and v_{F0} are the key static parameters for D which can be extracted directly from the diode I-V curve in the datasheet and the corresponding values for various temperatures can be estimated by linear interpolation. Furthermore, the third quadrant operation of eGaN HEMT as D is of special concern. Since the corresponding voltage drop is dependent on the gate drive voltage of D, thus it should be fitted by (5) based on the output curves in the third quadrant from the datasheet. The diode I-V curve fitted results for different devices are compared with the datasheet and illustrated in Figure 8. Notice that the conduction performance of the body diode in SiC MOSFET is generally worse than the anti-parallel diode of IGBT and SiC SBD. As for the eGaN HEMT, the reverse voltage drop is highly dependent on the gate drive voltage and the typical value for turn off (i.e., −3 V) will result in considerable conduction loss.

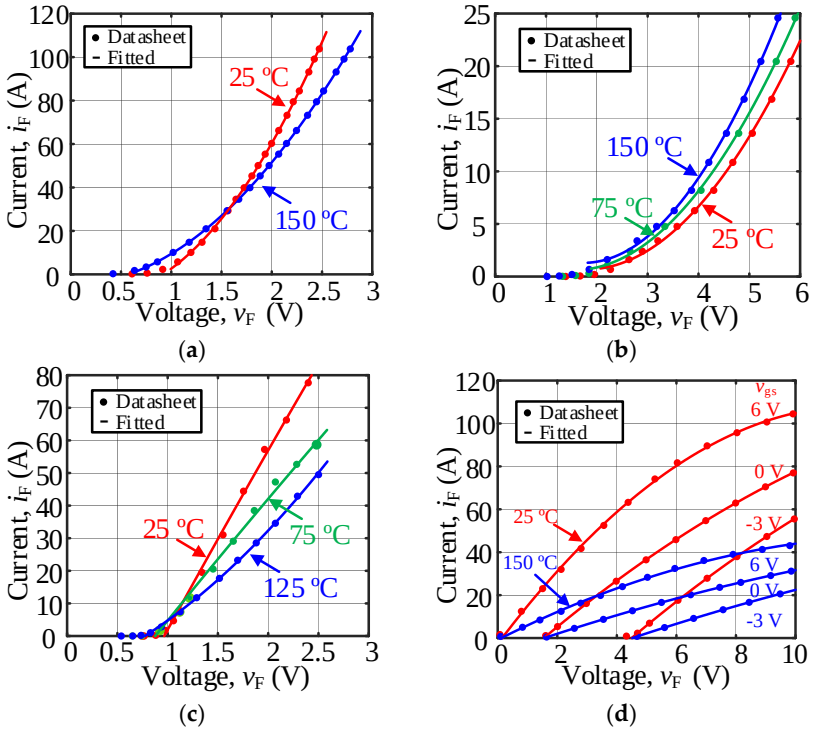


Figure 8. Diode static parameter extraction of (**a**) Si IGBT; (**b**) SiC MOSFET; (**c**) Si MOSFET; (**d**) eGaN HEMT.

In addition, C_F can be obtained using the same method as mentioned above for S from the capacitance curve in the datasheet. According to the previous switching transition analysis, it can be found that the reverse recovery behavior of diode plays a considerable role and the main parameters I_{rm} and Q_{rr} can be extracted from the diode curves as a function of T_j and di_F/dt [42],

$$I_{rm} = k_{rm0} + t_{rm0} \cdot di_F/dt + (k_{rm1} + t_{rm1} \cdot di_F/dt) \cdot (T_j - T_a) \quad (25)$$

$$Q_{rr} = k_{rr0} + t_{rr0} \cdot di_F/dt + (k_{rr1} + t_{rr1} \cdot di_F/dt) \cdot (T_j - T_a) \quad (26)$$

where k_{rm0}, t_{rm0}, k_{rm1}, t_{rm1}, k_{rr0}, t_{rr0}, k_{rr1} and t_{rr1} are all fitting coefficients. Besides, the reverse recovery time (t_{rr}) and τ_{re} can be further determined by

$$t_{rr} = 2\sqrt{Q_{rr}/(di_F/dt)} \quad (27)$$

$$\tau_{re} = 1/\ln 10 \cdot (t_{rr} - I_{rm}/(di_F/dt)) \quad (28)$$

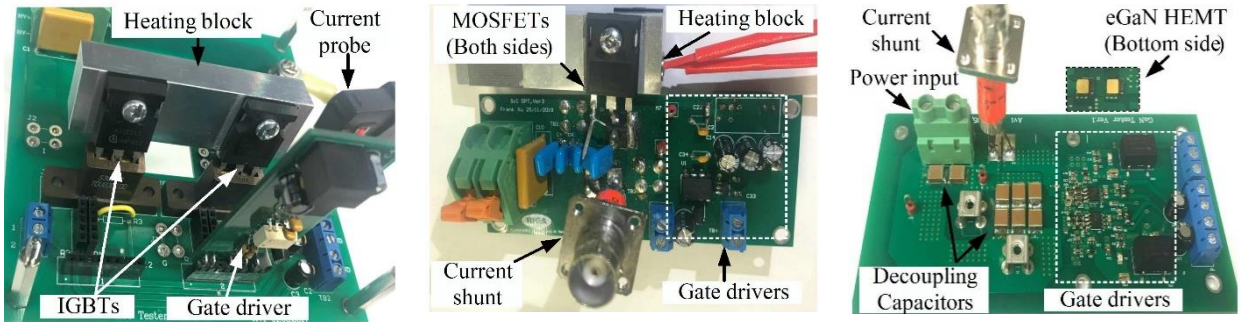
4. Experimental Verification

The objective of the proposed method is to reproduce the switching performance of the SDC and generate the corresponding power loss look-up table (LUT) with reasonable accuracy and fast simulation speed. The models are implemented in PSCAD/EMTDC and validated by comparing with the experimental waveforms and power loss results in the DPT bench for different semiconductor combinations.

4.1. Setup Description

An automatic DPT bench was designed and built for device characterization and loss validation [17]. Since the gate-drive requirements and device package are different for all the devices, three daughter boards were designed accordingly with a power supply (up to 1 kV) and the inductive load (5 mH) as shown in Figure 9. Tektronix High voltage differential probe THDP0200 and current probe TCP0030A were used for Si IGBT/MOSFET

voltage and current measurements, respectively, while passive voltage probe (TTP800) and 0.1 Ω current shunt resistor (SDN-414-01) were adopted for SiC MOSFET and eGaN HEMT measurements. The temperature was controlled by a heating block and monitored by a thermal imager (Fluke, TiS40). In the DPT, the desired test conditions (voltage, current, and temperature) were initially set in the personal computer (PC) and all the control signals were given by the microcontroller Arduino on the board. Afterwards, the DC capacitor bank was charged to the desired voltage by the power supply unit, and the device was heated to the desired temperature. When voltage and temperature conditions were ready, two gate pulses were given in sequence to turn on and turn off the device under test (DUT). The switching waveforms and data were obtained by oscilloscope and processed in the PC for transient information and power loss analysis. In order to mitigate the measurement error of power loss due to the asynchrony of voltage and current, it is necessary to calibrate the probes before conducting the DPTs. To further guarantee the accuracy, additional delay time adjustments for the transient waveforms are also needed for the turn-on and turn-off processes. Taking the current as the reference, the calibration time of probe and waveform are provided in Table 4. The calibrating fixture (067-1686-02) from Tektronix was used for calibration of the current and voltage probes. A 10 MHz sinusoidal signal was applied to both probes and the deskew time for voltage probe was adjusted until both measurements were synchronizing. Note that, these calibration times can be different for various probes and DUTs.



(**a**) (**b**) (**c**)

Figure 9. Device characterization DPT setups for (**a**) Si IGBT/MOSFET; (**b**) SiC MOSFET; (**c**) eGaN HEMT.

Table 4. Calibration time of probes and waveforms.

DUT Case	Si IGBT	SiC MOSFET	Si MOSFET	eGaN HEMT
Probes calibration (ns)	48	26	45	23
Turn-on calibration (ns)	35	13	26	14
Turn-off calibration (ns)	31	18	25	12

4.2. Switching Transient Verification

- Si IGBT

The daughterboard in Figure 9a was used for Si IGBT and MOSFET tests, and v_G was flipped between 15 V and 0 V to control the DUT's on and off, respectively. The simulated results of switching current and voltage waveforms for IKW40T120 are compared with the DPT measurements in Figure 10. The simulated results demonstrate good agreement with measurements for current and voltage switching waveforms under 25 °C and 150 °C. The switching details such as the tail current and the current spike resulting from the reverse recovery of D can be clearly observed. In addition, v_{ce} slightly drops to 500 V as current rising and reaches a peak of 700 V during turn-off transition due to parasitic inductance. Besides, as T_j increases from 25 °C to 150 °C, the reverse recovery behavior of D becomes more obvious resulting higher current peak (up to 60 A) and the rise of v_{ce} as well as the

decline of i_c during turn off transition slows down which will increase the switching power loss.

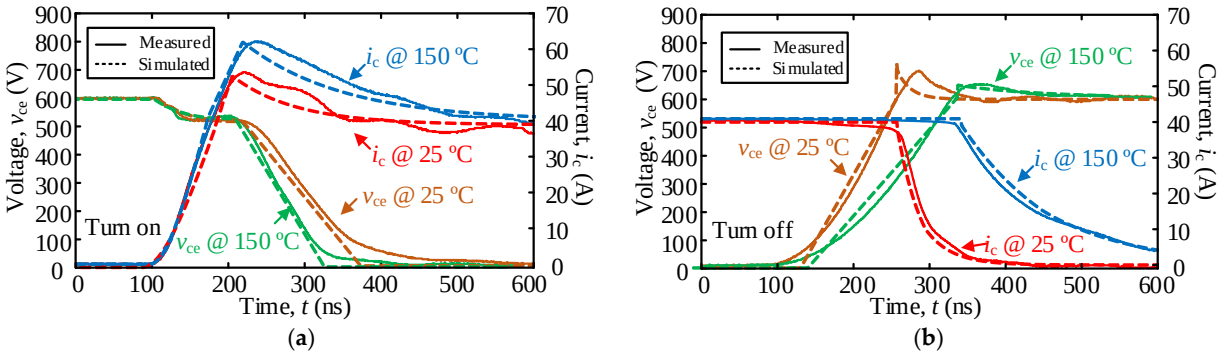


Figure 10. Switching waveforms of Si IGBTs (**a**) turn-on; (**b**) turn-off; @$R_G = 15\ \Omega$.

- SiC MOSFET

A more compact daughterboard as shown in Figure 9b was designed for testing SiC MOSFET. Additionally, the gate drive integrated circuit (IXDN609SI) was adopted as the gate driver onboard to provide 20 V/−5 V drive voltage for SiC MOSFET. Figure 11 shows the simulated switching waveforms of SiC MOSFET under the condition of 600 V and 20 A which match well with measured results. It can be observed that there is only a slight impact of T_j on the switching transients in terms of turn-on and turn-off time. Nevertheless, the current still can reach almost 40 A during the turn-on transition due to the reverse recovery behavior of the diode. Besides, it is found that a current ringing occurs during both turn-on and turn-off transitions because of the parasitic resonance. This ringing energy is generally consumed by the HF damping resistance in the circuit. Since either the voltage or current has typically dropped to a low level during the ringing period, thus this ringing loss is neglected in the model for simplicity.

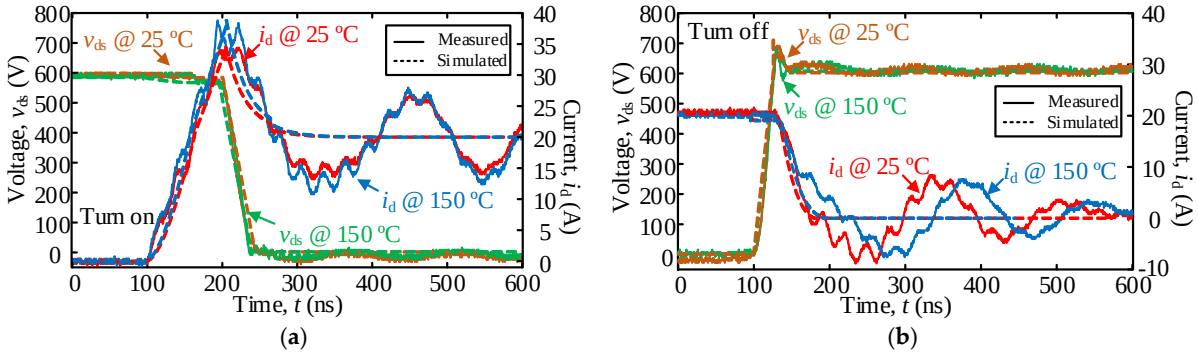


Figure 11. Switching waveforms of SiC MOSFETs (**a**) turn-on; (**b**) turn-off; @$R_G = 5\ \Omega$.

- Si MOSFET with SiC diode

The DPT results for Si MOSFET with SiC diode using the same daughterboard as for testing Si IGBT are shown in Figure 12. In general, the simulated results match well with the measured results for different R_G conditions. As R_G increases from 10 Ω to 33 Ω, a half less voltage drop of v_{ds} can be observed during turn-on transition due to the slower current rising speed. Likewise, only a slight increase of v_{ds} can be seen after v_{ds} climbs to V_{dd}. Moreover, it is noted that the current spike is significantly limited comparing with the previous testing using PIN diode due to the merit of zero reverse recovery for SiC SBD. Whereas, there is still a slight current bump causing by the resonance of parasitics as well as the capacitive displacement current as discussed previously.

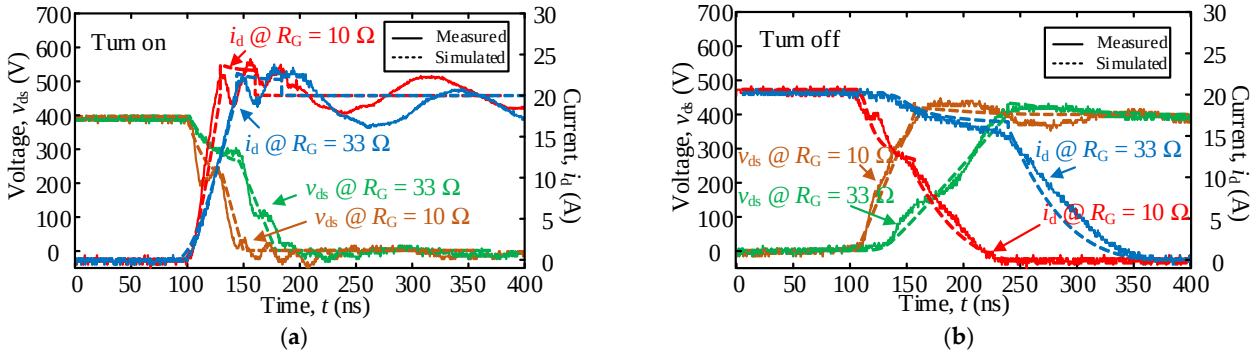


Figure 12. Switching waveforms of Si MOSFET with SiC SBD (**a**) turn-on; (**b**) turn-off; @400 V, 20 A, 25 °C.

- eGaN HEMT

In order to test the eGaN HEMT which is a surface-mount device (SMD), a specific DPT daughterboard was used as shown in Figure 9c. The gate driver provided 6 V/0 V as gate drive voltage to control the lower side GaN switch *S*, while the upper side SiC SBD served as a freewheeling diode when *S* turned off. The simulated switching results are compared with the measurements for the two operating conditions as shown in Figure 13. It can be seen that the simulation results are consistent with the experimental results. In the turn-on waveforms, the current rising time is only tens of nanoseconds. After i_d reaches I_L, it behaves in the similar manner as previous test using Si MOSFET with SiC SBD. However, during the turn-off period, it can be clearly observed that, i_d declines significantly and drops to zero almost the same time as v_{ds} reaches steady state while for the other cases of devices, the fast decrease of current typically occurs after v_{ds} climbs to v_{dd}. This is mainly because the channel of eGaN shuts down very fast before v_{ds} increase significantly as discussed in Section 2.3. Hence, when the channel turns off completely, the apparent i_d is dominated by the capacitive displacement current which is highly related to the change of v_{ds}.

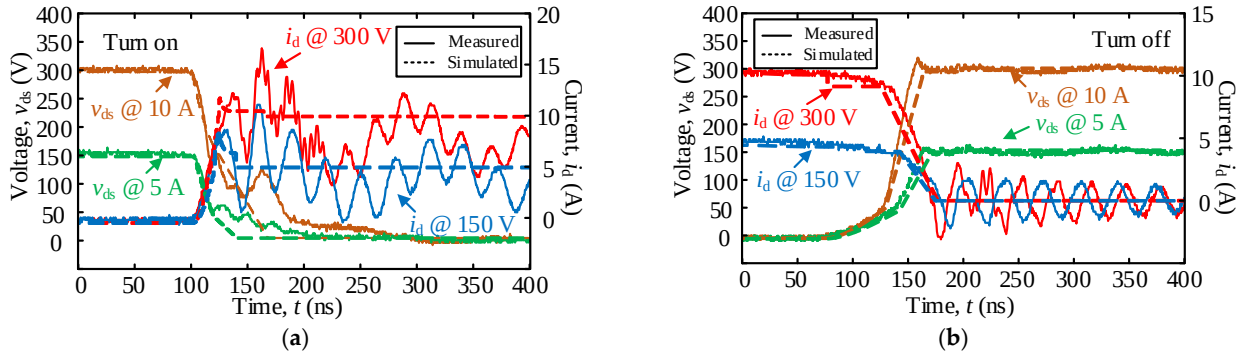


Figure 13. Switching waveforms of eGaN HEMT with SiC SBD (**a**) turn-on; (**b**) turn-off; @25 °C, $R_G = 5\ \Omega$.

4.3. Power Loss Verification

With the aim of power loss verification for various devices, the switching losses were measured in the DPT and compared with the simulated results. During the switching transients, p_S, which is the product of voltage and current, can be obtained using the math function in oscilloscope and similarly the E_{onm} and E_{offm} can also be obtained by integrating p_S. As mentioned previously, the current and voltage probes are calibrated for each test and additional delay time is also added to the waveforms results to keep transient voltage and current synchronous. The captured waveforms and simulated waveforms under the same test conditions are demonstrated in Figure 14 taking Si IGBT as an example. By comparing the measured results with the simulated results, a good agreement can

be clearly seen in terms of not only transient voltage and current waveforms but also computed p_S, E_{onm} and E_{offm}. Furthermore, the measured power loss results are compared with the simulated loss results for different devices under various operating conditions to validate the proposed method. The average error ($\bar{e}$) is calculated by averaging the absolute value of the error in each case.

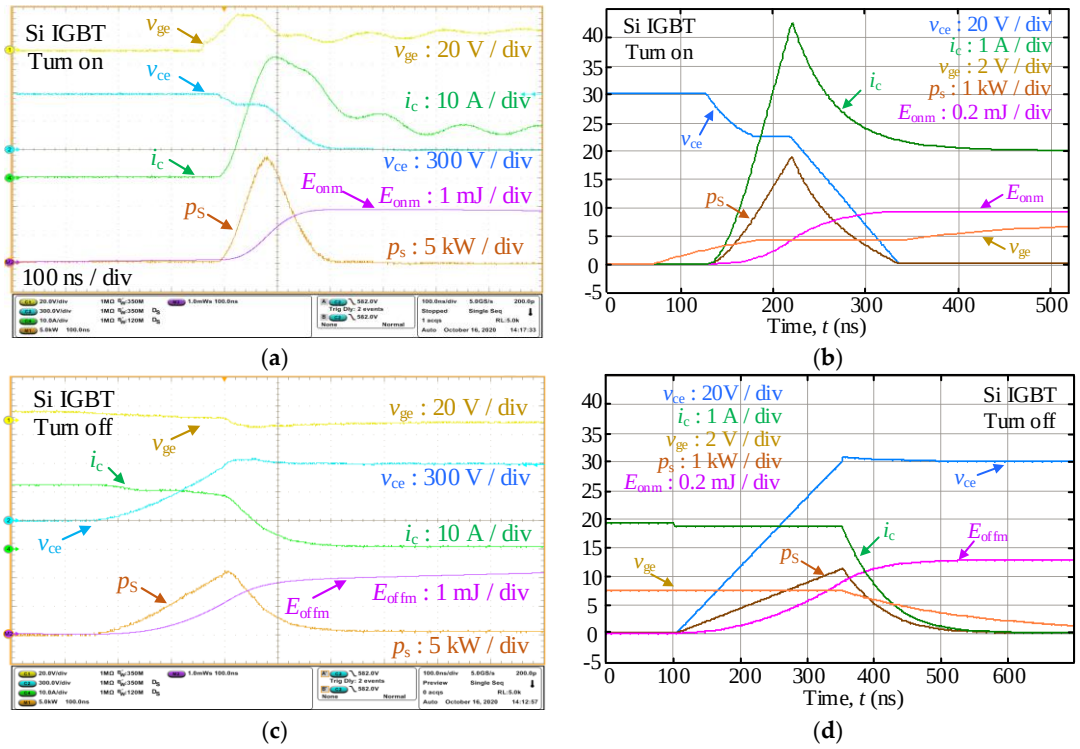


Figure 14. Si IGBT turn on waveforms (**a**) measured; (**b**) simulated; and turn off waveforms (**c**) measured; (**d**) simulated @600 V, 20 A, 25 °C, R_G15 Ω.

Figure 15 shows the power loss results of Si IGBT under different conditions of current, voltage, and temperature. Generally, the total power loss (E_{ts}) increases as the operating voltage and current increase, and E_{off} is less than E_{on} except for the high temperature condition. It can be seen that, the average errors of E_{ts} are within 7%, namely 5.1%, 5.5%, and 6.3% for different operating conditions of current, voltage, temperature, respectively.

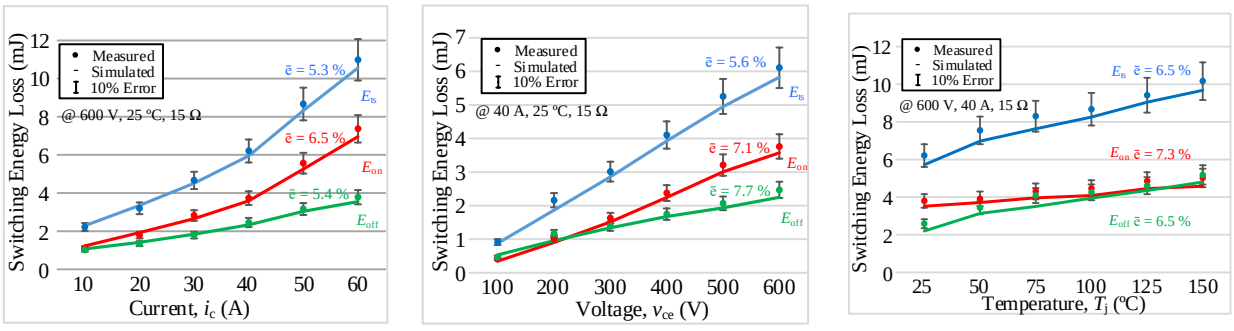
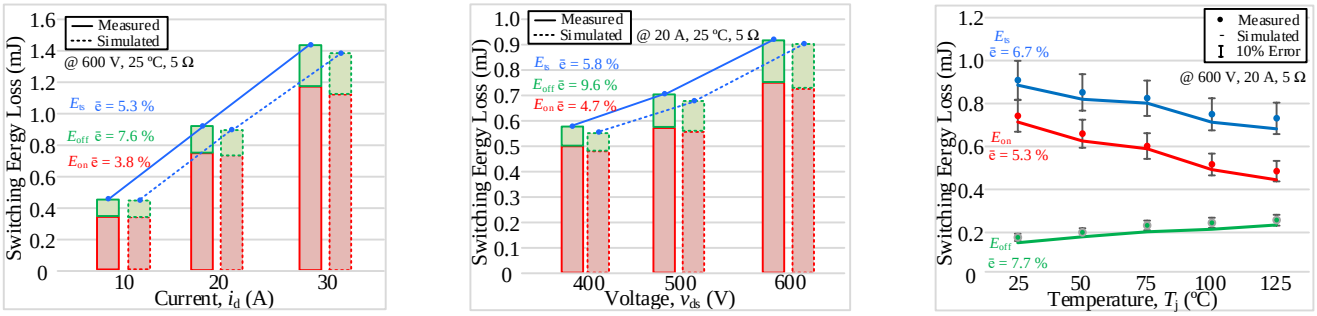


Figure 15. Si IGBT loss results under different values of (**a**) current; (**b**) voltage; (**c**) Temperature.

Likewise, the power loss comparison results for SiC MOSFET are illustrated in Figure 16. Note that the E_{ts} for SiC MOSFET is typically less than 1 mJ which is much less than the counterpart of Si IGBT for similar conditions. It also can be found in Figure 16c that, there

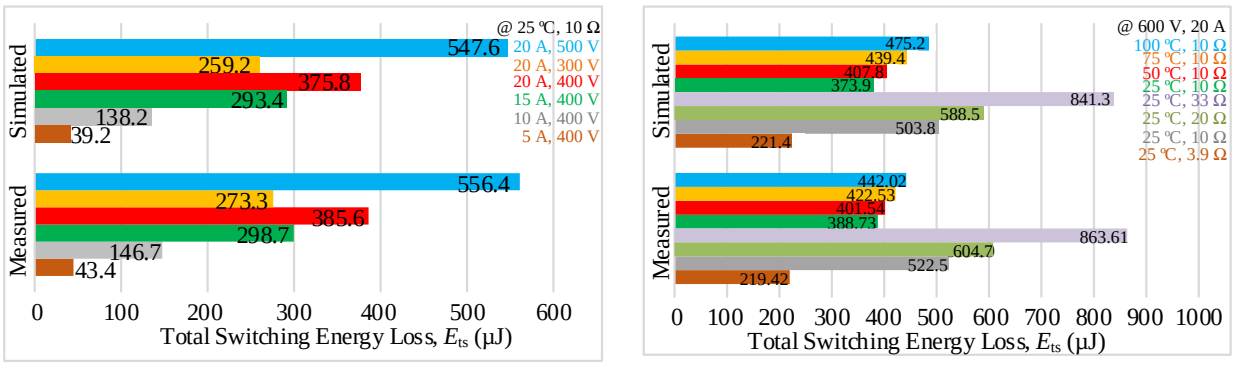
is a negative correlation between E_{on} and T_j. Since E_{on} is the dominated loss, as T_j rises, E_{ts} reduces accordingly though E_{off} increases slightly. It is also noted that ē of E_{off} for various conditions are more than 7% while ē for E_{on} and E_{ts} are still within acceptable range. The reasons for the loss deviation can be the underestimation of parasitics and ringing loss as well as measurement error. Besides, a relatively small amount of loss deviation can still result in a high error percentage when the overall loss is relatively low.



(**a**) (**b**) (**c**)

Figure 16. Power losses of SiC MOSFET under different values of (**a**) current; (**b**) voltage; (**c**) temperature.

Figure 17 shows E_{ts} results for the combination of Si MOSFET and SiC SBD as the SDC. It can be observed that E_{ts} increases as the operating voltage and current increase. In addition, a slight increase of E_{ts} can be found as the operating temperature rise from 25 °C to 150 °C, while E_{ts} increases significantly when 33 Ω R_G is used. Moreover, the power loss results for the case of eGaN HEMT with SiC SBD are illustrated in Figure 18. It should be mentioned that, in order to capture the switching waveforms and the power loss with reasonable accuracy, a 220 Ω gate resistance is used to relatively sacrifice the switching speed and avoid shoot through issue due to the very low v_{th} of GaN. Comparing with the simulated and measured results, a good agreement is achieved at various testing conditions and the error is within an acceptable range, although the ē of E_{off} is slightly higher.



(**a**) (**b**)

Figure 17. Power losses of Si MOSFET under various values of (**a**) voltage and current, (**b**) temperature.

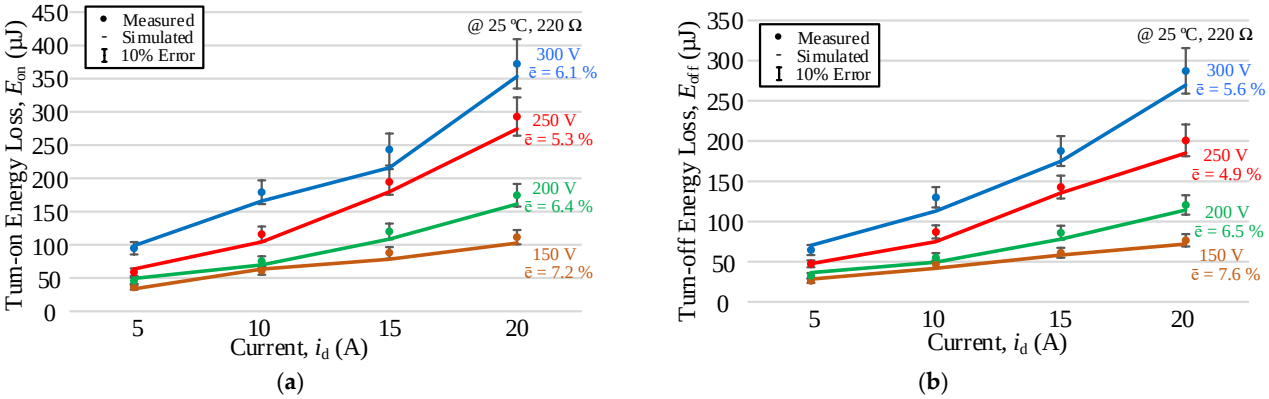


Figure 18. Power loss results of eGaN HEMT with SiC SBD (**a**) turn on, (**b**) turn off.

4.4. Discussion

- Accuracy

Comparing with the original two-state resistance switch model in PSCAD/EMTDC, the proposed model is capable to reproduce the switching transient waveforms considering various impacts of parasitics and interactive behavior of diode. In addition, the thermal effect is also considered to provide reasonably accurate results comparing with the measured results where the temperature is monitored by a thermal imager as shown in Figure 19a. Apart from the switching waveforms, multi-dimensional (i.e., voltage, current, temperature) power loss LUT as shown in Figure 19b also can be obtained simultaneously. The average error is within 10% comparing with measured results for various devices under various conditions. Comparing to the traditional physical model or analytical loss model, no significant advantage is found in the modelling accuracy using the proposed model due to the ignorance of parasitic resonance and some linear assumptions. Nevertheless, the complexity of the proposed model is reduced with no state equations and numerical calculations, and all the model parameters can be extracted from the datasheet.

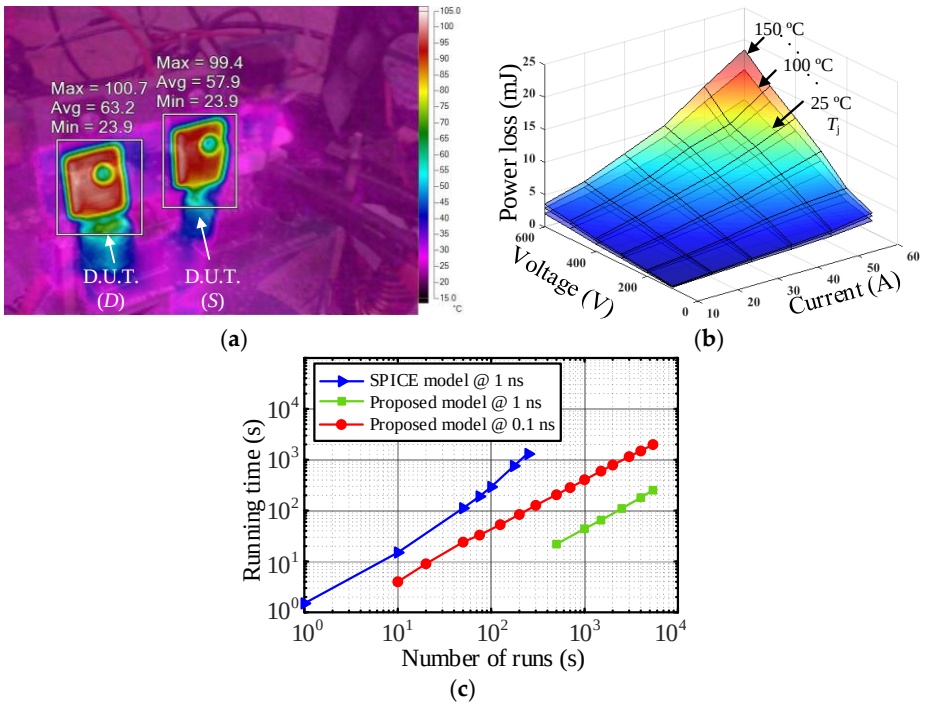


Figure 19. DPT results of (**a**) thermal image; (**b**) loss LUT for Si IGBT; (**c**) time cost comparison.

- Efficiency

The proposed model uses equivalent dependent voltage and current sources to represent the dynamic characteristics of devices based on the analytical equations for each sub-stage of the switching process. In addition, the gate loop and power loop are decoupled and the complicated numerical calculation as well as solving physical equations are not necessary which can boost the simulation efficiency and avoid convergence issue. In order to obtain an accurate power loss LUT with a wide range of operating conditions, there are numerous permutations to be taken into account and thousands of simulation runs are required instead of repetitive DPTs. For example, it requires around 5400 simulation runs to cover the operating range, namely voltage from 20 V to 600 V with 20 V step, current from 2 A to 60 A with a 2 A step, and temperature from 25 °C to 150 °C with a 25 °C step. Figure 19c demonstrates the time cost of using the SPICE model provided by the manufacturer and using the proposed model in PSCAD. In order to achieve reasonable accuracy, the simulation time step is typically one nanosecond or less. Notice that, it takes thousands of seconds to barely finish around 200 runs in SPICE, while more than 10 times less running time is needed to finish the same number of runs by the proposed model with even less time-step (i.e., 0.1 ns). Furthermore, to finish the whole 5400 simulation runs using the proposed model at 1 ns time-step, it takes less than 300 s which shows the merit of time-saving in generating the power loss LUT.

- Applicability

The proposed approach can be used to reproduce the switching waveforms and obtain the power loss LUT of SDC configured by various devices such as Si IGBT, Si/SiC MOSFET, eGaN HEMT, and SiC SBD. When it comes to other devices with a new structure such as Cascade GaN, the proposed model cannot be used directly and modifications are needed though the basic modelling method is still applicable. In addition, for each specific device, the curve fitting functions and algorithms for parameter extraction are needed to be adjusted for good fitting results. Apart from PSCAD/EMTDC, the proposed approach can also be applied to other simulators such as MATLAB/Simulink, PLECS, and Saber with respective modifications. Besides, the proposed model provides an insight into the device behavior and most of the elements have clear descriptions. As a result, it is more easily apprehensible than mathematical equations. Conversely, analytical loss models are normally limited to the specific device type or combination and it is difficult to extend the models to various PE applications for loss estimation. Besides, loss measurements are time-consuming, costly, and challenging especially for WBG devices due to the fast switching speed.

5. Conclusions

In this paper, a generalized behavioral modelling approach of the switch-diode cell for power loss prediction is proposed, implemented in PSCAD/EMTDC, and validated by experimental results in double-pulse tests. This proposed model consists of an active switch model and diode model and it can be used for different modern power semiconductors. The modelling approach along with power loss analysis is derived based on the comprehensive switching process analysis in a clamped inductive switching circuit. The static and dynamic characteristics of the switch-diode cell are modelled by dependent voltage and current sources with passive components. In addition, the proposed model is improved by considering the impacts of parasitic elements, interactive behavior of diode, and the temperature-dependent parameters. Besides, the extraction of the model parameters is introduced by curve fitting from the device datasheet. Moreover, the switching transient verification along with power verification is conducted for different devices under a wide range of operating conditions. A good agreement between the simulated results using the proposed model and experimental results can be achieved with less than 10% average error. Consequently, the proposed model provides a good balance in terms of accuracy, efficiency, and applicability.

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