Article

Interoperability of Modular Multilevel and Alternate Arm Converters in Hybrid HVDC Systems [†]

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Abstract: This paper demonstrates the interoperability of an emerging alternate arm converter (AAC) with the state-of-the-art modular multilevel converter (MMC) in high-voltage direct current (HVDC) systems based on a hybrid VSC-HVDC system. The paper also showcases the parameter derivation of the hybrid HVDC system and its detailed control structure. The study provides preliminary steps towards detailed analysis of AAC interoperability in complex hybrid dc grid configurations. A detailed set of results based on the 800 MVA hybrid voltage source converter (VSC)-HVDC system showcases the interoperability performance of the AAC under different operating scenarios and verifies its associated control functions.

Keywords: alternate arm converter (AAC); HVDC transmission; Hybrid HVDC; interoperability; modular multilevel converter (MMC)

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1. Introduction

The rising demand of global energy consumption and the wide variety of modern distributed energy resources bring forth the necessity for dc power systems to offer more advanced capabilities than ever before [1]. Over recent decades, high-voltage direct current (HVDC) technology has evolved from HVDC systems based on line-commutated converters (LCCs) through voltage source converters (VSCs) to modular multilevel converters (MMCs)-based systems [2]. The most recent research and development includes advanced dc transmission line/cable technologies, dc breakers, and dc fault-tolerant modular VSC topologies such as hybrid MMC configurations that include bipolar submodules (SMs) and the emerging alternate arm converter (AAC) [3–6].

LCC-based HVDC is a well-established technology in bulk power transmission and ultra-HVDC (UHVDC) applications due to the significantly high voltage and current ratings of thyristors, despite the additional device requirements for harmonic filtering and reactive power compensation [7]. Modular VSC topologies generate near sinusoidal output voltages, avoiding the need for bulky harmonic filters in HVDC applications. VSC-based HVDC systems are dominated by state-of-the-art MMCs owing to the unique features of the MMC, including flexibility and scalability to accommodate larger capacity and high voltages.

HVDC system implementations range from two terminal systems (back-to-back (BTB) and point-to-point (PTP)) to multiterminal DC (MTDC) systems [2]. The development of LCC-based MTDC systems has been limited to only three such systems over the last three decades and modular VSCs-based MTDC systems are becoming the main frontier network configurations towards more interconnected global dc super grids [8]. Moreover, the latest trends in research and development of hybrid HVDC configurations showcase the need for tackling the challenges of future power systems that will be inhabited by both LCC-based and modular VSC-based HVDC/MTDC systems, while aiming to offer more flexibility,

reliability, and resilience for better utilization of distributed energy resources on a global scale [9].

The availability of a wide variety of HVDC systems is key to perform interoperability studies and to augment new research for complex HVDC system configurations. Accessible HVDC system models provide a common basis for future research, allowing for performance comparison and cross-validation of results; if developed with input from the industry, they can be used to address design considerations and interoperability issues without intellectual property restrictions or specific project information.

The extensive body of literature in HVDC systems research presents various different types of HVDC configurations including, (i) LCC-based HVDC, (ii) VSC/modular VSC-based HVDC, (iii) LCC/VSC-HVDC [10–14]. However, all aspects of HVDC systems have not been addressed in the existing literature. Specifically, the current literature has the following research gaps: (i) interoperability studies and characterizations of emerging modular VSC topology-based implementations and applications are limited [15–19] and (ii) newer implementations and applications are also limited to HVDC models based on only LCCs [10], the same VSC/modular VSC topology [11,12,20], and a combination of LCCs and VSCs [13]. Therefore, the necessity for interoperability studies on emerging modular VSC topology-based hybrid HVDC systems and analysis of their characteristics are paramount for understanding complex hybrid HVDC system configurations and such implementations.

Based on the above and previous work, this paper showcases the interoperability of the emerging AAC with the MMC in HVDC transmission systems. The detailed contributions of the paper include: (i) derivation, development, and verification of a hybrid HVDC system model based on the state-of-the-art MMC and emerging AAC, (ii) demonstration of the interoperability of the MMC and AAC in a hybrid HVDC system, (iii) detailed illustration of the related control hierarchy including high-level and low-level controller functions, (iv) detailed analysis of the steady-state and transient operation demonstrating the appropriate utilization of circulating current control and energy regulation methods of the MMC and AAC, and (v) verification of the ac and dc fault handling capability of the hybrid HVDC system. The derived hybrid HVDC system is a key imitative for detailed studies of interoperability issues in future complex hybrid DC grids.

The paper is organized as follows. Section 2 describes the overview and basic operating principles of the MMC and the AAC. The derivations, parameters, and control of the MMC-AAC hybrid HVDC system are illustrated in Section 3. Section 4 provides results and performance verification of the proposed model and Section 5 summarizes the conclusions.

2. Modular VSC Topologies

Modular multilevel VSC topologies offer greater flexibility to HVDC and MTDC systems, as they do not require a series connection of multiple switching devices to reach higher operating voltages and the multilevel voltages offer improved harmonic performance. Figure 1 shows a single phase circuit configuration of the state-of-the-art MMC and the emerging dc fault-tolerant AAC that are utilized in the proposed hybrid VSC-HVDC system. The following sections discuss the topologies operation of the MMC and AAC briefly, with only the necessary explanations in the context of the work in this paper.

Figure 1. Single phase circuit configurations: (a) MMC phase-leg and (b) AAC phase-leg.

2.1. Modular Multilevel Converters

MMC topology and operation are extensively analyzed and described in the existing literature [21]. One MMC phase-leg (Figure 1a) consists of two arms which include N series-connected SMs and one inductor (L) per arm.

Various modulation techniques are applicable to the MMC, and staircase modulation is preferable for HVDC applications due to the large number of SMs per arm; subsequently, the voltage becomes level [22]. Capacitor voltage balancing is achieved by sort-and-select algorithms [23]. The common and differential mode currents (i_{comm} and i_{diff}) can be expressed as: $i_{comm} = (i_u + i_l)/2 = i_a/2$ and $i_{diff} = (i_u - i_l)/2$, respectively [24].

The differential current, i_{diff} , is also referred to as the circulating current (i_{circ}). The two main circulating current control techniques are: (i) circulating current suppression control (CCSC) [25] and (ii) forced circulating current control (FCCC) [24]. The CCSC technique suppresses the predominant second harmonic of i_{circ} based on the double synchronous reference frame. The FCCC technique actively controls i_{circ} based on the proportional resonant controllers. Unlike the CCSC technique, FCCC offers active dc circulating current control, average SM energy regulation, and upper/lower arm energy balancing. However, the FCCC technique can cause interactions between the high- and low-level controllers, and even between the MMC-based terminals within an HVDC system [26].

2.2. Alternate Arm Converters

The AAC (Figure 1b) combines a two-level converter and MMC arms in a modular topology belonging to the same family as the MMC. The AAC phase-leg includes two director switches (DS_u and DS_l), one in each arm. The AAC operates in the over-modulation range. Fully controllable bipolar SMs are necessary for the normal operation of the AAC and a full-bridge (FB)-SM is recommended [27].

The two director switches, DS_u and DS_l , operate alternatively, during the positive and negative half-cycles of the output reference voltage $v_{am} = m_a \cos(\omega t)$, respectively. The duty cycles of the upper and lower arms, d_u and d_l , are $(1 - v_{am})/M_a$ and $(1 + v_{am})/M_a$, respectively (Figure 2). The natural energy balance of the AAC exists at a single operating point $M_a = 4/\pi \approx 1.273$ which is defined as the sweet spot [6]. The sweet spot ac voltage is $\hat{V}_a = M_a V_{dc}/2$.

Unlike the MMC, the energy exchange between the upper and lower arms of the AAC is not continuous due to the alternate operation of the arms (Figure 2). Instead, energy exchange occurs only during the overlap period (t_{ov}) that is provided by closing both DSs around the zero crossing points of v_{am} . The circulating current (i_{circ}) exists only during the overlap operation of the AAC mimicking MMC operation. Hence, the two arm currents,

(i_u and i_l), during the overlap period are defined similar to the MMC as: $i_u = \frac{i_a}{2} + i_{circ}$ and $i_l = \frac{i_a}{2} - i_{circ}$, where $i_a = \hat{i}_a \cos(\omega t + \phi)$ is the phase current.

Figure 2. Operation of the director switches, duty cycles, and overlap period of the AAC.

The AAC can be configured with a short overlap ($\lesssim 18^\circ$) [28] or an extended overlap ($> 60^\circ$) [29,30] period to allow more flexibility for energy balancing. In addition to the function of the short overlap mode, the extended overlap mode offers dc current active filtering. This is at the cost of increased voltage stress on DSs requiring more redundant SMs in the arms depending on the zero-sequence voltage injection.

3. The AAC-MMC Hybrid HVDC System

Figure 3 shows the proposed hybrid VSC-HVDC system for interoperability of the AAC with the MMC. The MMC and AAC are configured as the rectifier and inverter, respectively, and are connected through a 200 km dc cable [12]. The AAC is configured with constant dc-voltage control as the dc-voltage controlling terminal plays a challenging role in the HVDC system's performance. The MMC is in active/reactive power control mode. Both MMC and the AAC stations are modeled based on widely accepted dc benchmark models. The MMC model is implemented based on [11]. The AAC model's implementation, translated from the MMC model, is summarized below.

3.1. AAC Modeling and MMC Equivalence

The AAC parameters are derived considering the MMC parameters of a system with similar voltage/power ratings, guidelines, and recommendations from the existing literature [12,31]. Detailed steps for determining the parameters of the AAC station are referred to in [12].

Figure 3. MMC and AAC-based hybrid VSC-HVDC system.

The standard AAC operating point:

$$m_a = \frac{\hat{m}_a}{1.1} \approx 1.15, \quad (1)$$

is determined considering $\pm 10\%$ tolerance in grid voltage variations, where the peak is assumed to be at the “sweet-spot” operation ($\hat{m}_a = M_a = 1.273$). The total number of SMs required per arm can be determined as:

$$N = \left\lceil \frac{\hat{V}_a}{V_C} \right\rceil = \left\lceil \frac{\hat{m}_a V_{dc}}{2V_C} \right\rceil, \quad (2)$$

considering the total arm voltage in the SM blocking state is sufficient to block the sweet spot ac voltage following a dc fault.

In order to contain the SM capacitor voltage ripples within $\pm 10\%$, the AAC energy storage requirement (E_{AAC}) is chosen as 11 kJ/MVA [31] and the SM capacitance is:

$$C = \frac{S E_{AAC}}{3 N V_C^2}. \quad (3)$$

The maximum overlap period:

$$\hat{t}_{ov} = \frac{2}{\omega} \sin^{-1} \left(\frac{\hat{m}_a - 1}{m_a} \right). \quad (4)$$

is determined based on the redundant voltage (V_r) availability [27]. The arm inductance:

$$L \leq \frac{3 V_{dc} V_r}{4 \omega \pi S} \sin^{-1} \left(\frac{\hat{m}_a - 1}{m_a} \right). \quad (5)$$

is determined predominantly to allow flexibility for circulating current control, also considering the impact of SM capacitor voltage ripples on V_r [32]. Based on the guidelines, the recommendations of [12,31], and the above derivations, parameters for the AAC and MMC HVDC stations are given in Table 1.

Table 1. Parameters of the MMC and AAC-based converter stations.

Parameter	MMC [11]	AAC [12]
Rated Power	800 MVA	800 MVA
DC Voltage	± 200 kV	± 200 kV
Number of SMs per arm	200	255
SM Voltage	2 kV	1 kV
Stored Energy	30 kJ/MVA	11 kJ/MVA
SM Capacitance	10 mF	11.5 mF
Arm Inductance (p.u.)	0.15	0.016
Nominal Frequency	50 Hz	50 Hz
Nominal Operating Point (p.u.)	0.9	1.15
AC Voltage	380 kV	380 kV
Transformer Resistance (p.u.)	0.006	0.006
Transformer Leakage Inductance (p.u.)	0.18	0.18
Transformer Ratio	0.995	0.778
Short-circuit Power	30 GVA	30 GVA

3.2. HVDC System Control Hierarchy and Structure

The control hierarchy of the hybrid HVDC system (Figure 4) consists of four main layers. The top most layer, the “Grid Control” layer, performs the timely planning of dispatch schedules for the entire power system [11]. The second intermediate layer, the “Coordinated System Control”, is in charge of handling unscheduled events (“Autonomous

adaptation control”) and coordinates all HVDC converter stations (“Global HVDC grid control”), defining the frequent reference set points of each station [33].

Figure 4. Hybrid MMC/AAC-based HVDC system control hierarchy.

The top three control layers are similar between MMC- and AAC-based HVDC stations and the bottom two control layers (high- and low-level) include the local controllers of an HVDC station. The high-level control layer, the “Converter Station Control”, regulates the output power, voltages, and frequency based on the referenced set points. The low-level control layer, “Internal Converter Control” is specific to the HVDC converter topology station. SM sorting and balancing is common between the MMC and the AAC [27,34]. However, the balancing of arm energy and regulation of the MMC and AAC are achieved by circulating current control methods [24,25] and overlap period-based methods, respectively [32,35–37]. In addition, the zero-current switching (ZCS) of the DSs is also ensured by coordinated control of the overlap period and circulating current of the AAC [38,39]. OLTC coordination is an alternative approach to extend the ZCS operation of the AAC [39].

The complete controller structure of the AAC-MMC hybrid HVDC system is shown in detail in Figure 5. The outer controller determines the current references for the inner current controller according to the desired power and voltage references. The inner current controller regulates the output current and calculates the output reference voltage. The modulation stage determines the required number of SMs to generate the output voltage based on the reference given from the inner current controller. Although pulse-width modulation (PWM) techniques can be used in the modulation stage, staircase modulation methods are the most efficient with a larger number of levels [22].

On the other hand, the overlap period-based circulating current controller determines the number of additional SMs that need to be inserted or bypassed to regulate the stored energy. Finally, the sorting and balancing algorithm provides the switching pulses for SMs. The control parameters of the hybrid HVDC system and the transmission line parameters are provided in Table 2.

Figure 5. Control structure for hybrid VSC-HVDC system: (a) high-level converter station control common to both MMC and AAC, (b) MMC internal converter control, and (c) AAC internal converter control.

Table 2. DC cable parameters and controller parameters.

Transmission Line Parameters [11]	
Length	200 km
Resistance	0.011 Ω /km
Inductance	0.2615 Ω /km
Capacitance	0.2185 Ω /km
Control Parameters (Figure 5)	
ine DC Voltage Control	$K_P = 8, K_I = 272$
Active/Reactive Power Control	$K_P = 0, K_I = 33$
AC Voltage/Frequency Control	$K_P = 0.2, K_I = 30, K_D = 0.0025$
Energy Balancing	$K_P = 2.9, K_I = 75$

4. Verification and Simulation Results

The interoperability of the AAC with MMC in the hybrid HVDC configuration is studied focusing on the steady-state performance, active/reactive power control, ac fault ride through (FRT) performance, and dc fault-handling capability. The performance of the AAC in the HVDC system and the impact on the AAC operation on the MMC under these different operating scenarios provide a comprehensive basis to characterize the interoperability of the AAC in HVDC systems.

4.1. Steady-State Operation

In steady-state, both the MMC and AAC operate at their standard operating points of Table 1 ($m_a = 0.9$ and $m_a = 1.15$, respectively) and unity power factor [11,12]. The MMC and AAC operate in rectifier and inverter modes, respectively, where the power flow is 800 MW from the MMC side to the AAC side.

Figure 6 shows the steady-state results of the MMC station. The %THD of ac currents (<0.5%) at the point of common coupling (PCC) verifies that the MMC station operates complying with network operating standards. The SM capacitor voltages are regulated to the reference 1 p.u. The arm currents and the circulating current show that the dominant

second harmonic and other even harmonics are suppressed. This verifies the proper operation of the applied circulating current control method (FCCC) [24]. Hence, the desired operation of the MMC station in the HVDC systems is ensured in order to appropriately study the interoperability of the AAC station.

Figure 7 shows the steady-state voltages and currents of the AAC station. The %THD of ac-currents at the PCC is below 1% and agrees with the network standards. SM capacitor voltages are regulated to the reference 1 p.u, demonstrating the desired operation of the utilized gradient-based energy regulation method [32]. The contained capacitor voltage ripples within the $\pm 10\%$ limit, verifying the sizing of SM capacitance based on the recommended stored energy (11 kJ/MVA) [31]. The arm AAC currents and the circulating current also demonstrate the appropriate utilization of the gradient-based energy balancing method [32].

Figure 6. Steady-state operation of the MMC: (a) ac voltages, (b) ac currents, (c) average SM capacitor voltages of phase *a*, (d) arm currents of phase *a* and (e) circulating current of phase *a*.

Figure 7. Steady-state operation of the AAC: (a) ac voltages, (b) ac currents, (c) average SM capacitor voltages of phase *a*, (d) arm currents of phase *a*, and (e) circulating current of phase *a*.

4.2. Active and Reactive Power Control

Independent active/reactive power control is a key capability of VSC-HVDC systems. Figure 8 shows the performance of the hybrid HVDC system for active power reversal and reactive power step changes at the AAC and MMC stations. The active power reference of the MMC is changed from -1 p.u. to 0.875 p.u. at 0.2 s with a ramp rate of 5 p.u./s. Following the power reversal, the active power reference is maintained at 0.875 p.u. and reactive power step changes of -0.5 p.u. and 0.5 p.u. at 0.8 s and 1.4 s are applied to the AAC and MMC, respectively, as shown in Figure 8a,b.

The dc side voltages of Figure 8c show an offset and ramp response during the power reversal, along with the ramping power and equivalent short transient responses at reactive power step changes in the ac sides demonstrating the desired behavior of an HVDC system. The dc currents of the two stations (Figure 8d) follow active power variation. The dc side quantities demonstrate the stable operation of the hybrid HVDC system during the transient, also verifying the constant dc voltage control performance of the AAC. The ac currents of the two stations also follow the corresponding active power response, performing the accurate power reversal and reactive power step changes of the hybrid VSC-HVDC system. The system maintains steady-state following all the transients.

Figure 8. Power reversal (at 0.2 s) and reactive power step changes (AAC at 0.8 s and MMC at 1.4 s): (a) active power, (b) reactive power, (c) dc voltage, (d) dc current, (e) ac currents of AAC, (f) ac currents of MMC, (g) SM capacitor voltages of AAC, and (h) SM capacitor voltages of MMC.

The SM capacitor voltage deviations of both the AAC and MMC (Figure 8g,h) are insignificant during power reversal. This demonstrates the energy balancing capability of the AAC and proper capacitor voltage regulation of the MMC by utilizing circulating current control techniques [24,32]. Only the capacitor voltage ripples are affected by the reactive power but are contained within the designed $\pm 10\%$ limit.

The ac and dc side voltages and currents of the hybrid HVDC system show that the impact of disturbances in one terminal on the other is insignificant and does not lead to larger energy deviations and unstable operation of the system.

4.3. AC Fault Ride Through

Robust operation under faults and unbalanced conditions is necessary for an HVDC system. The performance of the proposed hybrid VSC-HVDC system was studied under a single phase to ground (SLG) fault (with a fault impedance of 0.1Ω), a three-phase fault at the AAC, and a phase-to-phase fault at the MMC for a duration of 200 ms each, as shown in Figures 9–11.

Figure 9. AAC Single phase-to-ground fault at 0.2 s: (a) active power, (b) reactive power, (c) dc-voltage, (d) dc-current, (e) ac currents of AAC, (f) ac currents of MMC, (g) SM capacitor voltages of AAC, and (h) SM capacitor voltages of MMC.

Figure 10. AAC three phase fault at 0.2 s: (a) active power, (b) reactive power, (c) dc-voltage, (d) dc-current, (e) ac currents of AAC, (f) ac currents of MMC, (g) SM capacitor voltages of AAC, and (h) SM capacitor voltages of MMC.

Figure 11. MMC phase-to-phase fault at 0.2 s: (a) active power, (b) reactive power, (c) dc-voltage, (d) dc-current, (e) ac currents of AAC, (f) ac currents of MMC, (g) SM capacitor voltages of AAC, and (h) SM capacitor voltages of MMC.

4.3.1. SLG Fault at the AAC

The dc side voltage and current of the AAC (Figure 9) are affected by ac side power oscillations. The disturbances on the SM capacitor voltages include both oscillations and increased ripples in phase *a*. Moreover, the ac currents and the SM capacitor voltages of the MMC station show that the disturbance in the AAC station during the SLG fault propagates to the MMC station through the dc transmission line. However, the hybrid VSC-HVDC system completely recovers within 600 ms to steady-state riding through the 200 ms SLG fault, demonstrating the appropriate operation of the associated high-level and low-level control functions.

4.3.2. Three-Phase Fault at the AAC

Under a three-phase fault (Figure 10), power oscillations are comparatively lower than that of the SLG fault. The dc side voltages and currents deviate during the 200 ms fault and the disturbance in the dc side is significant at the beginning of the recovery stage. This is caused by a few hard switching transitions of the director switches of the AAC. The AAC capacitor voltage ripples are affected by the fault currents. However, the ac side currents demonstrate that the system rides through the fault and recovers within 600 ms following the fault. Moreover, the disturbance at the AAC station propagates to the MMC station but does not lead to a significant variation or deviation of the MMC operation, demonstrating the effectiveness of the high-level and low-level control functions in handling the three-phase fault.

4.3.3. Phase-to-Phase Fault at the MMC

A phase-to-phase fault (Figure 11) is applied to the MMC station in order to study the impact on the system's performance and the interoperability of the AAC. Similar to the SLG fault at the AAC, the dc side voltages and currents of the MMC are affected by the ac power oscillations. The active power deviation shows a significant impact on the AAC station where the ac currents reduce during the fault. The SM capacitor voltages of the MMC contain slight variations during the fault and the AAC capacitor voltages variations follow the dc voltage variation. However, the system rides through the fault and recovers within 600 ms without leading to larger energy deviations or unstable operation, demonstrating the effectiveness of the associated control functions.

4.4. DC Fault Handling Capability

One of the unique benefits of the AAC over the half-bridge SMs-based MMC is the dc fault-blocking capability. Resilient characteristics are a prime requirement for complex HVDC and MTDC network configurations [6,40]. The performance of the proposed hybrid HVDC system is studied under a pole-to-pole dc fault at the dc bus of AAC.

Following dc fault occurrence, the converters are blocked after a delay of 4 ms [11]. Typically in VSC-HVDC systems, ac-grid breakers open following converter blocking in order to prevent a persistent fault current from the ac side to the dc side. Similarly, the proposed hybrid HVDC system ac-breaker trip signals are triggered together with converter blocking and within 16 ms, all the ac breakers open.

Figure 12 shows the performance of the hybrid HVDC system under a pole-to-pole dc fault. The key difference between the dc fault response of the MMC and AAC is the dc fault-blocking capability. The AAC consists of bipolar SMs which can block the ac voltages and the typical half-bridge-based MMC does not offer dc fault-blocking capability. Unlike the MMC, dc voltage and the current of the AAC terminal drop to zero with oscillations due to the presence of a dc filter. The active power and reactive power of the AAC drop to zero soon after blocking the converter but the active power and reactive power of the MMC lead to a larger variation even after blocking the converter. This is due to the lack of dc fault-blocking capability of the MMC which has to be achieved by either using dc-breakers or utilizing other SMs with dc fault-blocking capability. It is visible in the ac currents of the two HVDC stations. The AAC ac currents do not increase following the dc fault as the AAC blocks the ac voltages after blocking the converter, but the MMC acts as a diode rectifier. Therefore, the MMC ac currents increase and the ac breaker takes longer to open.

Figure 12. DC fault at the AAC dc bus (at 0.05 s): (a) active power, (b) reactive power, (c) dc-voltage, (d) dc-current, (e) ac currents of AAC, (f) ac currents of MMC, (g) SM capacitor voltages of AAC, and (h) SM capacitor voltages of MMC.

4.5. Discussion

Analysis of Figures 6 and 7 demonstrates that the two HVDC stations deliver satisfactory steady-state operation. The transient performance of Figures 8–11 also show

that the proposed hybrid VSC-HVDC system delivers stable performance under power changes and ac faults without leading to sustained disturbances and energy deviations in the converters. Hence, the interoperability of AAC in hybrid HVDC systems can be ensured with appropriate selection of high- and low-level control functions. Moreover, the performance under dc faults of Figure 12 demonstrates the dc fault current limiting capability of the AAC over MMC.

5. Conclusions

The interoperability of emerging modular VSC topologies in established HVDC systems is critical for future dc grid implementations. The AAC's interoperability performance was studied in a hybrid VSC-HVDC system based on MMCs and AACs. Satisfactory operation of the AAC under different operating scenarios was verified by demonstration of detailed results including steady-state and power transient ac faults and dc faults where the hybrid VSC-HVDC system delivered stable operation without leading to sustained disturbances or deviations. This work is a prime step towards further analysis on AAC interoperability with different HVDC converter topologies and detailed validation of AAC interoperability in complex dc grid configurations that will lead future global dc super-grids.

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