

## Article

# Attenuation of Zero Sequence Voltage Using a Conventional Three-Wire Dynamic Voltage Restorer

Rafael Neto <sup>1,\*</sup>, Yandi Landera <sup>1</sup>, Francisco Neves <sup>1</sup>, Helber de Souza <sup>2</sup>, Marcelo Cavalcanti <sup>1</sup>  
and Gustavo Azevedo <sup>1</sup>

<sup>1</sup> Power Electronics and Drives Research Group (GEPAE), DEE, Universidade Federal de Pernambuco, Recife 50740-530, Brazil; yandi.gallego@ufpe.br (Y.L.); francisco.neves@ufpe.br (F.N.); marcelo.ccavalcanti@ufpe.br (M.C.); gustavomsa@aim.com (G.A.)

<sup>2</sup> Department of Industry, Instituto Federal de Educação, Ciência e Tecnologia de Pernambuco, Pesqueira 55200-000, Brazil; helberelias@pesqueira.ifpe.edu.br

\* Correspondence: rafael.cavalcantineto@ufpe.br

**Abstract:** Voltage sags/swells and harmonics are recurring problems in electric energy distribution systems. In order to solve these issues, several dynamic voltage restorer (DVR) topologies, such as the conventional three-wire DVR, have been proposed in the literature. Despite its capability of mitigating voltage disturbances, many researchers have established that conventional three-wire DVR cannot compensate for zero sequence voltage disturbances. In this paper, an in-depth study of the conventional three-phase DVR is presented, which shows that this DVR topology can also be used to attenuate zero sequence voltage components without increasing control complexity. The necessary conditions for this to occur are discussed in details and a brief comparison between the conventional three-wire DVR and other DVR topologies that can compensate for zero sequence voltage disturbances is made. Experimental results are included to validate the theoretical study.

**Keywords:** dynamic voltage restorer; power quality; voltage sags/swells; zero sequence attenuation



**Citation:** Neto, R.; Landera, Y.; Neves, F.; de Souza, H.; Cavalcanti, M.; Azevedo, G. Attenuation of Zero Sequence Voltage Using a Conventional Three-Wire Dynamic Voltage Restorer. *Energies* **2021**, *14*, 1247. <https://doi.org/10.3390/en14051247>

Academic Editor: Julio Barros

Received: 4 January 2021

Accepted: 18 February 2021

Published: 25 February 2021

**Publisher's Note:** MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.



**Copyright:** © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

## 1. Introduction

Due to the advance of microelectronics, sensitive power electronics devices have been increasingly used in all types of industries. The emergent use of such devices motivated discussions about power quality issues, which resulted in researches on solutions that could mitigate them. In this scenario, the dynamic voltage restorer (DVR) was proposed to compensate for momentary voltage disturbances and has been intensively studied in recent decades [1–6].

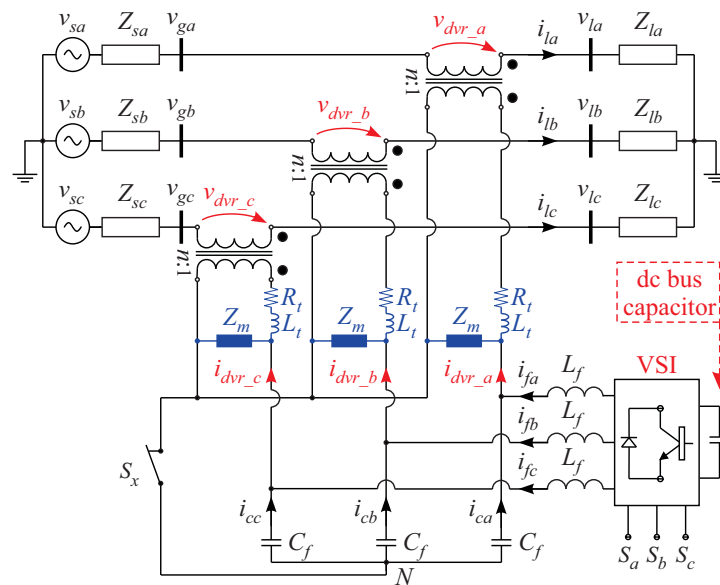
The DVR is a custom-made series active compensator, which means it works as a dependent voltage source placed in series with the supply grid [4]. Thus, with the proper reference generator, the DVR is capable of generating voltages with the same magnitude, but opposite phase angle, of the grid voltage disturbances (such as harmonic contamination and voltage sags). As exemplified in Figure 1 for a three-phase system, a typical topology of DVR is composed of: an energy storage system or a single DC power source (replaced by a DC bus capacitor in Figure 1); a voltage source inverter (VSI); an output filter; and an injection transformer [7].

Regarding the state of the art, the power converter topologies that are mostly used in three-phase DVRs are [6]: two-level (three-wire) inverters; two-level (four-wire) inverters with split-capacitor; four-leg (four-wire) inverters; and three single-phase H-bridge inverters [8–11]. These DVR topologies are typically used in low-voltage grid applications due to the simplicity of their modulation methods and due to their lower costs when compared to multilevel solutions. As the grid voltages are raised to medium-voltage level, the two-level topologies mentioned above become disadvantageous due to the voltage and current limitations of their semiconductor switches. Alternative options for

medium-voltage grid application are [6]: using series-parallel associations of semiconductor switches to increase their maximum blocking voltages and operating currents; or using multilevel inverters [12–14]. However, regardless of the DVR topology used, the solutions for medium-voltage can still be classified into three-wire or four-wire.

When focusing on voltage sags/swells that contain zero sequence components, e.g., a single-phase sag [15,16], it is established in the literature that a three-phase three-wire DVR (Figure 1), such as the scheme based in a two-level inverter, which is referred as conventional DVR in this paper, cannot compensate for these disturbances. As consequence, several authors have proposed new DVR topologies to solve this problem, such as the three-phase four-wire DVR with split capacitors and the four-leg DVR [6,16], both mentioned in the previous paragraph.

In this scenario, this paper presents an in-depth analysis of the conventional three-wire DVR. The contribution is not proposing any new DVR topology, but demonstrating that, differently from the usual assumption, three-phase three-wire DVRs can be used to compensate unbalanced voltage sags/swells (having zero-sequence component). Further, the limitations of this compensation are discussed. This is an important issue, since this topology is the most economical choice and could be applied in many practical situations. Experimental results are included to validate the theoretical study. To the best of the authors' knowledge, the analysis presented here has not been presented in any other publication, being an original contribution of this paper.



**Figure 1.** Three-phase circuit with a conventional three-wire dynamic voltage restorer (DVR).

## 2. Evaluation of the Zero Sequence Component in Three-Phase Circuits with a Conventional DVR

Figure 1 shows a conventional three-wire DVR topology with a single DC bus capacitor, where  $v_{dvr\_a}$ ,  $v_{dvr\_b}$  and  $v_{dvr\_c}$  are the voltages synthesized by the DVR. The parameters  $R_t$ ,  $L_t$  and  $Z_m$  represent the total winding resistance, total leakage inductance and magnetizing impedance of the injection transformers, respectively, all referred to the transformers' secondary side.

Based on the topology presented in Figure 1, the attenuation of zero sequence voltage is discussed below. Since the switch  $S_x$  is considered closed for the following analysis, the neutral point of capacitors  $C_f$  is connected to the neutral point of the transformers. The reader should notice that the switch  $S_x$  is only being used to show the options of filter connection of the conventional DVR evaluated in this paper.

### 2.1. Evaluation of Zero Sequence Component in the Load Voltages When Using a Conventional DVR

Considering the compensation provided by the DVR shown in Figure 1, the load voltages become

$$\mathbf{V}_{l_{abc}} = \mathbf{V}_{g_{abc}} + \mathbf{V}_{dvr_{abc}}, \quad (1)$$

where  $\mathbf{V}_{l_{abc}} = [\vec{V}_{l_a} \ \vec{V}_{l_b} \ \vec{V}_{l_c}]^t$ ,  $\mathbf{V}_{g_{abc}} = [\vec{V}_{g_a} \ \vec{V}_{g_b} \ \vec{V}_{g_c}]^t$  and  $\mathbf{V}_{dvr_{abc}} = [\vec{V}_{dvr_a} \ \vec{V}_{dvr_b} \ \vec{V}_{dvr_c}]^t$  are vectors whose elements are the load, grid and DVR voltage phasors, respectively. However, based on the symmetrical components theory, the zero sequence component of a three-phase signal can be obtained using the following equation:

$$\vec{S}_0 = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \end{bmatrix} \mathbf{S}_{abc}. \quad (2)$$

Therefore, the equation that relates the zero sequence load voltage ( $\vec{V}_{l0}$ ) with the zero sequence grid voltage ( $\vec{V}_{g0}$ ) can be written by

$$\begin{aligned} \frac{1}{3} \sum_{i=a,b,c} \vec{V}_{li} &= \frac{1}{3} \sum_{i=a,b,c} \vec{V}_{gi} + \frac{1}{3} \sum_{i=a,b,c} \vec{V}_{dvr_i} \\ &\downarrow \\ \vec{V}_{l0} &= \vec{V}_{g0} + \frac{(\vec{V}_{dvr_a} + \vec{V}_{dvr_b} + \vec{V}_{dvr_c})}{3}. \end{aligned} \quad (3)$$

Considering that the neutral points of grid and load are connected together, then the currents  $i_{la}$ ,  $i_{lb}$  and  $i_{lc}$  may contain homopolar component. If this happens, since the switch  $S_x$  is considered closed in this analysis, the zero sequence currents that circulate through the primary windings of the injection transformers will also be present in their secondary windings, being part of  $\vec{I}_{dvr_a}$ ,  $\vec{I}_{dvr_b}$  and  $\vec{I}_{dvr_c}$ . Thus, In view of the fact that a three-wire inverter is unable to supply zero sequence currents, i.e.,  $\vec{I}_{fa} + \vec{I}_{fb} + \vec{I}_{fc} = 0$ , the following relation holds when considering a high magnetizing impedance:

$$(\vec{I}_{dvr_a} + \vec{I}_{dvr_b} + \vec{I}_{dvr_c}) = (\vec{I}_{ca} + \vec{I}_{cb} + \vec{I}_{cc}) = 3n\vec{I}_{l0}, \quad (4)$$

in which  $\vec{I}_{l0}$  is the homopolar component of the load currents and  $n$  is the turns ratio of the injection transformers.

The voltage phasor at the primary winding of one injection transformer ( $\vec{V}_{dvr_a}$ ,  $\vec{V}_{dvr_b}$  or  $\vec{V}_{dvr_c}$ ) can be obtained, using the transformer's approximate equivalent circuit (indicated in blue in Figure 1), by summing the voltage over the converter filter capacitor  $C_f$  with the voltage drop in the transformer impedance, but taking the injection transformer turns ratio into account. Thus,

$$\mathbf{V}_{dvr_{abc}} = n \left( -\frac{1}{j\omega C_f} \mathbf{I}_{c_{abc}} - n(R_t + j\omega L_t) \mathbf{I}_{l_{abc}} \right). \quad (5)$$

Thus, when considering the definition of zero sequence component presented in (2), the following equation is obtained:

$$\frac{1}{3} \sum_{i=a,b,c} \vec{V}_{dvr_i} = -\frac{n}{j\omega C_f} \frac{1}{3} \sum_{i=a,b,c} \vec{I}_{ci} - n^2(R_t + j\omega L_t) \vec{I}_{l0}, \quad (6)$$

which can be rewritten as

$$\frac{(\vec{V}_{dvr_a} + \vec{V}_{dvr_b} + \vec{V}_{dvr_c})}{3} = -\frac{n^2}{j\omega C_f} \vec{I}_{l0} - n^2(R_t + j\omega L_t) \vec{I}_{l0}. \quad (7)$$

It should be noted that (7) considers injection transformers with same  $R_t$  and  $L_t$ .

Equation (7) can be substituted into (3) to allow  $\vec{V}_{l0}$  to be calculated in terms of the load impedance and the DVR's parameters. For example, if the load is balanced, ( $Z_{la} = Z_{lb} = Z_{lc} = Z_l = R_l + j\omega L_l$ ), then  $\vec{I}_{l0} = \vec{V}_{l0}/Z_l$  and it becomes possible to rewrite (7) as

$$\vec{V}_{l0} = \frac{\omega C_f (R_l + j\omega L_l)}{\omega C_f (R_l + n^2 R_t) + j(\omega^2 C_f (L_l + n^2 L_t) - n^2)} \vec{V}_{g0}. \quad (8)$$

Since unbalanced three-phase power systems can always be analyzed using symmetrical components [17], the zero sequence grid voltage ( $\vec{V}_{g0}$ ) can always be calculated. This means that (8) will be valid no matter the type of sags/swells present in the grid voltages (three-phase, two-phase, single-phase or two-phase-to-ground).

As presented in [16], none of the terms in (8) can be controlled by the converter. This means that a zero sequence disturbance in the grid voltage cannot be compensated by the DVR of Figure 1 and a homopolar voltage component would also appear in the load voltages. This restriction led researchers to seek alternatives that would make it possible to compensate  $\vec{V}_{l0}$ .

The use of a three-phase four-wire DVR with split capacitors in the DC-bus is a widespread solution to mitigate the zero sequence load voltage. In fact, when modeling the three-phase circuit for this solution (Figure 2) it is possible to obtain the following equation [16]:

$$\vec{V}_{l0} = \frac{(\omega C_f \vec{V}_{g0} - jn \vec{I}_{f0}) Z_l}{\omega C_f (R_l + n^2 R_t) + j(\omega^2 C_f (L_l + n^2 L_t) - n^2)}. \quad (9)$$

Equation (9) shows that the zero sequence load voltage can be eliminated when  $\omega C_f \vec{V}_{g0} = jn \vec{I}_{f0}$ . In this case, the necessary zero sequence current  $i_{f0}$  can be imposed by controlling  $i_{fa}$ ,  $i_{fb}$  and  $i_{fc}$ , what makes it possible to mitigate  $\vec{V}_{l0}$ .

Another well-known solution to this problem is the four-leg DVR topology, which is shown in Figure 3. The fourth leg of this strategy allows the circulation of the homopolar current  $i_0$ , which means that the steady-state mathematical model of the four-leg DVR topology also results in (9). Thus, once again,  $\vec{V}_{l0}$  can be attenuated through the proper control of  $i_{f0}$ , by means of imposing the appropriate values of the DVR's currents  $i_{fa}$ ,  $i_{fb}$  and  $i_{fc}$ .

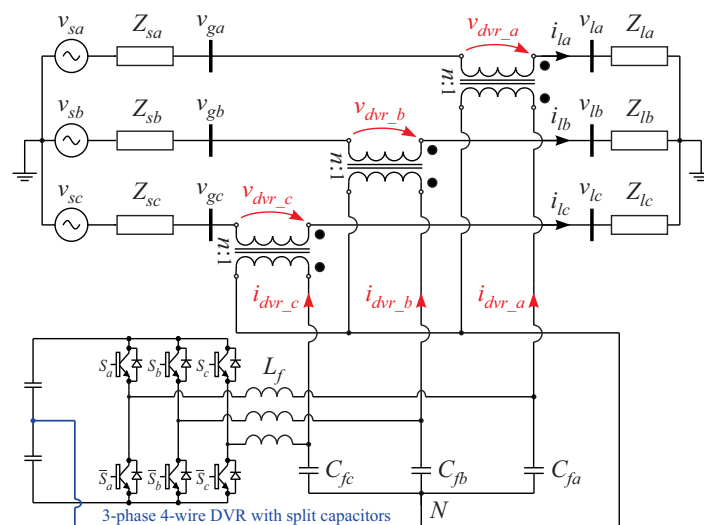
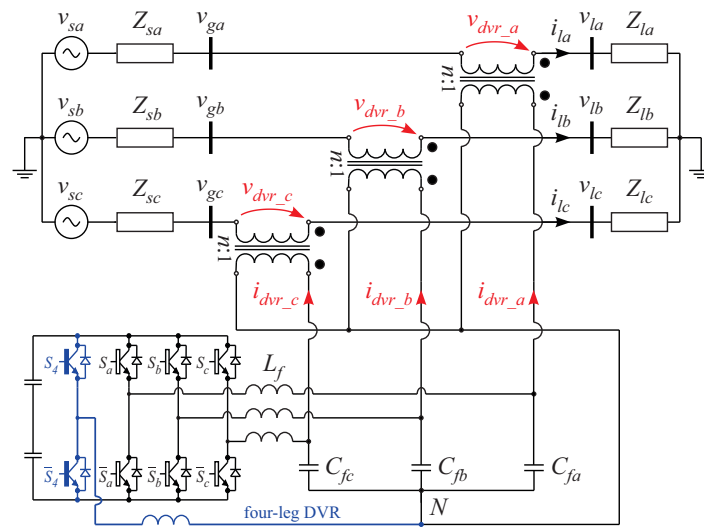


Figure 2. Three-phase circuit with a three-phase four-wire DVR with split capacitors.



**Figure 3.** Three-phase circuit with a four-leg DVR topology.

However, when re-evaluating the conventional three-wire DVR with  $S_x$  closed (Figure 1), (8) can be rewritten as

$$\vec{V}_{l0} = \frac{Z_l \vec{V}_{g0}}{(R_l + j\omega L_l) + (R_t + j\omega L_t)n^2 + \left(\frac{-j}{\omega C_f}\right)n^2} = \frac{Z_l}{Z_l + Z'_t + Z'_c} \vec{V}_{g0}. \quad (10)$$

Thus, if  $|Z'_t + Z'_c| \gg |Z_l|$  then it becomes possible to significantly attenuate  $V_{l0}$  without needing to use any of the solutions described above. If the magnetizing impedance of the injection transformers ( $Z_m$ ) is included in this analysis, Equation (10) becomes

$$\vec{V}_{l0} = \frac{Z_l}{Z_l + Z'_t + Z'_c // Z'_m} \vec{V}_{g0}, \quad (11)$$

which means that the condition to significantly attenuate  $V_{l0}$  becomes  $|Z'_t + Z'_c // Z'_m| \gg |Z_l|$ . Equation (11) is valid no matter the type of sags/swells present in the grid voltages (three-phase, two-phase, single-phase or two-phase-to-ground), showing the ability of strongly attenuating the zero-sequence load voltage. Besides that, (11) also demonstrates that there is a positive correlation between the zero-sequence grid and load voltages, meaning that the zero-sequence load voltage tends to decrease as the zero-sequence grid voltage decreases.

As a matter of fact, since  $i_{fa}$ ,  $i_{fb}$  and  $i_{fc}$  only contain positive and negative sequence currents, the zero sequence equivalent circuit of the electrical diagram in Figure 1 does not include the three-phase inverter and the inductors  $L_f$ . Then, when evaluating the effect of connecting the common points of the AC capacitors and of the injection transformers, it should be noted that:

#### 2.1.1. If $S_x$ Is Closed

- The zero sequence equivalent circuit of the electrical diagram in Figure 1 will include the capacitor  $C_f$ . Thus, the zero sequence equivalent impedance becomes the series association of: the load ( $Z_l$ ); the series impedance of the injection transformers ( $Z'_t$ ); and the RLC parallel impedance formed by  $Z'_c // Z'_m$ .
- The AC filter capacitors and inductors are responsible for filtering out the high frequency harmonic components (switching frequency and its multiples) present in the injected voltages. For the filter design, it must be observed that the capacitance  $C_f$ , inductance  $L_f$ , switching frequency of the DVR's inverter and bandwidth of the control system are all correlated [18]. Thus, the AC capacitors must be designed to behave almost like open circuits at fundamental frequency while providing a low-

impedance path for switching frequency signals. Consequently, it is expected that  $|Z'_t + Z'_c // Z'_m| \gg |Z_l|$  holds for a certain range of frequencies, making it possible to attenuate zero sequence voltage disturbances in this range of frequencies.

### 2.1.2. If $S_x$ Is Opened

- The zero sequence equivalent circuit of the electrical diagram in Figure 1 won't include the capacitor  $C_f$ . Therefore, Equation (11) would become:

$$\vec{V}_{l0} = \frac{Z_l}{Z_l + Z'_t + Z'_m} \vec{V}_{g0}. \quad (12)$$

This means that the condition to significantly attenuate  $V_{l0}$  becomes  $|Z'_t + Z'_m| \gg |Z_l|$ , resulting in a larger zero sequence attenuation range than that obtained if  $S_x$  is closed.

- Since the injection transformers generally have high magnetizing impedance, the conventional DVR is capable of attenuating low-frequency zero sequence voltage components whether the switch  $S_x$  is open or closed. As consequence, despite of the fact that the conventional DVR does not allow the use of single-phase loads, feature that is common to all three-wire DVRs, this solution still can attenuate single-phase sags/swells.

## 2.2. Comparison with Other Usual DVR Topologies

The main advantages of using the conventional DVR over other usual DVR topologies are presented below.

### 2.2.1. Three-Phase Four-Wire DVR with Split Capacitors

In this topology (Figure 2), the zero sequence current that flows through the mid-point of the DC bus can be controlled. On the other hand, when compared to the conventional DVR, this configuration creates a coupling between the DC and AC sides of the VSI, which causes resonance problems and an additional ripple on the DC bus [16]. This ripple can be attenuated by using larger dc bus capacitors [16]. Besides that, the zero sequence component and the voltage unbalance on the DC bus capacitors must be considered during the control system design.

Therefore, the proper design of the output filter of the conventional DVR avoids the problems described above, making it an attractive solution.

### 2.2.2. Four-Leg DVR Topology

In this topology (Figure 3), the VSI has a fourth leg that is connected to the common points of the AC capacitors and the injection transformers. By doing so, it enables the circulation of zero sequence current through the DVR while decouples the DC and AC sides of the VSI. However, this new leg demands two additional switches. The zero sequence component and the switching of the forth leg must be considered during the control system design, resulting in additional complexity.

The conventional DVR requires less semiconductor devices and demands less computational effort than the four-leg DVR does. Thus, the conventional DVR still is an attractive solution.

### 2.2.3. Three-Phase DVR Using Three Single-Phase H-Bridge Inverters

In this topology, an H-bridge is used to generate the DVR voltage over each injection transformer. Therefore, each phase operates independently to compensate for unbalanced voltage disturbances.

An important advantage of the H-bridge based topology over the conventional DVR is that it has higher maximum compensation capability [11]. On the other hand, this strategy requires twice as many semiconductor switches as the conventional DVRs does [11]. Despite the versatility of the H-bridge based topology, its high cost is a major disadvantage, and may even justify not choosing this topology in many situations.



### 3. Experimental Results

A prototype containing the three-phase circuit shown in Figure 1 was used to validate the theoretical analysis presented in Section 2. The parameters of the prototype are shown in Table 1. In this table,  $R_f$  is the inherent resistance of inductors  $L_f$ . Resistors  $R_c$  (not included in Figure 1) are used in series with capacitors  $C_f$  for current limitation purpose. A DC power source was used to supply the DC bus voltage  $V_{dc}$ .

Regarding the control system, the DVR's controllers and the reference generation were implemented in a dSPACE platform, model DS1005, featuring a processor running at 1 GHz [19]. The block diagram of the complete control system is shown in Figure 4. This control system was implemented considering: a fast inner current loop, for controlling the VSI output currents; and a slow outer voltage loop, for controlling positive and negative sequence voltages that must be synthesized over  $C_f$ . Both control loops were implemented in a  $dq$  reference frame aligned with the fundamental frequency grid voltage. As shown in Section 2, the conventional DVR could passively attenuate zero sequence voltage components of low-frequency, thus, as shown in Figure 4, no controller was required for compensating these disturbances.

In this scenario, Figure 5a shows the grid, load and DVR voltages in the occurrence of a single-phase sag of 30%. From Figure 5a, it can be seen that the conventional DVR could attenuate single-phase voltages sags, which contained zero sequence components, as stated in the previous section.

As the load became lighter, the condition  $|Z'_t + Z'_c // Z'_m| \gg |Z_l|$  is compromised. Consequently, it is expected that the conventional DVR will have its ability of attenuating zero sequence voltage component also compromised. In order to confirm this fact, the DVR used for obtaining the results shown in Figure 5a was simulated to attenuate a single-phase sag, but now considering four different loads (Table 2). The data shown in Table 2 were obtained through simulation results in an attempt to achieve a comparison free of disturbances, such as harmonics, unbalanced grid voltages during pre-fault condition or unbalanced load condition.

Table 1. Parameters of the prototype.

$V_g(\text{line})$	$R_l^1$	$L_f$	$R_f$	$C_f$	$R_c$	$V_{dc}$	$f_s^2$	$f_g^3$	$R_m^4$	$L_m^4$	$L_t$	$R_t$	$n$
220 $V_{rms}$	24.2 $\Omega$	2.87 mH	402.5 m $\Omega$	2.2 $\mu$ F	0.5 $\Omega$	350 V	17.28 kHz	60 Hz	1.93 k $\Omega$	1.53 H	1.39 mH	1.0 $\Omega$	1

<sup>1</sup>  $Z_l = Z_{base} = R_l$ . <sup>2</sup> Sampling and switching frequency. <sup>3</sup> Fundamental frequency. <sup>4</sup>  $Z_m = R_m // jX_m = R_m // j\omega L_m$ .

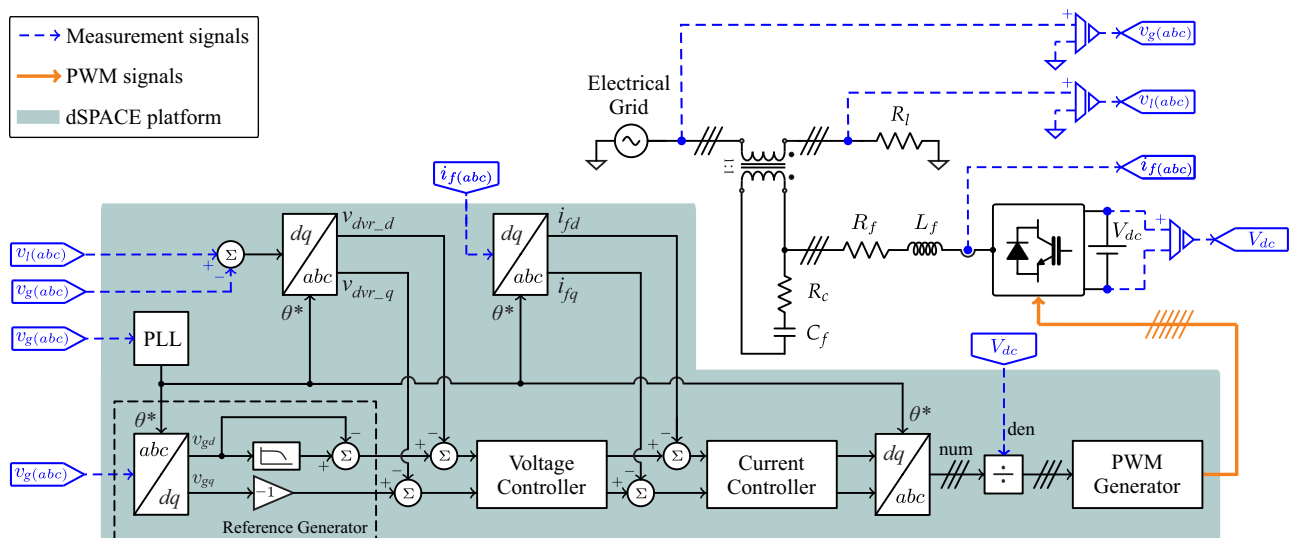
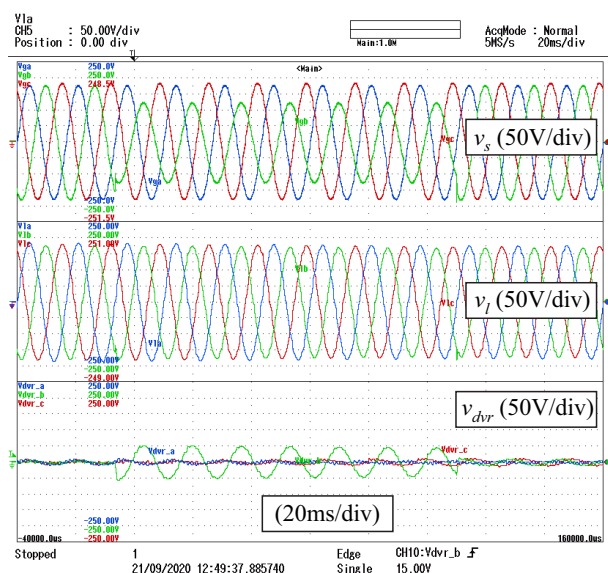


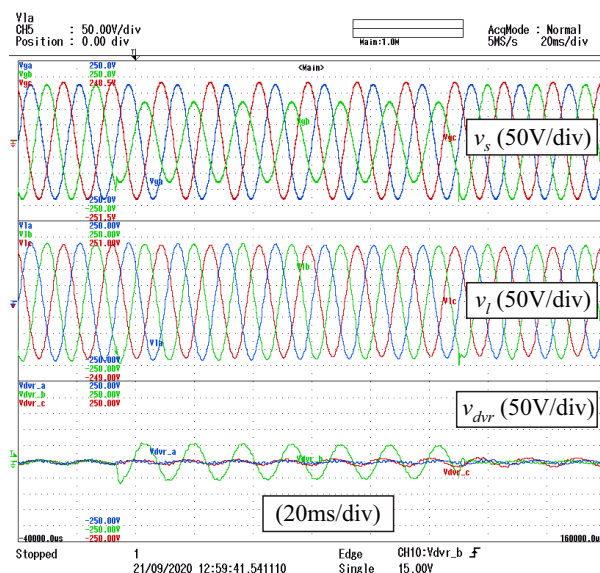
Figure 4. Block diagram of the complete control system used to evaluate the ability of the conventional DVR of attenuating zero-sequence voltages.

**Table 2.** Reduction in the zero sequence load voltage for different loads (simulation results).

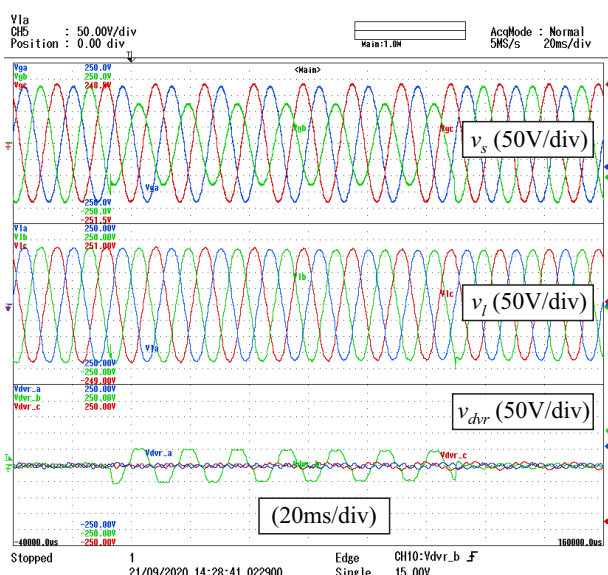
Load Impedance	1 p.u.	2 p.u.	5 p.u.	10 p.u.
Reduction in the zero sequence load voltage	97.6%	95.3%	88.3%	78.0%



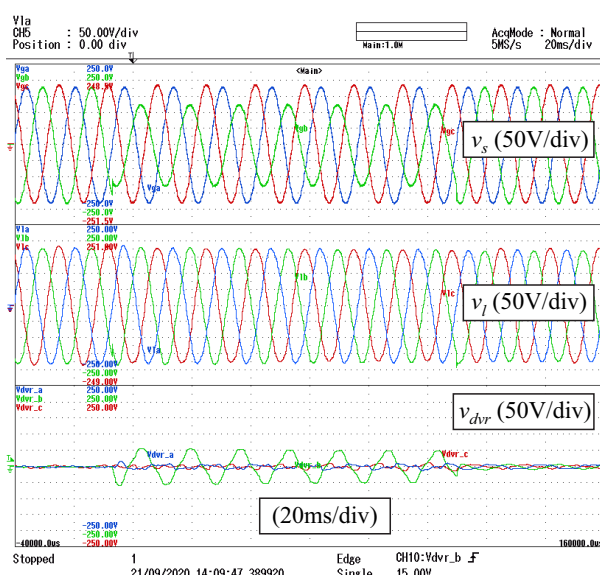
(a) Results for a load impedance of 1 p.u.



(b) Results for a load impedance of 2 p.u.



(c) Results for a load impedance of 5 p.u.



(d) Results for a load impedance of 10 p.u.

**Figure 5.** Grid, load and conventional DVR voltages for a single-phase sag (experimental results). Results obtained for  $S_x$  closed.

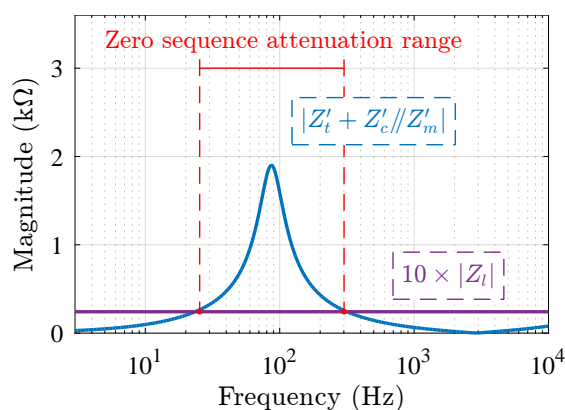
As can be seen in Table 2, the reduction in the zero sequence load voltage decreased as the load impedances increased. However, this reduction was still relevant for loads with impedance around 10 p.u. (apparent power around 0.1 p.u.). This happened because the magnetizing impedance and the AC filter capacitors had high impedances at the frequency of the zero sequence components to be compensated. In order to illustrate this aspect through experimental results, Figure 5b–d show the grid, load and DVR voltages in the occurrence of a single-phase sag of 30% for load impedances of 2 p.u., 5 p.u. and 10 p.u.,



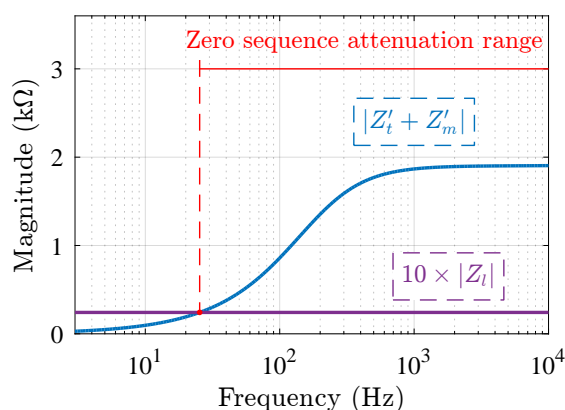
respectively. It should be noted that the waveforms of grid voltages in the laboratory used to obtain experimental results contained some harmonic components. Although these components were less evident in the grid voltage waveforms, they could be easily recognized in the correction voltage (injected by the DVR), due to its lower magnitude.

Since capacitive and inductive impedances depended on the frequency, the conditions  $|Z'_t + Z'_c // Z'_m| \gg |Z_l|$  (for  $S_x$  closed) and  $|Z'_t + Z'_m| \gg |Z_l|$  (for  $S_x$  opened) only held for a certain range of frequencies. In order to evaluate this issue, these conditions were approximated by  $|Z'_t + Z'_c // Z'_m| > 10 \times |Z_l|$  (for  $S_x$  closed) and  $|Z'_t + Z'_m| > 10 \times |Z_l|$  (for  $S_x$  opened) in the following analysis. Therefore, Figures 6 and 7 show the evaluation of the zero sequence attenuation range for a conventional DVR with the parameters shown in Table 1. As discussed in the Section 2.1, a larger zero sequence attenuation range was obtained if  $S_x$  was opened.

In order to extend the analysis presented in the previous paragraph, Figures 8 and 9 show the evaluation of the zero sequence attenuation range for a conventional DVR with the parameters shown in Table 1, but now considering RL loads ( $|Z_l| = Z_{base}$  and  $PF = 0.8$ ). For this new scenario,  $S_x$  opened still led to a larger zero sequence attenuation range, as expected. Since the attenuation range of all four scenarios presented in Figures 6–9 covered the fundamental frequency (60 Hz), single-phase sags/swells would be attenuated by using a conventional three-wire DVR for all four scenarios.

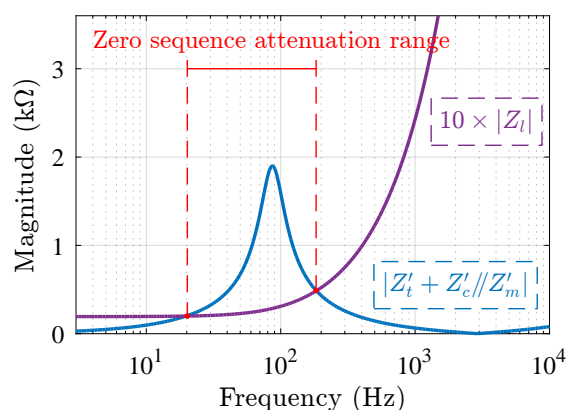


**Figure 6.** Evaluation of the zero sequence attenuation range for resistive loads ( $|Z_l| = Z_{base}$  and  $PF = 1$ ). Analysis for  $S_x$  closed: attenuation range between 25 and 301 Hz.

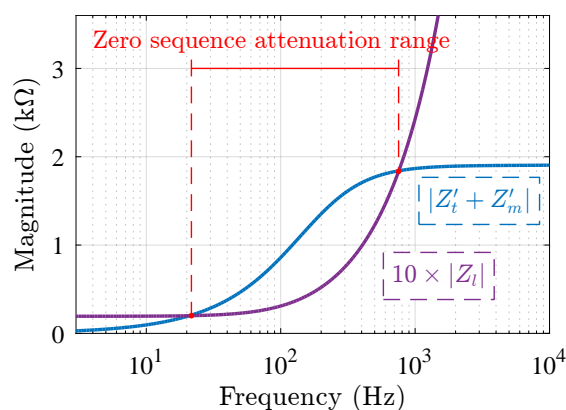


**Figure 7.** Evaluation of the zero sequence attenuation range for resistive loads ( $|Z_l| = Z_{base}$  and  $PF = 1$ ). Analysis for  $S_x$  opened: attenuation range  $> 25$  Hz.

Considering no load operation, the conventional DVR lost the ability of attenuating zero sequence voltages. In this scenario, there would be no zero sequence current circulating in the injection transformers, therefore, no zero sequence voltage would be seen over the capacitors  $C_f$ . This result is in accordance with (11) and (12) for  $Z_l$  tending to infinite.



**Figure 8.** Evaluation of the zero sequence attenuation range for RL loads ( $|Z_l| = Z_{base}$  and  $PF = 0.8$ ). Analysis for  $S_x$  closed: attenuation range between 21 Hz and 183 Hz.



**Figure 9.** Evaluation of the zero sequence attenuation range for RL loads ( $|Z_l| = Z_{base}$  and  $PF = 0.8$ ). Analysis for  $S_x$  opened: attenuation range between 21 Hz and 753 Hz.

### 3.1. Comparative Study between the DVR Topologies Discussed in This Paper

The three DVR topologies that have been discussed in this paper (Figures 1–3) are compared in this subsection. For this purpose, simulation results and technical aspects that differentiate these three topologies are used (Table 3).

**Table 3.** Summary of the comparative study of the DVR topologies discussed in this paper (simulation results).

DVR Topology	Conventional Three-Wire DVR (Figure 1)	Three-Phase Four-Wire DVR with Split Capacitors (Figure 2)	Four-Leg DVR Topology (Figure 3)
Reduction in the zero sequence load voltage *	97.6%	97.8%	96.9%
Does not require dedicated controller for attenuation of zero sequence voltage	✓	✗	✗
Does not couple the DC and AC sides of the VSI	✓	✗	✓
Number of power semiconductor switches	6	6	8

\* Simulation results considering a load impedance of 1 p.u.

As can be seen in Table 3, the conventional DVR did not require dedicated controller for attenuation of zero sequence voltage, did not couple the DC and AC sides of the DVR's inverter, and demanded fewer power semiconductor devices than the other evaluated DVR topologies. These features highlight the economical advantage of using the conven-

tional DVR in applications where it can be used, what emphasizes the importance of this paper's contribution.

However, before choosing the conventional DVR for an application in which the grid voltages may contain zero sequence components, the engineer must evaluate the electrical system in order to determine the DVR's zero sequence attenuation range (as done in Figures 6–9). In fact, depending on the load impedance, the conventional DVR can lead to a reduction in the zero sequence load voltage similar to the four-wire DVR topologies evaluated in this paper (second row of Table 3), which is an advantageous scenario of use of the conventional DVR.

### 3.2. Attenuation of Zero Sequence Voltage for Other Faults Using a Conventional DVR

As stated in Section 2, the conventional DVR can attenuate zero sequence voltages no matter the type of sags/swells present in the grid voltages (three-phase, two-phase, single-phase or two-phase-to-ground). This characteristic was evaluated in simulation for different faults, as indicated in Table 4 and shown in Figure 10.

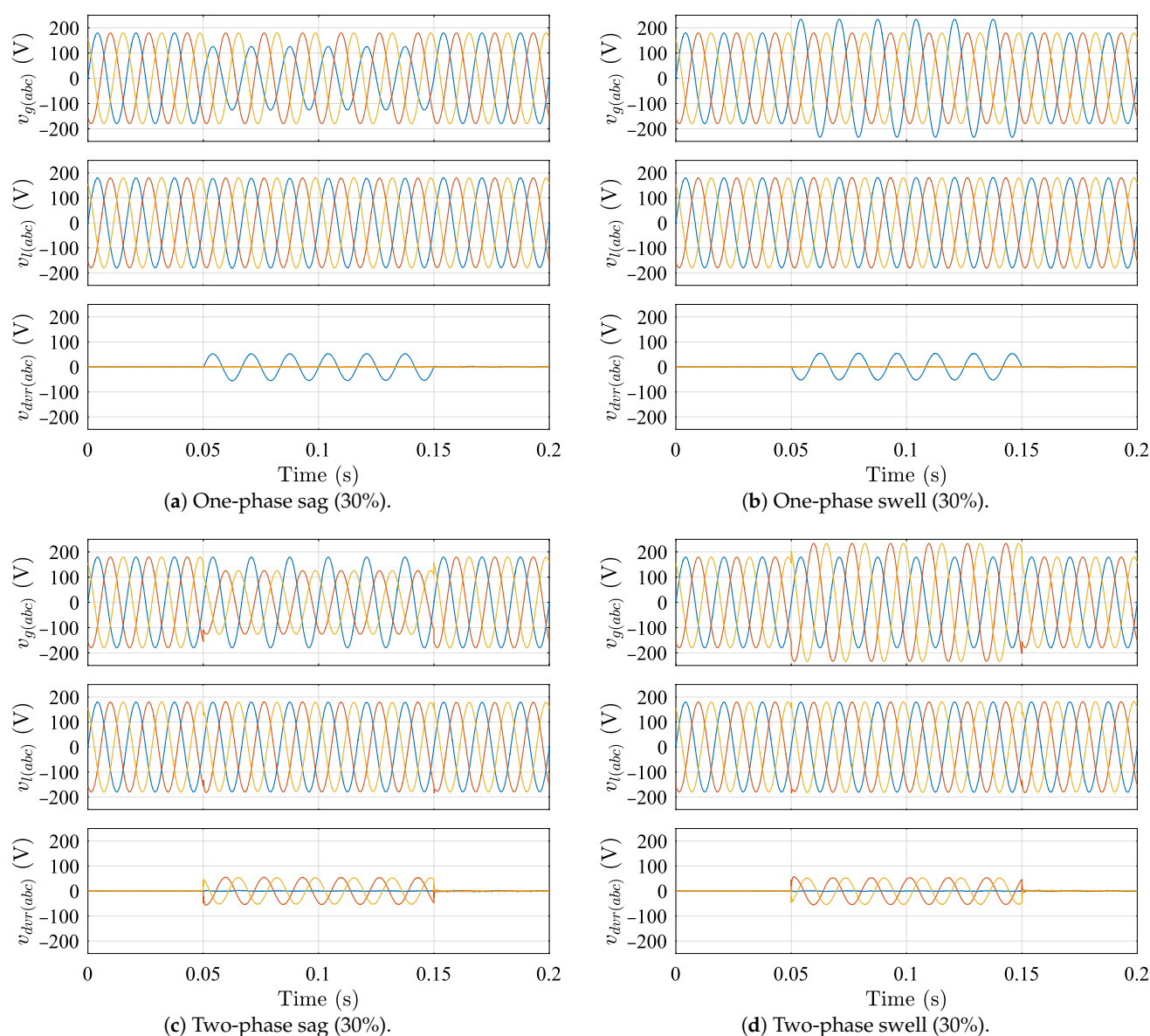
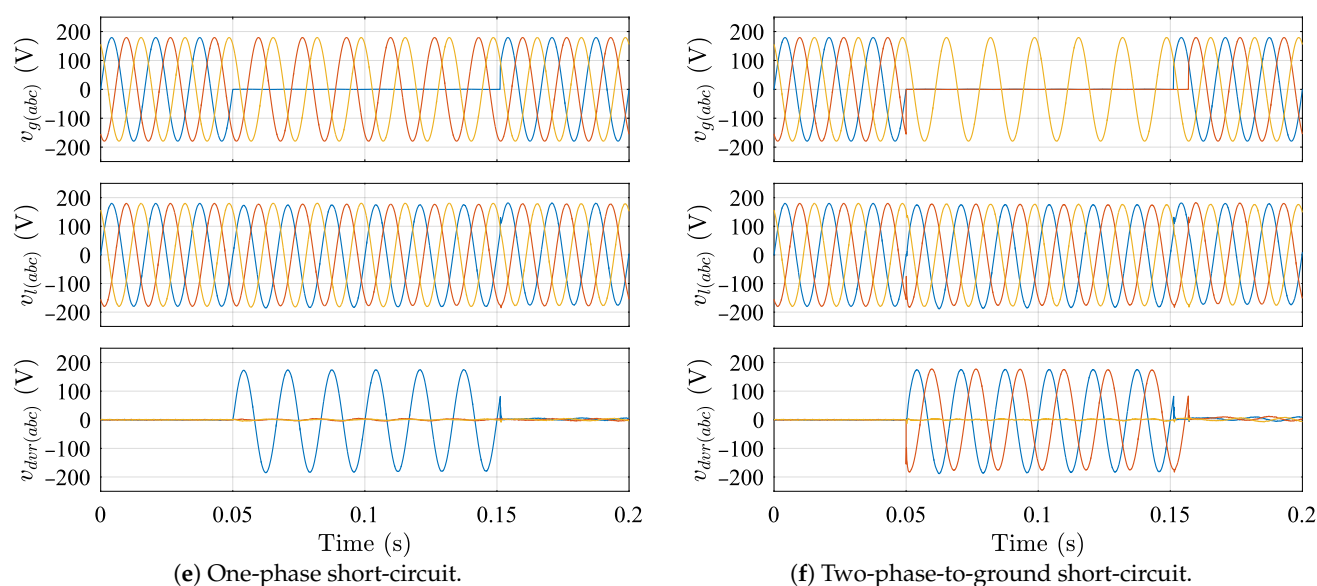


Figure 10. Cont.



**Figure 10.** Grid, load and conventional DVR voltages for different types of faults (simulation results).

As can be seen in Table 4, different faults may lead to different amplitudes of zero sequence grid voltage. However, despite this fact, since all evaluated voltage disturbances were applied to the same electrical circuit, the circuit impedances were the same, which led to:

$$\vec{V}_{l0} = \underbrace{\frac{Z_l}{Z_l + Z'_t + Z'_c // Z'_m}}_{\text{constant}} \vec{V}_{g0}. \quad (13)$$

Equation (13) indicates that the conventional DVR reduces the zero sequence load voltage ( $\vec{V}_{l0}$ ) by a constant factor, regardless of the amplitude of the zero sequence grid voltage ( $\vec{V}_{g0}$ ). This feature can also be seen in the last row of Table 4.

**Table 4.** Summary of the attenuation of zero sequence voltage for different faults being applied to the grid voltages (simulation results).

DVR Topology		Conventional Three-Wire DVR (Figure 1)				
Disturbance	One-phase sag (30%)	One-phase swell (30%)	Two-phase sag (30%)	Two-phase swell (30%)	One-phase short-circuit	Two-phase-to-ground short-circuit
Amplitude of the zero sequence grid voltage *	18.0 V	18.0 V	18.0 V	18.0 V	59.6 V	59.6 V
Reduction in the zero sequence load voltage *	97.6%	97.6%	97.6%	97.6%	97.6%	97.6%

\* Simulation results considering a load impedance of 1 p.u.

#### 4. Conclusions

The great majority power converters used in three-phase DVRs are the three-leg three-wire converter (called conventional topology in this paper), three-leg four-wire split capacitor converter, four-leg converter and three full-bridge single-phase converters. Despite being the simplest and less expensive of them, the conventional topology has been avoided whenever it is necessary to compensate for unbalanced sags/swells, which have zero-sequence component. In this paper, it is shown that, differently from the usual assumption, three-phase DVRs using the conventional topology can be used to compensate unbalanced voltage sags/swells. The theoretical analysis presented shows that the injection transformer zero-sequence current must flow through the parallel association of its magnetizing impedance and of the converter filter capacitor. Once these impedances must be

high in the fundamental frequency, it is demonstrated that the zero-sequence load voltage becomes greatly attenuated. It was observed that the ability of the conventional topology to attenuate unbalanced sags/swells is reduced for very low power loads. The mathematical conclusions are validated through experimental and simulation results, considering several types of sags and swells and comparing the response of the conventional and other types of topologies. Further, it is shown how the AC filter capacitors can be tuned so that the parallel resonance between the capacitive reactance and the magnetizing impedance of the injection transformers results in maximum impedance around a frequency of interest, improving the zero sequence attenuation at that frequency.

**Author Contributions:** Conceptualization, R.N. and Y.L.; methodology, R.N. and F.N.; formal analysis, R.N. and F.N.; investigation, R.N., F.N., H.d.S. and G.A.; validation, R.N. and Y.L.; resources, F.N., M.C. and G.A.; data curation, R.N. and Y.L.; writing—original draft preparation, R.N., F.N. and H.d.S.; visualization, R.N.; supervision, F.N.; project administration, F.N.; funding acquisition, F.N. and M.C. All authors have read and agreed to the published version of the manuscript.

**Funding:** This research was funded by Universidade Federal de Pernambuco—UFPE, Conselho Nacional de Desenvolvimento Científico e Tecnológico—CNPq and Coordenação de Aperfeiçoamento de Pessoal de Nível Superior—CAPES.

**Institutional Review Board Statement:** Not applicable.

**Informed Consent Statement:** Not applicable.

**Data Availability Statement:** No new data were created or analyzed in this study. Data sharing is not applicable to this article.

**Acknowledgments:** The authors would like to thank Universidade Federal de Pernambuco, CNPq and CAPES, for the financial support.

**Conflicts of Interest:** The authors declare no conflict of interest.

## Abbreviations

The following abbreviations are used in this manuscript:

DVR	Dynamic Voltage Restorer
VSI	Voltage Source Inverter
PF	Power Factor

## References

1. Goharrizi, A.Y.; Hosseini, S.H.; Sabahi, M.; Gharehpetian, G.B. Three-Phase HFL-DVR with Independently Controlled Phases. *IEEE Trans. Power Electron.* **2012**, *27*, 1706–1718. [\[CrossRef\]](#)
2. de Almeida Carlos, G.A.; dos Santos, E.C.; Jacobina, C.B.; Mello, J.P.R.A. Dynamic Voltage Restorer Based on Three-Phase Inverters Cascaded Through an Open-End Winding Transformer. *IEEE Trans. Power Electron.* **2016**, *31*, 188–199. [\[CrossRef\]](#)
3. Ye, J.; Gooi, H.B.; Zhang, X.; Wang, B.; Pou, J. Simplified Four-Level Inverter-Based Dynamic Voltage Restorer with Single DC Power Source. *IEEE Access* **2019**, *7*, 137461–137471. [\[CrossRef\]](#)
4. Tu, C.; Guo, Q.; Jiang, F.; Wang, H.; Shuai, Z. A Comprehensive Study to Mitigate Voltage Sags and Phase Jumps Using a Dynamic Voltage Restorer. *IEEE J. Emerg. Sel. Top. Power Electron.* **2020**, *8*, 1490–1502. [\[CrossRef\]](#)
5. Roldán-Pérez, J.; García-Cerrada, A.; Rodríguez-Cabero, A.; Zamora-Macho, J.L. Comprehensive Design and Analysis of a State-Feedback Controller for a Dynamic Voltage Restorer. *Energies* **2018**, *11*, 1972. [\[CrossRef\]](#)
6. Moghassemi, A.; Padmanaban, S. Dynamic Voltage Restorer (DVR): A Comprehensive Review of Topologies, Power Converters, Control Methods, and Modified Configurations. *Energies* **2020**, *13*, 4152. [\[CrossRef\]](#)
7. Tu, C.; Guo, Q.; Jiang, F.; Chen, C.; Li, X.; Xiao, F.; Gao, J. Dynamic voltage restorer with an improved strategy to voltage sag compensation and energy self-recovery. *CPSS Trans. Power Electron. Appl.* **2019**, *4*, 219–229. [\[CrossRef\]](#)
8. Al Hosani, K.; Nguyen, T.H.; Al Sayari, N. An improved control strategy of 3P4W DVR systems under unbalanced and distorted voltage conditions. *Int. J. Electr. Power Energy Syst.* **2018**, *98*, 233–242. [\[CrossRef\]](#)
9. Fernandes, D.A.; Naidu, S.R.; Lima, A.M.N. A four leg voltage source converter based dynamic voltage restorer. In Proceedings of the 2008 IEEE Power Electronics Specialists Conference, Rhodes, Greece, 15–19 June 2008; pp. 3760–3766.
10. Nielsen, J.G.; Newman, M.; Nielsen, H.; Blaabjerg, F. Control and testing of a dynamic voltage restorer (DVR) at medium voltage level. *IEEE Trans. Power Electron.* **2004**, *19*, 806–813. [\[CrossRef\]](#)

11. Babaei, E.; Kangarlu, M.F. Comparison four topologies for three-phase dynamic voltage restorer. In Proceedings of the 2015 International Conference on Renewable Energy Research and Applications, Palermo, Italy, 22–25 November 2015; pp. 1527–1532.
12. Wang, B.; Illindala, M. Operation and control of a dynamic voltage restorer using transformer coupled H-bridge converters. *IEEE Trans. Power Electron.* **2006**, *21*, 1053–1061. [[CrossRef](#)]
13. Roncero-Sanchez, P.; Acha, E. Dynamic Voltage Restorer Based on Flying Capacitor Multilevel Converters Operated by Repetitive Control. *IEEE Trans. Power Deliv.* **2009**, *24*, 951–960. [[CrossRef](#)]
14. Farhadi Kangarlu, M.; Hosseini, S.H.; Babaei, E.; Khoshkbar Sadigh, A. Transformerless DVR topology based on multilevel inverter with reduced number of switches. In Proceedings of the 2010 1st Power Electronic Drive Systems Technologies Conference (PEDSTC), Tehran, Iran, 17–18 February 2010; pp. 371–375.
15. Chung, I.Y.; Park, S.Y.; Moon, S.I.; Hur, S.I. The control and analysis of zero sequence components in DVR system. In Proceedings of the 2001 IEEE PES Winter Meeting (Cat. No.01CH37194), Columbus, OH, USA, 28 January–1 February 2001; Volume 3, pp. 1021–1026.
16. Vilathgamuwa, D.M.; Wijekoon, H.M. Mitigating Zero Sequence Effects in Dynamic Voltage Restorers. In Proceedings of the 38th IEEE Power Electronics Specialists Conference, Orlando, FL, USA, 17–21 June 2007; pp. 3079–3085.
17. Fortescue, C.L. Method of symmetrical co-ordinates applied to the solution of polyphase networks. *Trans. Am. Inst. Electr. Eng.* **1918**, *37*, 1027–1140. [[CrossRef](#)]
18. Sasitharan, S.; Mishra, M.K. Design of passive filter components for switching band controlled DVR. In Proceedings of the 2008 IEEE Region 10 Conference (TENCON 2008), Hyderabad, India, 19–21 November 2008; pp. 1–6.
19. dSPACE Inc. DS1005 PPC Board. Brochure, 2007. Available online: [http://www.ceanet.com.au/Portals/0/documents/products/dSPACE/dSPACE-flyer2007\\_DS1005\\_p484.pdf](http://www.ceanet.com.au/Portals/0/documents/products/dSPACE/dSPACE-flyer2007_DS1005_p484.pdf) (accessed on 9 February 2021).