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A New Robust Digital Non-Linear Control for Power Factor Correction—Arc Welding Applications

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Abstract: A welding power source is commonly assimilated to a non-linear load. Arc welding market being in full growth, the resulting harmonic pollution is becoming an increasingly difficult problem to ignore. Therefore, the main purpose of this work is to define and implement the most suitable solution for power factor correction in a welding power source. Due to the high non-linearity of the electric arc, the current controller used to control grid current need to show high robustness. Consequently, this paper focuses on the digitization of a very robust Phase-Shift Self-Oscillating Current Controller (PSSOCC), which only exists in its analog version until then, to carry out this task. After quick descriptions of the entire energy conversion chain and the PSSOCC operation principle, a model of the digital PSSOCC is proposed. Then, the quality and the accuracy of the aforementioned model are evaluated and its operating limits are identified. Afterwards, the behavior of the digital controller is studied within a Power Factor Correction (PFC) regulation for several specific arc welding operating modes. Finally, excellent robustness of this new FPGA-based digital current controller, named DPSSOCC, is confirmed on a three-phase Vienna converter test bench.

Keywords: power factor correction; arc welding; non-linear control; robust current controller; self-oscillation; digital control; three phase Vienna converter; FPGA

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1. Introduction

The global welding market size was $ 19.53 billion in 2019 and forecast to reach more than $ 25 billion by 2027 [1]. At the European scale, 2018 sales reached € 2 billion [2]. Then, in addition being important, the welding market is in full expansion. The origins of this strong growth can be explained by many factors. Among them, the huge diversity of areas using arc welding devices such as automotive industry and building trades, but also the diversity of arc welding techniques are the most relevant. Moreover, with the current trend dealing with arc welding automation, robotized welding parks are becoming more and more common.

Traditionally, welding power sources use a grid-connected diode rectifier with capacitive load for the AC/DC energy conversion stage. This electronic architecture leads to a strong distortion of the current consumed on the grid. As a result, arc welding devices are seen as non-linear loads generating harmonic pollution with potential harmful consequences for electrical grid installations and devices using the electrical grid energy [3]. The arc welding market size associated to this harmonic pollution constitutes a problem that need to be solved. To do so, standards have been established in order to impose on manufacturers the marketing of products that consume electricity properly, which translates into a unitary power factor. The most commonly used solutions used for power factor correction are passive filters, active filters [4,5] and Power Factor Correction (PFC) commands [6–8]. The small size and the low weight of a welding power source being very important, a PFC control law is preferred.

The electric arc at the output of the welding power source shows high non-linearity that impacts the whole energy conversion chain including the mains supply. Moreover, those power devices are likely to be used in stressful conditions where the mains supply quality can be poor. In addition, the lack of knowledge of power supply cables lengths and the sudden variations in power demand, specific to welding power sources, strongly affect the grid voltage. As the welding market is in full expansion, optimization of current consumption is sough-after. The introduction of a standard requiring a more restrictive unitary power factor being expected in the near future, a robust PFC command needs to be used.

Besides, with current trends towards compactness and connectivity of products, a digital control is ineluctable. Focusing on the current controller, hysteresis control [9], one cycle control (OCC) [10] and phase-shift self-oscillating current controller (PSSOCC) [11] are among the most robust. The hysteresis controller, in its simplest version, shows limitations regarding the control of the maximum switching frequency. The OCC control does not need any grid voltage measurement for the synchronization on the grid but might be in default in case of voltage grid distortion, or if the arc welding device is supplied by a power generator having a huge output inductance value [12]. The PSSOCC controller limits the maximum switching frequency and can operate in a wide range of configurations, making it the best solution in the area considered in this work. The main problem is that this controller only exists in its analog version.

The performances of this phase-shift self-oscillating current controller has been compared with auto adaptive Hysteresis control [13], sliding current control without limitation on the maximum switching frequency [14] and with a control on the maximum oscillation frequency [15]. The results of those studies have demonstrated the superior performances of the PSSOCC and its high robustness. Indeed, this controller depends only very little on system parameters such as input inductance or DC bus voltage and is only slightly influenced by external disturbances. In addition, this variable frequency controller allows the maximum switching frequency of the system to be controlled, thus ensuring high operational reliability. Besides its good performances, the PSSOCC has the advantage of being easy to adjust since its concept simply depends on the design of a second order low-pass filter.

The peculiarities of the PSSOCC controller make its digitization different from most classic digital controllers. Indeed, the need to preserve the harmonic content of the measured current as well as the importance of the consideration of the time delays related to the digital processing of information, involves the introduction of a specific digitization process. Hence, the aim of this work is to design, to study and to develop the first digital version of the PSSOCC, named DPSSOCC, within a PFC control law for welding power source. To reach this objective, the paper is organized as follows. Firstly, the whole arc welding architecture is described and main regulation features, such as PSSOCC operation principle, are introduced. Then, the first model of the DPSSOCC is proposed, and then analyzed. Its performances and limits are evaluated in Section 3. Thereafter, Section 4 shows the behavior of the new current controller within the complete energy conversion chain of a welding power source. Finally, experimental results present the DPSSOCC, implemented on FPGA, used for the current control in a three-phase Vienna converter. Limits and likely improvements of the whole study are discussed before to conclude.

2. Arc Welding System Description

2.1. Energy Conversion Chain Description

The energy conversion chain modelled in this paper, and depicted in Figure 1, is very close to the one inside a metal inert/active gas (MIG/MAG) [16,17] welding power source. Nevertheless, it should be noted that the considered energy conversion chain could be included in a multi-process welding power source including MIG/MAG, MMA, TIG and gouging. The main restriction is that the electric arc cannot be an AC one since the DC/DC converter architecture doesn't allow reverse polarity.

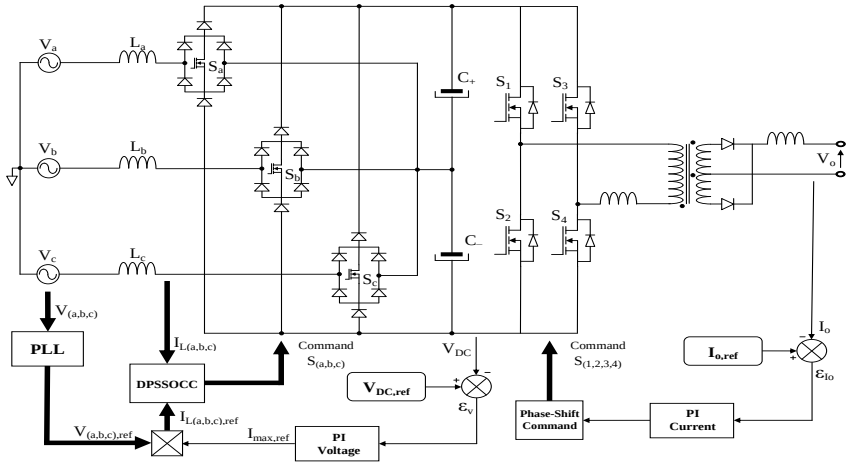


Figure 1. Circuit schematic of the complete energy conversion chain of a welding power source.

The global energy conversion chain can be split into two stages of energy conversion. On the one hand, a three-phase Vienna converter performs the AC/DC conversion from the grid to the DC voltage bus. A PFC control on this converter topology permits to reach a unitary power factor and allows the DC voltage bus control. On the other hand, the DC voltage bus is used as a supply voltage for the second DC/DC stage providing the electric arc. The DC/DC converter is composed by a single phase Full-Bridge, a center tapped voltage step-down transformer, a diode rectifier and an output inductor. This power converter, operating at fixed frequency, controls the output power thanks to the phase-shift between full-bridge legs.

The electric arc at the output of the device is seen as a highly non-linear load by the grid. It is characterized by a high current and a low voltage. In this case, the welding power source architecture described could operate for a range of output current from 10 to 650 A. The duty cycle at the maximum output current would then depend on the semi-conductors' design and properties. It should be noted that to comply with standards and to protect the user, the galvanic isolation between grid and electric arc is mandatory and ensured by a power transformer.

2.2. PSSOCC Operation Principle

Before digitizing the PSSOCC, basis of its operation principle are recalled in this sub-section. The distinctive feature of the PSSOCC is that low but also high frequencies of the measured current are used in the control loop. Indeed, the current feedback loop is used to control the low frequencies content whereas the high frequencies content is generated by a self-oscillation of the system in closed loop. Then, that oscillation frequency generation defines the power converter maximum switching frequency. Its expression can be easily determined assimilating the non-linear power converter to a linear amplifier [18]. Figure 2 gives a simplified synoptic of the PSSOCC regulation per phase of a three phase Vienna converter.

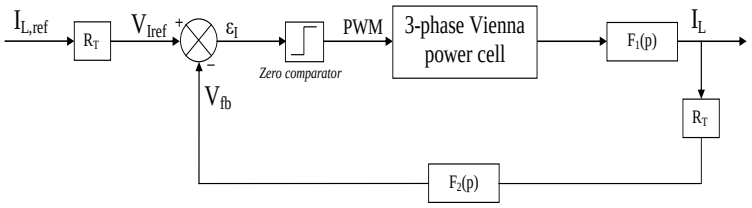


Figure 2. PSSOCC current control technique synoptic per phase.

The PFC coil L, with its internal resistance R, is modeled by a first order low-pass filter. Its transfer function $F_1(p)$ is given by Equation (1). Furthermore, $F_2(p)$ transfer function

given by Equation (2) depicts a second order low-pass filter included in the PSSOCC controller and R_T is the transfer function of an ideal current sensor [19]:

$$F_1(p) = \frac{1}{R} \times \frac{1}{1+\tau p} \tag{1}$$

$$F_2(p) = \frac{1}{1+\frac{2\xi}{\omega_o}p+\frac{p^2}{\omega_o^2}} \tag{2}$$

with ω_o the natural pulsation of the 2nd order low-pass filter, ξ its damping factor and τ_1 the time constant of the coil.

It is very common in the electrical engineering area, including the arc welding sector, that the cut-off frequency due to the presence of the coil at the input of the power converter be much lower than the switching frequency of the system. Considering this hypothesis, it is admitted that the first order low-pass filter, i.e., the voltage to current coil transfer function, produces a phase rotation almost equal to $-90°$ at the switching frequency and upper components. As well, the error detector generates a $\pm 180°$ phase rotation. Assuming, thanks to Barkausen's criterion, that a system self-oscillates if its phase rotation is equal to $0°$ modulo $360°$ and considering the negative input of the error comparator, $-90°$ are missing to reach the self-oscillation. This remaining $-90°$ phase rotation is then provided by the second order low-pass filter at its natural frequency f_o. In case the coil value cannot be modified, F_2's natural frequency is the main element which affects the maximum switching frequency value. The influence of f_o on the maximum oscillation frequency value f_{osc} is illustrated by its expression given by Equation (3) from [20,21]:

$$\frac{f_{osc}}{f_o} = \sqrt{1+\frac{2\xi}{\omega_o \tau_1}} \tag{3}$$

Equation (3) also confirms the theoretical robustness of the PSSOCC since 2ξ, uses to be much lower than $\omega_o \tau_1$ in the considered application. To complete the PSSOCC operating mode description, Figure 3 illustrates how each component of the system acts on the total phase rotation, setting the maximum oscillation frequency.

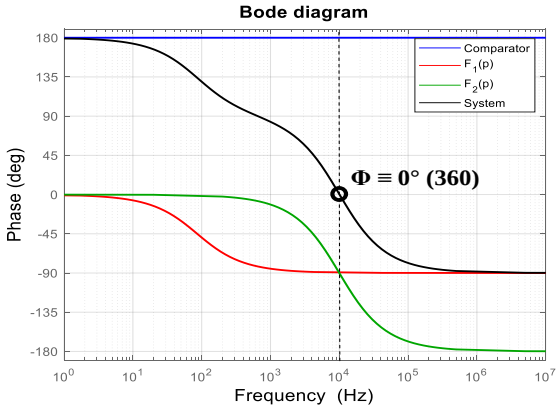


Figure 3. Phase rotation of the system and of each element of the PSSOCC ($f_o = 10$ kHz).

2.3. DC Bus Balance Management

Since the signal acquisition, measurement and processing chains cannot be rigorously perfect, there are always offsets and imperfections in phase and amplitude of the signals. Adding to these irregularities the drifts and the tolerances of the various components of the power converter, an asymmetry is observed within the Vienna topology. An imbalance can then exist between the voltages of the two electrochemical capacitors of the DC bus. Hence, the entire DC voltage bus still follows its reference, but an overvoltage appears on one of

the two capacitors. The simplest solution to correct this imbalance is to use an additional control loop that adds a component to the reference current [22,23] as shown in Figure 4.

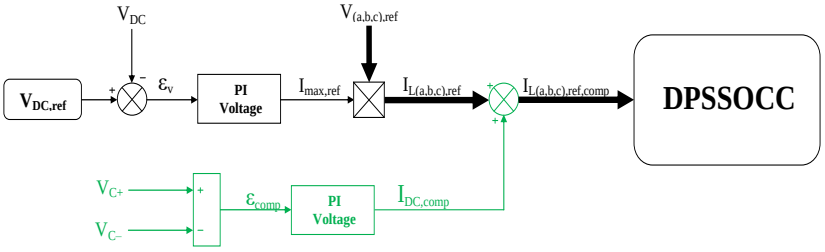


Figure 4. Synoptic of the imbalance voltage compensation loop.

3. Digital Phase-Shift Self-Oscillating Current Controller

3.1. PSSOCC Model Inaccuracy

Studies presented in [24,25] investigated the accuracy of the PSSOCC controlling the output current of a DC/AC converter. A main result of those works is that there is an important error between the theoretical value of the maximum oscillation frequency and the maximum switching frequency observed in practice, especially in case the maximum switching frequency targeted is pretty high. This error of the model is clarified with Figure 5 depicting the input current spectrum of a single-phase Vienna converter controlled by PSSOCC.

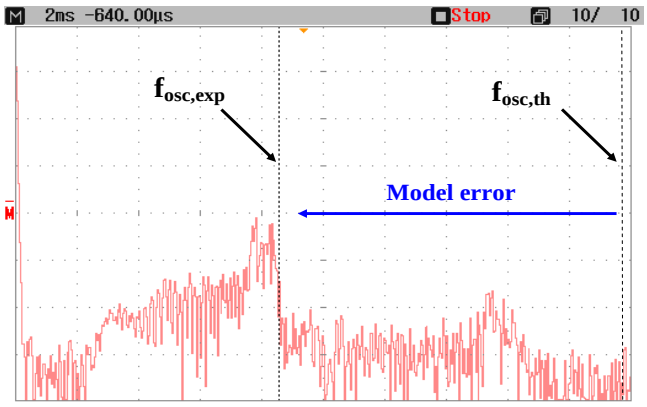


Figure 5. Spectrum of the current input of a single-phase Vienna converter (f_o = 49.25 kHz, ξ = 1).

The original model of the PSSOCC with Equation (3) gives a theoretical value of the maximum oscillation frequency $f_{osc,th}$ of 49.341 kHz, considering a time constant τ_1 of 1.8 ms, whereas the experimental test bench provides a maximum oscillation frequency $f_{osc,exp}$ of 21.4 kHz. The resulting error is then about 56.63% which implies the need to improve the PSSOCC model.

3.2. PSSOCC Model Improvement

It has been shown in [24,25] that the inaccuracy of the model came from missing components. Indeed, each element of the system acting on its total phase shift has an impact on the maximum self-oscillation point depicted in Figure 3. Consequently, those elements change the maximum oscillation frequency value. In the context of this paper, main component related to the maximum switching frequency decrease are additional low-pass filters, in particular the current sensor bandwidth, and time delays, regardless of their origins. Taking into account the time delays and low-pass filters in the model leads to a complex expression of the frequency [24]. The best way to make use of this expression is to plot the evolution of this frequency as a function of the time delay and/or of the bandwidth of the current sensor. A representation of both curves is proposed in

Figures 6 and 7. The maximum oscillation frequency including only the time delays is noted $f_{osc,\delta}$. If the current sensor bandwidth is also taken into account, $f_{osc,BW,\delta}$ is the notation adopted. The cut-off frequency of the current sensor is f_3.

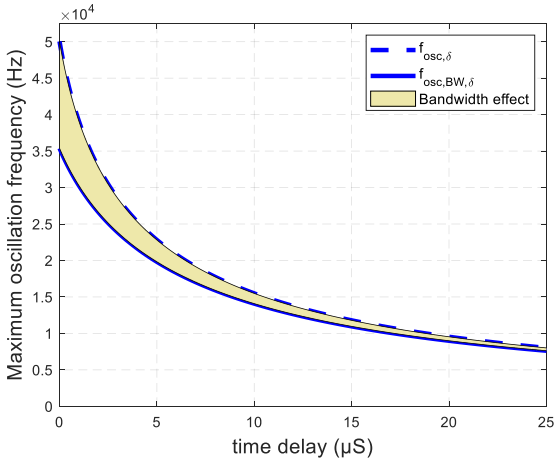


Figure 6. Evolution of the maximum oscillation frequency under PSSOCC control, as a function of the time delay, for a natural frequency f_o of 50 kHz, a unitary damping factor ξ, a time constant τ_1 of 3.6 ms and a current sensor bandwidth of 100 kHz.

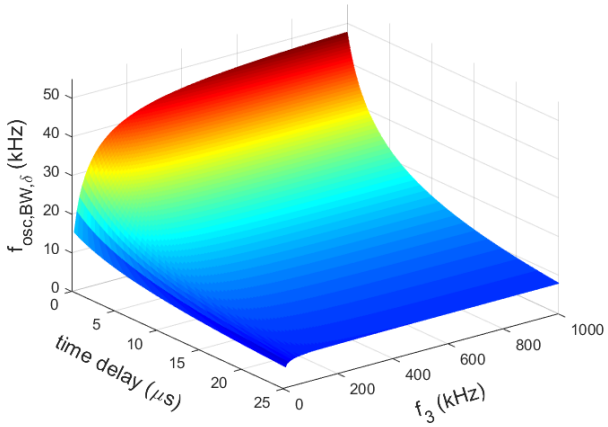


Figure 7. Evolution of the maximum oscillation frequency under PSSOCC control, as a function of the time delay and the current sensor bandwidth ($f_o = 50$ kHz; $\xi = 1$; $\tau_1 = 3.6$ ms).

It clearly appears from those results that the minimization of the time delays and the use of a high bandwidth for the current sensor are fundamental in order to increase the maximum switching frequency. Eventually, the knowledge of the current sensor bandwidth and a good estimation of the system time delays permits to precisely determine the maximum switching frequency of the power converter controlled by PSSOCC. It should be noted that the aforementioned theoretical approach does not depend on the power converter topology since the PSSOCC is extremely robust.

3.3. DPSSOCC Proposed Model

The proposed model of the Digital Phase-Shift Self-Oscillating Current Controller (DPSSOCC) is described in this subsection. This digital model is based on the analog one. Indeed, the difference between the analog and the digital controller is that digital implementation comes with signals sampling. A very often used sampling method is the zero-order hold. This is the one considered in this work.

The PSSOCC model improvement study is focused on the knowledge of the maximum oscillation frequency through an approach in the frequency domain. In that respect,

we assume that each digital component operating at a defined sampling frequency can be modelled by its corresponding time delay. Hence, the DPSSOCC FPGA-based model is depicted in Figure 8.

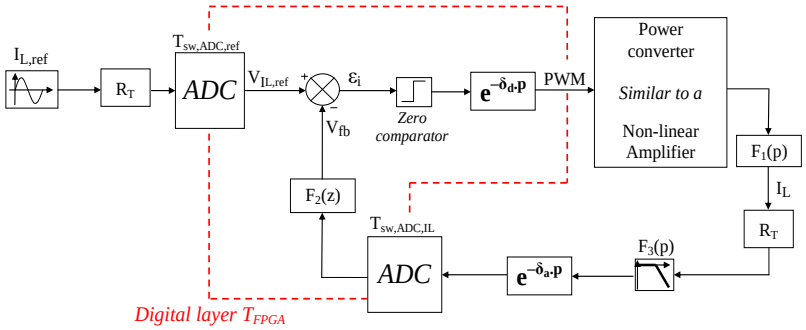


Figure 8. DPSSOCC proposed model.

The digital layer can be divided in three parts with three distinct sampling frequencies. Firstly, the global clock of the FPGA has the fastest clock frequency which is imposed by an external clock at a frequency f_{FPGA} of 50 MHz. As a result, the system can be modified each 20 ns corresponding to the time period T_{FPGA}. All other clocks of the system are based on this global clock since FPGA are known to have better performances if the digital architecture is synchronous. Secondly, the data conversion from analog to digital is done with a specific frequency $f_{sw,ADC}$, thus a specific sampling period $T_{sw,ADC}$. This sampling frequency is limited by the ADC features. Thirdly, the digital second order low-pass filter $F_2(z)$ acts at a sampling frequency $f_{sw,F2}$, so a time period $T_{sw,F2}$. The filter sampling frequency is limited by the FPGA Clock and by the VHDL filter design.

The total system time delay δ_{system} is then made up of two types of time delays. Indeed, δ_a is the time delay of the analog part whereas δ_d is the time delay dedicated for the digital part. Formally, the total time delay is defined by Equation (4) where the first term is the sum of the m time delays of the analog part and the second term is the sum of the n time delays of the digital part of the electronic board:

$$\delta_{system} = \sum_{i=1}^{m} \delta_{a,i} + \sum_{i=1}^{n} \delta_{d,i},\ (m,n) \in \mathbb{N}^* \tag{4}$$

Analog time delays come from analog components, thus they are constant if it is considered that no component of the system are modified. Digital time delays also come from components features, but they can be changed without modification on the electronic board. For instance, sampling frequencies are easy to modify in the VHDL code. Therefore, with the knowledge of each component features and each sampling frequency, the δ_{system} value can be defined, leading to the determination of the maximum oscillation frequency.

In the same manner as for the PSSOCC, the method to find the frequency $f_{osc,BW,\delta}$ with DPSSOCC control is to consider the linear transfer function chain S(p) given by Equation (5) in [24,25]:

$$S(p) = R_T F_1(p) F_2(p) F_3(p) e^{-\delta_{system} p} \tag{5}$$

Then, $Im(S(j\omega)) = 0$ has to be solved which leads to solve the 4th-order Equation (6) [24,25]:

$$a\omega^4 + b\omega^3 + c\omega^2 + d\omega + e = 0$$

$$with \begin{cases} a = -\tau_1\tau_3 \tan(\vartheta) \\ b = \tau_1 + \tau_3 + 2\tau_1\tau_3\xi\omega_o \\ c = \left(1 + 2(\tau_1+\tau_3)\xi\omega_o + \tau_1\tau_3\omega_o^2\right)\tan(\vartheta) \\ d = -\left(2\xi\omega_o + (\tau_1+\tau_3)\omega_o^2\right) \\ e = -\omega_o^2 \tan(\vartheta) \end{cases} \tag{6}$$

The resulting complex expression permits to plot curves similar to those depicted in Figures 6 and 7.

3.4. Evaluation of Model Quality

To extract the maximum oscillation frequency, thereafter the maximum switching frequency of power devices, from the model developed in this paper, the digital time delays within the simulations have to be identified and then quantified. The expression of those digital time delays is expressed as shown by Equation (7):

$$\delta_d = \max\{\delta_{ADC}; \delta_{sw,F2}\} + \delta_{F2,z} \tag{7}$$

With δ_{ADC} the time delay due to the ADC converter, $\delta_{sw,F2}$ the time delay resulting from the filter sampling and $\delta_{F2,z}$ the time delay associated to the z-transform method used for the digital filter design. Therefore, the total time delay can be defined according to Equation (8):

$$\delta_{system} = \delta_a + \max\{\frac{T_{sw,ADC}}{2}; \frac{T_{sw,F2}}{2}\} + \delta_{F2,z} \tag{8}$$

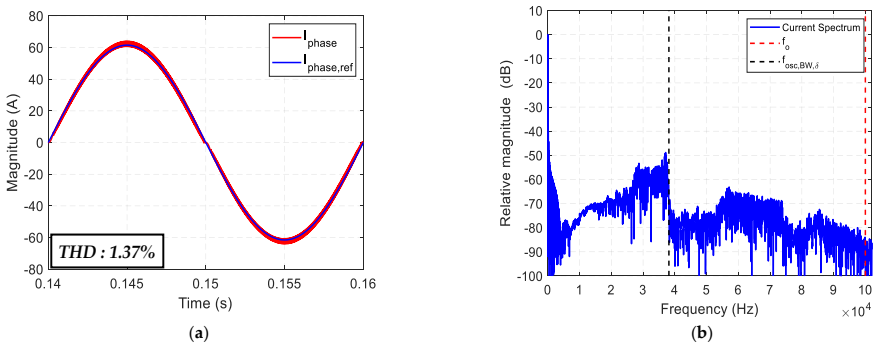
For the following simulations, the ADC converter samples measures at 5 MHz and digitizes them on 12 bits. The digital filter is also sampled at 5 MHz and the Tustin method is used to obtain its discrete transfer function. A pre-warping at f_o is applied to compensate the phase distortion observed after a filter discretization. Then, the time delay $\delta_{F2,z}$ is null. With an analog time delay of 1.9 µs and assuming that the time delays due to the resolution of the simulation and due to the rounding of the ADC block used under Matlab/Simulink are too small to be considered, then the global time delay of the system is:

$$\delta_{system} = \delta_a + \max\{\frac{T_{sw,ADC}}{2}; \frac{T_{sw,F2}}{2}\} + \delta_{F2,z} = 1.9\ \mu s + \max(100\ ns; 100\ ns) + 0\ \mu s = 2\ \mu s \tag{9}$$

With the aim of evaluating the DPSSOCC performances, the evaluation of the model quality is initially carried out with a single-phase Vienna power converter. Based on the simulation parameters of Table 1, results are presented in Figure 9 for a maximum oscillation frequency $f_{osc,BW,\delta}$ of 38.128 kHz. To confirm that the digital DPSSOCC provides performances close to the ones of the analog PSSOCC, simulation results are presented in Figure 10 with the use of the PSSOCC using the same parameters.

Table 1. Simulations parameters.

Passive Components	Grid Features	$F_2(p)$ Features	Current Sensor Bandwidth	δ_{system}
$L = 730\ \mu H$ $R = 0.2\Omega$ $C = C_+ = C_- = 2200\ \mu F$ $R_{load} = 65\ \Omega$	$V_{phase,rms} = 230$ V $I_{phase,ref,rms} = 43.5$ A $f_{grid} = 50$ Hz	$f_o = 100$ kHz $\xi = 1$	$f_3 = 100$ kHz	2 µs



(**a**) (**b**)

Figure 9. (**a**) Input current controlled by digital DPSSOCC and (**b**) its related current spectrum.

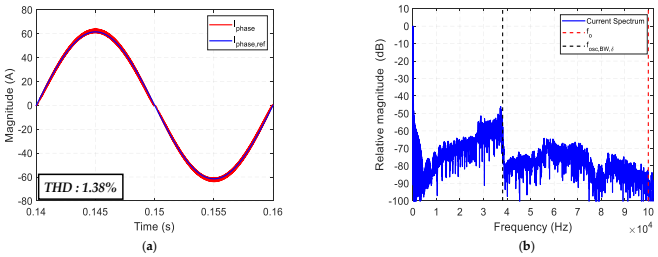


Figure 10. (**a**) Input current controlled by analog PSSOCC and (**b**) its related current spectrum.

The current controlled by DSPSSOCC follows its reference with a very low THD of 1.37%. The spectrum analysis confirms this value with a strong reduction of low frequencies harmonics. Moreover the upper edge of the first intermodulation lobe is steep and allows a good interpretation of the maximum switching frequency value.

Considering both figures, a high similarity is observed. It indicates the good performances retention of the discretized PSSOCC. The gap between the natural frequency of the second order filter and the maximum oscillation frequency from the theoretical approach increases with increasing f_o value. Then the model of the DPSSOCC developed in this work is validated since it allows a perfect determination of the maximum oscillation frequency with excellent performance in regulation.

3.5. Controller Operating Limits

Simulation results from the preceding sub-section are relevant. However, the parameters used for the study assume that the experimentally implemented components operate at high sampling rates. As a result, the discretized signals waveforms are very close to analog signals ones, making the operating conditions conducive to efficient regulation. The industrial cost is often an important criterion in the design of a product, thus the use of high cost high performance ADC for instance, can be a hindrance to the use of the DPSSOCC. In that respect, DPSSOCC parameters are modified in this section with the aim of reducing the industrial cost. The evaluation of the low-cost DPSSOCC performances also permits to define the operating limits of this current controller.

3.5.1. Second Order Filter Sampling Frequency Variations

Firstly, the frequency $f_{sw,ADC}$ is still set to 5 MHz but the frequency $f_{sw,F2}$ is varied between 500 kHz and 2 MHz. Simulation results are presented in Figure 11.

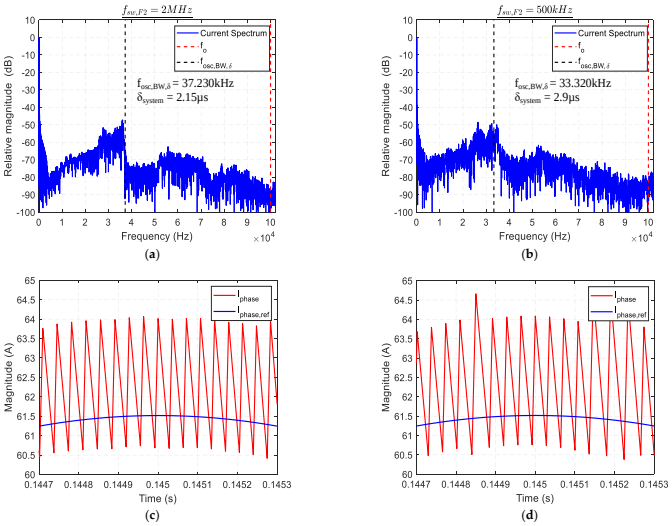


Figure 11. (**a**) Input current controlled by DPSSOCC and (**c**) its related current spectrum for a frequency $f_{sw,F2}$ of 2 MHz. (**b**) Input current controlled by DPSSOCC and (**d**) its related current spectrum for a frequency $f_{sw,F2}$ of 500 kHz.

When the filter sampling frequency is sufficiently high in relation to the value of the maximum switching frequency, the current ripple is perfectly reproduced and the theoretical model precisely defines the value of the maximum oscillation frequency of the system. On the other hand, reduction of the filter sampling frequency alters the regularity of the current ripple. This deterioration is found at the spectral level with the sagging of the edge defining the maximum switching frequency. Indeed, the theoretical model remains valid as long as the current ripple is regular. Otherwise, the analytically determined value of $f_{osc,BW,\delta}$ is inaccurate as shown by Figure 11.

3.5.2. Analog to Digital Converter Sampling Frequency Variations

Secondly, the frequency $f_{sw,F2}$ is set to 5 MHz and the frequency $f_{sw,ADC}$ is varied between 500 kHz and 2 MHz. Simulation results are presented in Figure 12.

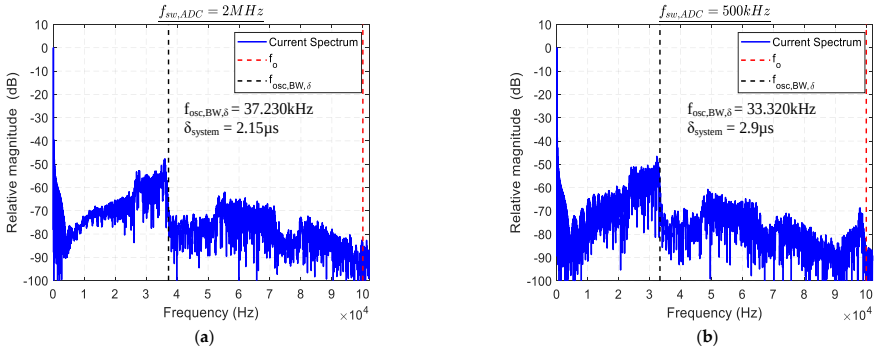


Figure 12. Spectra of input current controlled by DPSSOCC with a frequency $f_{sw,ADC}$ of (**a**) 2 MHz and (**b**) 500 kHz.

The maximum switching frequency logically decreases, but the well-defined edge in the spectrum reflects the good quality of the current ripple. There are no simulation results of the current ripple in those cases because there are very similar to Figure 11c. Moreover, these results confirm the fact that the performances of the DPSSOCC are greatly influenced by the use of a high sampling rate for the digital filter. The sampling frequency of the ADC also influences the performances of the DPSSOCC but to a lesser extent with a reduced impact on current ripple quality.

3.5.3. Multiplexing Effect

In order to reduce the cost of the digital card, seat of the DPSSOCC implementation, the use of a multiplexer allows the acquisition of several signals at lower cost since it reduces the number of ADC converters needed. In the context of this study, the multiplexing can potentially pose a problem because it implies a loss of information during data acquisition. By setting n the number of inputs of the multiplexer and $T_{sw,mux}$ the acquisition time per input, it is assumed that during a time $(n-1)T_{sw,mux}$, the measurement of the current seen by the FPGA is fixed. This can result in a time delay δ_{mux} estimated by:

$$\delta_{mux} = \frac{(n-1)^2}{2n} T_{sw,mux} \quad if\ n > 1,\ else\ \delta_{mux} = 0,\ n \in \mathbb{N}^* \tag{10}$$

The combination of multiplexer and ADC time delays is then expressed as:

$$\delta_{mux} + \delta_{ADC} = \frac{(n-1)^2}{2n} T_{sw,mux} + \frac{T_{sw,ADC}}{2n},\ \ n \in \mathbb{N}^* \tag{11}$$

At the system level, the global time delay $\delta_{system,mux}$ is then defined by:

$$\delta_{system,mux} = \delta_a + \max\{(\delta_{mux} + \delta_{ADC});\ \delta_{sw,F2}\} + \delta_{F2,z} \tag{12}$$

The simulation results are given in Figure 13 for a multiplexer performing the acquisitions at 1 MHz, i.e. 1 µs per input, with an input number n varying between 2 and 8.

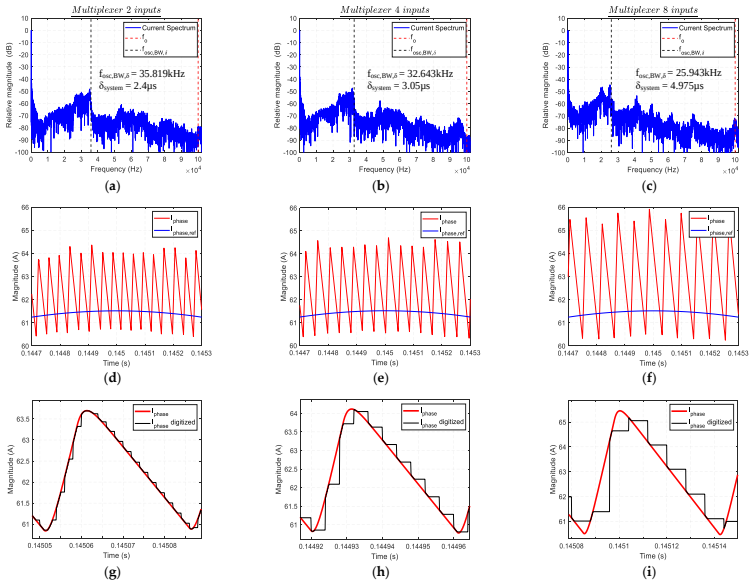


Figure 13. Effect of multiplexing of (**a**,**d**,**g**) 2 inputs, (**b**,**e**,**h**) 4 inputs and (**c**,**f**,**j**) 8 inputs on the current controlled by DPSSOCC. ($f_{sw,ADC} = 5$ MHz, $f_{sw,F2} = 1$ MHz, $f_o = 100$ kHz and $\xi = 1$).

The spectra presented validate the accuracy of Equation (12). The use of a multiplexer does not affect the quality of the current as long as the switching frequency of the multiplexer is sufficiently high and its number of inputs is relatively low. In other words, the model is inaccurate if the loss of information due to multiplexing is too important.

3.5.4. Miscellaneous Issues

Among the multiple causes of time delays not discussed so far, two can be highlighted. On the one hand, the z-transform method used affects the phase rotation provided by the digital filter in comparison with the behavior of an analog filter. Indeed, the choice of the z-transform method used for the passage from the time domain to the frequency domain generates more or less large errors. Table 2 illustrates the additional time delay for a digital second order low-pass filter sampled at 1 MHz for the mains z–transforms.

Table 2. Mains z-transforms and resulting time delays after 2nd order low-pass filter discretization.

Z-Transform Method	Equation	Estimation of $\delta_{F2,z}$
Euler's Backward Method	$p = \frac{1-z^{-1}}{T_{sw,F2}}$	-125 ns
Tustin Method	$p = \frac{2}{T_{sw,F2}} \frac{1-z^{-1}}{1+z^{-1}}$	$\frac{1}{4f_o}\left(\frac{1-k}{k}\right) = 85$ ns
Tustin method with pre-warping at f_o	$p = \frac{\omega_o}{\tan\left(\frac{\omega_o T_{sw,F2}}{2}\right)} \frac{1-z^{-1}}{1+z^{-1}}$	None

On the other hand, a part of the total digital time delay comes from the code structure of the digital control device used for the DPSSOCC implementation. The strong parallelism offered by an FPGA minimizes this issue. However, in case a DSP or a µcontroller would be used, this issue should be studied carefully.

4. DPSSOCC Performances Evaluation in Three-Phase Arc Welding Operating Modes

To confirm the ability of the DPSSOCC to control the input currents of a three-phase welding power source, its performances are evaluated in simulation within the global

system aforementioned in Figure 1. Simulations are done for the operating modes encountered in a welding process MIG/MAG. This welding process is characterized by an electric arc defined by a current I_o and a voltage V_o. Equation (13) gives the relationship between these two physical quantities:

$$V_o = 0.05I_o + 14 \quad (13)$$

Three types of arc welding operating mode are studied. Firstly, the continuous mode where the controlled output current is constant and which is the most common mode. Secondly, still with a constant output current but when abrupt load variations are observed. These load non-linearities occur when there is a contact between the torch and the metal to weld, creating a short-circuit, and when the trigger of the torch is activated without the presence of an electric arc, which can be assimilated to a no-load operating mode. Finally, the DPSSOCC behavior is observed in pulsed current operating mode. This last mode is used to weld thin pieces of metal and to facilitate rising welds.

4.1. Simulations Parameters

Simulations are done for an output current of 400 A. Then the arc voltage is 34 V according to Equation (13). The DC voltage bus is set to 850 V for a grid voltage of 400 V between phases. Grid coils are 730 µH, the capacitors of the DC bus are 1880 µC. The digital filter is sampled at 1 MHz and the F_2's natural frequency is set to 100 kHz with a unitary damping factor.

To get closer to the configuration of the previous part, the analog time delay is set to 1.9 µs. A multiplexer is used to the measurements for the grid currents. It switches at 500 kHz adding a digital time delay of 1.333 µs. The ADC samples the measurements at 50 MHz adding 33.33 ns since it is associated to the multiplexer. Moreover it is assumed that a time delay of 100 ns comes with the z-transform method used since the pre-warping is realized at the natural frequency of the second order low-pass filter and not at the maximum oscillation frequency. Then with a global time delay of 3.4 µs and according to the model of the DPSSOCC developed in this paper, a maximum oscillation frequency of 31.170 kHz is expected.

4.2. Continuous Mode

Simulation results in the continuous mode are presented in Figure 14. The ability of the DPSSOCC to control the input currents of the welding power source is verified with a THD of 2.14%. Moreover, the maximum oscillation frequency from the theoretical approach matches with the maximum switching frequency obtained in simulation.

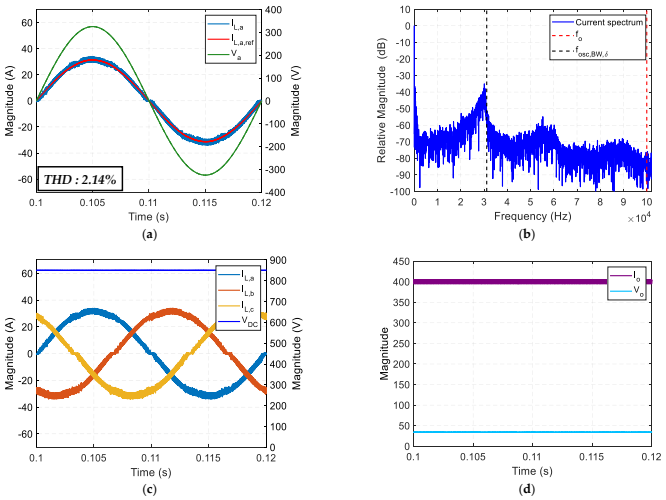


Figure 14. Waveforms of the global energy conversion chain: (**a**) grid voltage, grid current controlled by DPSSOCC and its reference, (**b**) current spectrum of the phase a, (**c**) input currents and DC voltage bus and (**d**) arc current and voltage.

4.3. Abrupt Load Changes

4.3.1. Short-Circuit Appearance

Figure 15 exposes system behavior for a transient from short-circuit to on load at $t = 0.16$ s and for a transient from on load to short-circuit at $t = 0.24$ s.

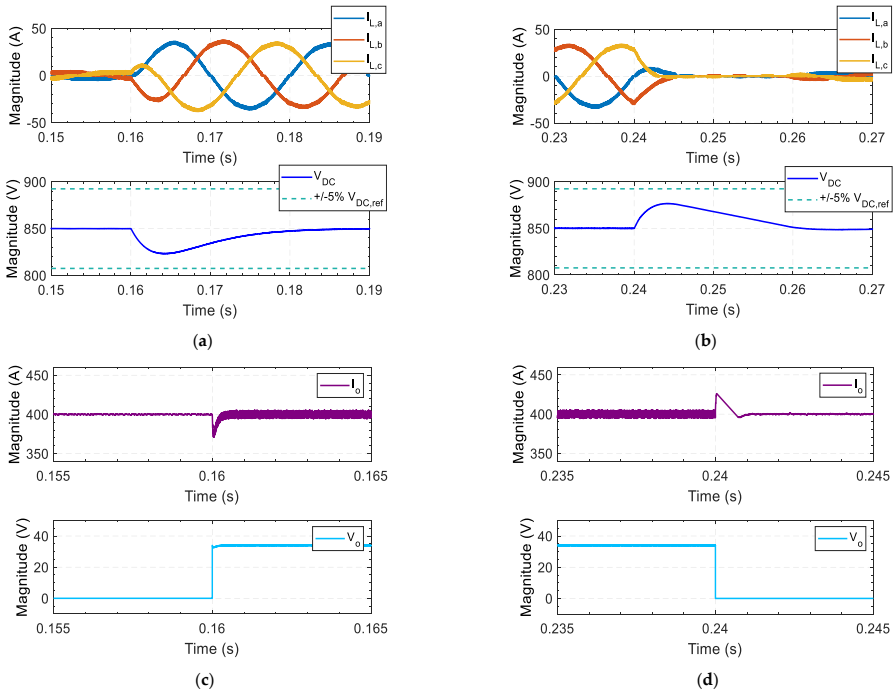


Figure 15. Grid current, DC voltage bus and output physical quantities waveforms during (**a**,**c**) transient from short-circuit to on load and during (**b**,**d**) transient from on load to short-circuit.

The appearance of short-circuits of significant duration impacts the physical output of the system but also currents and voltages within the global energy conversion chain. In fact, the effect of short circuits on the DC voltage bus is observed with voltage peaks at 877 V, i.e. an increase of 3.18% of the reference value, and voltage dips at 823 V, i.e. a decrease of 3.18% of the reference value. These voltage fluctuations are considered acceptable when they do not exceed 5% of the reference value, which is the case in this configuration. Finally, the arcing short circuit requires a reduction in the output power demand, which logically has repercussions on the input consumption.

4.3.2. No-Load Operation Mode

Figure 16 presents system behavior in case of transient from no-load to on load at $t = 0.16$ s and of a transient from on load to no load at $t = 0.24$ s.

In the absence of electric arc, thus with a null output current, the return of the voltage bus to its reference value is slower after a voltage peak since the circuit dynamics for draining the energy stored in the DC bus capacitors is slower. As with short-circuits, the 878V (+3.29%) voltage peaks and 822 V (-3.29%) voltage dips are less than 5% of the DC bus reference value. The regulation can therefore be considered satisfactory.

4.4. Pulsed Current Mode

Since the welding of certain metals requires reduced heat release, alternating between high and low current is recommended. Synergies are then set up to adapt the pulsed control. Among the multitude of adjustable parameters, the amplitude differential of the high pulsed current compared the low pulsed current, and the pulse frequency can be varied. Figure 17 shows simulations results for pulses of 3 ms at 50 Hz. The welding current value alternates between 5 A and 500 A with a slope of 1 A/µs.

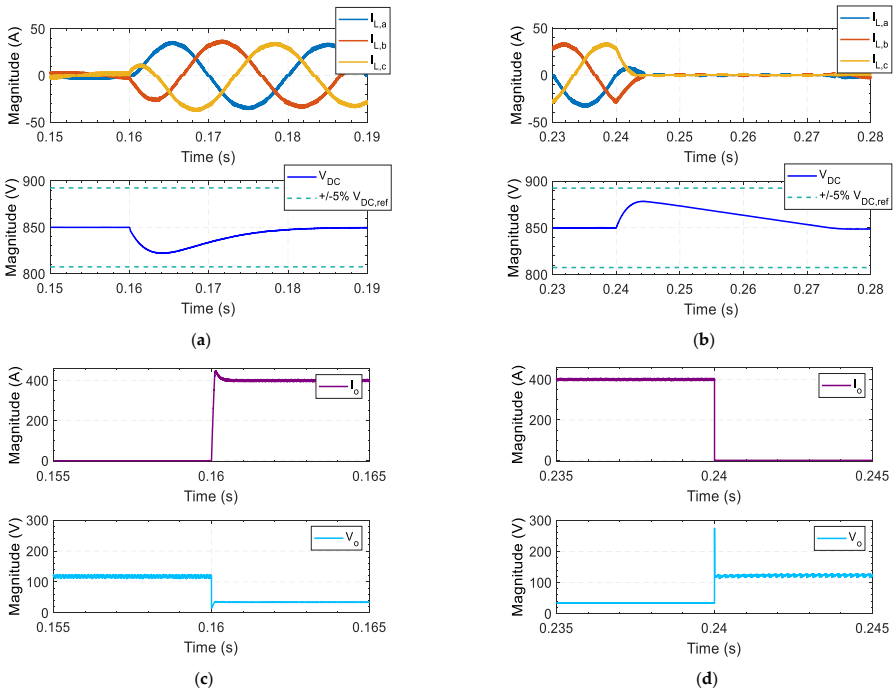


Figure 16. Grid current, DC voltage bus and output physical quantities waveforms during (**a**,**c**) transient from no-load to on load and during (**b**,**d**) transient from on load to no-load.

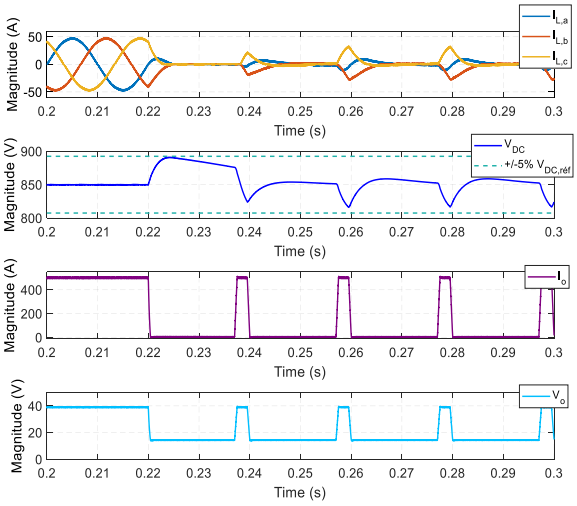


Figure 17. Waveforms in pulsed current operation mode.

The high demands placed on the system by the pulsed operating regime are clearly visible, especially on the DC voltage bus. In fact, following the ignition, a voltage peak at 891 V (+4.82%) occurs. As the following sequence of pulses has a higher dynamic range than the voltage loop regulation, the voltage bus oscillates around its reference value, which results in a sequence of transient sequences without ever reaching the desired value on a permanent basis.

Qualitative welding in pulsed operation is then based on two factors. On the one hand, the limitation of voltage peaks and dips of the DC bus stabilizes the voltage source supplying the inverter of the DC/DC converter, which results in superior welding comfort. On the other hand, when switching from high to low current, the regulation of the output current must be such that the output current never cancels. Otherwise, an arc rupture is observed forcing the welder to re-ignite the arc, which degrades the quality of the weld.

Those simulation results established the impact of the electric arc non-linearities on the grid current consumed when a PFC control is used. Especially, it demonstrates the

ability of the three-phase DPSSOCC regulator/modulator to perform its task even under the most constraining operating regimes.

5. Experimental Results and Discussion

The experimental validation of the DPSSOCC is performed on three-phase Vienna converter associated to a PFC control law. The DC/DC converter is assimilated to a resistive load since experimental results are in continuous mode.

5.1. Test Bench Features

The test bench used for this experimental part is composed of five electronic boards. The regulation is implemented on a Cyclone 10LP FPGA (Intel, Santa Clara, CA, USA) on the digital card. The signal processing chain of the digital card, as well as the sampling frequencies associated with the various components used, is summarized in Figure 18.

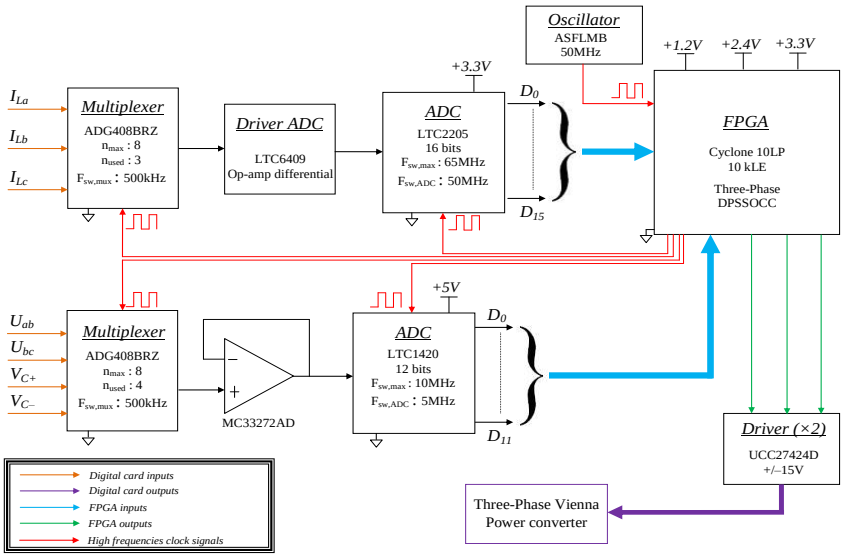


Figure 18. Synoptic of the signal processing chain of the digital card.

The three-phase Vienna converter card is designed with three VUM 25-05e units (IXYS, Milpitas, CA, USA). The current references are provided thanks to a synchronization card. The three-phase Phase Locked Loop is assured by three MC14046B (ON Semiconductor, Phoenix, AZ, USA). Absence of a neutral wire implies a measurement of the phase to phase voltages. The neutral-phase voltages are rebuilt within the FPGA. Each voltage measurement uses a LV25-P LEM sensor (LEM, Geneva, Switzerland). A closed loop Hall effect sensor permits current measurements. The sensor reference used is a CSM300B (Chieful, Nanjing, China) with a bandwidth of 100 kHz. DC bus capacitors are 1880 µF (4 × 470 µF) with a working voltage of 450V. The inductors are 730 µH. A programmable AC source 6490 is used as power supply which is limited to 3000 VA per phase. Finally, measurement and visualization equipment references are given in the Table 3.

Table 3. Measurement and visualization equipment references.

Current Probe (Oscilloscope)	Current Probe (THD Measurement)	Differential Voltage Probe	Oscilloscope
Amplifier TCPA300 Tektronix Probe TCP303 Bandwidth: 15 MHz	Harmonic Power Meter Model F25 Chauvin Arnoux Harmonic rank max: 25 THD accuracy: 5% ± 2 dg	700V_{DC}/500 $V_{AC,RMS}$ Bandwidth: 100 MHz	WaveJet Touch 334 Bandwidth: 250 MHz Sampling rate: 2 GS/s

5.2. Three-Phase Vienna FPGA-Based Control Experimental Results

Experimentations are performed with a resistive load of 50 Ω for an input voltage of 200 V at 50 Hz and a DC bus regulation at 650 V. The natural frequency of the second order low-pass filter is set to 50 kHz with a unitary damping factor. The Tustin method with pre-warping at f_o is used. The results of the tests carried out are shown in Figure 19.

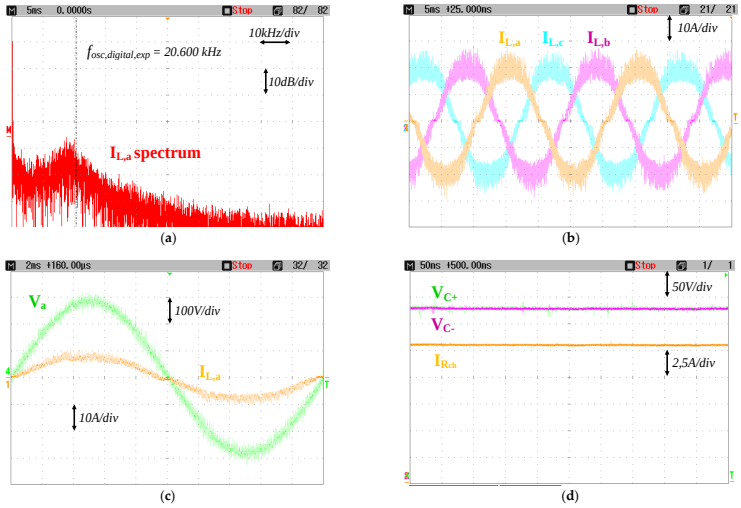


Figure 19. Experimental waveforms of the Three-Phase Vienna converter with PFC regulation including DPSSOCC control: (**a**) current spectrum, (**b**) input current, (**c**) grid voltage and current for one phase and (**d**) output current and regulated DC voltage bus.

First of all, these experimental results confirm the good performances of the DPSSOCC with three sinusoidal grid currents in line with grid voltages. The DC voltage bus is perfectly regulated at the targeted voltage of 650 V_{DC}. Moreover, Figure 19d proves the correct imbalance correction with two voltages of 325 V_{DC}. The load current is about 12.6 A_{DC} whereas the grid current is 14.95 A_{RMS}. It leads to a converter's efficiency of 91.4% for an input power of 8.970kW and an output power of 8.204 kW. In addition, focusing on the DPSSOCC performances and the Figure 19a depicting the current spectrum, a maximum oscillation frequency $f_{osc,digital,exp}$ of 20.600 kHz is measured.

To complete the study of the DPSSOCC implementation, tests with load variations are performed. Experimental results are presented in Figure 20.

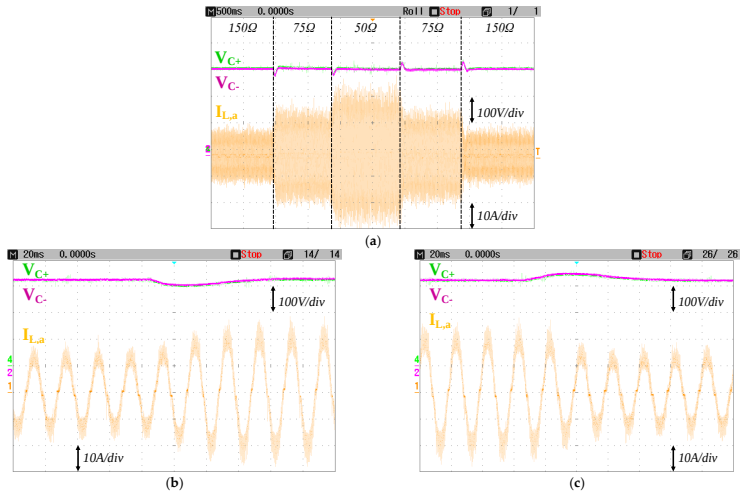


Figure 20. DPSSOCC performances with resistive load variations: (**a**) between 150 Ω and 50 Ω, (**b**) transient from 75 Ω to 50 Ω (zoom) and (**c**) transient from 50 Ω to 75 Ω (zoom).

The DPSSOCC regulation remains very efficient during load impacts. These latest results allow us to definitively validate the choice of the DPSSOCC for the control of the current at the input of a three-phase welding power source.

5.3. Accuracy and Relevance of the Model

The first step to evaluate the concordance between the maximum oscillation frequency obtained in practice and that resulting from the model developed in this work, is to define the global time delay of the system. Simulation parameters defined in the Section 4.1. match with test bench features. Then a time delay of 1.5 µs comes from the multiplexer, the ADC sampling frequency and the z-transform used.

The 16-bit ADC needs seven 50 MHz clock rising edges to convert the analog signal which is equivalent to an additional time delay of 140 ns. Moreover, with 500 ns of time delay due to the drivers and the opto-couplers, isolating the control of the power board, the time delay is then 2.140 µs. Finally, considering 150 ns of time delay during Mosfet switching and 460 ns resulting from the digital architecture of the VHDL code within the FPGA, the overall time delay of the system is 2.750 µs. The expected theoretical maximum oscillation frequency is then about 24.460 kHz. By performing a simulation with this time delay, Figure 21 results.

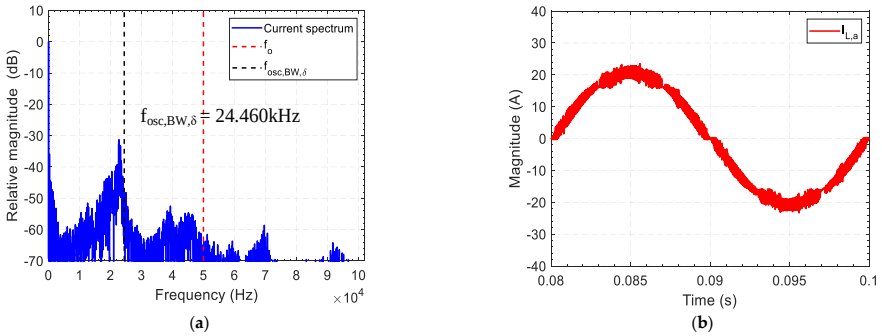


Figure 21. Simulation results under DPSSOCC control with experimental parameters: (**a**) current spectrum and (**b**) input current.

Under these simulation conditions, the error between theoretical and practical maximum oscillation frequencies is significant since it is of the order of 15.8%. Moreover, the grid current shape differs between simulation and experimentation. Even considering an error in the oscilloscope reading and/or admitting an error in the estimates of the global time delay of the system, the developed model lacks precision. The only notable difference between the test bench and its modeling is the existence of noise and parasitic elements, within the electronic boards used, which are neglected in the modeling considered. Consequently, some white noises are added on the current measurements giving results of Figure 22.

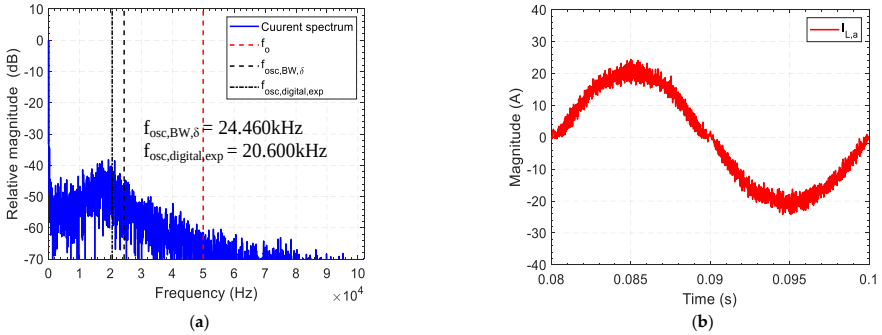


Figure 22. Simulation results under DPSSOCC control with experimental parameters and white noise: (**a**) current spectrum and (**b**) input current.

By setting the Matlab/Simulink block "Band-Limited White Noise", introducing white noise in a simulation, for a "Noise power" parameter of 2.5×10^{-7} at a frequency of 10 MHz, there is a very good match between the analytical model and the experimental results. These results highlight two facts regarding the quality of the DPSSOCC and its modeling. On the one hand, the operation of the DPSSOCC, even in a highly parasitic environment, reinforces the idea that this current regulator is extremely robust with respect to its external environment. On the other hand, these results imply an imprecision in the estimation of the maximum oscillation frequency since interferences and noises within a system are complex to quantify before having experimental results.

Eventually, in order to validate the hypothesis that the DC/DC converter can be substituted for a resistive load, simulations are performed on the global energy conversion chain by considering a power demand at output similar to the one of the experimental tests. Thus, the power of the electric arc is set to 8 kW. For a MIG welding process, this is equivalent to regulating the arc current at 284 A for an arc voltage of 28.2 V. With an overall time-delay of 2.750 µs, it leads to results of Figure 23.

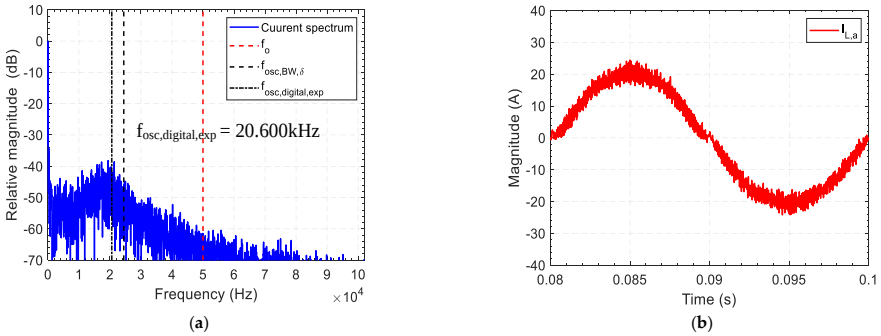


Figure 23. Simulation results under DPSSOCC control with DC/DC converter: (**a**) current spectrum and (**b**) input current.

The results with a resistive load and with the DC/DC converter are extremely similar. Therefore, the use of a resistive load to replace the power converter is sufficient to validate the regulation principle applied to the complete energy conversion chain of a three-phase welding power source.

5.4. Compliance Study

In addition to reducing current consumption and managing the DC voltage bus, one of the major challenges behind the implementation of DPSSOCC, and the associated PFC control, is to have a system that meets the standards in terms of harmonic pollution of the grid in accordance with IEC 61000-3-12. The results presented show a consumption of 15 A_{RMS} while the aforementioned standard is stated for products consuming 16 A_{RMS} and more. Due to the operating limits of the test bench, it is impossible to position the system perfectly under the test conditions of the standard in force. Nevertheless, the configuration considered is sufficiently close to the conditions of the standard to be able to perform a consistent analysis. Therefore, it is proposed with Table 4 to establish a comparison between experimental and simulated THD in order to assess the degree of belonging of the system to the standard in terms of harmonic limitations.

Table 4. IEC 61000-3-12 compliance study: Harmonic emission analysis in simulation and in practice.

	h_5	h_7	h_{11}	h_{13}	$THC/I_{rms,total}$	$PWHC/I_{rms,total}$
Standard Limits	10.7%	7.2%	3.1%	2%	13%	22%
Experimental Values	4.2%	2.3%	1.0%	1.0%	5.55%	7.71%
Simulation Values	1.92%	1.88%	0.59%	0.48%	4.17%	6.92%
Compliance	✓	✓	✓	✓	✓	✓

The Total Harmonic Current (THC) and the Partial Weighted Harmonic Current (PWHC) are indicators provided by the standard. Their expressions are given by Equations (14) and (15):

$$THC = \sqrt{\sum_{h=2}^{40} {I_{h,rms}}^2} \tag{14}$$

$$PWHC = \sqrt{\sum_{h=14}^{40} {I_{h,rms}}^2} \tag{15}$$

THC and PWHC are 1% lower in simulation compared to practical results. However, the results remain of a sufficiently low and similar order of magnitude to admit a good concordance between theory and practice. Finally, with the existing uncertainty on harmonics measurements, it is possible to affirm that the system is up to standard in terms of harmonic emissions. As the current increases, THD tends to decrease. Hence, an increase in power will confirm, with a high probability, that the system will comply with standards if the input current of the system is regulated by a three-phase DPSSOCC.

6. Conclusions

In this paper, a study was led to define and implement the most suitable digital solution for power factor correction in welding power source. Robustness of this control law being fundamental in arc welding applications, the study was focused on a very robust phase-shift self-oscillating current controller named PSSOCC. The use of a digital control being a prerequisite of this work, the excellent performances of this analog controller and the non-existence of its digital version have oriented the work towards its digitization.

To reduce and almost eliminate the important maximum switching frequency estimation error, an improvement of the former PSSOCC model was analyzed. The main conclusions about the improved PSSOCC model is that bandwidth current sensor and time delays of the system must be taken into account to well characterized a system regulated by PSSOCC. Then, thanks to this model improvement, the digital version of this current controller can be modelled. This first DPSSOCC model is built around an FPGA base considering both the analog and digital time delays of the system. The quality of the new digital model, developed in this document, was then proved in simulations by comparing the performances offered by the analog and digital models of the PSSOCC.

In order to properly characterize the DPSSOCC proposed model, key parameters of the digital controller were varied. These parameter changes have made it possible to identify the operating limits of the controller. Therefore, to ensure efficient regulation, it is necessary to use sufficiently high sampling frequencies to maintain the high-frequency information of the regulated current. As a result, the use of elements such as a multiplexer within the measurement chain can seriously deteriorate the quality of the regulated current ripple.

Afterwards, the analysis of the DPSSOCC's performances within the complete energy conversion chain of a welding power source and its ability to bring the system into compliance with the standard made it possible to validate the solution studied in this work. The ability of the DPSSOCC to control the grid current was also validated in practice on a three-phase Vienna converter.

However, the experimental part highlighted an inaccuracy of the model when the system is strongly noisy. Indeed, the presence of noise within the electronic boards implies a modification of the spectrum of the regulated current, which complicates the determination of the maximum oscillation frequency of the system with the model proposed in this paper. In spite of this imprecision, the study carried out allows, on the one hand, the validation of the very good performances of this new DPSSOCC regulator and, on the other hand, confirms the great robustness and the capacity of the DPSSOCC to control the current at the input of a three-phase welding power source.

The proposed solution still can be improved by using cheaper components. For instance, three 12-bits series ADC converters with lower sampling frequencies could be used instead of unique expensive 16-bits parallel ADC converter associated to a multiplexer. Furthermore, the results of this work will provide a solid basis for the development of a future multi-process 650 A welding power source.

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