energies

MDPI

Article

Discrete Fundamental AC Voltage Controller for Three-Phase Standalone Converters

Alejandro García-Fernández †, Jesús Doval-Gandoy *,† and Diego Pérez-Estévez †

Applied Power Electronics Technology Research Group (APET), University of Vigo, Lagoas Marcosende, 36310 Vigo, Spain; alejagarciafer@uvigo.es (A.G.-F.); dieperez@uvigo.es (D.P.-E.)

* Correspondence: jdoval@uvigo.es

† These authors contributed equally to this work.

Abstract: Voltage control of standalone converters with LC filter is usually based on proportional-resonant or proportional-integral controllers, which often require further active damping methods to achieve stability. These solutions place design constraints in the selection of the closed-loop pole locations which limit the achievable bandwidth and increase the design complexity. In contrast, in state-space based controllers, the closed-loop poles can be placed freely through state feedback, which makes them particularly suitable for high order plants and/or low sampling frequencies. Among the modern control methods, direct pole placement is a simple technique that enables the establishment of a straightforward relationship between outcome and design, as opposed to more advanced approaches. This paper presents a discrete state-space voltage controller for standalone converters with LC output filter. The proposed method combines the direct pole placement technique with a virtual disturbance observer in order to compensate the effects produced by the load and model mismatches. The design process takes into account both the filter parameters and the sampling frequency, rendering the performance of the obtained controller independent of both. The result is a streamlined design procedure that leads to consistent outcomes for a wide range of plant parameter variations, requiring only one input: the desired closed-loop bandwidth.

Keywords: LC filter; pole placement; standalone converter; state-space voltage control

Citation: García-Fernández, A.; Doval-Gandoy, J.; Pérez-Estévez, D. Discrete Fundamental AC Voltage Controller for Three-Phase Standalone Converters. *Energies* **2021**, *14*, 650. https://doi.org/10.3390/en14030650

Academic Editor: Federico Barrero and Jorge Rodas

Received: 19 December 2020

Accepted: 21 January 2021

Published: 27 January 2021

1. Introduction

Voltage source inverters (VSI) have commonly been used for uninterruptible power supplies (UPS), distributed generation systems (DG), dynamic voltage restorers (DVR), ground power units (GPU) for airplanes and other high-performance AC voltage sources. In order to meet the requirements in terms of voltage waveform quality, an LC filter is commonly used at the output of the inverter (sometimes LCL filters are used where the second inductor operates as part of the feeder impedance [1,2]) which brings up the issue of damping the LC resonance otherwise system stability and/or waveform quality might be compromised. Passive damping, being the easiest way, produces high energy losses [3] thus a more suitable method to dampen the LC resonance is by means of a properly designed control scheme.

Plenty of voltage controllers belonging to both the classic (transfer function) and modern (state-space) control theory have been proposed in the past. Classic controllers can be, in general, categorized into two groups regarding the control structure, namely the dual-loop voltage-current control [4–8] and the single-loop voltage control [9–12].

Dual-loop control strategies [4] have been widely employed in DG and UPS applications due to their good performance and inherent robustness. They involve the usage of an outer voltage loop to ensure steady-state tracking performance and an inner current loop to provide fast dynamic compensation for system disturbances and improving stability. By behaving as a virtual impedance [5], the inner current loop increases the dampening of the filter resonance and the load disturbance rejection but it also bounds

the overall bandwidth [6]. Moreover, it has been shown that the aforementioned approach only presents good results when the intrinsic delay regarding digital implementation has a negligible phase lag effect [6] or is specifically taken into account in the design [7]. Still, continuous-time domain design and subsequent discretization for digital implementation can introduce discrepancies depending on the discretization method used [13], therefore direct design in the discrete-time domain is advisable [8].

Single-loop control methods are the preferred choice in low pulse ratio applications such as GPUs due to their improved dynamic performance [9]. However, the lack of degrees of freedom implies a tradeoff between performance and stability difficult to overcome. In order to mitigate this issue, some strategies have already been published. An active damping scheme is presented in [12], but it involves an iterative complex design procedure based on root locus and Bode plots to obtain the controller gains. In [11], a signal-shaping based control method to improve the dampening of the filter resonance is proposed but its sensitivity to parameter variation and sampling frequency limits its application. The pole placement technique is employed in [10] but with limited performance because only the output voltage is measured and no mechanism is included to estimate the rest of the plant information.

State-space control is particularly attractive in the case of LC filters because it enables the setting of the resonant dynamics (i.e., resonance damping) directly through state feedback. As a result of this, similar performance as in dual-loop controllers can be achieved but without the bandwidth constraints of cascade control [14]. In addition, by adopting a direct discrete-time design, it is possible to model the sample-and-hold and time lag effects in an accurate manner [15], further improving the achievable bandwidth and overall robustness.

The most popular methods among the state-space linear controllers are linear quadratic control (LQ), robust control (H_∞) and deadbeat control. Solutions based on optimal control theory like LQ [16,17] rely on the optimization of a performance index but the selection of the weighting matrices is not clear. H_∞ based controllers [18–20] allow the designer to stablish a set of predefined objectives but the design methodology is highly complex and the outcome is not guaranteed thus, the viability of the controller has to be checked by trial an error. Deadbeat controllers [21,22] achieve the fastest dynamic response at the cost of a large control effort which leads to a high sensitivity to model mismatches difficult to address.

As opposed to the previous techniques, the direct pole placement method [23,24] is interesting because it enables the specification of performance goals in terms of the closed-loop pole locations therefore, a direct relationship between outcome and design is established. However, to the best of the authors' knowledge, very few works has been published taking advantage of this technique. In [24], the controller is designed in the continuous-time domain without taking into account the time delays nor the effects of discretization, therefore, its performance is diminished since it relies on multiple pole-zero cancellations. The controller presented in [23] is developed in the discrete-time domain but it relies on the minimization of the output impedance at the fundamental frequency to increase the overall robustness. This strategy requires the usage of bandpass filters to avoid differentiation, therefore, a tradeoff between noise amplification and the derivative range has to be established. In [25], a controller combining a pole-placement designed compensator and a Kalman filter is presented. The controller offers good performance but the key parameters which define the behavior of the observer have to be estimated, therefore, the relationship between outcome and design is not straightforward.

In this paper, a design methodology for a discrete state-space voltage controller for VSIs with LC output filter is presented. The proposal employs a compensator to establish the overall performance and an observer to estimate the unmeasured state (only the output voltage is sensed) and to eliminate the steady-state errors. The proposed controller is developed in the stationary reference frame ($\alpha\beta$) using the pole placement technique and designed directly in the discrete-time domain for maximum accuracy and improved ro-

bustness. As opposed to classical transfer function based designs, the closed-loop poles are placed in suitable locations regardless of the LC filter resonance and sampling frequencies and without requiring further damping nor decoupling terms. Placing the poles in specified locations establishes a direct relationship between performance and design, leading to fast and predictable transient responses with low control effort and no overshoot. Moreover, integration with external control loops (such as droop control for instance) is facilitated since the separation of their respective dynamics—thus avoiding undesired interactions is easier. The net result is a streamlined design procedure that leads to consistent outcomes for a wide range of plant parameter variations and which it only requires one input from the designer: the desired closed-loop bandwidth.

The rest of the paper is organized as follows: In Section 2, the models for the plant and load disturbance are obtained. Section 3 presents the design methodology for the proposed controller. Section 4 assesses the robustness of the proposal to different loads. In Section 5, the proposed controller is validated through experimental tests and Section 6 ends this work with the conclusions.

2. Plant and Disturbance Models

In this section, the model of the system dynamics—including disturbances—for the voltage controller shown in Figure 1 is obtained. L_f and C_f are the reactive elements of the filter whereas R_L represents the inductor parasitic resistance; i_L is the inductor current, i_C the capacitor current and i_o the load current; v_C is the capacitor voltage and u_d is the VSI output voltage. The plant models for both the compensator and the observer are obtained through a multi-stage process in which each step adds features to the model obtained in the previous stage.

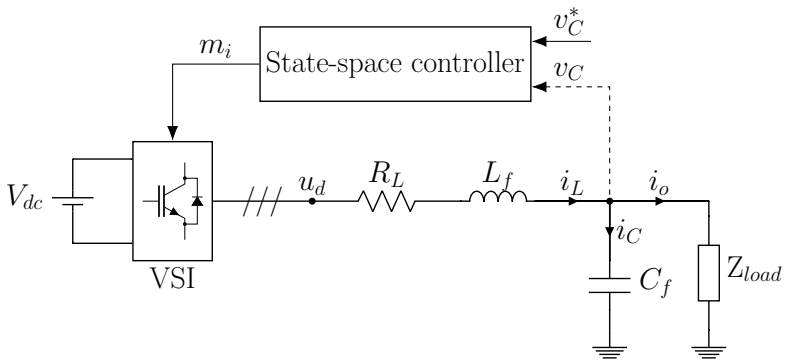


Figure 1. Standalone loaded VSI with LC output filter and voltage controller.

2.1. Plant Model for the Compensator

The process begins with the formulation of a continuous-time description of the system dynamics in the stationary reference frame. This model, already expressed in state-space notation, relates the LC filter output voltage $v_C(t)$ to the VSI output voltage $u_d(t)$:

$$\begin{aligned} \frac{d}{dt}\begin{bmatrix} v_C(t) \\ i_L(t) \end{bmatrix} &= \underbrace{\begin{bmatrix} 0 & \frac{1}{C_f} \\ -\frac{1}{Lf} & -\frac{R_L}{L_f} \end{bmatrix}}_{\text{A}} \begin{bmatrix} v_C(t) \\ i_L(t) \end{bmatrix} + \underbrace{\begin{bmatrix} 0 & -\frac{1}{C_f} \\ \frac{1}{L_f} & 0 \end{bmatrix}}_{\text{B}} \begin{bmatrix} u_d(t) \\ i_o(t) \end{bmatrix} \\ v_C(t) &= \underbrace{\begin{bmatrix} 1 & 0 \end{bmatrix}}_{\text{C}} \begin{bmatrix} v_C(t) \\ i_L(t) \end{bmatrix} \end{aligned} \tag{1}$$

The continuous-time model of the plant for the compensator is described by (2). The load current i_o is a disturbance and, consequently, non-controllable therefore its contribution is eliminated from the previous model (1) (the effect of the load current will be handled by the observer). In addition, the equivalent series resistance (ESR) of the filter capacitor

(C_f) is disregarded, since its effect appears far above the frequencies of interest [26] and its contribution to the overall dynamics is negligible.

$$\begin{aligned} \frac{d}{dt}\begin{bmatrix} v_C(t) \\ i_L(t) \end{bmatrix} &= \underbrace{\begin{bmatrix} 0 & \frac{1}{C_f} \\ -\frac{1}{Lf} & -\frac{R_L}{L_f} \end{bmatrix}}_{\mathrm{A}} \underbrace{\begin{bmatrix} v_C(t) \\ i_L(t) \end{bmatrix}}_{x_1(t)} + \underbrace{\begin{bmatrix} 0 \\ \frac{1}{L_f} \end{bmatrix}}_{\mathrm{B}} u_d(t) \\ v_C(t) &= \underbrace{\begin{bmatrix} 1 & 0 \end{bmatrix}}_{\mathrm{C}} \begin{bmatrix} v_C(t) \\ i_L(t) \end{bmatrix} \end{aligned} \tag{2}$$

The discrete representation is obtained by means of the zero-order-hold equivalent (ZOH) [27] which allows for the half sample delay introduced by the pulse width modulator (PWM) [28] to be included.

$$\begin{aligned} x_1(k+1) &= \mathrm{F}_1 x_1(k) + \mathrm{G}_1 u_d(k) \\ v_C(k) &= \mathrm{H}_1 x_1(k) \end{aligned} \tag{3}$$

One sample delay is then added to the control output (u) to account for the computational delay as follows [27]:

$$u_d(k+1) = u(k) \tag{4}$$

The discrete model of the control plant is obtained by joining expressions (3) and (4):

$$\begin{aligned} \underbrace{\begin{bmatrix} x_1(k+1) \\ u_d(k+1) \end{bmatrix}}_{x_2(k+1)} &= \underbrace{\begin{bmatrix} \mathrm{F}_1 & \mathrm{G}_1 \\ 0 & 0 \end{bmatrix}}_{\mathrm{F}_2} \underbrace{\begin{bmatrix} x_1(k) \\ u_d(k) \end{bmatrix}}_{x_2(k)} + \underbrace{\begin{bmatrix} 0 \\ 1 \end{bmatrix}}_{\mathrm{G}_2} u(k) \\ v_C(k) &= \underbrace{\begin{bmatrix} \mathrm{H}_1 & 0 \end{bmatrix}}_{\mathrm{H}_2} \underbrace{\begin{bmatrix} x_1(k) \\ u_d(k) \end{bmatrix}}_{x_2(k)} \end{aligned} \tag{5}$$

The final plant model (5) relates the output voltage $v_C(k)$ to the control output $u(k)$.

2.2. Plant and Disturbance Model for the Observer

In order to eliminate the steady state error produced by the load current and plant modeling mismatches, the proposed controller implements the disturbance estimation technique [27] through a resonant action in the observer. The resonant action is accomplished by means of a pair of conjugated poles at the fundamental frequency ω_1, as to be able to compensate for both the positive and negative sequences of the disturbance, and determines the manner in which the plant and disturbance models are developed.

The procedure to obtain the plant for the observer is detailed below. First, the load current i_o is stricken from the real plant and replaced with an input equivalent disturbance ω [27] as shown in Figure 2. Next, a description of ω is required: a sinusoidal signal at the fundamental frequency ω_1 containing both sequences is described in the continuous-time domain by

$$\frac{d^2}{dt}\omega(t) = -\omega_1^2 \omega(t) \tag{6}$$

which, after being rewritten in state-space notation, results in

$$\begin{aligned} \frac{d}{dt}r(t) &= \underbrace{\begin{bmatrix} 0 & 1 \\ -\omega_1^2 & 0 \end{bmatrix}}_{\mathrm{A_d}} r(t) \\ \omega(t) &= \underbrace{\begin{bmatrix} 1 & 0 \end{bmatrix}}_{\mathrm{C_d}} r(t) \\ r(t) &= \begin{bmatrix} r_1 & r_2 \end{bmatrix}^{\mathrm{T}} = \begin{bmatrix} \omega & d\omega/dt \end{bmatrix}^{\mathrm{T}} \end{aligned} \tag{7}$$

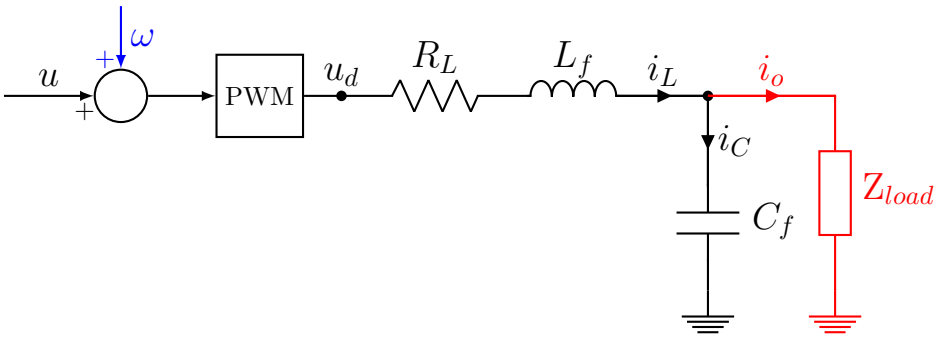


Figure 2. Relationship between the real disturbance (**red**) and the input equivalent disturbance (**blue**).

The discrete state-space disturbance model is obtained by means of the ZOH equivalent (again, to include the effect of the PWM modulator):

$$\begin{aligned} r(k+1) &= \mathrm{F_d}\, r(k) \\ \omega(k) &= \mathrm{H_d}\, r(k) \end{aligned} \tag{8}$$

In order for the observer to be able to estimate the input equivalent disturbance ω, the compensator plant model previously developed (5) is augmented with the disturbance model (8):

$$\begin{aligned} \underbrace{\begin{bmatrix} x_2(k+1) \\ r(k+1) \end{bmatrix}}_{x_3(k+1)} &= \underbrace{\begin{bmatrix} \mathrm{F_2} & \mathrm{G_2H_d} \\ 0 & \mathrm{F_d} \end{bmatrix}}_{\mathrm{F_3}} \underbrace{\begin{bmatrix} x_2(k) \\ r(k) \end{bmatrix}}_{x_3(k)} + \underbrace{\begin{bmatrix} \mathrm{G_2} \\ 0 \end{bmatrix}}_{\mathrm{G_3}} u(k) \\ v_C(k) &= \underbrace{\begin{bmatrix} \mathrm{H_2} & 0 \end{bmatrix}}_{\mathrm{H_3}} \underbrace{\begin{bmatrix} x_2(k) \\ r(k) \end{bmatrix}}_{x_3(k)} \end{aligned} \tag{9}$$

The resulting plant model allows the observer to estimate the filter states x_2 and the input equivalent disturbance ω from the system output v_C and the controller output u.

3. Controller Design

The structure of the proposed controller (Figure 3) comprises an state feedback gain K to stablish the overall performance, a feedforward gain N to correct the open-loop errors at the fundamental frequency and a Luenberger observer to estimate the unmeasured state i_L and the steady-state error characterized by the virtual signal ω defined in the previous section. The resulting control law is

$$u(k) = N v_C^*(k) - \mathrm{K} \begin{bmatrix} v_C(k) \\ \widehat{i}_L(k) \\ \widehat{u}_d(k) \end{bmatrix} - \widehat{\omega}(k) \tag{10}$$

where u is the control output, v_C^* is the reference, v_C is the measured state and the variables marked with the caret are estimates produced by the observer.

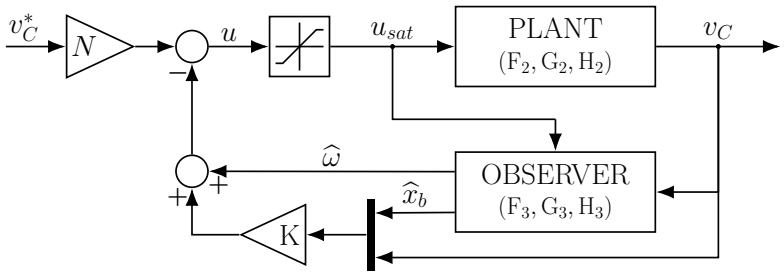


Figure 3. Block diagram of the proposed controller.

In addition, for implementation purposes, a saturator is included between the control output and the plant as to include a simple anti-windup mechanism [29]. By feeding back the saturated signal (u_{sat}) to the observer, the consistency between the estimated states and the plant states is maintained, thus the windup problem is avoided.

The key characteristic of this proposal is the usage of the observer to produce the correction effort required to compensate the steady-state error. The input equivalent disturbance (ω), embodies all the negative effects derived from model mismatches and disturbances in a single signal which is then cancelled through the addition of its estimate $(\widehat{\omega})$ to the control output. This technique enables the placement of the controller in the feedback path rather than in the more common direct path [23,24]. As a result, faster responses are achieved due to the existence of a direct path from the reference to the plant therefore, excitation of the controller modes is avoided. In addition, less control effort is required since both the plant and the controller are driven by the same signal and estimation errors are minimized as a consequence.

The design procedure for the proposed controller presented below is carried out in two steps. First, the compensator is obtained assuming all states are known. Next, the observer is designed by selecting the dynamics of the estimation error thanks to the separation principle [27].

3.1. Compensator Design

The plant model in (5) is comprised of a pair of conjugated poles at the resonance frequency ω_r and an extra pole as a result of the state augmentation with the computational delay. The main goal is to achieve a stable response with minimum control effort by preselecting the closed-loop poles positions in a suitable manner through the following control law:

$$u(k) = Nv_C^*(k) - \mathrm{K}\,x_2(k) \tag{11}$$

The closed-loop system model is obtained by substitution of the aforementioned control law in the compensator plant (5) resulting in

$$\begin{aligned} x_2(k+1) &= (\mathrm{F}_2 - \mathrm{G}_2\mathrm{K})x_2(k) + \mathrm{G}_2 N v_C^*(k) \\ v_C(k) &= \mathrm{H}_2 x_2(k) \end{aligned} \tag{12}$$

and the characteristic polynomial containing the desired closed-loop locations is

$$det(z\mathrm{I} - \mathrm{F}_2 + \mathrm{G}_2\mathrm{K}) = \prod_{i=1}^{3}(z - p_i) \tag{13}$$

The closed-loop pole locations can be picked out in a straightforward manner by selecting p_i but the task becomes easier to carry if the locations are determined first in

the continuous-time domain and mapped afterwards onto the discrete domain via the pole-zero matching method $\left(z = e^{j\omega T_s}\right)$ [27]:

$$\underbrace{\left(z - e^{-\omega_c T_s}\right)}_{\substack{\text{dominant}\\ \text{dynamics}}} \underbrace{\left(z - e^{\omega_r T_s\left(-\zeta \pm j\sqrt{1-\zeta^2}\right)}\right)}_{\substack{\text{resonant}\\ \text{dynamics}}} \tag{14}$$

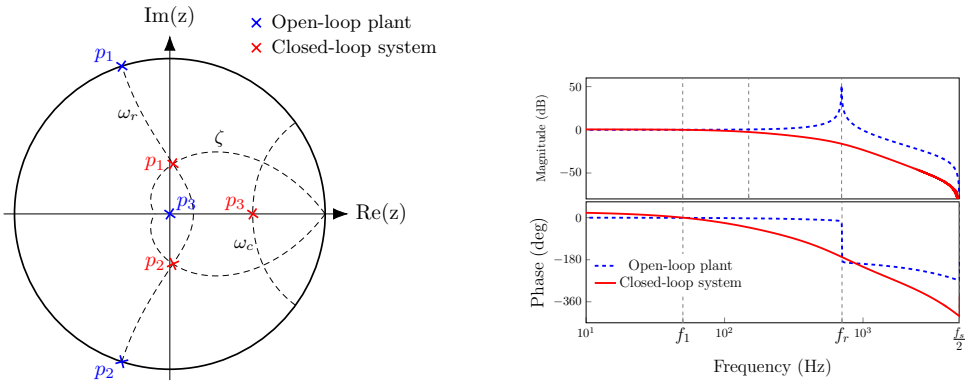
The location of the resonant poles $(p_{1,2})$ is determined in agreement with the radial projection technique [27]. This method aims to minimize the control effort by increasing the damping factor of poorly damped open-loop poles without altering their natural frequency. An additional benefit of this technique is that it allows the design procedure to be independent of the LC filter configuration since it is taken into account through its resonance frequency.

The remaining pole (p_3) determines the overall response of the closed-loop system through its bandwidth (ω_c), thus enabling the usage of the well known formulas for time and frequency domain specification for first order systems [27]. The maximum achievable bandwidth is determined by the DC-link dynamics and the LC filter frequency response. Higher bandwidths improve the transient response by giving rise to large control efforts at the cost of increasing the stress on the DC-link [30]. Beyond the resonance frequency, the required control effort to overcome the filter attenuation would be substantial, leading the power converter into the overmodulation region. Furthermore, the higher the bandwidth the closer the dominant pole is to the resonant pair and the greater the interaction between them.

The final step in the compensator design procedure is to determine the value of the input gain N. The purpose of this gain is to achieve unity gain at the fundamental frequency by adjusting the location of the transmission zero from the reference to the output.

$$N = \left(\mathrm{H_2}(\mathrm{zI} - (\mathrm{F_2} - \mathrm{G_2K}))^{-1}\mathrm{G_2}\right)^{-1}\Big|_{z=e^{j\omega_1 T_s}} \tag{15}$$

Figure 4 shows the closed-loop pole distribution and the subsequent frequency response obtained after applying the following criterion: for the damping factor of the resonant poles $(p_{1,2})$ a value of $\zeta = 0.707$ is proposed, which allows for a good tradeoff between speed of response and overshoot. As for the frequency of the dominant pole (p_3), a value ω_c of three times the fundamental frequency has been selected, which corresponds to a 2.3 ms rise time.



(**a**) (**b**)

Figure 4. Open-loop plant (blue) and closed-loop compensator (red) comparison: (**a**) Pole distribution: p_{1-2} are the resonant poles and p_3 is the result of the computational delay. (**b**) Frequency response comparison between the plant and the closed-loop compensator.

The state-feedback gain K can be obtained numerically by solving the Ackermann's formula [27] for the compensator but the usage of a software tool such as Matlab (the one used in this case) is recommended in order to avoid errors.

3.2. Observer Design

Regarding the selection of the type of discrete observer, two alternatives are available: full order observers or reduced order observers [27]. Full order observers estimate all the state variables and this is the recommended option would the control variable measurements be too noisy. Reduced order observers allow the order of the estimator to be reduced by the number of sensed outputs, thus achieving higher bandwidth and faster response. Since the ability to reject disturbances depends on the efficiency and speed of the observer to estimate them, this characteristic is of particular interest in this application.

The procedure to determine the closed-loop positions for the observer poles is similar as for the compensator. The characteristic polynomial containing the desired locations is

$$det(\mathrm{zI} - \mathrm{F_{bb}} + \mathrm{F_{ab}L}) = \prod_{i=4}^{7}(z - p_i) \tag{16}$$

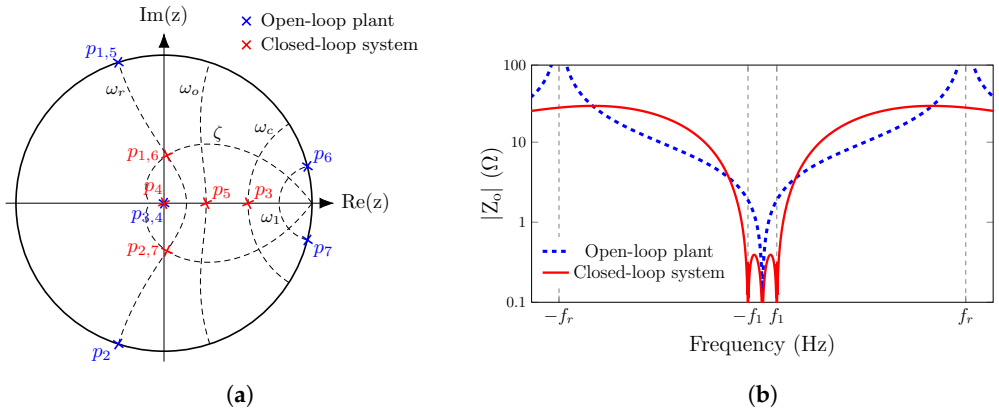
where $\mathrm{F_{bb}}$ and $\mathrm{F_{ab}}$ are submatrices of $\mathrm{F_3}$ obtained after eliminating the contribution of the measured variable (the full procedure for obtaining them can be found in [27]) and L is the state feedback gain to place the poles in the desired locations. The discrete parameterized expression is obtained in the same manner as before:

$$\underbrace{z}_{\text{delay}} \underbrace{\left(z - e^{-\omega_o T_s}\right)}_{\substack{\text{dominant} \\ \text{dynamics}}} \underbrace{\left(z - e^{\omega_r T_s\left(-\zeta \pm j\sqrt{1-\zeta^2}\right)}\right)}_{\substack{\text{resonant} \\ \text{dynamics}}} \tag{17}$$

As opposed to the compensator, there is no physical actuator to be driven here, therefore there are no restrictions on where to place the poles but beyond the Nyquist frequency of course. However, in order for the overall response of the controller to be governed by the compensator, the dominant pole of the observer (p_5) should be placed at a higher frequency than the one from the compensator (p_3). As a rule of thumb, the frequency of the dominant pole of the observer (ω_o) should be at least twice the frequency of the dominant pole of the compensator to avoid interactions [27]. As for the resonant poles $(p_{6,7})$, the same locations selected for the compensator $(p_{1,2})$ can be used here as long as they are sufficiently apart from the dominant pole. The delay pole (p_4) is already well placed, there is no need to relocate it.

Figure 5 illustrates the relationship between the open-loop and closed-loop poles for both the observer and the compensator as well as the output impedance. The closed-loop frequency response remains the same as in Figure 4b since the closed-loop system is still governed by the dominant pole of the compensator. The proposed design provides zero output impedance at both sequences of the fundamental in addition to the dampening of the resonance frequency. As a result, both the transient and steady-state responses are improved since the output voltage distortion is reduced.

As in the case of the compensator, the usage of a software tool to obtain the state feedback gain L is recommended, otherwise the gain has to be obtained by solving Ackermann's formula for the observer [27].



(**a**) (**b**)

Figure 5. Open-loop plant (blue) and closed-loop controller (red) comparison: (**a**) Pole distribution: p_{1-2} belong to the LC filter, p_3 is the result of the computational delay and p_{4-7} belong to the observer. (**b**) Output impedance comparison between the plant and the closed-loop system.

4. Stability Analysis

Both modeling mismatches and loads displace the closed-loop poles with respect to their intended locations but the latter is far more threatening hence the former is disregarded. The analysis is conducted in a similar fashion as it is done in [10]. The root locus of the closed-loop system when the system is loaded with a purely resistive and a purely inductive load is plotted in order to represent the extremes between which an R-L load can vary (mixed R-L loads will produce similar outcomes as the inductive loads but less severe due to the extra damping provided by the resistive component). The parameters of both the controller and the output filter employed in the analysis are displayed in Table 1.

Table 1. Control and hardware parameters

Parameter	Value
f_s	10 KHz
ω_1	314.15 rad/s
L_f	0.0143 p.u.
C_f	0.3739 p.u.
R_L	0.0038 p.u.
P	4 kW
V_{dc}	750 V
v_C^*	230 V RMS
ω_c	$3\,\omega_1$
ω_o	$2\,\omega_c$
K	$[-0.422 \quad -0.884 \quad -0.510]$
L	$[0.171 \;\; 1.243 \;\; 1.367 \;\; 1.240]^T \times 10^3$

Figure 6a shows the effects on the system poles for a purely resistive load. At extremely low impedances, the system becomes marginally stable due to the resonant poles of the plant (farthest pair to the right) being displaced to the low frequency region. As the impedance increases, the controller is quite capable of compensating the influence of the load. The net effect is an slight reduction on the overall bandwidth, represented by an small displacement of the dominant pole (farthest real pole to the right).

Figure 6b depicts the impact of connecting a purely inductive load to the system. The main effect of this type of loads is the increment of the resonance frequency of the combined system, which it can lead to instability. As opposed to the previous case, small load impedances push the resonant poles of the plant to higher frequencies. In addition, the system response is no longer determined by a single real pole but by a complex pair as a result of the displacement of the dominant poles of both the observer and the compensator.

The extra pole introduced by the load (farthest to the right) barely contributes to the overall dynamics since it is always partially cancelled by its own zero. As the load inductance increases, the closed-loop poles travel towards the intended locations, both increasing the stability and the speed of response.

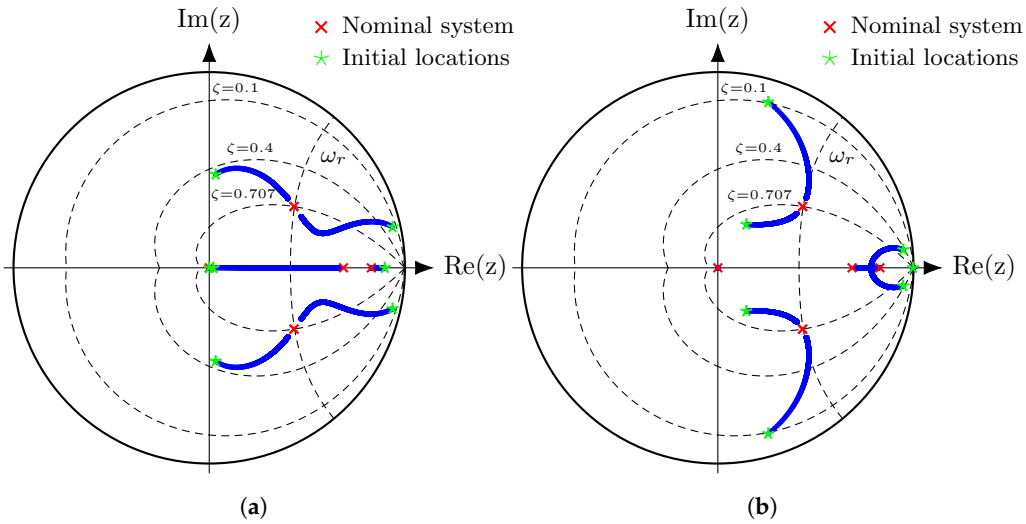


Figure 6. Root locus of the close-loop system loaded with: (**a**) Purely resistive load varying from 0.0025 to 0.75 p.u. (**b**) Purely inductive load varying between 0.4 and 8 p.u. (note: zeros have not been represented for readability reasons).

5. Experimental Results

The proposed controller is tested in a 4 kW two-level three-phase VSC working as an inverter and connected to a 10 kW DC voltage source. The hardware and control parameters are presented in Table 1 and a photograph of the experimental setup is shown in Figure 7. The LC filter is designed in accordance with the method proposed in [31]. The third test is carried out at half the sampling and switching frequencies which sets the critical frequency ($f_s/6$) [12] close to the resonance frequency of the output filter. The evaluation of the obtained results is done accordingly to the IEC 62040 standard [32], which it specifies the performance and test requirements of voltage-controlled standalone converters.

Figure 7. Testbed.

- Test 1: Balanced R-L load (50 Ω 125 mH), $f_s = 10$ KHz, $f_{sw} = 5$ KHz. Results presented in Figure 8.
- Test 2: Unbalanced R load (100 Ω, 140 Ω, 170 Ω), $f_s = 10$ KHz, $f_{sw} = 5$ KHz. Results presented in Figure 9.
- Tests 3: Nonlinear load (rectifier with R-L load 105 Ω 166 mH), $f_s = 5$ KHz, $f_{sw} = 2.5$ KHz. Results presented in Figure 10.

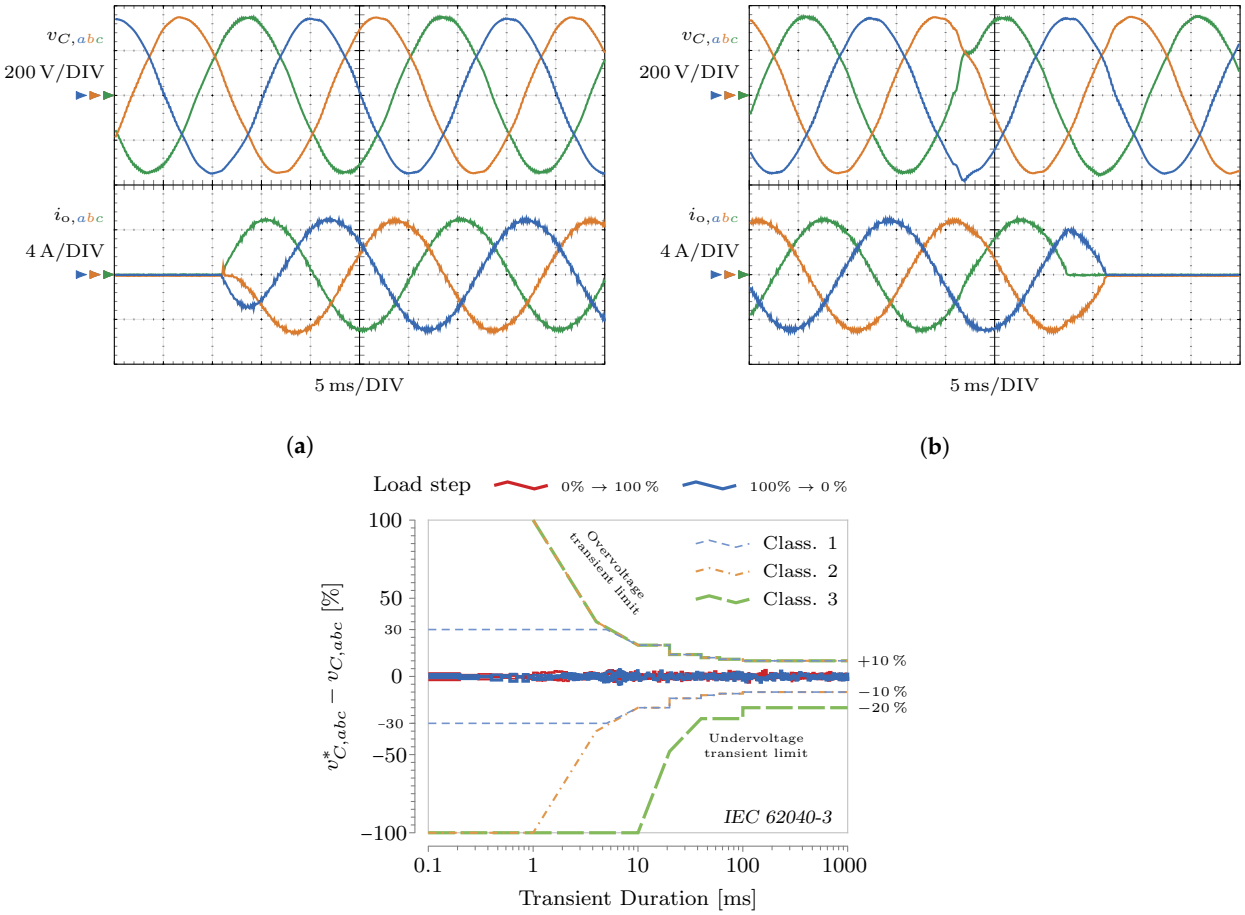


Figure 8. Experimental Test 1 (balanced R-L load): (**a**) Load connection. (**b**) Load disconnection. (**c**) Normalized tracking error and IEC limits. The beginning of the time axis corresponds to the moment of connection or disconnection of the load.

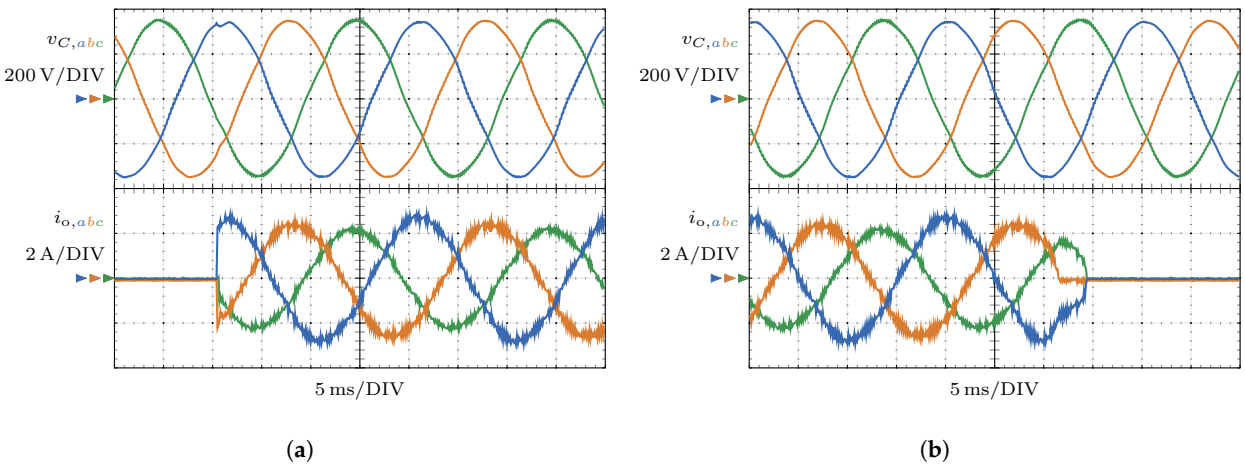
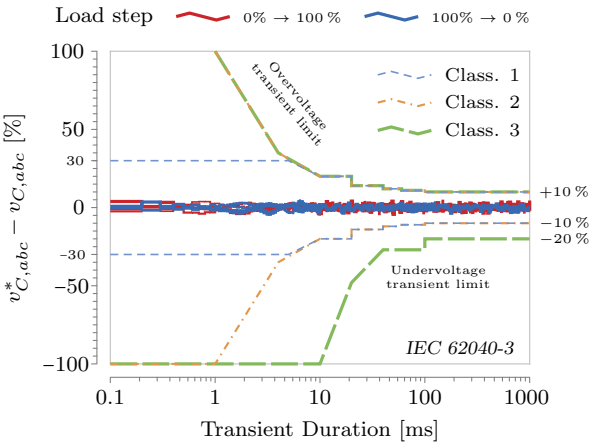


Figure 9. *Cont.*



(**c**)

Figure 9. Experimental Test 2 (unbalanced R load): (**a**) Load connection. (**b**) Load disconnection. (**c**) Normalized tracking error and IEC limits. The beginning of the time axis corresponds to the moment of connection or disconnection of the load.

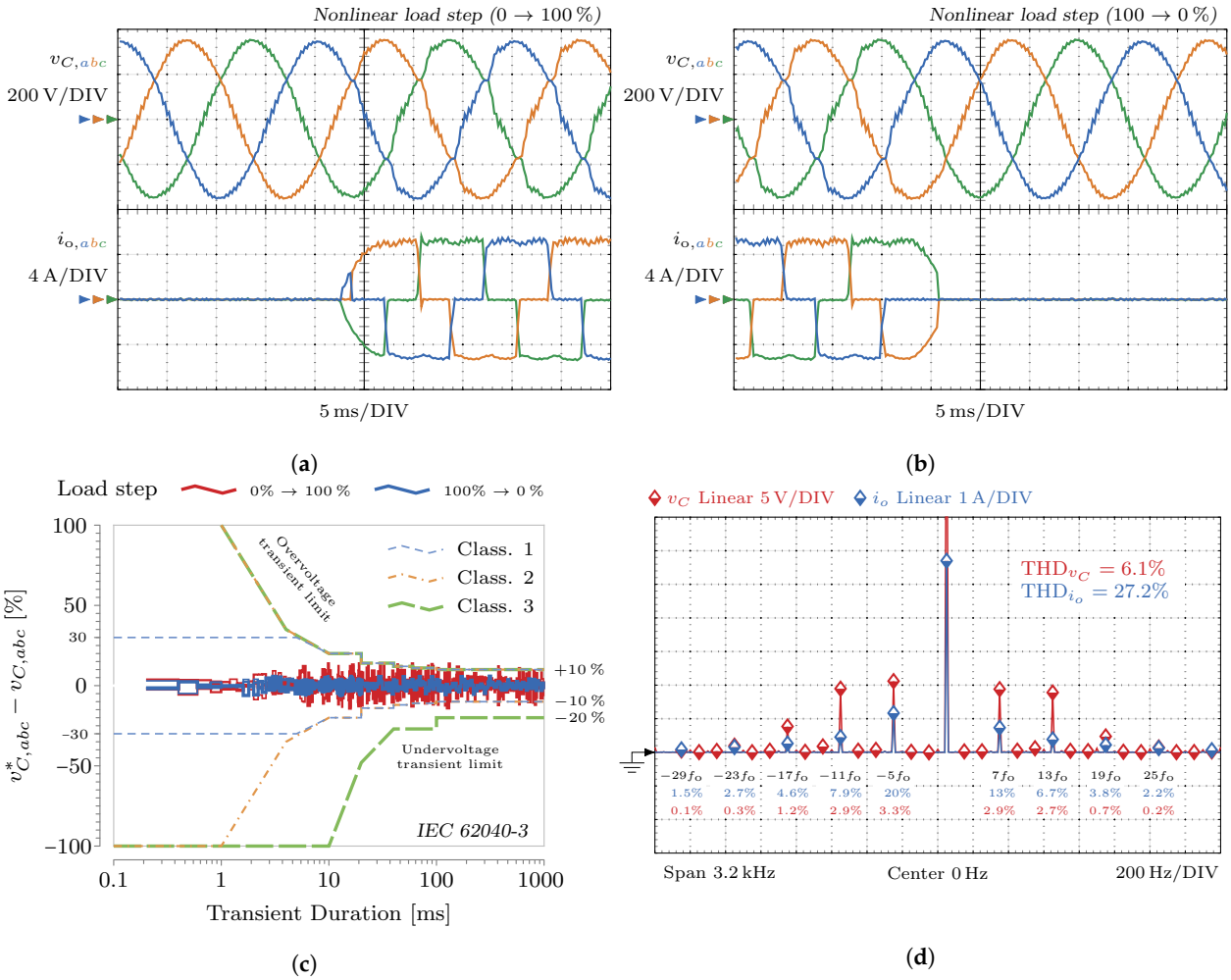


Figure 10. Experimental Test 3 (nonlinear R-L load): (**a**) Load connection (**b**) Load disconnection (**c**) Normalized tracking error and IEC limits (**d**) Harmonic spectrum.

Figure 8a,b show the output voltage and load current waveforms at the time of connection and disconnection respectively. The output voltage remains stable at both load steps indicating that the controller has been able to fully compensate them. In Figure 8c,

the normalized tracking error is depicted alongside the limits imposed by the IEC standard. It can be seen that the system reaches steady-state in around 2 ms and the normalized voltage error is around 1–2%.

Figure 9a,b show the output voltage and load current waveforms at the time of connection and disconnection respectively. As it can be seen, the converter is able to supply the load with a distorted current while maintaining the output voltage. In Figure 9c, the normalized tracking error is depicted alongside the limits imposed by the IEC standard. The lack of a discernible voltage transient means that the load step is fully compensated by the control and the absence of distortion in the voltage error indicates that the load disturbance is successfully rejected.

Figure 10a,b show the output voltage and load current waveforms at the time of connection and disconnection respectively. The load current displays the classic square shape of rectifiers, however, the output voltage waveform remains much less distorted. Figure 10c depicts the normalized tracking error and the limits defined in the IEC standard. It can be seen that the response of the converter has been slightly slowed and, despite the distortion, the tracking error is within the limits defined by the standard. Figure 10d displays the harmonic spectrum of the output voltage and the load current. Although the harmonic content of the load current is quite high, the controller is able to impose an output impedance low enough so that the total voltage distortion does not exceed the limit imposed by the IEC standard (8%). The largest amplitude harmonics are, as expected, the fifth and the seventh, which are below the limits as well.

6. Conclusions

In this paper, a voltage controller for standalone converters with LC output filter, capable of controlling both sequences of the fundamental component with zero steady-state error, has been presented. The proposed controller offers fast transient responses with low control effort regardless of the output filter parameters and sampling frequency. The design procedure, based on the direct pole placement technique, is straightforward and it only requires the designer to define the desired closed-loop bandwidth. The theoretical analysis has shown a wide stability range, therefore, the controller can be applied in situations in which the load can reach very low values of impedance. The viability of the presented controller has been validated through experimental tests and the obtained results were found in compliance with the IEC 62040 standard.

Author Contributions: A.G.-F.: conceptualization, investigation, formal analysis, methodology, validation, and writing of the original draft. J.D.-G.: conceptualization, investigation, formal analysis, methodology, validation, and supervision. D.P.-E.: conceptualization, investigation, formal analysis, methodology, validation, and supervision. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by the Spanish Ministry of Science and Innovation and by the European Commission, European Regional Development Fund under Project PID2019-105612RB-I00.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

VSI	Voltage Source Inverter
VSC	Voltage Source Converters
SRF	Synchronous Reference Frame

PI	Proportional-Integrator
PR	Proportional-Resonator
RMS	Root Mean Squared

References

1. Balaguer, I.J.; Lei, Q.; Yang, S.; Supatti, U.; Peng, F.Z. Control for Grid-Connected and Intentional Islanding Operations of Distributed Power Generation. *IEEE Trans. Ind. Electron.* **2011**, *58*, 147–157. [CrossRef]
2. Corradini, L.; Mattavelli, P.; Corradin, M.; Polo, F. Analysis of Parallel Operation of Uninterruptible Power Supplies Loaded Through Long Wiring Cables. *IEEE Trans. Power Electron.* **2010**, *25*, 1046–1054. [CrossRef]
3. Cespedes, M.; Xing, L.; Sun, J. Constant-Power Load System Stabilization by Passive Damping. *IEEE Trans. Power Electron.* **2011**, *26*, 1832–1836. [CrossRef]
4. Loh, P.C.; Newman, M.J.; Zmood, D.N.; Holmes, D.G. A comparative analysis of multiloop voltage regulation strategies for single and three-phase UPS systems. *IEEE Trans. Power Electron.* **2003**, *18*, 1176–1185.
5. He, J.; Li, Y.W. Generalized Closed-Loop Control Schemes with Embedded Virtual Impedances for Voltage Source Converters with LC or LCL Filters. *IEEE Trans. Power Electron.* **2012**, *27*, 1850–1861. [CrossRef]
6. Geng, Y.; Yun, Y.; Chen, R.; Wang, K.; Bai, H.; Wu, X. Parameters Design and Optimization for LC-Type Off-Grid Inverters with Inductor-Current Feedback Active Damping. *IEEE Trans. Power Electron.* **2018**, *33*, 703–715. [CrossRef]
7. De Bosio, F.; de Souza Ribeiro, L.A.; Freijedo, F.D.; Pastorelli, M.; Guerrero, J.M. Effect of State Feedback Coupling and System Delays on the Transient Performance of Stand-Alone VSI With LC Output Filter. *IEEE Trans. Ind. Electron.* **2016**, *63*, 4909–4918. [CrossRef]
8. De Bosio, F.; de S. Ribeiro, L.A.; Freijedo, F.D.; Pastorelli, M.; Guerrero, J.M. Discrete-Time Domain Modeling of Voltage Source Inverters in Standalone Applications: Enhancement of Regulators Performance by Means of Smith Predictor. *IEEE Trans. Power Electron.* **2017**, *32*, 8100–8114. [CrossRef]
9. Li, Z.; Li, Y.; Wang, P.; Zhu, H.; Liu, C.; Gao, F. Single-Loop Digital Control of High-Power 400-Hz Ground Power Unit for Airplanes. *IEEE Trans. Ind. Electron.* **2010**, *57*, 532–543.
10. Turner, R.; Walton, S.; Duke, R. Robust High-Performance Inverter Control Using Discrete Direct-Design Pole Placement. *IEEE Trans. Ind. Electron.* **2011**, *58*, 348–357. [CrossRef]
11. Li, Y.W.; Loh, P.C.; Blaabjerg, F.; Vilathgamuwa, D.M. Investigation and Improvement of Transient Response of DVR at Medium Voltage Level. *IEEE Trans. Ind. Appl.* **2007**, *43*, 1309–1319. [CrossRef]
12. Wang, X.; Loh, P.C.; Blaabjerg, F. Stability Analysis and Controller Synthesis for Single-Loop Voltage-Controlled VSIs. *IEEE Trans. Power Electron.* **2017**, *32*, 7394–7404. [CrossRef]
13. Yepes, A.G.; Freijedo, F.D.; Doval-Gandoy, J.; López, O.; Malvar, J.; Fernandez-Comesaña, P. Effects of Discretization Methods on the Performance of Resonant Controllers. *IEEE Trans. Power Electron.* **2010**, *25*, 1692–1712. [CrossRef]
14. Shinskey, F.G.; Liptak, B.G.; Bars, R.; Hetthéssy, J. *Control Systems—Cascade Loops*, 4th ed.; CRC Press: Boca Raton, FL, USA, 2006; Volume 2.
15. Maksimovic, D.; Zane, R. Small-Signal Discrete-Time Modeling of Digitally Controlled PWM Converters. *IEEE Trans. Power Electron.* **2007**, *22*, 2552–2556. [CrossRef]
16. Kim, E.K.; Mwasilu, F.; Choi, H.H.; Jung, J.W. An Observer-Based Optimal Voltage Control Scheme for Three-Phase UPS Systems. *IEEE Trans. Ind. Electron.* **2015**, *62*, 2073–2081. [CrossRef]
17. Quan, X.; Wu, Z.; Dou, X.; Hu, M.; Huang, A.Q. Load Current Decoupling Based LQ Control for Three-Phase Inverter. *IEEE Trans. Power Electron.* **2018**, *33*, 5476–5491. [CrossRef]
18. Lee, T.S.; Chiang, S.J.; Chang, J.M. H-infinity loop-shaping controller designs for the single-phase UPS inverters. *IEEE Trans. Power Electron.* **2001**, *16*, 473–481.
19. Willmann, G.; Coutinho, D.F.; Pereira, L.F.A.; Libano, F.B. Multiple-Loop H-Infinity Control Design for Uninterruptible Power Supplies. *IEEE Trans. Ind. Electron.* **2007**, *54*, 1591–1602. [CrossRef]
20. Lim, J.S.; Park, C.; Han, J.; Lee, Y.I. Robust Tracking Control of a Three-Phase DC–AC Inverter for UPS Applications. *IEEE Trans. Ind. Electron.* **2014**, *61*, 4142–4151. [CrossRef]
21. Kojima, M.; Hirabayashi, K.; Kawabata, Y.; Ejiogu, E.C.; Kawabata, T. Novel vector control system using deadbeat-controlled PWM inverter with output LC filter. *IEEE Trans. Ind. Appl.* **2004**, *40*, 162–169. [CrossRef]
22. Mattavelli, P. An improved deadbeat control for UPS using disturbance observers. *IEEE Trans. Ind. Electron.* **2005**, *52*, 206–212. [CrossRef]
23. Kim, H.; Jung, H.; Sul, S. Discrete-Time Voltage Controller for Voltage Source Converters With LC Filter Based on State-Space Models. *IEEE Trans. Ind. Appl.* **2019**, *55*, 529–540. [CrossRef]
24. Quan, X.; Dou, X.; Wu, Z.; Hu, M.; Song, H.; Huang, A.Q. A Novel Dominant Dynamic Elimination Control for Voltage-Controlled Inverter. *IEEE Trans. Ind. Electron.* **2018**, *65*, 6800–6812. [CrossRef]
25. Pérez-Estévez, D.; Doval-Gandoy, J.; Guerrero, J.M. AC-Voltage Harmonic Control for Stand-Alone and Weak-Grid-Tied Converter. *IEEE Trans. Ind. Appl.* **2020**, *56*, 403–421. [CrossRef]
26. Ryan, M.J.; Brumsickle, W.E.; Lorenz, R.D. Control topology options for single-phase UPS inverters. *IEEE Trans. Ind. Appl.* **1997**, *33*, 493–501. [CrossRef]

27. Franklin, G.F.; Workman, M.L.; Powell, D. *Digital Control of Dynamic Systems*, 3rd ed.; Addison-Wesley Longman Publishing Co., Inc.: Boston, MA, USA, 1997; pp. 110–114, 202–203, 328–330.
28. VandeSype, D.M.; DeGusseme, K.; DeBelie, F.M.L.L.; VandenBossche, A.P.; Melkebeek, J.A. Small-Signalz-Domain Analysis of Digitally Controlled Converters. *IEEE Trans. Power Electron.* **2006**, *21*, 470–478. [CrossRef]
29. Goodwin, G.C.; Graebe, S.F.; Salgado, M.E. *Control System Design*, 1st ed.; Prentice Hall PTR: Upper Saddle River, NJ, USA, 2000; pp. 293–298.
30. Kim, H.; Sul, S.-K. Compensation voltage control in dynamic voltage restorers by use of feed forward and state feedback scheme. *IEEE Trans. Power Electron.* **2005**, *20*, 1169–1177. [CrossRef]
31. Kim, H.S.; Sul, S.K. A Novel Filter Design for Output LC Filters of PWM Inverters. *J. Power Electron.* **2011**, *11*, 74–81. [CrossRef]
32. *Uninterruptible Power Systems (UPS)—Part 3: Method of Specifying the Performance and Test Requirements*; Standard, International Electrotechnical Comission: Geneva, Switzerland, 2011.