Review

The Road to a Robust and Affordable SiC Power MOSFET Technology

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Abstract: This article provides a detailed study of performance and reliability issues and trade-offs in silicon carbide (SiC) power MOSFETs. The reliability issues such as threshold voltage variation across devices from the same vendor, instability of threshold voltage under positive and negative gate bias, long-term reliability of gate oxide, screening of devices with extrinsic defects by means of gate voltage, body diode degradation, and short circuit withstand time are investigated through testing of commercial devices from different vendors and two-dimensional simulations. Price roadmap and foundry models of SiC MOSFETs are discussed. Future development of mixed-mode CMOS circuits with high voltage lateral MOSFETs along with 4–6× higher power handling capability compared to silicon circuits has been described.

Keywords: SiC MOSFET; threshold voltage; oxide reliability; body diode; short circuit withstand time

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1. Introduction

The developments in the materials and power devices in silicon carbide (SiC) during the last two decades have led to the use of SiC devices in power electronics in a more efficient and cost-effective manner [1–3]. The progress can be represented in terms of performance, reliability, cost, and foundry models. In this article, we have summarized the previous work published by our group in regards to the reliability of SiC MOSFETs and have also added some new data as appropriate.

As we know, Silicon power devices have dominated the semiconductor industry in the past few decades [4]. In the power electronic applications where fast switching and lower losses are important metrics, silicon devices are gradually being replaced by SiC and GaN devices [5–7]. The objective is to replace silicon bipolar devices (both electrons and holes conduct current) with SiC and GaN unipolar devices (only electrons conduct current). Because of high reverse recovery charge, Silicon PIN diodes and IGBTs Figure 1; [8] give rise to switching losses, which in turn decrease the efficiency of power electronic converters. In contrast, SiC devices such as Schottky barrier diode (SBD) and MOSFETs have minimal reverse recovery charge (Q_{RR}) and tail current, respectively, which leads to reduced switching losses at a given switching frequency. Furthermore, SiC MOSFETs do not have a 0.7 V junction drop of Silicon IGBT, which results in lower conduction losses. Consequently, approximately 3% higher efficiency per power conversion is achieved (considering 1200 V devices) with SiC devices, and this advantage grows with increasing voltage. This advantage grows to approximately 7% roundtrip efficiency in battery electric vehicles (BEV) [9], which is the reason for the mass adaption of SiC power MOSFETs and SBD in BEVs.

The above discussion points out that the silicon PIN diodes and IGBTs (600 V to 6.5 kV) can be replaced by SiC SBDs and MOSFETs (600 V to 12 kV range). For example, SiC SBDs

are now being used in place of silicon PIN diodes in applications such as switched-mode power supplies, where switching loss is a crucial issue [1,10]. We have not mentioned the use of SiC PIN diodes and IGBTs because these SiC devices are still not reliable due to the presence of basal plane dislocations (BPDs). BPD-induced stacking faults reduce lifetime, increase on-resistance, and cause higher leakage currents in SiC PIN diodes and IGBTs [11].

It should be noted that the low switching losses allow higher switching frequencies along with reduced size of the converter as a trade-off with efficiency gain. In some applications such as BEVs, photovoltaic (PV) converters, and power supplies, higher efficiency is more useful. On the other hand, in applications such as aircraft, space vehicles, drones, variable-speed motor drives for high-speed motors, and power adaptors, smaller size is achieved by increasing the switching frequency at the expense of efficiency gains [2,12].

Figure 1. Comparison of reverse recovery charge of silicon PIN diode (or Fast Recovery Diode) and SiC Schottky diode [8].

2. Reliability

Since commercial SiC MOSFETs are readily available in the market from different vendors, it is convenient to study the reliability and ruggedness of these devices. In the following sections, test results on commercially available devices are presented.

2.1. Threshold Voltage Instability of Commercial SiC MOSFETs

The defects in SiC material raise questions about the long-term reliability of the devices and hence it is important to focus on the defects. Commercial SiC devices in the voltage range of 600 V–1.7 kV have passed standard reliability tests over 1000 h [13], but these tests may not be sufficient to ensure reliable operation without failure under long-term operation. The drift in the threshold voltage (V_{TH}) up to 0.5 V under long-term operation at room temperature is one such issue [14]. This issue may not seem to be a major impediment but indicates a higher defect density in the bulk of the gate oxide. The threshold voltage instability can be due to ionic contamination in the bulk oxide, but also due to SiC/SiO₂ interface defects and border traps. Interface states cause hysteresis of the threshold voltage; border traps can cause permanent drift of V_{TH} . Moreover, V_{TH} drifts cause overdrive variations in the on-state which affect the channel resistance (see Equation (1)).

In addition, it also has high interface state defects (D_{it}), leading to low-field effect (FE) inversion layer mobility. The presence of a high density of interface states near the conduction band edge in SiC MOSFETs results in reduced FE mobility of approximately 20 cm²/V-sec—a factor of 20 times less than the inversion layer mobility in Silicon MOSFETs (~400 cm²/V-sec) [15]. The bulk oxide defects and interface states have proven to be difficult to reduce or reproduce. These defects vary from wafer to wafer, batch to batch and may result in uneven threshold voltages, which may result in uneven current sharing among paralleled devices in a power module. Therefore, it is fair to conclude that the gate oxide is the weakest link in the SiC MOSFETs, and hence there is a need to improve the bulk

and interface quality. If we analyze the inversion channel resistance given in Equation (1), the impact of low inversion channel mobility can be compensated by reducing the channel length and the oxide thickness of the SiC device. This trend has been followed by industry to fabricate SiC MOSFETs where channel length and oxide thickness have been reduced while keeping the gate voltage at 20 V. However, this approach increases the electric field in the gate oxide of SiC MOSFET by nearly 2.5 times in the on-state compared to silicon IGBTs resulting in threshold voltage instability. The effects of short channel length are discussed later in the context of short circuit withstand time (SCWT).

$$R_{ch} = \frac{L_{ch}}{W} \frac{t_{ox}}{\mu_n \epsilon_{ox} (V_G - V_T)}, \quad (1)$$

where R_{ch} is the inversion channel resistance, L_{ch} is the channel length, W is the width of the device, t_{ox} is the oxide thickness, μ_n is the effective inversion layer electron mobility, ϵ_{ox} is the oxide permittivity and V_G and V_T are gate and threshold voltages, respectively.

Nearly 50 devices were procured from several vendors named C, D, and E. The threshold voltage of each device was measured using the constant current method. Table 1 lists the devices and their respective current, voltage rating, and R_{ds-on} . The results are presented in Figure 2. The measured results show that vendor C has the maximum variation in threshold voltage of about 3 V from device to device. Vendors D and E show <1 V threshold voltage variation. The reason behind such variation is the presence of uncontrolled fixed positive charges in the oxide and negative charges in the interface states. The balance between these two numbers determines the threshold voltage.

Table 1. Devices under Tests (DUTs).

Vendors	Type	Voltage Rating	Current Rating	Typ. R_{ds-on}
C	MOSFET	1200 V	12 A	500 m Ω
D	MOSFET	1200 V	10 A	450 m Ω
E	MOSFET	1200 V	10 A	350 m Ω

Figure 2. Threshold voltage variation of 50 SiC MOSFETs from each vendor.

The variation of threshold voltage with temperature is shown in Figure 3. The data show that the devices from vendor C have maximum variation when compared to other vendors. It can be observed that the threshold voltage reduces as temperature increases. This is because, with the increase in temperature, electrons emit from interface states into the conduction band, reducing the negative charge (Q_{it}) and decreasing the threshold voltage as predicted by Equation (2). The change in the threshold voltage by 3 V in the device from vendor C indicates a very high density of interface states. Vendors D and E show a reduced threshold voltage shift but compared to silicon the variation is still far

from ideal, indicating a relatively high density of interface states. The threshold voltage shift in silicon devices shows a very low density of interface states, as expected.

$$V_{th} = \phi_{ms} + 2\phi_F + \frac{Sqrt(4\epsilon_s q N_a \phi_F)}{C_{ox}} - \frac{Q_{it}}{C_{ox}} - \frac{Q_F}{C_{ox}} \quad (2)$$

where ϕ_{MS} is the metal-semiconductor work function difference, ϕ_F is Fermi potential, q is the elementary charge, N_a is the acceptor concentration, C_{ox} is the oxide capacitance per unit area, Q_F is the fixed oxide charge per unit area, and Q_{it} is the interface trapped charge per unit area.

Figure 3. Typical threshold voltage versus temperature curves in SiC MOSFETs from different vendors.

Measurements to study shifts in threshold voltage were conducted on the same devices listed in Table 1. The scheme for threshold voltage instability measurement is shown in Figure 4. After each stress (positive or negative) for a specified period, the threshold was measured at room temperature. The band diagrams of MOS structure under equilibrium for positive and negative gate bias stress are shown in Figure 5. Under the positive gate stress, the threshold voltage shifts in the positive direction due to electrons tunneling from the inversion layer into the traps in the gate oxide near the SiC/SiO₂ interface (called border traps). As shown in Figure 5b, holes can also tunnel from traps to SiC valence band when positive gate stress is applied. During the negative bias stress (Figure 5c), the holes can tunnel into the oxide and electrons can tunnel back into the conduction band of SiC. Before and after each bias stress for 5, 10, 20, and 50 h at room temperature, the threshold voltages were measured at room temperature and high temperatures with an Agilent 4145 parameter analyzer.

Figure 4. Time sequence for gate stress and threshold voltage measurement.

Figure 5. Energy band diagrams of MOS structure under (a) equilibrium; (b) positive; (c) negative bias conditions showing tunneling of electrons and holes in either direction.

The curves in Figure 6 demonstrate threshold voltage shifts under various bias-stress conditions. In the case of devices from vendors C, D, and E, threshold voltage shifts of 0.50, 0.35, and 0.10 V, respectively, are measured with a positive DC bias of +20 V for 50 h. Devices from vendor C showed the greatest shift in threshold voltage, possibly due to the high density of border traps within the gate oxide. Almost all vendors exhibit the same trend in threshold voltage shift with different bias stresses. In contrast, when the gate is biased at -10 V for 50 h, the threshold voltage shifts in the negative direction. For device C, the maximum shift is about -0.2 V while devices A and B show shift less than -0.1 V. Considering the differences in device performance among various manufacturers, some vendors, such as vendor E, have significantly reduced the border traps in the gate oxide by means of the better gate oxidation process.

The positive bias stress measurements at high temperatures for vendors C and D are also shown in Figure 7. At high temperatures, the threshold voltage shift under positive bias is much more pronounced. Since the temperature dependence of the F–N tunneling mechanism is small, trap-to-trap tunneling is postulated to be the dominant mechanism.

Figure 6. Threshold voltage shifts for (a) positive bias-stress of +20 V; (b) negative bias-stress of -10 V for 50 h for commercial SiC MOSFETs. The error bars represent the spread of 5 devices measured for each vendor.

Figure 7. Time-dependent threshold voltage shift at high temperature for a positive bias-stress of +20 V. PBTI (positive bias temperature instability) has been measured at 150 °C.

2.2. Screening of Extrinsic Defects in Gate Oxide of SiC MOSFETs

The surface of the SiC epitaxial layer may contain many surface defects such as particle inclusions, pits, Si fall downs, etc., which in turn translate into defects in the gate oxide when the SiC surface is oxidized and may result in premature breakdown of the gate oxide. These defects are called extrinsic defects. After completing the device processing, it is critical to screen out the devices with extrinsic defects and all vendors do this by gate voltage screening. The gate screening method is one of the ways to remove the devices with extrinsic oxide defects at the wafer level by applying a high voltage to the gate electrode for a very short amount of time (<1 s). The device with the extrinsic defects will result in a short or open, and they can be removed from further consideration. The higher the applied gate voltage, the more devices with extrinsic defects can be eliminated. Therefore, the failure rate in the field, known as the FIT rate (failures per billion device hours of operation), can be reduced as shown in Figure 8 reproduced from reference [16]. For planar MOSFETs, the gate oxide thickness is approximately 40 nm, and so only about 34 V on the gate electrode may be applied (maximum gate oxide field of 8.5 MV/cm to avoid the impact ionization in the gate oxide or hole injection from the gate electrode as shown in reference [17]. A value of 8.5 MV/cm, as opposed to 9 MV/cm given in reference [17], has been used to guard the band for the gate oxide variation during manufacturing). Thus, the ratio of the screening voltage to use voltage is approximately 1.5 for planar MOSFETs. Consequently, the gate voltage screening may not effectively remove many of the extrinsic defects leading to higher FIT rates in the field. On the other hand, Trench MOSFETs from Infineon have much thicker gate oxide (typically 70 nm) due to higher inversion layer mobility along the vertical plane. Therefore, the screening voltage can be as high as 60 V to maintain the oxide electric field of 8.5 MV/cm [17]. Thus, the ratio of the screening voltage to use voltage is approximately three for trench MOSFETs. According to Figure 8 (reproduced from [16]), the reduction in FIT rate can be three orders of magnitude smaller for trench devices compared to planar devices. This means that most of the extrinsic defects can be removed by the application of higher screening gate voltage, making the devices that pass the screening highly reliable. Furthermore, if we compare the device structure of planar MOSFET, which is a standard for many vendors with the Infineon's Trench MOSFET as shown in Figure 9, it can clearly be noted that the pitch of a planar MOSFET is much higher, and the gate oxide is exposed to the higher density of extrinsic defects on the surface when compared to the Trench MOSFET. This implies that, for the same current rating, the trench MOSFET will be approximately 2× smaller in size, and the likelihood of exposure to extrinsic defects is much less [18]. Figure 10 shows typical defect maps supplied by epi vendors, representing the high and low defect densities on a wafer surface. The large and small device areas have been overlaid on the defect map. Obviously, the wafer with large devices and high defect density result in much-reduced yield. There is a clear need to focus on the reduction of surface defects in epilayers to allow higher current MOSFETs needed for electric vehicles and other applications requiring high

current. Infineon's Trench MOSFET is less prone to surface defects which provides a very real advantage for large area device fabrication.

The above advantages of the trench MOSFET with high current density, thicker gate oxide, and much higher ability to remove extrinsic defects during gate voltage screening make them rugged compared to planar MOSFETs.

Figure 8. More efficient screening of extrinsic defects in Trench MOSFETs by means of gate voltage screening as compared to planar MOSFETs [16]. The above figure is reproduced from reference [16]. The dots do not represent experimental data.

Figure 9. Schematic structure of planar and trench MOSFET [18]. The above figure is reproduced from reference [18].

2.3. Recent Breakthrough in the Gate Oxidation Process

Recently reported publications [19,20] describe a method of formation of SiC/SiO₂ interfaces via in situ H₂ etch, silicon deposition followed by low-temperature oxidation, and high-temperature nitridation. The authors reported a reduction in the interface state density typical of Si/SiO₂ MOS structures and a 2× improvement in the inversion layer field-effect mobility in lateral SiC MOSFETs. However, the positive fixed gate oxide charge density was not significantly reduced, which makes the devices normally on or with negative threshold voltage since there is not enough counter-balancing charge in the interface states. To take full advantage of this low interface density, the SiC MOSFET design needs to be changed and this may be achieved by using thicker gate oxide and higher P-well doping to keep the threshold voltage positive. For planar MOSFETs, a 60–70 nm thicker gate oxide can be considered. Furthermore, the use of thicker gate oxide will lead to better screening for extrinsic defects, as mentioned in the previous section.

Figure 10. (a,b) Simulated defect maps with die areas of 10 mm × 10 mm and 4 mm × 4 mm for the wafer with 1.69 cm⁻² defect density. (c,d) Simulated defect maps with die areas of 10 mm × 10 mm and 4 mm × 4 mm for the wafer with 0.14 cm⁻² defect density. The extracted device yields are annotated within the subfigures.

In order to examine the above proposition, a reference design with high D_{it} (Ref) and high fixed positive gate charge representing a commercial device was simulated using TCAD Silvaco. The cross-section of the device is shown in Figure 11, with parameters listed in Table 2. A small amount of counter-doping was used in the P-well to reduce the threshold voltage and improve the inversion layer mobility making it accumulation mode. The same design with much lower D_{it} (Ref-A) is also simulated with the same fixed oxide charge (1×10^{12} cm⁻²) in keeping with recent fabrication advancements. The interface trap density used, and other design parameters are tabulated in Table 2. As expected, the Ref-A device becomes normally on due to high positive fixed charge and low D_{it} . In order to increase the threshold voltage of the Ref-A device, an increase in the P-well doping and oxide thickness is necessary, leading to the Ref-B device. The P-Well counter-doping was removed to increase the threshold voltage, making it a pure inversion mode device. The transfer characteristics are shown in Figure 12 for all three reference designs mentioned in Table 2. As shown in Table 2 and Figure 12, the Ref-B device has a much higher on-resistance negating the effect of reduction in D_{it} . This increase in on-resistance is caused by the decrease in channel mobility due to increased scattering by ionized acceptor impurities in higher doped P-well. The conclusion is that it is not enough to just reduce D_{it} . Fixed positive oxide charge density must also be reduced to take advantage of the reduced D_{it} .

Table 2. Summary of the work tabulated with various scenarios. Each case represents a variation in design parameters with a reference design. The resultant threshold voltage and on-resistance are also tabulated.

Structure	D_{it} ($eV^{-1}cm^{-2}$)	L_{ch} (μm)	T_{ox} (nm)	V_{th} (V)	P- well (cm^{-3})	Surface Net Doping (cm^{-3})	$\frac{1}{2} P$ (μm)	$R_{on} (\Omega)$ ($V_{GS} = 20 V$ and $V_{DS} = 1.5 V$)
Ref	1.06×10^{13}	0.5	40	5.3	X (Accu)	3.73×10^{16} (n)	2.9	0.1
Ref-A	1.0×10^{10}	0.5	40	−0.68	X (Accu)	3.73×10^{16} (n)	2.9	0.089
Ref-B	1.0×10^{10}	0.5	80	5.17	8×10^{17}	4.76×10^{16} (p)	2.9	0.275

Figure 11. Cross-sectional view of a half-cell of the planar MOSFET.

Figure 12. Transfer characteristics of the device with high D_{it} (Ref), low D_{it} (Ref-A) and proposed design modification (Ref-B).

2.4. Time-Dependent Dielectric Breakdown Measurements (TDDB)

To predict the lifetime of gate oxide under a normal operating voltage of 20 V, TDDB measurements were performed on vendor H. Table 3 provides information on the MOSFET from vendor H. The experiments include the application of very high gate voltages, recording the time at which various devices fail, and then projecting the lifetime back to the operating voltage. This provides information on the lifetime of the gate oxide at the operating voltage of 20 V. The application of very high voltage is such that the electric field in the gate oxide (>9 MV/cm) initiates the impact ionization at the gate oxide and in the

polysilicon gate due to which generated holes get injected into the oxide and accelerate the breakdown [17]. As a result, the predicted lifetime is not useful at the operating voltage of 20 V. In order to achieve realistic results, gate voltages such that the electric field in the gate oxide is less than 9 MV/cm should be used. The gate leakage behavior is explained through the energy band diagram as shown in Figure 13. If the electric field is higher than 9 MV/cm, the injected electrons accelerate in the conduction band of the gate oxide and gain enough energy to cause impact ionization in the gate oxide and polysilicon gate. The injected holes accelerate towards the SiC/SiO₂ interface and get trapped. This increases the electric field in the gate oxide near the SiC/SiO₂ interface enhancing the Fowler–Nordheim tunneling/injection of electrons into the gate oxide. This leads to more carrier multiplication and more holes. This cycle results in positive feedback till the oxide breaks down. On the other hand, if the electric field in the gate oxide is less than 9 MV/cm, the holes are not generated, and the gate oxide breaks down at a time scale predicted by the charge to breakdown theory [21,22]. Figure 14 shows the TDDDB measurements performed on planar MOSFET from a specific vendor. The approach using $E_{ox} < 9$ MV/cm provides more realistic results and takes a longer time to perform the measurements. One can also perform these experiments at a much higher temperature such as 300 °C to reduce the measurement time. A detailed explanation of TDDDB studies is provided elsewhere [23,24].

Table 3. Information of commercial SiC MOSFET (Vendor H).

Vendors	Type	Voltage Rating	Current Rating	V _{th} Voltage Range	Oxide Breakdown Voltage	Estimated Oxide Thickness
H	MOSFET	1200 V	40 A	4.62~4.77 V	43 V	40 nm

Figure 13. Schematic diagram showing gate leakage behavior where oxide electric field is above and below the critical electric field of 9 MV/cm.

2.5. Body Diode Reliability

One of the major concerns in the implementation of high voltage SiC MOSFETs is the degradation of the internal body diode. Despite breakthroughs in SiC wafer technology and device processing, basal plane dislocations (BPDs) have always been an issue. The BPDs may originate in the substrate [25], or be created during the growth of epilayer [26], or may be created by certain steps during the device fabrication [27]. Stahlbush et al. reported recently that implantation of high-dose Aluminum (Al) at room temperature results in BPDs [28]. The stacking faults (SFs) are activated due to the energy produced by the recombination of electron–hole pairs in a forward-biased body diode. The carrier lifetime also decreases due to the SFs resulting in an increase in the forward voltage drop of the body diode [29].

Figure 14. (a) Weibull distribution at 150 °C with different gate biases; (b) predicted failure times [17].

The effect of SFs on the on-resistance and the forward leakage current in a 10 kV SiC MOSFET [30] was first reported by Agarwal et al. in 2007. The body diodes are expected to degrade more in thicker or high voltage epilayers due to the bigger size of the stacking fault.

Commercially available 1700 V SiC power MOSFETs from three vendors were used in the experiments. The objective was to study the effect of SFs on the body diode and on-resistance in these devices. The I_D - V_D characteristics in the third quadrant (Figure 15) and first quadrant (shown in Figure 16) were measured at room temperature as a function of the stress time of the forward-biased body diode. The detailed experimental study can be found in reference [31].

The third quadrant and first quadrant I_D - V_D characteristics with gate voltages of 20 V and forward stress times of 10, 20, and 100 h at 5 or 3.5 A have been plotted in Figures 15 and 16, respectively. The degradation of on-resistance ($R_{ds,on}$) follows the degradation of the body diode. This $R_{ds,on}$ increases due to enhanced scattering by the SFs [30]. Device D'' exhibited the greatest increase in the $R_{ds,on}$ (about 3.8 times) after 100 h of stress, demonstrating the presence of the highest number of SFs in the active areas.

Results from this study are relevant to the design and processing of SiC MOSFETs of voltages equal to or greater than 1.7 kV. Some vendors may be using a heavy dose of Al implants at room temperature to form p+ contacts in the SiC MOSFETs. Although the room temperature implant would reduce cost, this process may generate additional BPDs [26]. The body diode will conduct during a portion of the switching cycle if SiC MOSFETs are used in switching applications without freewheeling Schottky diode chips. To reduce the degradation of body diode, SiC MOSFETs with integrated Schottky diodes have been investigated [32]. Furthermore, the use of external Schottky diode chips is also a viable option.

Figure 15. Third-quadrant I_D - V_D characteristics for built-in body diode of 1.7 kV SiC DMOSFET from three vendors. The body diodes were stressed at 5 A for (a) Device E'' (b) Device G and 3.5 A for (c) Device D''.

Figure 16. First quadrant I_D - V_D characteristics at gate voltage $V_{GS} = 20$ V of 1.7 kV SiC DMOSFET from three vendors. The curves are shown before and after stressing the body diode at 5 A for (a) Device E'' (b) Device G and 3.5 A for (c) Device D''.

2.6. Short Circuit Withstand Time

Low short circuit withstand time (SCWT) is a very critical issue in SiC MOSFETs. If we use a 1.2 kV device as an example and apply a drain bias of 800 V and gate bias of 20 V, the device must last at least for 7–10 μ s which unfortunately is not true for most of the commercially available SiC devices. Generally, the SCWT of SiC MOSFETs is lower than the Si IGBTs. When a high drain (800 V) and full gate operating voltage (20 V) is applied, the drain current rises rapidly, the device temperature increases, and then the mobility decreases, reducing the drain current, but the temperature continues to increase due to high power dissipation. The device breaks down when critical energy has been dissipated in the device. When the internal temperature rises above 660 $^{\circ}$ C, aluminum starts to melt and diffuse through the grain boundaries in the passivation layer. It may take a few microseconds after aluminum melts for the device to break down. Typical drain current and temperature variation are shown in Figure 17. The non-isothermal simulations were performed using Sentaurus TCAD for 1.2 kV MOSFET. This SCWT of devices varies from vendor to vendor and approximately 1 μ s variation can be found from devices from the same vendor. This difference is most likely due to the variation in the channel length and JFET width of SiC MOSFET. The output current density variation with channel length and width of JFET is illustrated in Figure 18a,b. We can observe from the graph that with a 0.1 μ m increase in L_{ch} , the drain current decreases, and the same is true when W_{JFET} is decreased by 0.1 μ m.

Figure 17. Short circuit simulation result showing current and temperature trend with $V_{ds} = 800$ V and $V_{gs} = 20$ V pulse.

Figure 18. Output current density (a) with L_{ch} variation; (b) W_{JFET} variation obtained using TCAD simulations.

In order to increase the SCWT, the device design must be modified and in the next section, we will discuss the design parameters which can enhance the SCWT.

There are various approaches in literature such as shielded MOSFET [33]; narrow JFET [34,35]; longer channel length [35]; built-in or external source resistance [36]; inclusion of depletion type silicon MOSFET in series with the source [37]; thin gate oxide with lower V_G [38]; using fast-acting gate driver to rapidly detect the short circuit and reduce gate voltage [39]; using a different metal (such as copper) with a melting point greater than aluminum [40] to increase the SCWT. The preferred method is to use the very highly doped P^+ shielding at the bottom of the P-well which shows a significant improvement in SCWT without compromising the on-resistance of the device. The cross-sectional view of the design of the MOSFET and the current reduction is shown in Figure 19. The design predicts a drop of current to 30–40% for a channel length of 0.5 μm when compared with Figure 18a, which will improve the SCWT.

Figure 19. (a) Cross-sectional view of a half-cell of the MOSFET showing the highly doped P^+ shielded region; (b) Graph showing the drain current reduction with increase in channel length when compared with Figure 19a.

SiC MOSFETs with three different channel lengths were designed and fabricated. It was observed that the SCWT could be improved from 2 to 4 μs by increasing the channel length from 0.4 to 1 μm. The results are shown in Figure 20a,b. This work was performed in collaboration with SUNY POLY, Albany, NY, USA. However, this method is not favored because the on-resistance increases with an increase in channel length.

The other experimental method (in collaboration with SUNY POLY, Albany, NY, USA) is the design with a thinner gate oxide and lower gate voltage. A $0.9 \mu\text{s}$ SCWT improvement is obtained with a thinner gate oxide as shown in Figure 21. The improvement in SCWT is impressive, but the thinner gate oxides will lead to failure of the gate oxide in a converter operation under high dv/dt or di/dt due to gate voltage bounce with a parasitic capacitor or stray inductance. It is customary to protect the gate with a Zener diode but that leads to extra input capacitance, and the Zener diode can only be placed outside the power module near the gate driver.

Figure 20. (a) Graph showing the SCWT variation with channel length; (b) the device short circuit test waveforms at room temperature with $V_{gs-on} = 20 \text{ V}$ and $V_{ds-off} = 800 \text{ V}$; (b1) $L_{ch} = 0.4 \mu\text{m}$, $\frac{1}{2}W_{JFET} = 0.6 \mu\text{m}$; (b2) $L_{ch} = 0.5 \mu\text{m}$, $\frac{1}{2}W_{JFET} = 0.6 \mu\text{m}$ (b3) $L_{ch} = 1.0 \mu\text{m}$, $\frac{1}{2}W_{JFET} = 0.6 \mu\text{m}$.

Figure 21. The device short circuit test waveforms at room temperature with $V_{gs-on} = 20 \text{ V}$ and $V_{ds-off} = 800 \text{ V}$ (a) THICKER GATE OXIDE, $\frac{1}{2}W_{JFET} = 0.6 \mu\text{m}$, $L_{ch} = 0.5 \mu\text{m}$, Cell Pitch = $5.4 \mu\text{m}$, SCWT = $2 \mu\text{s}$; (b) THINNER GATE OXIDE, $\frac{1}{2}W_{JFET} = 0.6 \mu\text{m}$, $L_{ch} = 0.5 \mu\text{m}$, Cell Pitch = $5.4 \mu\text{m}$, SCWT = $2.9 \mu\text{s}$.

3. Cost Roadmap for WBG Devices

The cost of SiC power MOSFETs based on a fabless approach using commercial 150 mm manufacturing has been calculated by Agarwal et al. [41]. The cost calculation of

SiC MOSFETs from 1.2–15 kV MOSFETs has been reproduced in Table 4 and predicts a price of 4.6 cents per amp for a 1.2 kV SiC MOSFET assuming a 50% profit margin.

The assumptions in Table 4 are based on prevailing and projected prices of 150 mm SiC substrates and epilayers from a third party and a conservative cost of processing of SiC wafers as USD 800/wafer, which is slightly on the high side assuming high-temperature implants. Furthermore, 50% gross margin i.e., $\text{Price} = 2 \times \text{cost}$, has been added. Realistic assumptions about the manufacturing yield have been made consistent with 20 A chips and typical defect densities for various voltage nodes as higher defect density is expected in higher voltage epilayers.

The prices predicted in Table 4 are quite feasible for the upcoming surge in electric vehicle demand. The introduction of 200 mm wafers is expected in 2023, which will further reduce the manufacturing costs over the next decade as volumes of SiC may double every two-three years. The calculations assume that fabless companies would design their SiC MOSFET products using the Production Development Kits (PDK) of a given commercial SiC manufacturing line processing both Si and SiC power devices/Si CMOS circuits in the same fabrication facility. The volume of Si wafers will generally subsidize the cost of manufacturing equipment. Furthermore, it is assumed that the SiC substrates and epilayers are supplied by third-party vendors with their own profit margins. The testing and sawing costs are included while the packaging cost is not.

Table 4. Estimation of the price of SiC power MOSFETs at various voltage nodes for a 20 A chip in high volume hybrid Si/SiC foundry [41].

	1.2 kV	1.7 kV	3.3 kV	4.5 kV	6.5 kV	10 kV	15 kV
Drift layer doping [cm^{-3}]	1×10^{16}	7×10^{15}	3×10^{15}	2×10^{15}	1.2×10^{15}	7×10^{14}	4×10^{14}
Drift layer thickness [μm]	10	15	30	40	60	95	145
$R_{\text{on-sp}}$ [mohm- cm^2]	1.7	2.5	7.8	14.5	34.0	89.1	237.8
Chip Area [mm^2]	3.7	4.5	8.0	11.0	17.3	29.5	50.9
Yield [%]	86.8	86	83	80.6	75.7	67	54
Packing factor	0.945	0.939	0.925	0.914	0.902	0.890	0.846
Price for 150 mm SiC + epilayer [USD]	800	881	1126	1289	1615	2185	3000
Price per Amp (USD/A) (50% Gross margin assumed)							
Price (USD/A) for 20 A max.	0.046	0.061	0.131	0.203	0.399	0.960	2.744

4. Foundry Model

To substantially reduce the costs of WBG semiconductors while promoting innovation, the concept of fabless manufacturing offers a viable solution. This model involves separately designing the semiconductor devices and then outsourcing their fabrication to a specialized semiconductor foundry.

Traditionally, SiC devices have been fabricated in dedicated SiC foundries owned by a single business entity. This has resulted in considerably slowing their development over time as many researchers and companies did not have access to commercial fabs.

SiC fabs are expensive requiring an investment of USD 100–200 M USD as well as a significant annual cost of running the fab. Clearly, this is not a viable approach for small and medium-size companies. Under the PowerAmerica initiative, XFAB in Lubbock, Texas was funded to manufacture SiC power devices as a pure-play foundry. The main idea was that SiC devices could be processed at an incremental cost given the large volume of Si

wafers. Contracting out their fabrication processes has enabled small and medium-size design companies to gain a foothold in SiC development. By utilizing an existing well-functioning, high-quality production facility with established high yields, the major cost of running the fab is borne by the fab's existing high Si volume.

XFAB has been highly successful in attracting more than 25 companies to use its SiC manufacturing line. SiC design innovations and production quantities have significantly increased. More players in the field produce more innovations in technology.

A secondary benefit of this approach has been to rescue many outdated silicon fabs which can continue to make profitable SiC chips for the next 10–15 years. Once the 200 mm fabs establish a foothold over the next decade or so, 150 mm lines can continue to function as long as the supply of substrates and epilayers can be maintained. Once the 200 mm becomes the norm, the same model can be applied to existing 200 mm Si foundries.

The key strategy behind this approach is that largely the same process be utilized by all the customers of the SiC foundry. This means that the customers can innovate on the design of their specific chips while using the same general process. Of course, small variations in the process should be allowed if required by a high-volume customer. Since the same processes would be utilized for a large number of customers, high volumes spread over a large number of customers are possible further lowering the cost of manufacturing SiC power MOSFETs and minimizing logistical challenges of supporting many customers.

Ultimately, as the market grows with the electrification of vehicles, many foundry approaches will evolve and co-exist as is the case in silicon, today.

5. Future

The future ahead will bring many interesting applications of SiC MOSFET and other devices. One which warrants discussion is SiC smart power IC technology [42,43]. This technology platform is being developed in collaboration between The Ohio State University and SUNY POLY group, Albany, NY headed by Prof. Woongje Sung. The platform includes low-voltage CMOS devices integrated with the high voltage (400–600 V) SiC lateral power MOSFETs which will lead to the development of SiC power integrated circuits. This platform will offer new opportunities in automotive electronics, battery management systems, industrial electronics, telecommunications, and server farms.

The design and fabrication of integrated circuit (high-voltage (HV) power MOSFET with low-voltage (LV) CMOS circuits) are explained in the reference [43]. Figure 22 shows the cross-section of the fabricated HV NMOS, LV NMOS, and LV PMOS on an N-epi grown on N⁺ substrate. A five-stage ring oscillator was also designed to validate the fabricated CMOS, the operating frequency of which increases from 0.69 MHz at 25 °C to 1.38 MHz at 200 °C at a supply voltage of 25 V. This new technology will be the basis of fully integrated and isolated 4H-SiC power ICs designed in future. The advantage of SiC over Si mixed-mode ICs is the fact that SiC lateral NMOS can support 400–600 V compared to a typical 100–150 V in Si Technology.

Figure 22. Cross-section of the fabricated HV NMOS, LV NMOS, and LV PMOS on an N-epi grown on N⁺ substrate.

6. Conclusions

In conclusion, the article provides a broad perspective of SiC MOSFET performance, reliability, and ruggedness. The major issues such as gate oxide lifetime and yield, threshold voltage variations and instability, body diode instability, and short circuit performance are discussed. Commercial SiC MOSFETs are generally robust and reliable but reliability can be further improved by design and process.

The threshold voltage variation of SiC MOSFETs is caused by variations in oxide charges and trapped interface charges. Both types of charges are somewhat uncontrollable during the process. Therefore, there is a considerable variation in the threshold voltage in devices from the same vendor. The threshold voltage is very sensitive to temperature. As the temperature increases, the threshold voltage of the device decreases. The device may turn on easily at elevated temperatures due to the gate bounce in converter operation. A positive DC bias of 20 V on the gate for 50 h shifts threshold voltage in a positive direction by about 0.3–0.4 V at room temperature, and 2–3 V at 150 °C. The positive shift is due to the electron captured by the defects in the gate oxide. When a negative DC bias of −10 V is applied to the gate for 50 h, the threshold voltage shifts in the negative direction by about 0.1–0.2 V at room temperature. In real converter operation, the device exhibits successive positive and zero gate voltage pulses. Thus, the positive shift recovers during the off-state, and it is not a pressing problem.

The key problem of low inversion layer mobility has been partly solved by Prof. Kimoto's group in Japan, which will allow SiC power devices to penetrate the high volume 600 V market provided certain device and process changes are made to increase the threshold voltage. It has been shown that the advantage of the reduction in D_{it} alone without simultaneous reduction in the fixed positive oxide charge is negated by the need to increase the threshold voltage through higher P-well doping and increased gate oxide thickness. The on-resistance of the optimized device turns out to be higher than the original device with higher D_{it} . Therefore, it is strongly recommended that future research be focused on reducing both D_{it} and the fixed positive charge in the gate oxide.

Constant Voltage TDDDB measurements should be conducted at gate voltages such that the electric field in the gate oxide is below 9 MV/cm to avoid hole generation. Evaluation of all the commercial devices shows $t_{63\%}$ predictions longer than 100 years at 150 °C indicating that the gate oxide reliability of commercial products is sufficient. Morphological defects on the SiC surface result in weak gate oxide, the so-called extrinsic defects. The extrinsic defects must be screened out by an application of high gate voltage.

The gate oxide screening should be performed under an oxide electric field of less than 9 MV/cm to avoid hole generation and trapping. The hole trapping reduces the lifetime of an otherwise good device. The thicker gate oxide in trench MOSFETs is advantageous w.r.t planar MOSFETs since a higher gate oxide screening voltage may be applied to remove almost all the devices with extrinsic defects with three orders of magnitude better FIT rate.

In 1200 V devices, there is no degradation of the body diode that can be observed for up to 100 h. Therefore, the built-in body diode may be used as a free-wheeling diode for devices up to 1200 V. In 1700 V devices, significant degradation of the body diode, as well as the on-resistance, has been observed. Thus, a separate or built-in Schottky diode is warranted for ≥ 1700 V devices.

When high drain (800 V) and full gate operating voltage (20 V) are applied in a 1200 V MOSFET, short circuit withstand times (SCWT) for devices from different vendors vary between 2–5 μ s for 1.2 kV devices measured at room temperature. Approximately 1 μ s variation can be found from devices from the same vendor due to process variation. This can be a major issue because the gate driver must be designed to detect and protect the device within 1 μ s. Various methods of improving the SCWT have been discussed. Among these, the shielded MOSFET by means of high p^+ doping at the bottom of the P-well and smaller JFET width along with higher JFET doping can be implemented without affecting the on-resistance. Smaller JFET width has the further advantage of lowering C_{gd} and hence switching losses.

Finally, the price projections with 150 mm substrate diameter indicate 4.6 cents per amp (50% gross margin) is possible for 1200 V SiC MOSFETs. With 200 mm diameter substrates, the price can fall below three cents per amp, which will make the technology competitive with Silicon IGBTs and wide adoption of SiC MOSFETs will be possible across many applications. The preferred and scalable fabless model to make the technology widely available to many companies and researchers is a hybrid silicon/silicon carbide foundry with one process for all the products (minor process changes should be allowed for large-volume users). This approach would allow low cost for design innovations. A SiC-based mixed-mode CMOS technology platform, combining low voltage CMOS devices with 400–600 V LDMOSFET, is being developed to address higher power applications in many sectors. The main advantage of the SiC-based platform over the well-established Si platform is 4–6 times higher power output.

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