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Gate Current in p-GaN Gate HEMTs as a Channel Temperature Sensitive Parameter: A Comparative Study between Schottky- and Ohmic-Gate GaN HEMTs

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Abstract: In this work, a comparison between the gate-driving requirements of p-GaN HEMTs with gate contact of Schottky and Ohmic type is presented. Furthermore, the presence of a gate current of different magnitude is experimentally verified for both types of devices. Successively, the possibility of using the gate current as a temperature-sensitive parameter and its monitoring during real circuit operation is proposed. The viability of monitoring the gate current without introducing additional complexity in the gate driver is examined through experimental measurements on commercially available p-GaN HEMTs.

Keywords: GaN; HEMT; gate driver; p-GaN gate; TSEP; Schottky contact; Ohmic contact; short circuit; boost converter

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1. Introduction

Gallium Nitride (GaN) is a III-V wide-bandgap compound semiconductor exhibiting excellent properties for high-temperature and high-frequency power electronics applications [1]. At present, the most adopted GaN-based power device is the GaN-on-Si lateral high electron mobility transistor (HEMT). In it, the current conduction occurs in a highly conductive electron gas confined in a narrow region beneath the AlGaN/GaN heterointerface (2DEG, i.e., two-dimensional electron gas). To yield greater intrinsic safety to power-switching systems, the active devices of which they are made are usually required to be normally-off, (i.e., to have a positive threshold voltage, V_{TH}). However, since the 2DEG is inherently present at the AlGaN/GaN hetero-interface, even when no gate bias is supplied, the resulting HEMTs are innately normally-on devices (also referred to as depletion-mode devices) [2]. To overcome this problem and achieve an enhancement-mode behavior, multiple solutions have been proposed in the literature. One option is the recessed gate [3,4], which consists in reducing the thickness of the AlGaN barrier layer beneath the gate contact. Another possibility is the treatment of the gate region with negative fluorine ions [5,6]. The joint effect of both gate recession and fluorine implantation was also investigated [7]. A different approach is that of realizing a cascode configuration by connecting in series a low-voltage enhancement-mode Si MOSFET and a high-volage depletion-mode GaN HEMT [8,9]. A further solution is the introduction of a p-GaN cap layer between the gate contact and the AlGaN region [10]. The latter is the technological choice currently adopted by most manufacturing companies and, except for cascode devices, GaN HEMTs of such a kind are of common commercial availability. Despite the normally-off characteristic, the gate contact of p-GaN gate HEMTs is not isolated as in a conventional MOS-based transistor, thus causing the absorption of a gate leakage current. Moreover, depending on the technological and design parameters of the gate stack, two distinct types of gate contacts can arise [11,12], i.e., Schottky and Ohmic contact. What

implications the gate current has on the driving circuitry must be understood since the complexity of the gate driver scheme has a relevant impact on the manufacturing cost. On the other hand, tailored and more complex gate drivers can help to exploit the full potential of GaN devices in terms of both efficiency and robustness [13]. Moreover, there is growing interest in smart gate-driving solutions [14–16] that can monitor the conditions of the power devices and actuate control algorithms that seek to enhance the system lifetime by reducing over-stress. Several aging and failure phenomena are temperature-induced and some of them might be single-shot events triggered by a sudden fault. Therefore, sensing the channel (or junction) temperature during converter operation with a good degree of time resolution (online sensing) can prove considerably useful. On the other hand, measuring the temperature via an equivalent electrical parameter oftentimes needs to be done in specific electrical conditions and it requires alternation between the normal operation of the converter and a temperature sensing phase.

The main objectives of this paper can be summarized as follows:

(i) Discussing the requirements of the gate-driver circuit for the two different classes of normally-off GaN HEMTs with p-type gate;
(ii) Given the sensitivity of the gate current to the channel temperature [17], discussing the viability of using it as a temperature-sensitive electrical parameter (TSEP) and proposing a sensing circuit for its online monitoring.

The structure of this study is organized as follows. The second section introduces the two different types of p-GaN-based gate contacts from a theoretical perspective. The third section illustrates the gate-driving requirements for the Schottky- and Ohmic-gate devices. In the fourth section, the experimental results concerning the possibility of monitoring the gate current during real circuit operation are presented. The fifth section concludes the analysis.

2. Gate Contact Types in Normally-Off p-GaN HEMTs

A well-established type of GaN-on-Si lateral HEMT employs a GaN/AlGaN heterojunction to achieve the formation of the 2DEG, i.e., a shallow sheet of electrons confined in the GaN at the interface with the AlGaN layer. The advantage of having such an electron gas is that it features a conductivity that is much higher than that of the electron in the bulk GaN [18]. Therefore, if a transistor exploits the 2DEG as the conductive channel between source and drain, it will exhibit a very small on-state resistance. However, GaN HEMTs based on the metal/AlGaN/GaN heterostructure usually show a normally-on behavior, i.e., the drain-to-source current conduction is possible even when no gate bias is supplied. The reason behind this can be explained with the help of the idealized band diagram for a hypothetical metal/AlGaN/GaN heterostructure, as illustrated in Figure 1. Figure 1b shows that when the metal/AlGaN/GaN stack is at thermodynamic equilibrium (i.e., the Fermi energy level E_F is constant along x), the 2DEG is already formed since the lower edge of the conduction band (E_C) lies below E_F at the AlGaN/GaN interface. This can be explained by considering that when an AlGaN layer is grown on GaN, a sheet of positive bound charge develops at the AlGaN/GaN interface due to the spontaneous and piezoelectric polarizations induced by the difference between the two materials in terms of polarization field and lattice constant, respectively [19,20]. This results in a strong electric field, attracting a high concentration of electrons to compensate for the positive fixed charge in the AlGaN, thus leading to the formation of a conductive channel also when no gate voltage is provided.

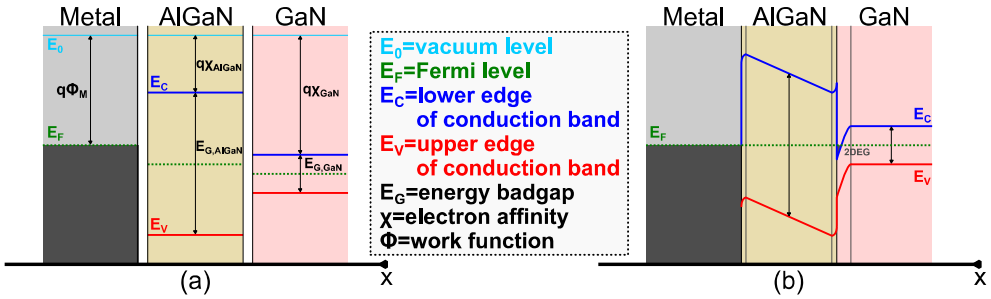


Figure 1. Ideal representation of a monodimensional band diagram of a metal/AlGaN/GaN heterostructure (not to scale) when (**a**) the three materials are isolated from each other and (**b**) when the materials are in contact at thermodynamic equilibrium. The correct band bending depends on the exact charge spatial distribution.

To deplete the 2DEG and make the HEMT normally-off, several solutions have been suggested in the literature [3–7]. Among these, Uemoto et al. proposed to grow a p-doped GaN layer above the AlGaN one [10]. The presence of the p-GaN lifts the lower edge of the conduction band and inhibits the formation of the 2DEG at zero gate bias. The representation of the band diagram reported in Figure 2 helps to visualize this effect. To restore the 2DEG in the metal/p-GaN/AlGaN/GaN stack, a positive gate voltage must be supplied. By doing so, the quantum notch in the GaN layer is shifted below E_F and is populated by free electrons.

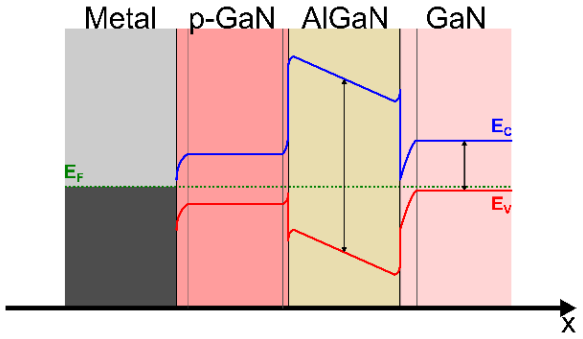


Figure 2. Ideal representation of a monodimensional band diagram of a metal/p-GaN/AlGaN/GaN heterostructure (not to scale) at thermodynamic equilibrium. The correct band bending depends on the exact charge spatial distribution.

Depending on the height and thickness of the barrier between E_F in the metal and the upper edge of the valence band (E_V) in the p-GaN layer, a metal/semiconductor contact with either a resistive or rectifying nature can be obtained. In other words, by properly shaping the Schottky barrier, a HEMT with a Schottky-type or Ohmic-type gate can be manufactured (Figure 3). The main design parameters controlling the shape of the Schottky barrier are the work function of the gate metal (Φ_M), the acceptor concentration, and the thickness of the p-GaN layer. Several contributions addressing the single or joint effects of these parameters are available in the literature [11,12,21–23]. The choice of these parameters not only determines the type of gate contact but it also affects other device properties, such as the value of V_{TH}, breakdown voltage, and transconductance [11,12]. Consequently, several studies have been focused on finding optimum design criteria [11,12,24].

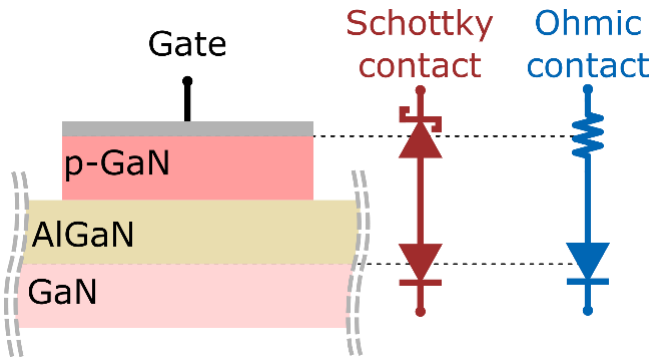


Figure 3. Ideal representation of the cross-section of the region forming the gate heterostructure in a p-GaN gate HEMT. The equivalent circuits corresponding to the Schottky and Ohmic gate contact types are also reported.

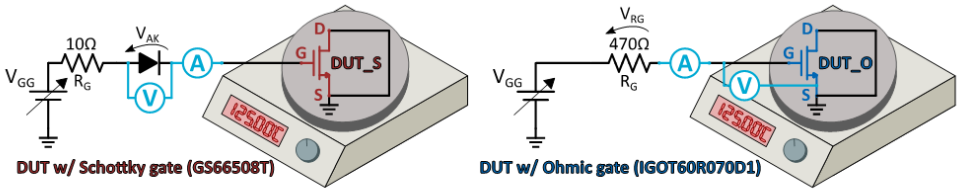
Experimental Investigation of Gate Leakage Current

The contact formed by the metal/p-GaN junction has a direct impact on the turn-on gate current absorption. If the metal deposited on the p-GaN forms a Schottky contact, then the metal/p-GaN/AlGaN/GaN stack can be modeled by two diodes connected back to back: a Schottky rectifier representing the metal/semiconductor junction and a pn rectifier modeling the AlGaN/GaN interface (Figure 3). In this case, when the gate signal is positive, a limited current flows through the reversely biased Schottky diode (in the order of some μA up to few mA). On the other hand, when the contact between the gate metal and the p-GaN layer is of Ohmic type, the gate heterostructure can be modeled by a resistor and a pn diode connected in series—Figure 3—(the corresponding class of GaN HEMTs is also elsewhere referred to as gate injection transistor). In this case, the gate turn-on current is more pronounced (in the order of some mA up to tents of mA). Although both solutions give a positive V_{TH}, i.e., an enhancement-mode behavior, the magnitude of the gate current has a direct impact on the gate-driving scheme. In this work, the presence of this current was experimentally verified for two different kinds of commercially available GaN HEMTs of similar voltage and current rating. These are a 650 V-30 A-rated GaN HEMT manufactured by GaN Systems (GS66508T [25]) with a Schottky-type gate (this device under test is referred to as DUT_S) and a 600 V-31 A-rated HEMT manufactured by Infineon (IGOT60R070D1 [26]) with a Ohmic-type gate (this device is referred to as DUT_O).

To verify the presence of a gate current (I_G) and assess its dependence on the gate-to-source voltage (V_{GS}), the I_G-V_{GS} characteristic was measured through the test setup reported in Figure 4, where the voltmeter and the ammeter are two Keithley 2000 bench multimeters. As previously done in [27,28], the I_G-V_{GS} characteristic of the DUT_S was measured—Figure 4a—by also connecting in series an external pn diode and while monitoring its voltage drop. The reason for this will be explained in the following sections. For the DUT_O, a current limiting resistor R_G = 470 Ω was connected to the gate terminal to avoid damages. For both DUTs, the case temperature was set through a hot plate while the drain and source terminals were connected together to prevent self-heating. The resulting I_G-V_{GS} characteristics are reported in Figure 5 and confirm the presence of a current of larger magnitude through the Ohmic gate—Figure 5b—compared to the one through the Schottky gate—Figure 5a. Nevertheless, in both cases, I_G has a remarkable dependence on V_{GS} and, more importantly, it exhibits a positive variation with the junction temperature of the device. Having a measurand with a consistent and monotonic dependence on the temperature constitutes the first requirement to make it a feasible TSEP. However, the data of Figure 5 were obtained with short-circuited drain and source terminals and do not account for possible variations in the gate current induced by the drain and source potentials [29,30].

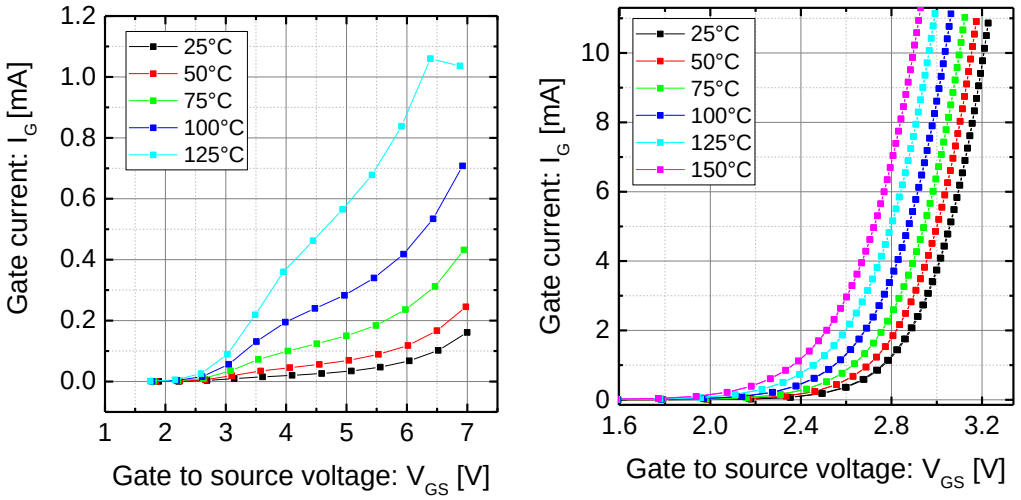
Having the possibility of sensing the gate current during real circuit operation without complicating the gate driver network and without affecting the switching performance

constitutes a major advantage. Therefore, for the DUT_S, we propose to monitor I_G as the voltage drop on a diode in series with the gate—Figure 4a—and, for the DUT_O, the voltage drop on the R_G resistor—Figure 4b. As will be clarified in the following, these components are already present in the conventional gate-driving networks for the respective devices. To estimate the temperature sensitivity of the two different cases, the voltage drops on both the diode (V_{AK}) and on the series resistor R_G (V_{RG}) are reported in Figure 6 as a function of the device temperature at various fixed values of V_{GG}. Both V_{AK} and V_{RG} linearly depend on the temperature of the DUT in the explored range of voltage and temperature but $V_{RG}(T_{DUT\_O})$ shows a more pronounced slope (≈2.5 mV/K) than $V_{AK}(T_{DUT\_S})$ (≈1.3 mV/K). The positive variation of the I_G as a function of the temperature hints that such a current can be used as a temperature-sensitive parameter for both types of devices when no drain-to-source voltage is supplied. Although encouraging, this electrical condition is unrealistic and it is important to understand whether I_G shows a consistent temperature dependence also under drain-to-source bias.



(**a**) (**b**)

Figure 4. Schematic of the test setup for the static measurement of the gate current as function of the gate-to-source voltage for (**a**) the DUT with Schottky-type gate and (**b**) the DUT with Ohmic-type gate.



(**a**) (**b**)

Figure 5. Experimental gate current at various temperatures as a function of the gate-to-source voltage when drain and source are short-circuited for (**a**) DUT_S and (**b**) DUT_O.

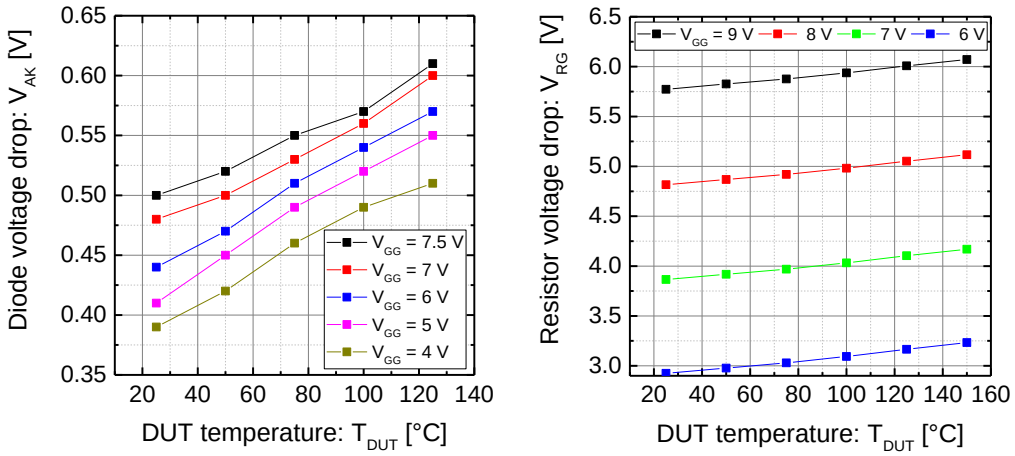


Figure 6. Voltage drop (**a**) on the diode as a function of the temperature on the DUT_S and (**b**) on the series resistor as a function of the temperature on the DUT_O. The data were measured at different values of gate supply voltage.

3. Gate-Driving Circuits for Schottky- and Ohmic-Gate p-GaN HEMTs

The different levels of current absorption of the Schottky- and Ohmic-gate contacts require different gate driver networks to optimally control the corresponding classes of devices.

Given the small current flow through the Schottky contact, this category of GaN HEMTs can be considered to be voltage-driven and is compatible with standard (MOSFET-like) gate drivers. A basic scheme of a driving circuit is depicted in Figure 7a [31]. In this topology, the charge and discharge of the gate capacitance happen via two symmetrical and independent branches: one consisting of R_{Gon} and D_{on} and the other consisting of R_{Goff} and D_{off}. Having two separate paths allows usto individually control the slew rate of the gate voltage at turn-on and at turn-off via the resistors R_{Gon} and R_{Goff}, respectively. To achieve this, only one of the two diodes (D_{on} or D_{off}) is sufficient. Nevertheless, placing the diode D_{on} enables us to measure the gate current during the on-time, as highlighted in the previous section. Since it has been previously reported that a gate voltage stress might result in a shift in V_{TH} for this type of transistor [32–36], a clamping diode might optionally be placed between the gate and source terminals to limit the overvoltage.

On the other hand, the higher gate current required by Ohmic-gate HEMTs makes these devices current-driven ones. A basic gate driver network for such devices is sketched in Figure 7b. The role of the capacitance C_G is twofold: (i) it provides the current spikes (up to few A) during the turn-on and turn-off transients and (ii) it keeps the gate negatively biased during turn-off, thus decreasing the chances of false turn-on events. Once C_G is charged, the gate current decreases to a steady-state value determined by R_G. Therefore, for Ohmic-gate HEMTs, the I_G slew rate at turn-on and turn-off is controlled by the R_1-C_G branch, while the on-state I_G is provided by R_G. Since typical values of driving voltage (V_{GG}) are around 9 V and the on-state gate current is around 10 mA, the value of R_G should be selected in the range of hundreds of Ω [37,38]. Given the values of R_G and I_G, a voltage drop of a few volts will develop across R_G. In addition to the basic gate-driving requirements, a more complex network can be designed to optimize the switching performance and the robustness of the devices [13].

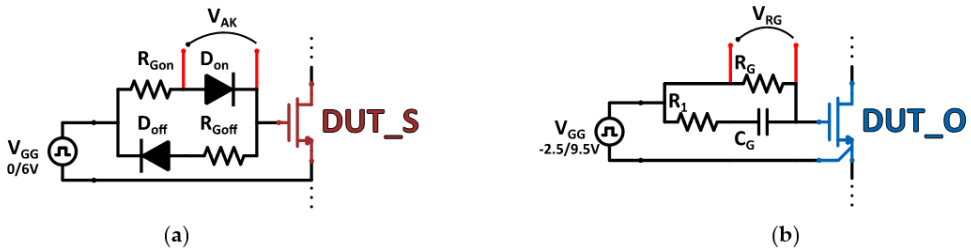


Figure 7. Typical gate driver networks for (**a**) Schottky−gate and (**b**) Ohmic−gate GaN HEMTs.

4. Experimental Results

4.1. Gate Driver Circuit for Schottky-Gate p-GaN HEMTs and Monitoring of Gate Current

In a previous work [28], the concept of using I_G as a TSEP for Schottky-gate p-GaN HEMTs was introduced and its applicability was tested during real circuit operation. The results of this analysis are briefly recalled in this section to draw a comparison with results related to the Ohmic-gate GaN HEMT. The gate driver of Figure 7a was equipped with a differential amplifier for sensing the voltage drop across the diode D_{on}. The so obtained gate driver and sensing circuit are shown in Figure 8a. The output of the operational amplifier was fed to an RC-envelope detector to smooth the commutations of the output signal attributed to the switching nature of the input V_{AK}. This gate driver network was used to drive the Schottky-gate GaN HEMT (GS66508T) serving as a switch in the prototype boost converter outlined in Figure 8a. To modulate the power dissipated by the DUT_S and, consequently, to vary the steady-state temperature reached by the device, various acquisitions were performed at different steps of switching frequencies. For each tested frequency, the converter was operated until a steady-state electrothermal condition was reached, with a duty cycle of 50% and a DC input voltage V_{in} = 100 V. The results reported in Figure 8b show that an output signal of the sensing circuit with a higher amplitude corresponds to increasing values of switching frequency.

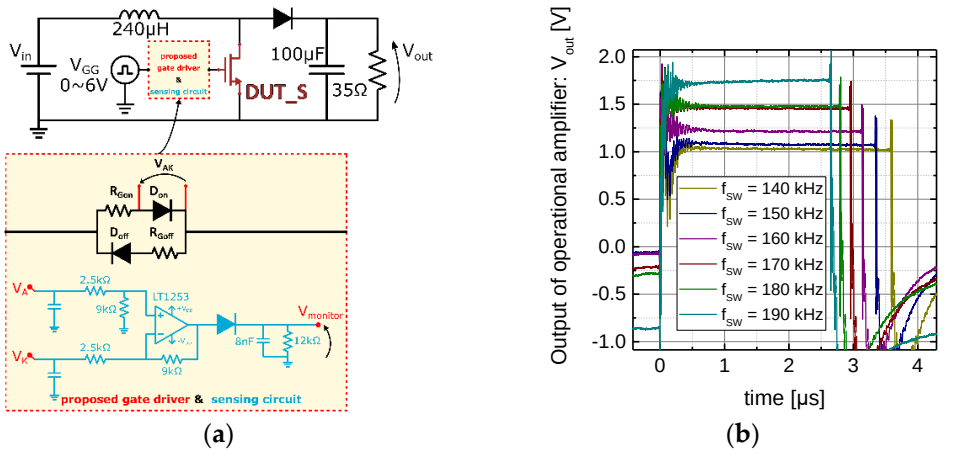


Figure 8. (**a**) Circuit schematic of the prototyped step-up converter based on Schottky-gate p-GaN HEMT and gate driver with the sensing differential amplifier; (**b**) output waveforms of the sensing circuit at different switching frequencies.

To study the response of the gate driver and sensing circuit also to abrupt changes in the temperature of the device, the DUT_S was subjected to short circuit pulses of 10 µs with an increasing supplied DC voltage. A schematic representation of the test setup is reported in Figure 9a, while Figure 9b,c report the experimental waveforms of the drain current and the output of the sensing circuit. In particular, the latter reaches higher levels at higher test voltages and it has faster growth during the first phase of the short circuit pulse, i.e., when the current peak occurs. The outcomes reported in this section support

the possibility of adopting I_G as a TSEP for Schottky-gate GaN HEMTs since it exhibits a monotonic increasing variation with the channel temperature, both during tests at low V_{DS} and high I_D (converter operation) and during tests at high V_{DS} and high I_D (short circuit operation). However, to relate the value of I_G to the actual temperature of the DUT, a further calibration phase is necessary, and it needs to be performed during real operation of the device.

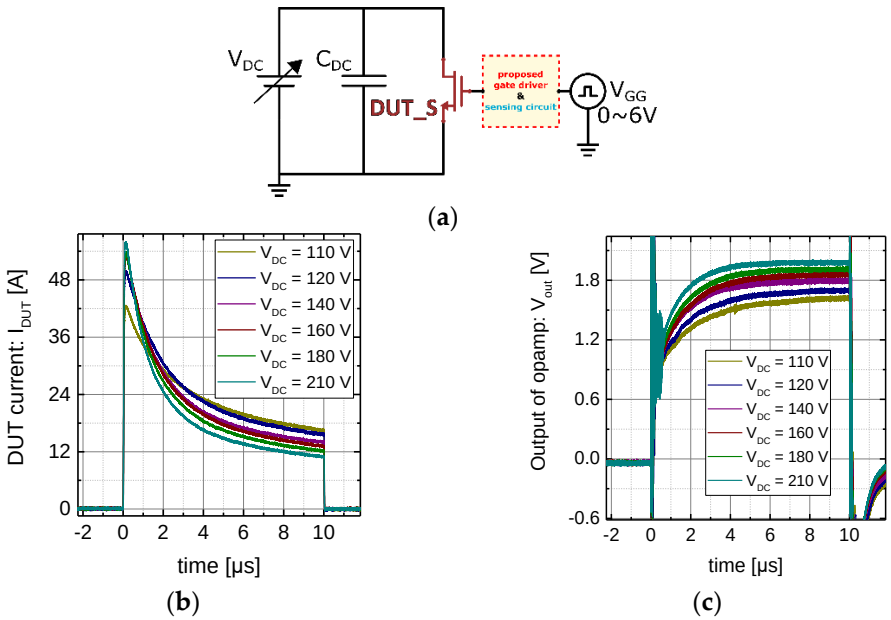


Figure 9. (**a**) Schematic representation of the setup for short circuit test and corresponding experimental waveforms of (**b**) the drain current through the DUT_S and (**c**) the output of the sensing circuit.

4.2. Gate Driver Circuit for Ohmic-Gate p-GaN HEMTs and Monitoring of Gate Current

A testing plan similar to the one followed for the DUT_S was adopted also for the DUT_O. First, the feasibility of monitoring the gate current and using it as an indicator of the temperature of the DUT_O was experimentally tested within the safe operating area (SOA). For this purpose, the synchronous boost converter sketched in Figure 10 was utilized. It consisted of a half bridge where two DUT_Os were connected in parallel per switching side. The details of the converter are reported in Table 1. In this case, the adopted gate driver slightly differs from the one reported in Figure 7b for the presence of common mode inductors connected between the gate and the Kelvin-source terminals. This helps in damping high-frequency oscillations arising from circuit asymmetries and stray components [39].

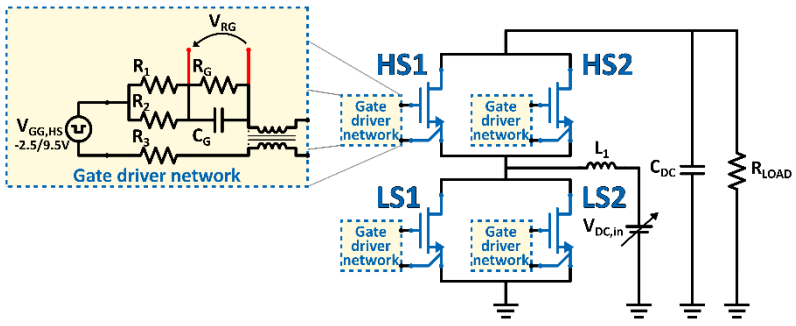


Figure 10. Circuit schematic of the synchronous step-up converter based on Ohmic-gate p-GaN HEMTs and of the gate driver.

Table 1. Main parameters of the DCDC boost converter used for testing the DUT_S and depicted in Figure 10.

Parameter	Value	Unit
$V_{DC,in}$	20 to 120	[V]
f_{sw}	500	[kHz]
C_{DC}	100	[µF]
R_{LOAD}	50	[Ω]
L_1	240	[µH]
R_G	470	[Ω]
C_G	3	[nF]
R_1	10	[Ω]
R_2, R_3	1	[Ω]

To avoid shoot-through, a dead time of around 200 ns was kept between the commutation edges of the V_{GS} of the high-side and low-side DUT_Os. In this case, the modulation of the power dissipated by the DUT_Os was achieved by a variation of the converter input DC voltage. Since no heatsink was placed on the DUT_Os, the supplied voltage was kept well below the voltage rating of the devices to prevent overheating. Figure 11a reports the output voltage of the converter at different values of input voltage. The corresponding waveforms of the voltage drop (V_{RG}) across the resistor R_G of the HS1 device are reported in Figure 11b,c.

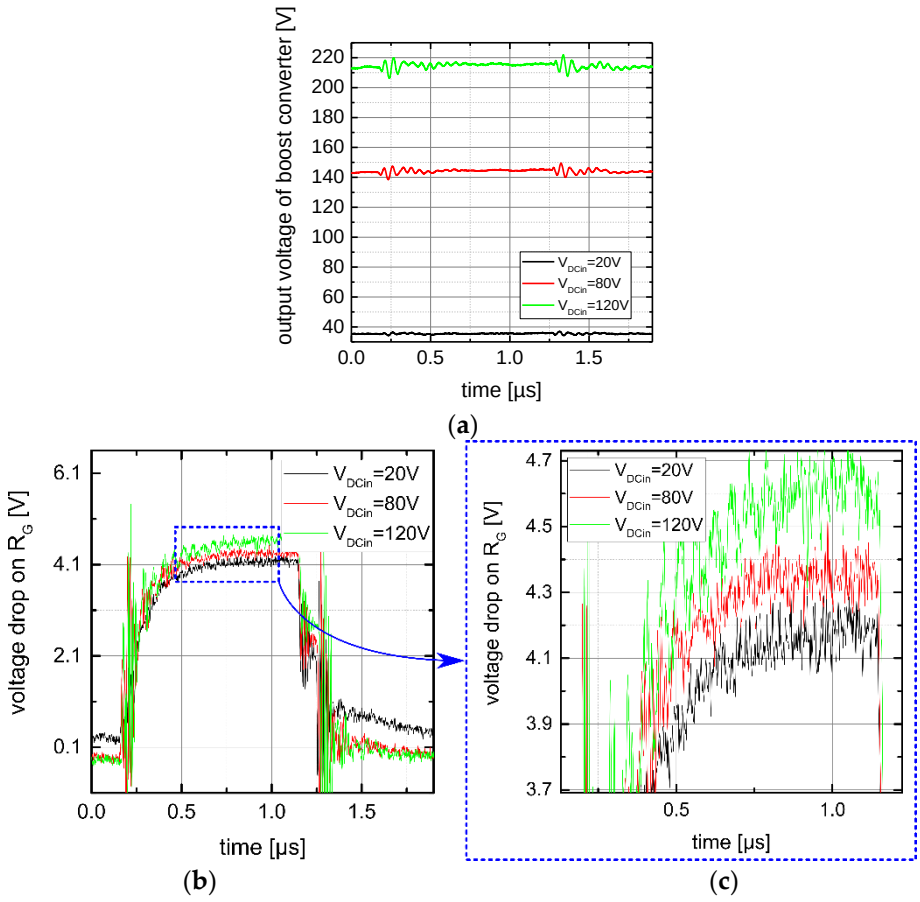


Figure 11. Waveforms associated with the synchronous step-up converter based on Ohmic-gate p-GaN HEMTs. (**a**) Output voltage of the boost converter, (**b**) voltage drop on the gate resistor, and (**c**) magnified view during the on-phase.

An increase in V_{RG} from ≈4.2 V to ≈4.6 V was observed as a function of the converter output power.

Successively, the circuit was rearranged as shown in Figure 12a to perform short circuit tests with a pulse width of 10 µs. Moreover, in this case, the power dissipation was varied by increasing the test voltage and, in order to avoid the destruction of the device, it was swept in a relatively low range spanning from 10 V to 60 V—see Figure 12b,c. The insurgence of sustained high-frequency oscillations at V_{DC} = 60 V prohibited us from further increasing the test voltage. Contrarily to what was observed in the previous test, under these circumstances, V_{RG} decreased despite the rise in power dissipation—see Figure 12d. The reason might be attributed to the lateral nature of the GaN HEMTs and to the formation of a high electrical horizontal field when a high value of V_{DS} is applied. Further investigation of the phenomenon is necessary to confirm this hypothesis. For the DUT_O, conversely to what was observed for the DUT_S, I_G showed opposite variation depending on the electrical conditions. I_G had a positive variation with the power dissipation when the DUT_O was used in a boost converter, while it decreased when the device was subjected to high V_{DS} and I_D during the short circuit tests. Therefore, these findings discourage the adoption of I_G as a TSEP for Ohmic-gate p-GaN HEMTs.

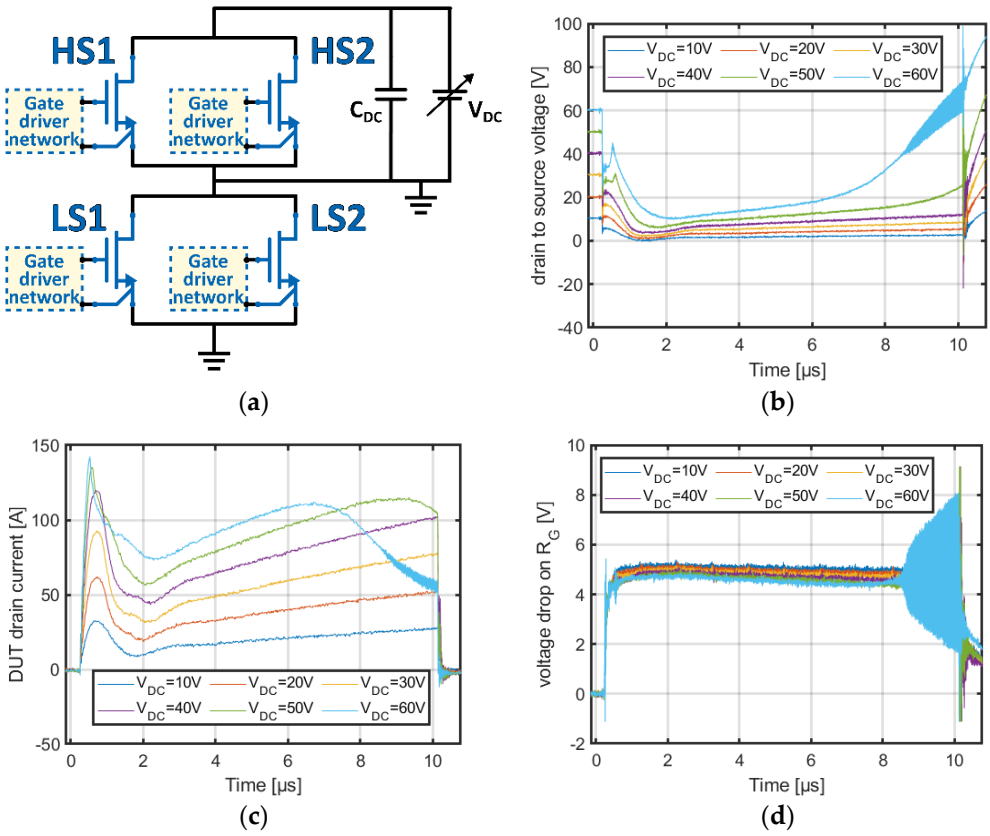


Figure 12. (**a**) Circuit schematic of the short circuit test setup adopted for the DUT_O and corresponding waveforms of (**b**) drain-to-source voltage, (**c**) drain current, and (**d**) voltage drop on the resistor R_G.

5. Summary

In this paper, a comparison between the gate-driving requirements of p-GaN HEMTs with Schottky and Ohmic types of gate contact has been presented. The different magnitudes of gate current have been experimentally verified on commercially available devices for the two classes of GaN HEMTs. The strong influence of the temperature on the I_G, associated with the monotonic dependence of I_G on the temperature when no drain-to-source voltage is supplied, has led to the idea of exploiting it as a TSEP. After considering typical

driving circuits for the Schottky- and Ohmic-gate HEMTs, a means of monitoring I_G has been proposed for both driving schemes. The sensing elements bring no additional complexity to standard driving topologies and I_G can be monitored during regular operation of the device, thus allowing for online estimation of the I_G. The experimental results for the Schottky-type gate show that an increase in power dissipation leads to an increase in the I_G during tests both in and out of the SOA. On the other hand, the tests conducted on the Ohmic-type DUT highlight that when the power dissipated by the device rises, I_G increases when the device is operated as a switch in a boost converter but decreases when the device is subjected to short circuit stress. In conclusion, the variation in I_G in a single direction obtained under different test conditions for the Schottky-type gate makes I_G a good candidate to be used as a TSEP. For Ohmic-gate GaN HEMTs, this possibility is the hindered by the variations in opposite directions of I_G observed during the converter and short circuit operation.

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