

Article

A Multilevel Inverter Topology Using Diode Half-Bridge Circuit with Reduced Power Component

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Abstract: This paper presents a new multilevel converter with a reduced number of power components for medium voltage applications. Both symmetric and asymmetric structures of the presented multilevel converter are proposed. The symmetric topology requires equal dc source values, whereas the asymmetric topology uses minimum switch count. However, both structures suffer from high blocking voltage across the switches. To reduce the blocking voltage on switches, an optimal topology is presented and analyzed for the selection of the minimum number of switches and dc sources, while maintaining a low blocking voltage across the switches. A comparative analysis with recently published topologies was performed. The simulation results, as well as the comparative analysis, validated the robustness and effectiveness of the proposed topology in terms of the reduced power loss, lowered number of components, and cost. Furthermore, in addition to the simulation results, the performance of the proposed topology was verified using experimental results of 9, 17, and 25 levels.

Keywords: multilevel inverter; diode half-bridge circuit; power devices; asymmetric inverter; symmetric inverter



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1. Introduction

In recent years, utilization of multilevel inverters (MLIs) has increased in different applications such as renewable energy systems, utility interfacing schemes, automotive applications, and adjustable speed drives. Compared to two-level inverters, multilevel inverters offer low harmonic distortion, voltage stress on switches, and electromagnetic interference; in addition, there is no need for passive filter usage [1]. In the literature, many researchers are paying much attention to improving the structure of multilevel inverters to minimize power component number and dv/dt ratings of switches, while developing new modulation techniques to reduce the total harmonic distortion (THD) and switching losses [2,3]. The most frequently used MLIs, according to the literature, are diode clamped (dc-MLI) [4], flying capacitor (FC-MLI) [5], cascaded H-Bridge topologies (CHB-MLI) [6] and Modular Multilevel Converter (MMC) [7]. The FC-MLI topology provides better voltage balance and a more redundant state compared to the diode clamp topology. However, real power utilization is not good in FCs and a large size of dc-link capacitors is required [7,8]. Furthermore, both dc and FC topologies suffer from extra power components such as clamping diodes, dc-link capacitors. Unlike them, the CHB topology does not require any additional components or voltage balancing circuits [9]. Moreover, a cascaded connection of the two-level converter is more suitable to generate a higher

number of levels and it provides enhanced modularity and reliability. Additionally, the CHB-MLI topology can be configured in both symmetric (which uses the equal magnitude of sources) and asymmetric (where the magnitudes of the dc sources are determined by geometric progression) configurations. The determination of the dc source magnitude in the case of asymmetric configurations is based on binary and trinary Algorithms [10–12]. Unfortunately, the CHB topology requires a large number of switches and separate dc sources. At the same time, many researchers have tried new multilevel inverter structures, while considering different criteria such as minimum number of IGBTs, dc sources, gate driver circuits, and IGBTs' voltage rating. Several basic units and extended topologies are recommended in [13–17]. However, one can observe that each topology may be more suitable for specific applications, based on requirements, but may not satisfy all the design criteria at the same time. As well, the cascaded structure is introduced to reduce voltage rating on switches. The ladder structure of bidirectional switches is used for series connection of non-isolated dc sources, and it was observed that as the number of levels goes high, the blocking voltage on the bidirectional switches increases, and most of the switches are in different voltage ratings in symmetric methods [18–21]. In [22], a series-connected half-bridge structure is used to produce multilevel dc/dc voltage waveforms. A high number of IGBTs was required because unidirectional switches are used. In [23–33], the bidirectional switches are replaced with a diode and series-connected unidirectional IGBTs. In [23–25], the topologies are proposed with cascaded structure and optimal topology to determine the minimum number of power components against the number of voltage levels. However, the number of power electronics components and blocking voltage on switches is increasing. Further, topologies [26–33] have recently been published and these topologies are generating a higher number of voltage levels, but the stress on the switch, the number of power components, and dc sources are increasing as the number of levels increases. The modular multilevel converter (MMC) [34–37] is quite famous for high voltage applications. However, this NPC MLI and MMC circuit needs separate control techniques to balance the capacitors, and also the number of device counts is high [36,38]. It was observed that the presented topology required a low number of IGBTs.

From the above discussion, most of the MLI topologies required a higher number of switches, gate driver circuits and heat sink modules which are further directly involved in the cost and size of the inverter. In order to reduce the switches and required number of dc sources, in this paper, new symmetric and asymmetric multilevel converter topologies are proposed with a reduced number of switches and power components (dc sources, IGBTs, and driver circuits), while maintaining acceptable blocking voltage values. The proposed multilevel inverter is configured in symmetric, asymmetric, and cascaded methods by connecting a k -unit of the sub-multilevel inverter. A comparative analysis of the proposed topologies and other recently published topologies is presented, and the advantages of the proposed topologies are as follows:

- (1) The number of switches is reduced, which further reduces the number of driver circuits and heat sinks.
- (2) Due to the reduction of the number of switches, the power loss is minimized.
- (3) The number of isolated dc sources is reduced.

The cost of the inverter is reduced, and efficiency is increased. The proposed topologies are more suitable for medium voltage applications due to blocking voltage considerations. The paper is organized as follows: Section 2 presents the basic module of the proposed topology and the switching sequence. Additionally, in Section 2, an extended topology of the basic module is proposed and discussed for the symmetric configuration. The asymmetric configuration is proposed in Section 2. A comparison of both symmetric and asymmetric configurations is shown. Drawbacks of both configurations are highlighted. In Section 3, a cascaded topology is recommended, and two different Algorithms are presented to determine the magnitudes of the dc sources. The proposed topology is optimized for different goals and compared with recent topologies in Section 4. The comparison with recent topologies is given in Section 5. In Section 6, the modulation scheme is presented.

The experimental test results are presented and discussed in Section 7. Finally, conclusions are given in Section 8.

2. Proposed Multilevel Inverter Topology

The basic module is shown in Figure 1, and it consists of two dc-link capacitors (C_1 and C_2), two diodes (D_1 and D_2), and two IGBTs (S_x and S_y). It produces output voltage levels as $+V_{dc}$ and $2V_{dc}$ as shown in Table 1. When the diode D_1 is conducted and S_y is turned on, V_{dc} will be produced. Further, $2V_{dc}$ will be produced when both S_x and S_y are turned on. The D_2 is used to avoid short-circuiting of the source. By using this proposed basic module, three different topologies, named Symmetric Diode Half-Bridge Multilevel Inverter, Asymmetric Diode Half-Bridge Multilevel Inverter, and Cascaded Asymmetric Diode Half-Bridge Multilevel Inverter, can be introduced.

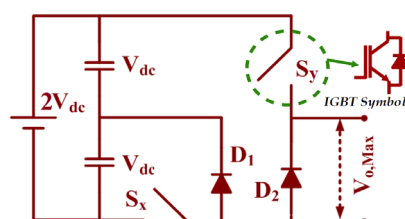


Figure 1. Basic module of proposed converter.

Table 1. Switching Sequence of the Proposed Basic Module.

State	S_x	D_1	S_y	Voltage ($V_{o,max}$)
0	0	0	0	0
1	0	1	1	V_{dc}
2	1	0	1	$2V_{dc}$

2.1. Symmetric Diode Half-Bridge (SDHB) Multilevel Inverter Topology

A generalized structure of the proposed multilevel inverter of the symmetric configuration is shown in Figure 2. It consists of $n - 1$ basic module and the n th module has one IGBT and one diode. In the symmetric configuration, the dc sources are equal as given in (1). By using (2), the corresponding maximum output voltage ($V_{o,max}$) can be obtained.

$$V_1 = V_2 = V_3 = \dots = V_n = V_{dc} \quad (1)$$

$$V_{o,max} = 2nV_{dc} \quad (2)$$

The switching sequence and corresponding states are given in Table 2 to synthesize the multiple stepped dc output voltage waveforms. The full-bridge inverter at the load side produces the positive and negative output voltage levels such as $\pm V_{dc}$, $\pm 2V_{dc}$ up to $\pm nV_{dc}$. The required number of switches (N_{IGBTs}), diodes (N_{diode}), and the dc-link capacitors ($N_{capacitor}$) are obtained, respectively, as expressed in (3) and (4), where n represents the number of modules.

$$N_{Level} = 4n + 1, N_{IGBTs} = 2n + 3 \quad (3)$$

$$N_{Capacitor} = 2n, N_{diode} = 2n - 1 \quad (4)$$

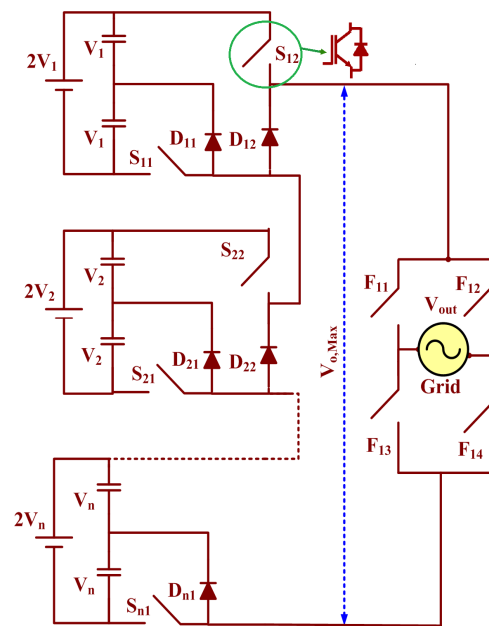


Figure 2. Proposed SDHB multilevel inverter topology.

Table 2. Switching Sequence of the Proposed Symmetric Topology.

State	ON/OFF State Switches										Output Voltage
	S ₁₁	S ₂₁	S ₃₁	...	S ₁₂	S ₂₂	...	S _{n1}	F ₁₁	F ₁₃	
0	0	0	0	...	0	0	...	0	1	0	0
1	0	0	0	...	0	0	...	0	1	1	+V _n
2	0	0	0	...	0	0	...	1	1	1	+2V _n
...
n − 1	0	1	1	...	1	1	...	1	1	1	2∑ _{i=1} ⁿ V _{n−1}
n	1	1	1	...	1	1	...	1	1	1	2∑ _{i=1} ⁿ V _n

2.2. Asymmetric Diode Half-Bridge (ADHB) Multilevel Inverter Topology

The symmetric topology is more suitable when the values of the dc sources are equal; but the required number of power components like switches, dc sources, and gate driver circuits will increase in proportion to the number of voltage levels. This is an obvious disadvantage with a large number of voltage levels. On the other side, the asymmetric topology requires low numbers of components compared with the symmetric topology. The structure of the ADHB is given in Figure 3 and the switching sequence is given in Table 3. The ADHB topology consists of n number of basic modules connected in series, in addition to the full-bridge inverter on the load side. Similar to the conventional CHB topology, the proposed asymmetric method is also configured in trinary configuration, and determination of the magnitude of the dc voltage sources and the maximum output voltage, is expressed as follows,

$$V_1 = V_{dc}, V_2 = 3V_{dc}, \dots, V_n = 3^{n-1}V_{dc} \quad (5)$$

$$V_{o,max} = \left[\frac{(2 \times 3^n) - 2}{2} \right] V_{dc} \quad (6)$$

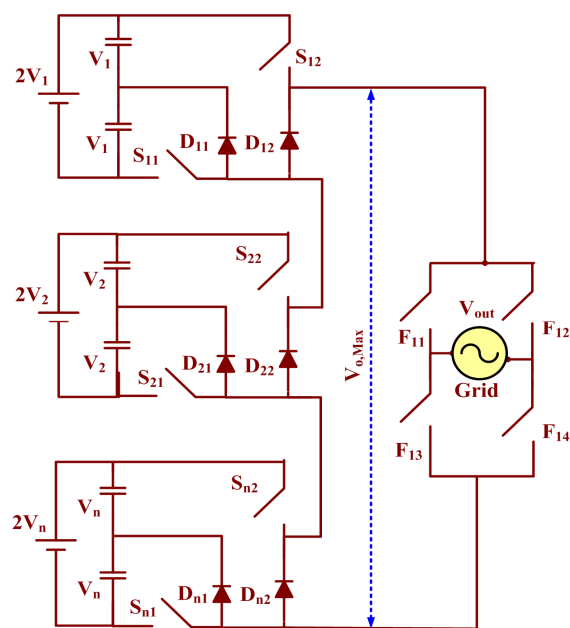


Figure 3. Proposed ADHB multilevel inverter topology.

Table 3. Switching Sequence of the Proposed Asymmetric Topology.

State	ON/OFF State Switches										Output Voltage
	S_{11}	S_{21}	S_{31}	...	S_{12}	S_{22}	...	S_{n1}	F_{11}	F_{13}	
0	0	0	0	...	0	0	...	0	1	0	0
1	0	0	0	...	1	0	...	0	1	1	$+V_n$
2	1	0	0	...	1	0	...	0	1	1	$+2V_n$
3	0	0	0	...	0	1	...	0	1	1	$+3V_n$
...
$n-1$	0	1	1	...	1	1	...	1	1	1	$2\sum_{i=1}^n V_{n-1}$
n	1	1	1	...	1	1	...	1	1	1	$2\sum_{i=1}^n V_n$

For this topology, numbers of the output voltage levels and IGBTs are given in (7) and (8), respectively.

$$N_{Level} = (2 \times 3^n) - 1 \quad (7)$$

$$N_{IGBTs} = 2n + 4 \quad (8)$$

The comparison of the symmetric and asymmetric DHB topologies, in addition to the topologies presented in [13–17], is shown in Figure 4.

As obvious, the proposed topologies require a lower number of power components compared to the conventional topologies. Moreover, in the proposed topologies, the required number of isolated dc sources is lower than that required in the other topologies. This makes it more suitable for renewable energy source applications, especially photovoltaic systems. However, a remarkable disadvantage is that these topologies suffer from high voltage stresses on the full-bridge inverters switches because of dc voltage sum across the switches (F_{11} – F_{14}). Consequently, the proposed topologies are more suitable for medium voltage applications. In addition, the series connection of the dc-link capacitors results in a non-equal share of the voltages. Thus, an extra circuit that has one capacitor and three diodes as provided in [23] will be required to stabilize the voltage across the capacitors.

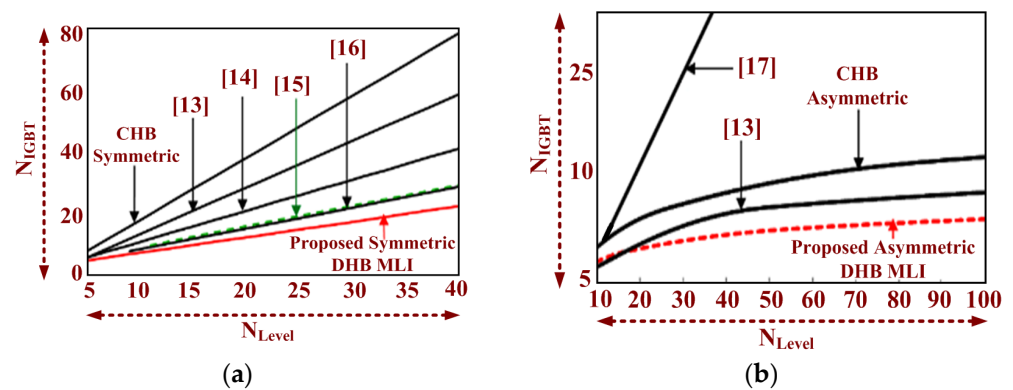


Figure 4. Comparison of N_{IGBT} versus N_{Level} for the proposed topologies with other recent MLI topologies (a) Symmetric DHB, (b) Asymmetric DHB.

3. Cascaded Asymmetric Diode Half-Bridge Multilevel Converter

The symmetric and asymmetric configurations suffer from high blocking voltage across the switches, which necessitate the design of the full-bridge switches to withstand the sum of all the dc source values as well as the increase of the ratings of the gate driver and snubber circuits and using cooling schemes (which increase the cost of inverters). Hence, to avoid such problems, a cascaded topology is recommended for a higher number of levels with reduced maximum blocking voltage across the switches. However, the uneven power distribution is occurred in asymmetric topologies due to the number of switching of few switches are higher than other switches. This is even occurring in conventional CHB topology asymmetric configuration and this is a remarkable drawback of asymmetric configuration.

A cascaded diode half-bridge configuration consists of k units, and each unit has $2n$ number of capacitors and diodes. Each unit is named as a sub-multilevel inverter (SMLI) with n modules so that each SMLI has an equal number of modules as given in Figure 5. Each SMLI produces $V_{o,1}, V_{o,2} \dots V_{o,k}$, so that the output voltage (V_{out}) equals the k th voltage sum. A high number of levels can be achieved by the determination of magnitudes of the dc sources. In this work, two possible algorithms are proposed to determine the magnitudes of the dc sources.

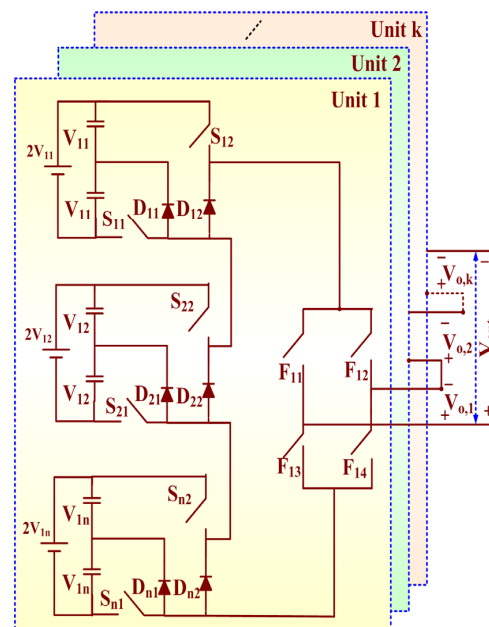


Figure 5. Generalized structure of the proposed cascaded ADHB multilevel inverter topology.

3.1. The First Algorithm

In the first algorithm, all the dc source values are equal. For each SMLI, the determination of the magnitudes of the dc sources is given as follows.

For 1st SMLI:

$$V_{11} = V_{12} = V_{13} = \dots = V_{1n} = V_{dc} \quad (9)$$

$$V_{o1,max} = \left[\frac{(4n+1)-1}{2} \right] = 2nV_{dc} \quad (10)$$

The number of output voltage levels generated by the first SMLI is given as follows,

$$N_{Level,1} = 4n + 1 \quad (11)$$

2nd SMLI:

$$V_{21} = 2(V_{o1,max}) + V_{dc} \quad (12)$$

$$V_{21} = V_{22} = V_{23} = \dots = V_{2n} = (4n+1)V_{dc} \quad (13)$$

$$V_{o2,max} = 2n(4n+1)V_{dc} \quad (14)$$

The numbers of output voltage levels generated by the first and second SMLIs are obtained as follows,

$$N_{Level,2} = (4n+1)^2 \quad (15)$$

kth SMLI:

$$V_{k1} = V_{k2} = V_{k3} = \dots = V_{kn} = (4n+1)^{k-1}V_{dc} \quad (16)$$

$$V_{ok,max} = 2n(4n+1)^{k-1}V_{dc} \quad (17)$$

The maximum output voltage and number of output voltage levels based on the first algorithm are expressed as follows,

$$V_{o,max} = \left(\frac{N_{Level} - 1}{2} \right) V_{dc} \quad (18)$$

$$N_{Level,k} = (4n+1)^k \quad (19)$$

3.2. The Second Algorithm

In the second algorithm, all the dc source values are unequal, i.e., each SMLI has a trinary geometric progression of dc source magnitudes. The dc source values of each SMLI are determined as follows,

1st SMLI:

$$V_{11} = V_{dc}, V_{12} = 3V_{dc}, V_{13} = 9V_{dc}, V_{1n} = 3^{n-1}V_{dc} \quad (20)$$

$$V_{o1,max} = (1 + 3 + 9 + \dots + 3^n)V_{dc} = \left(\sum_{i=1}^n V_{1i} \right) V_{dc} \quad (21)$$

2nd SMLI:

$$V_{21} = 2(2V_{11} + 2V_{12} \dots + 2V_{1n}) + V_{dc} = [2(3^n) - 1]V_{dc} \quad (22)$$

$$V_{22} = 3V_{21}, V_{23} = 3^2V_{22} \dots V_{2n} = [2(3^n) - 1](3^{n-1})V_{dc} \quad (23)$$

$$V_{o2,max} = \sum_{i=1}^n V_{2i} = \sum_{i=1}^n \left[\frac{[2(3^i) - 1] \times (3^{i-1}) - 1}{2} \right] V_{dc} \quad (24)$$

kth SMLI:

$$V_{kn} = [2(3^n)^{k-1} \times (3^{n-1})] V_{dc} \quad (25)$$

$$V_{o,k,\max} = \sum_{i=1}^n V_{ki} = \sum_{i=1}^n \frac{([2(3^i) - 1]^{k-1} \times (3^{i-1}) - 1)}{2} V_{dc} \quad (26)$$

The maximum output voltage and number of output voltage levels based on the second algorithm are expressed as follows,

$$V_{o,\max} = \left(\frac{N_{Level} - 1}{2} \right) V_{dc} \quad (27)$$

$$N_{Level,k} = [2(3^n) - 1]^k \quad (28)$$

Numbers of IGBT, drivers, diodes and dc-link capacitors are given by,

$$N_{IGBTs} = N_{driver} = (2n + 4)k \quad (29)$$

$$N_{Capacitor} = N_{diode} = 2nk \quad (30)$$

3.3. Total Blocking Voltage

The voltage and current ratings of the switches is an important factor that decides the cost of an inverter. In general, all the switches carry the same current with respect to the load. However, this is not true for voltages, as switches withstand different voltages based on the topology structure. In this work, a total blocking voltage (T_{Block}) represents the sum of the maximum blocking voltage of all the switches. It is expressed as follows,

$$T_{Block} = V_{T,Module} + V_{FB} \quad (31)$$

where $V_{T,Module}$ and V_{FB} represent the total blocking voltage of the switches in a module and full-bridge, respectively. $V_{T,Module}$ is expressed as follows,

$$V_{T,Module} = \frac{3}{2} \left(\sum_{j=1}^n \sum_{i=1}^n V_{i,j} \right) V_{dc} = \left(\frac{3(N_{Level} - 1)}{4} \right) V_{dc} \quad (32)$$

Additionally, V_{FB} is given by,

$$V_{FB} = 4 \left(\sum_{j=1}^n \sum_{i=1}^n V_{i,j} \right) = 2(N_{Level} - 1) V_{dc} \quad (33)$$

Hence, by summing (32) and (33), one can express T_{Block} of the switches of the proposed topologies as follows,

$$T_{Block} = \left(\frac{11(N_{Level} - 1)}{4} \right) V_{dc} \quad (34)$$

4. Optimal Topology of the Proposed Multilevel Converter

In this section, a comparative study of the results of various topologies given in [18–23] is presented to show the advantages of the proposed topology. In the comparative study, R_{11} denotes the topology of the first algorithm, while R_{12} denotes the topology of the second algorithm presented in [18], R_{21} and R_{22} denote the same but for the algorithms presented in [19]. Like so, R_{31} denotes the topology in [20], R_{41} and R_{42} denote the topologies of Algorithms 1 and 3 in [21], R_{15} denotes the topology in [22], R_{16} denotes the topology in [23], and CDHB₁ denotes the proposed topology based on the first algorithm, while CDHB₂ denotes the proposed topology based on the second algorithm.

The comparative analysis is presented in Figures 6 and 7 in terms of a number of components such as N_{IGBT} , N_{diode} , N_{source} , $N_{capacitor}$, and N_{driver} , as well as T_{Block} .

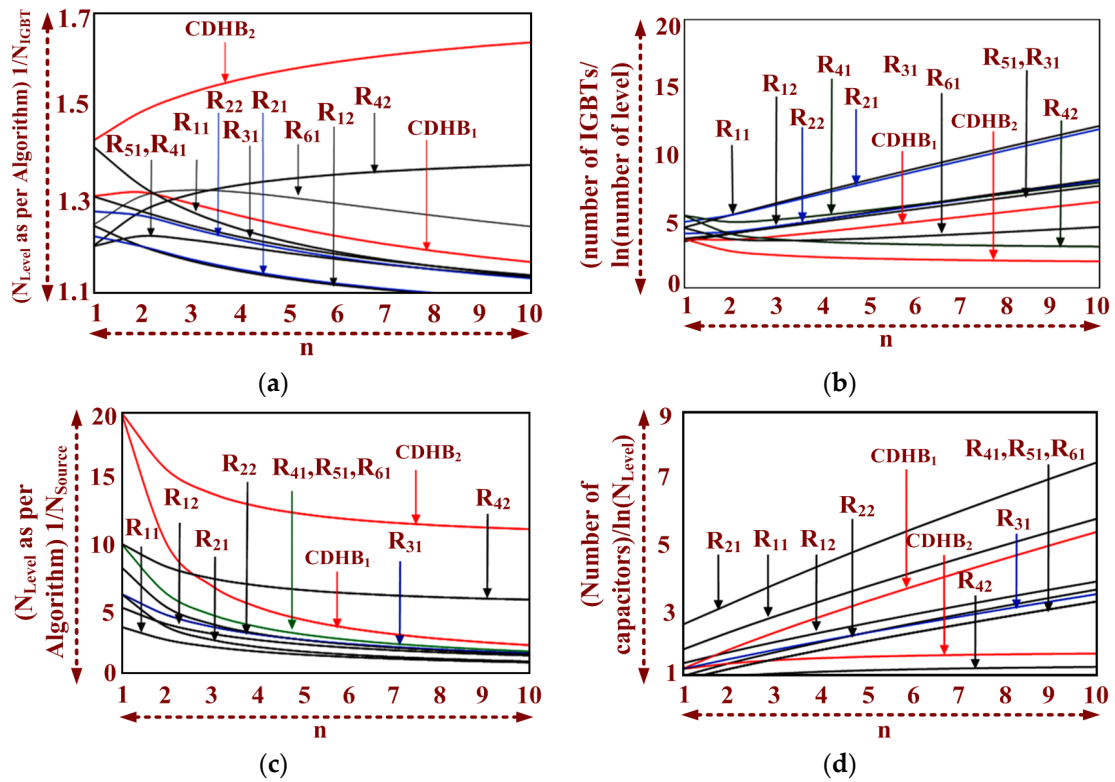


Figure 6. Comparison of proposed topology with various topologies algorithms for (a) N_{Level} with constant N_{IGBTs} , (b) N_{IGBTs} with constant N_{Level} , (c) N_{Level} with constant N_{source} , (d) $N_{capacitor}$ with constant N_{Level} .

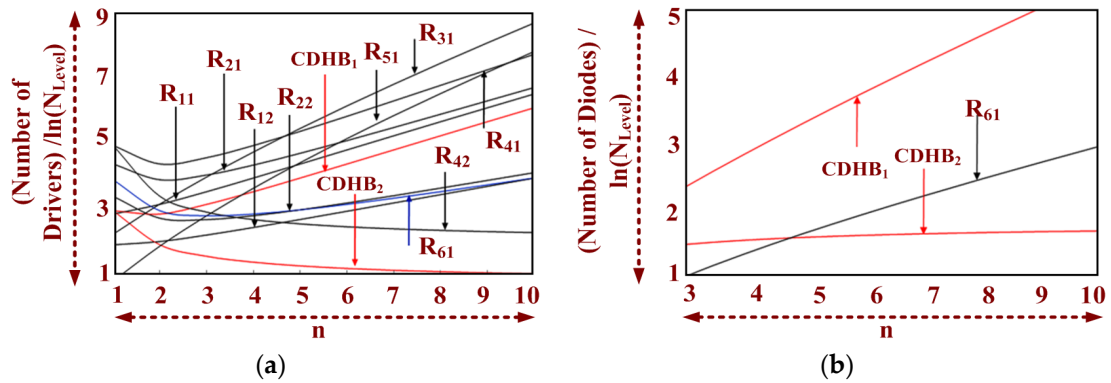


Figure 7. Comparison of proposed topology with various topologies algorithms for (a) N_{driver} with constant N_{Level} , (b) N_{diode} with constant N_{Level} .

4.1. Number of Voltage Levels with a Constant Number of IGBTs

Considering the constant number of switches is kept in each unit. Thus,

$$N_{IGBTs} = (2n_1 + 4) = (2n_2 + 4) \dots = (2n_k + 4) \quad (35)$$

$$k = N_{IGBTs} / 2n + 4, (\text{when } n_1 = n_2 = \dots = n_k)$$

Hence, numbers of voltage levels of the first and second algorithms are determined with a constant number of IGBTs as follows,

$$N_{Level,1} = \left[(4n + 1)^{1/(2n+4)} \right]^{N_{IGBT}} \quad (36)$$

$$N_{Level,2} = \left[(2(3^n - 1))^{1/(2n+4)} \right]^{N_{IGBT}} \quad (37)$$

Figure 6a shows that CDHB₂ gives the maximum number of output voltage levels, when $n > 1$, compared to the other topologies.

4.2. Number of IGBTs with a Constant Number of Voltage Levels

The number of IGBTs of the first and second algorithms is determined with a constant number of voltage levels, respectively, as follows,

$$N_{IGBTs} = \ln(N_{Level,1}) \left(\frac{(2n+4)}{\ln(4n+1)} \right) \quad (38)$$

$$N_{IGBTs} = \ln(N_{Level,2}) \left(\frac{(2n+4)}{\ln(2(3^n-1))} \right) \quad (39)$$

Figure 6b shows that the proposed cascaded structure gives the minimum number of IGBTs when $n = 1$. When $n > 1$, the required number of IGBTs are increasing for the topologies presented in [18–23] and CDHB₁; but is decreasing gradually with the increase of levels for the proposed CDHB₂.

4.3. Number of Voltage Levels with a Constant Number of Sources

Recalling Figure 5, the number of sources required for each unit is given as $N_{source} = n_1 + n_2 + n_3 + \dots + n_k$, thus for the k th unit, it is given as $N_{source} = nk$. Hence, numbers of voltage levels of the first and second algorithms are determined with a constant number of sources as follows,

$$N_{Level,1} = \left[(4n+1)^{1/n} \right]^{N_{sources}} \quad (40)$$

$$N_{Level,2} = \left[(2(3^n-1))^{1/n} \right]^{N_{sources}} \quad (41)$$

Figure 6c shows that the proposed cascaded structure gives the minimum number of sources and produces the maximum number of output voltage levels compared to the other considered structures, especially with $n = 1$.

4.4. Number of Capacitors with a Constant Number of Voltage Levels

The number of capacitors of the first and second algorithms is determined with a constant number of voltage levels, respectively, as follows,

$$N_{Capacitors} = \ln(N_{Level}) \left(\frac{2n}{\ln(4n+1)} \right) \quad (42)$$

$$N_{Capacitors} = \ln(N_{Level}) \left(\frac{2n}{\ln(2(3^n-1))} \right) \quad (43)$$

As shown in Figure 6d, it is clear that all the topologies require a minimum number of capacitors when $n = 1$. Additionally, the required number of power components is high in first algorithm as compared to the second algorithm to generate the same stepped voltage level.

4.5. Number of Drivers with a Constant Number of Voltage Levels

The driver circuits are related to the cost and reliability of the inverter directly. The presented topologies in [18–20] have used bidirectional switches which require single driver circuits to turn the two switches. As shown in Figure 7a, CDHB₂ uses a fewer number of driver circuits compared to the other topologies. Furthermore, an equal number is required of the IGBTs and driver circuits for the proposed topologies. Therefore, Equations (38) and (39) express also the number of driver circuits of CDHB₁ and CDHB₂, respectively.

4.6. Number of Diodes with a Constant Number of Voltage Levels

The lifetime of diodes is higher than other power electronic components. Each module of the proposed topology uses two diodes. Thus, the minimum numbers of diodes for a constant number of voltage levels are given for CDHB₁ and CDHB₂ as follows,

$$N_{diode} = \ln(N_{Level}) \left(\frac{2n}{\ln(4n + 1)} \right) \quad (44)$$

$$N_{diode} = \ln(N_{Level}) \left(\frac{2n}{\ln(2(3^n - 1))} \right) \quad (45)$$

Figure 7b shows that the proposed CDHB topology requires a minimum number of diodes compared to the topology in [23]. Additionally, the second algorithm is better than the first algorithm and the topology in [23], especially with the increase of n . For diode count, the IGBTs parallel diodes are not considered.

4.7. Blocking Voltage Rating with a Constant Number of Voltage Levels

As the blocking voltage increases, the voltage rating of IGBTs and supporting components (snubber circuit, heat sink, and cooling system) increase. To identify the minimum blocking voltage of the proposed topologies, a constant number of levels are considered, and it was found that the switches require minimum blocking voltage when N_{Level} is low, i.e., $n = 1$.

5. Comparative Study with Recent Cascaded Multilevel Inverter Topologies

The cascaded DHB topology is compared with recent cascaded multilevel inverter topologies presented in [18–23] to show its advantages as shown in Figure 8. In this comparative analysis, all the topologies were considered for $k = 2$.

5.1. The Required Number of IGBTs against the Number of Levels

The increased number of IGBTs results in using extra components such as anti-parallel diodes, heat sinks, cables, layouts, and digital logic gates to generate the switching pattern. It is observable from Figure 8a that the proposed topology based on the two suggested algorithms produces the maximum number of levels with a lower number of IGBTs compared to the trinary configuration of the conventional cascaded topology and the other considered topologies.

5.2. The Required Number of Driver Circuits against the Number of Levels

The driver circuits and some associated components such as optocouplers are usually taken into account to measure the performance of a multilevel inverter. An increasing number of driver circuits degrades the reliability of the multilevel inverter and leads to a further increase of the complex switching control. As presented in Figure 8b, the proposed cascaded topology using the second algorithm requires fewer driver circuits than the other topologies.

5.3. The Required Number of Dc Sources/Capacitors Number of Levels

For the n module, the proposed structure requires a $2n$ number of dc-link capacitors while the other topologies use one dc-link capacitor but with a higher peak magnitude. Figure 8c shows the graph of the number of capacitors versus the number of levels. The proposed topology offers a reduction of the size and cost of the dc-link capacitors. However, it should be mentioned that series connection of the dc-link capacitors requires balancing circuits. As shown in Figure 8d, dc sources varieties are equal in all the topologies and CDHB₁. However, CDHB₂ requires n varieties dc sources.

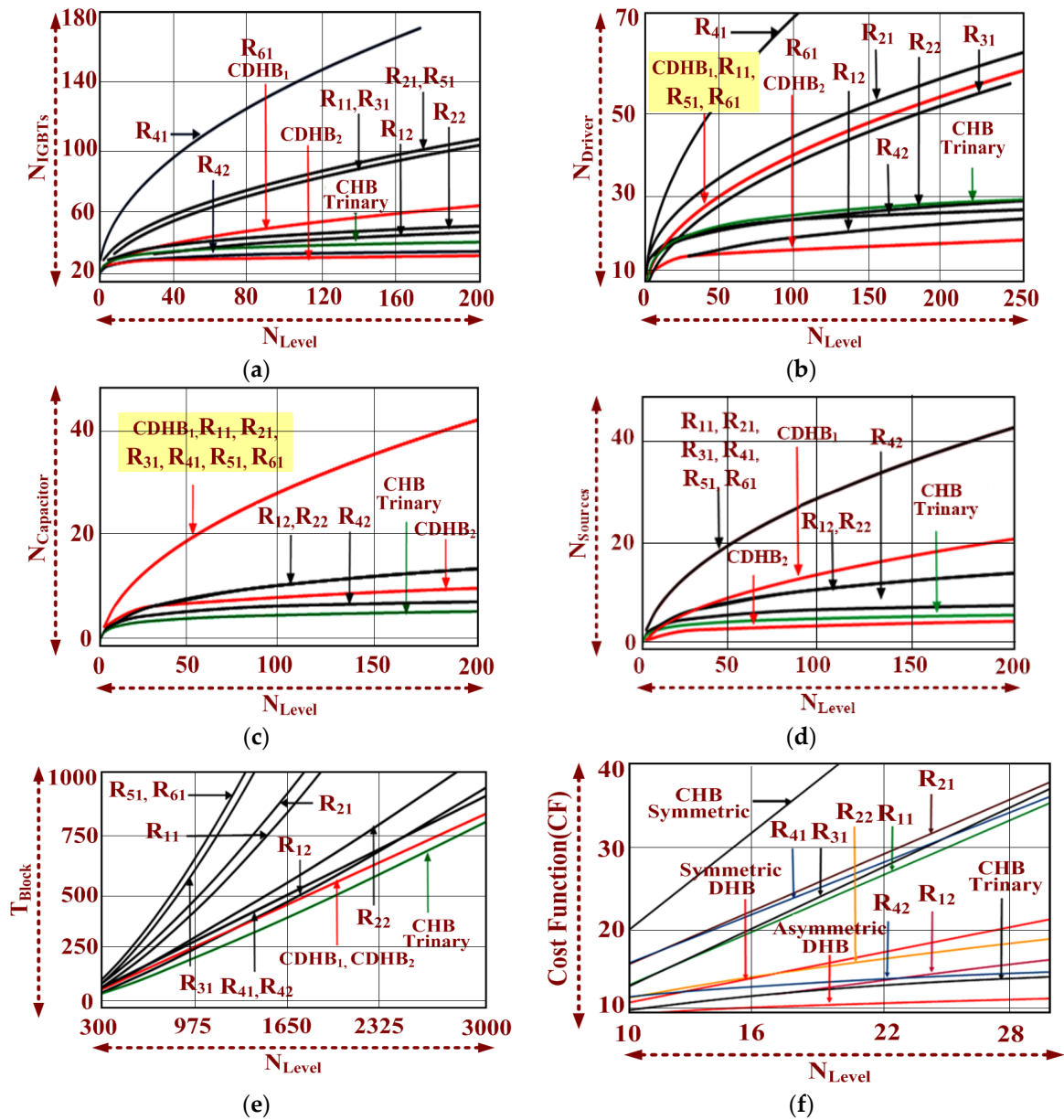


Figure 8. Comparison (a) N_{IGBTs} versus levels (b) N_{driver} versus levels, (c) $N_{capacitor}$ versus levels (d) N_{source} versus levels, (e) T_{Block} versus levels (f) Cost versus levels.

5.4. Total Blocking Voltage against the Number of Levels

For all the considered cases, the cascaded trinary configuration and the proposed cascaded structure introduce the lowest total blocking voltage compared to the other topologies particularly with a high number of levels, as shown in Figure 8e. The topology presented in [24] needs a higher number of IGBTs and Maximum blocking voltage on the switch.

5.5. Cost

The multilevel inverter cost is a good index to decide the topology's effectiveness from a customer viewpoint. The cost depends on the number and rating (voltage and current) of the power components, as well as the number of driver circuits and dc sources [20]. Recalling that the proposed topology uses a fewer number of IGBTs, driver circuits with low total blocking voltage; accordingly, the cost of the proposed inverter is lower than the other topologies. Furthermore, the cost of the switches increases by the increase of the

current rating of the switches. In this work, the current rating of switches is determined by factor α . For the same voltage rating, increasing α will increase the MLI cost. Figure 8f shows a comparison of the proposed symmetric and asymmetric topologies and the other considered topologies at $\alpha = 0.5$. In this comparison, the driver circuits and dc sources are not included. It is clearly obvious that the cost of the asymmetric topology (CDHB₂) is considerably less than the other topologies. Further, in Table 4, recent multilevel inverter topologies [27–30] are compared with the proposed topology. However, the front-end converter is not considered for the cost comparison because the front-end converter is most required and common to all the topologies for voltage regulation. For example, the conventional CHB topology needs two sets of voltage regulations to generate a five-level stepped voltage waveform likewise other topologies also require the front-end regulation circuits. It is here worth mentioning that the required number of front end dc/dc converters depends on the dc source, so, the proposed topology required two dc sources to generate the 25 L as compared to other topologies.

Table 4. Comparison of proposed topology and other recent MLI topologies [27–30].

Topologies	N_{Level}	$N_{Switches}$	N_{Diode}	N_{Driver}	M_{Block}	T_{Block}	Efficiency (%)	Voltage THD (%)
Proposed	9	7	3	7	$4V_{dc}$	$20V_{dc}$	94.50%	9.07%
	17	8	4	8	$8V_{dc}$	$44V_{dc}$	94.76%	4.76%
	25	10	4	10	$10V_{dc}$	$66V_{dc}$	95.10%	3.10%
[12]	17	10	-	10	$8V_{dc}$	$36V_{dc}$	93.91%	6.17%
[27]	25	10	16	10	$12V_{dc}$	$70V_{dc}$	99.7%	3.25%
[28]	17	8	8	8	$8V_{dc}$	$36V_{dc}$	98.5%	6.8%
[29]	25	14	-	11	$12V_{dc}$	$76V_{dc}$	NA	NA
[30]	17	10	8	10	$8V_{dc}$	$36V_{dc}$	96.7%	5.41%

6. Nearest Level Modulation Technique

The nearest level modulation technique operates in fundamental switching frequency and produces low THD at a higher number of voltage levels [12]. The NLC method $\{x\}$ is rounded to the nearest integer value, where x represents the reference value and the comparing value is half-integer value 0.5, i.e., round (1.6) = 2 and round (1.4) = 1. The half-integer always rounded off to the real integers. Figure 9 shows the simulation output voltage and current waveforms. Figure 10 shows the schematic pulse generation using the NLC method. In conventional NLC the output voltage error is $0.5 V_{dc}$ whereas in proposed NLC the output voltage error is minimized to $0.4 V_{dc}$ as given in Equation (46) and the output voltage RMS is higher than the conventional NLC.

$$\theta = \sin^{-1} \left(\frac{2(i - 0.6)}{N_{Level} - 1} \right) \quad (46)$$

where, $i = 1, 2, \dots, N_{Level} - 1/2$.

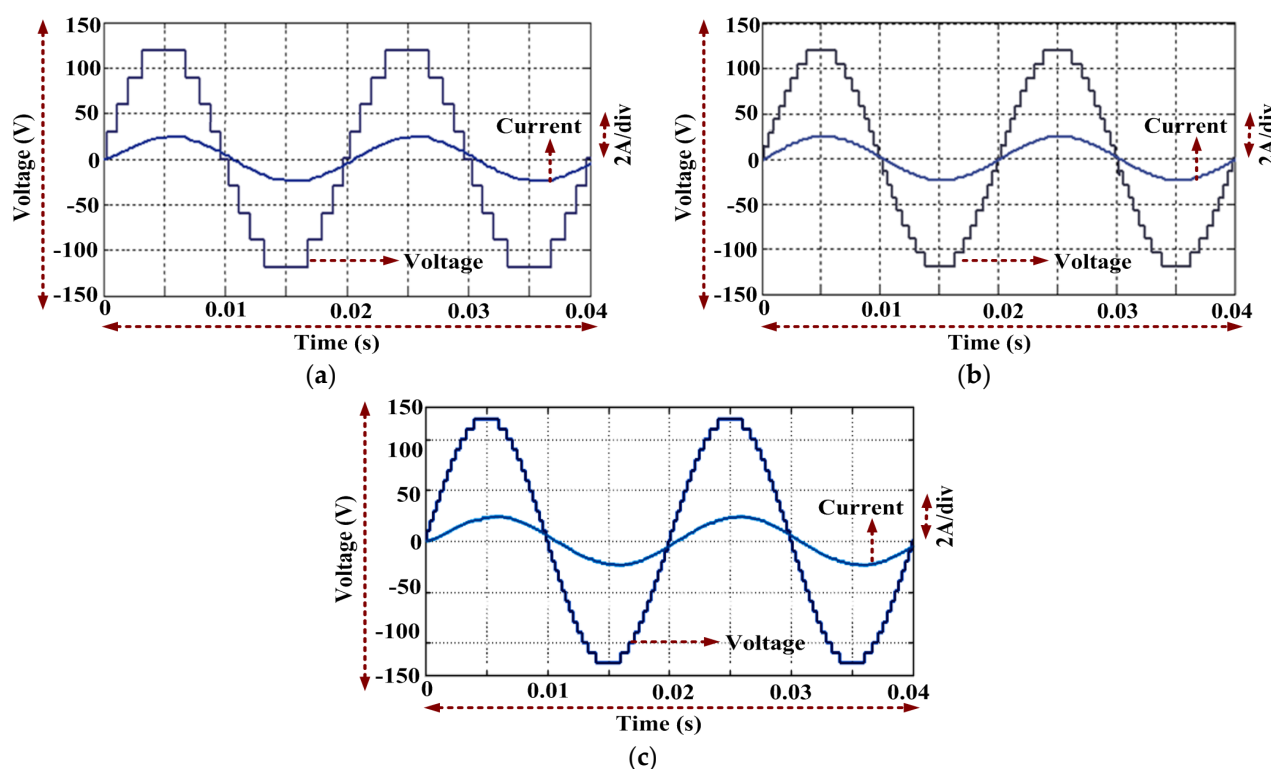


Figure 9. Simulation output voltage and current waveform results (a) 9-Level, (b) 17-Level, (c) 25-Level.

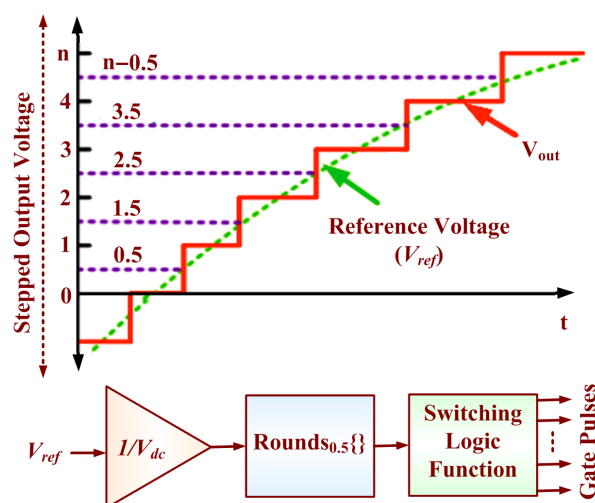


Figure 10. Nearest Level Modulation Technique (a) Stepped voltage waveform and (b) schematic block diagram.

7. Experimental Test Results

The experimental results for a 9-level symmetric topology, 17-level asymmetric topology, and 25-level of the cascaded structure based on the first and the second algorithm at $n = 1$ and $k = 2$, respectively, are presented. In the experimental setup, IGBTs (BUP400D), and IGBT drivers (HCPL316j) are used. A resistive-inductive (RL) load with $R = 100 \, \Omega$ and $L = 65 \, \text{mH}$ is used. The prototype of the proposed inverter is shown in Figure 11. The fundamental switching method [18] is implemented via the FPGA 3E Spartan controller. The obtained experimental results for 9-level, 17 level, and 25 levels are shown in Figure 12a–c, respectively.

FPGA and Power Circuit

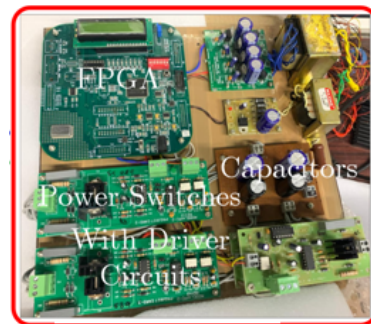


Figure 11. Experimental setup of proposed converter.

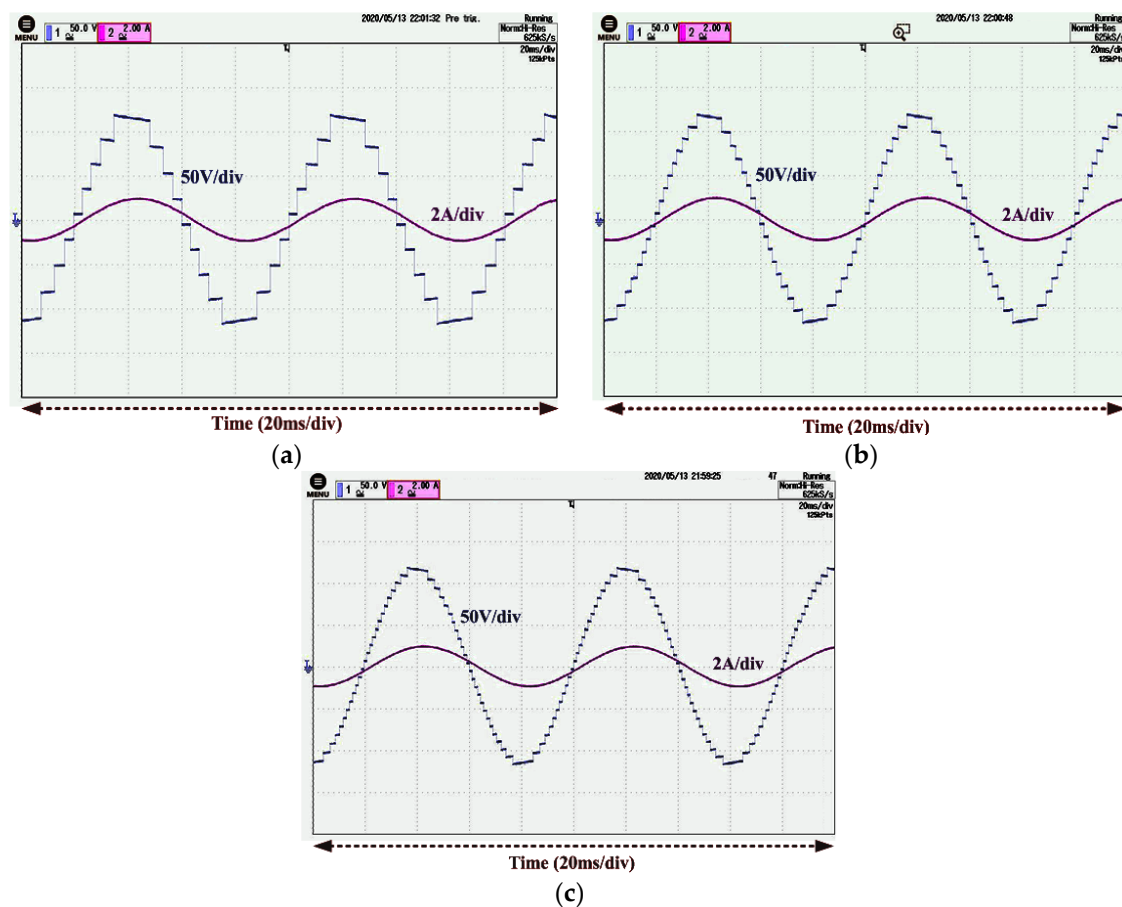


Figure 12. Experimental output voltage and current waveform results (a) 9-Level, (b) 17-Level, (c) 25-Level.

7.1. Symmetric Topology for 9-Level Inverter

Two modules ($n = 2$) are used with dc source values of 60 volts ($V_1 = V_2 = 60$ V) and the voltage across each capacitor equals 30 V to generate the 9-level output voltage waveform in the symmetric configuration. The c output voltage and current waveform with modulation index ($M_a = 1$) are shown in Figure 12a. To balance the voltage across the capacitors, a voltage balancing circuit that was presented in [23,26] was used. The output frequency is 50Hz with a peak magnitude of 120 V. The maximum blocking voltage across the full-bridge inverter switches is 120 V. The output voltage levels are 0, ± 30 V, ± 60 , ± 90 V, and ± 120 V. The blocking voltages of the switches are $S_{12} = S_{22} = 30$ V, $S_{11} = S_{21} = 60$ V, and $F_{11} = F_{12} = F_{13} = F_{14} = 120$ V for the full-bridge switches. The voltage and current total harmonic distortion (THD) are measured as 9.07% and 2.79%, respectively. Due to

the presence of the unidirectional device (diode) the circuit will operate in two- quadrants. Further, the maximum allowable power factor is 0.97 to unity power factor and it is not suitable for high inductive load applications.

7.2. Asymmetric Topology for 17-Level Inverter

For the proposed asymmetric structure, the dc voltage source magnitudes are given as $V_{11} = V_{12} = 15$ V, and $V_{21} = V_{22} = 45$ V for the 17-level with a maximum output voltage ($V_{o,max}$) of 120 V. The experimental output voltage waveform is shown in Figure 12b. Two modules ($n = 2$) are used with eight switches. The maximum blocking voltage of the switches in the module is 30 V and 60 V, respectively, and is 120 V for the full bridge. The output voltage levels are 0, ± 15 V, ± 30 V, ± 45 V ... ± 120 V, respectively. The voltage and current THD values are measured as 4.76% and 1.45%, respectively.

7.3. Cascaded Asymmetric Structure for 25-Level Inverter

In the cascaded structure, the first and second algorithms result in the same output voltage when $n = 1$ for the k th unit. In the experimental structure of this work, the MLI is designed for $n = 1$ and $k = 2$. The magnitudes of the dc sources are $V_{11} = V_{12} = 10$ V for the first unit and $V_{21} = V_{22} = 50$ V for the second unit. $V_{o,max}$ equals 20 V and 100 V for the first and second units, respectively. The output voltage and current waveforms for the 25-level are shown in Figure 12c with voltage and current THD values measured as 3.10% and 1.24%, respectively. A comparison of the proposed topologies is given in Table 5. As shown, the cascaded DHB topology requires low blocking voltage and generates a higher number of output voltage levels. In Table 6, the various parameters of the proposed topology with different configurations are compared. Moreover, the dynamic performance of the proposed topology was tested in both simulation and experimental setup.

Table 5. Comparison of the proposed symmetric, asymmetric, and cascaded Configuration.

Description	Symmetric	Asymmetric	Cascaded
V_{Block} in volts	120	120	100
Number of switches	8	8	10
Number of driver circuit	8	8	10
Variety of dc source	1	2	2
$N_{source}/N_{capacitors}$	2/4	2/4	2/4
Number of levels	9	17	25
Voltage THD (%)	Experimental	4.76%	3.10%
	Simulation	4.69%	2.97%

Table 6. Comparison of proposed topology for various output voltage levels for same power rating.

Number	N_{switch}	V_{Block} (V)	N_{Level}	T_{Block} (V)	$N_{source}/N_{capacitor}$	N_{Sub}	η (%)
1	6	2	5	11	1/2	1	88.12
2	8	4	9	22	2/4	1	88.9
3	8	8	17	44	2/4	1	89.46
4	12	10	25	66	2/4	2	89.97
5	14	34	85	231	3/6	2	90.11
6	14	40	85	231	3/6	2	90.37
7	18	50	125	341	3/6	3	90.23

As shown in Figure 13a for the proposed 25-level topology, it was verified by varying the modulation index. This confirmed that the proposed topology can adjust the load voltage based on the load demand. The experimentally observed voltages across the switches are shown in Figure 13b,c. From the cascaded structure, the first and second unit of switches $S_{1,1}$, $S_{2,1}$, $F_{1,1}$, $F_{1,2}$, $F_{2,2}$ and $F_{2,4}$ shown in Figure 13b,c. As shown, it was validated that the maximum blocking voltage across the switch is 100 V. The experimental

performance of the proposed 25-level was tested in the hardware setup by varying the load as shown in Figure 13d. The maximum output voltage was 120 V with a load varying from 0.9 A to 2.2 A ($Z = 100 \Omega + j 60 \Omega$ to $Z = 50 \Omega + j 30 \Omega$). However, the proposed topology is more suitable to operate near the unity power factor due to each module can carry only a positive current due to the presence of the diode. Once again it was proved that the proposed converters are more suitable for distributed- power generation. It should be mentioned that the series-connected dc-link capacitor voltages are balanced using the voltage-divider circuits presented in Figure 14 and this external circuit ensures the balanced capacitor voltages for both high and low switched cells. The circuit in Figure 14a is used for regulated dc sources whilst that in Figure 14b can be used for the unregulated dc sources (like photovoltaic as a source). The experimental balanced output voltage for the second full-bridge inverter is shown in Figure 14c. However, by adding a new dc/dc converter, an extra power conversion stage will be added, but it is here worth mentioning that the overall efficiency will be slightly less than the inverter efficiency. The additional converter is a non-isolated type which introduces the EMI effect during the high duty cycle. The efficiency (η) of the proposed topologies in terms of the number of SMLIs (N_{Sub}), blocking voltage, and switches is listed in Table 5.

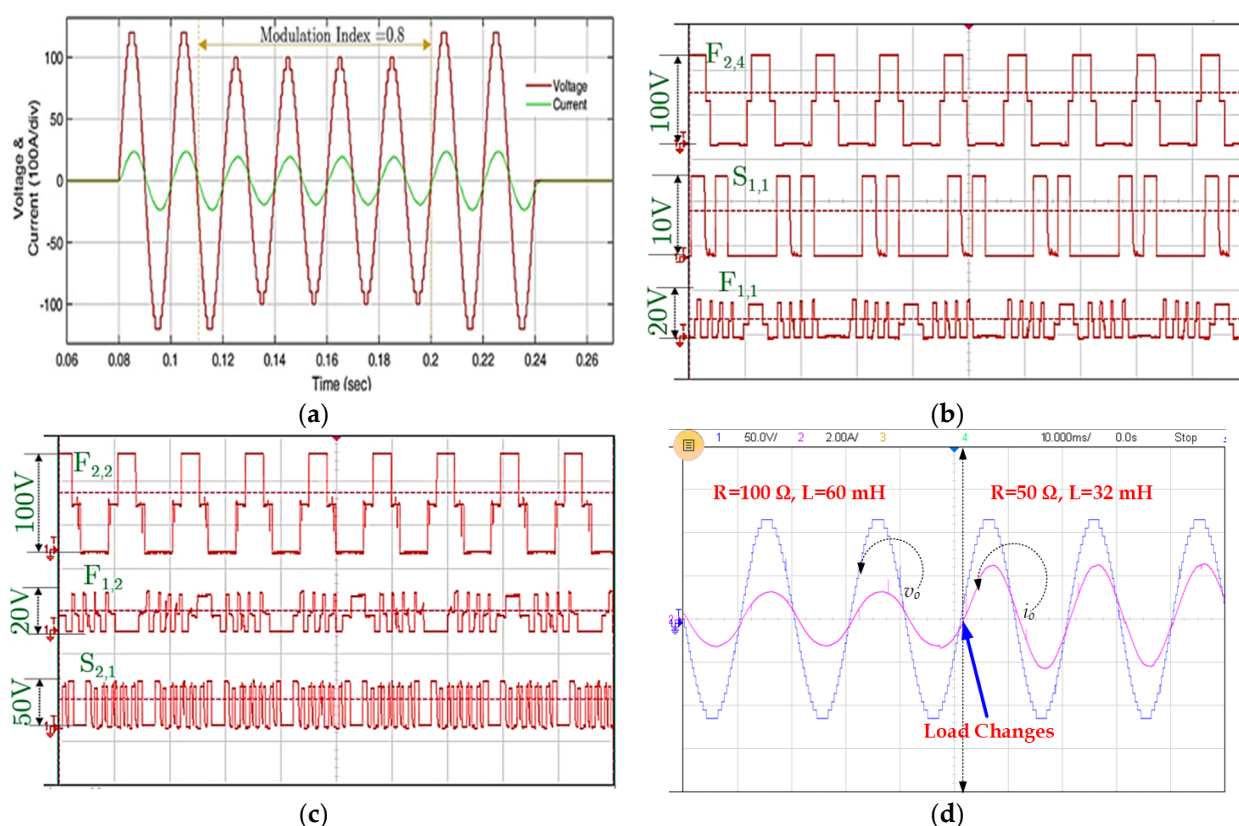


Figure 13. Performance assessment (a) Simulation results for various modulation (b) Experimental blocking voltage of switches $F_{2,1}$, $S_{1,1}$ and $F_{1,1}$ (c) Experimental blocking voltage of switches $F_{2,2}$, $F_{1,2}$, and $S_{2,1}$, (d) Experimental dynamic performance of the proposed 25-Level converter.

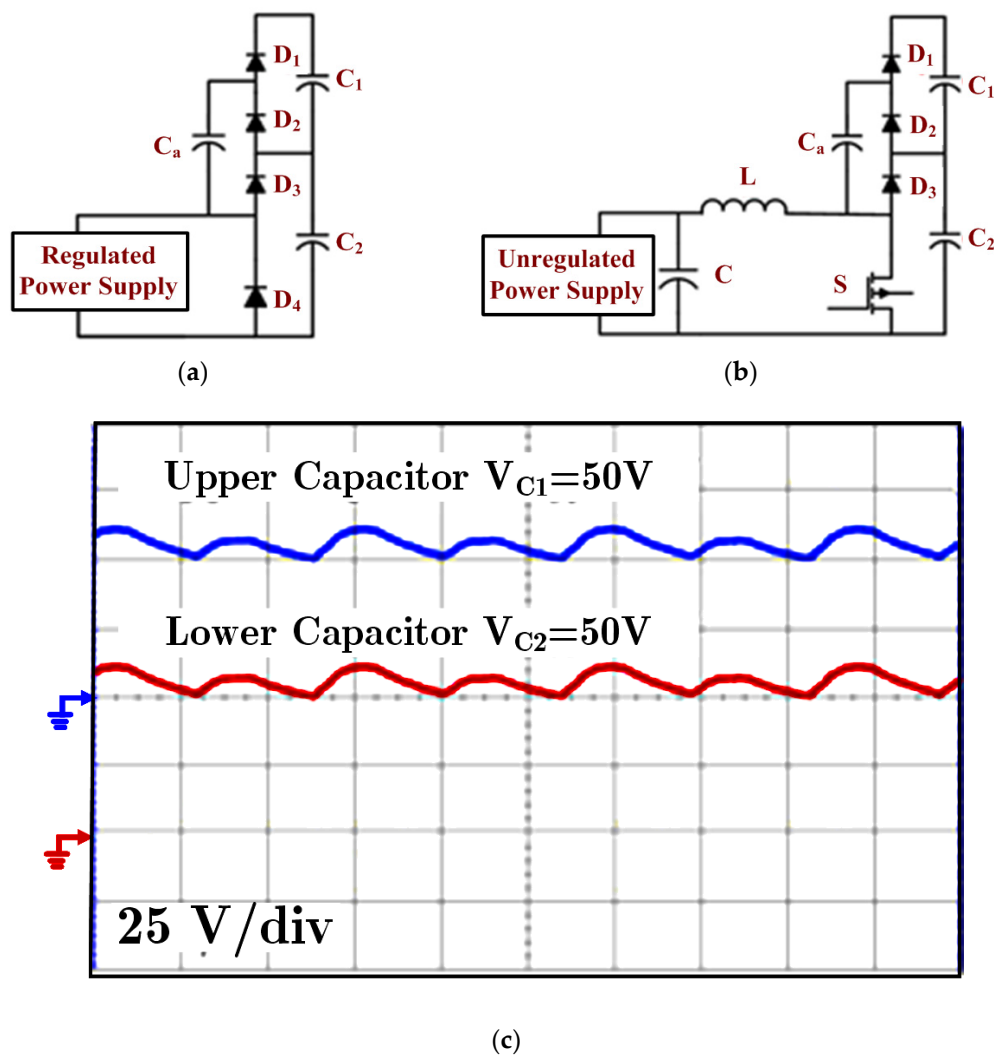


Figure 14. Circuit diagram of the voltage divider (a) For regulated dc sources, (b) For unregulated dc sources, (c) Capacitors' balanced waveforms for the 25-Level: second unit.

In Table 6, for the 85-level, two possible combinations are presented: (i) $n = 2$ with $k = 1$, and $n = 1$ with $k = 2$, which requires a maximum blocking voltage of 34 V in the second SMLI, and (ii) $n = 1$ with $k = 1$ and $n = 2$ with $k = 2$ with maximum blocking voltage of 40 V is required. Additionally, the various power loss across each device and efficiency (η) are presented in Figure 15a–c, respectively. The major loss depends on the switching scheme of the converter. The fundamental switching methods were used because of their low switching losses. As is obvious, the percentage of losses is low when the output power is high.

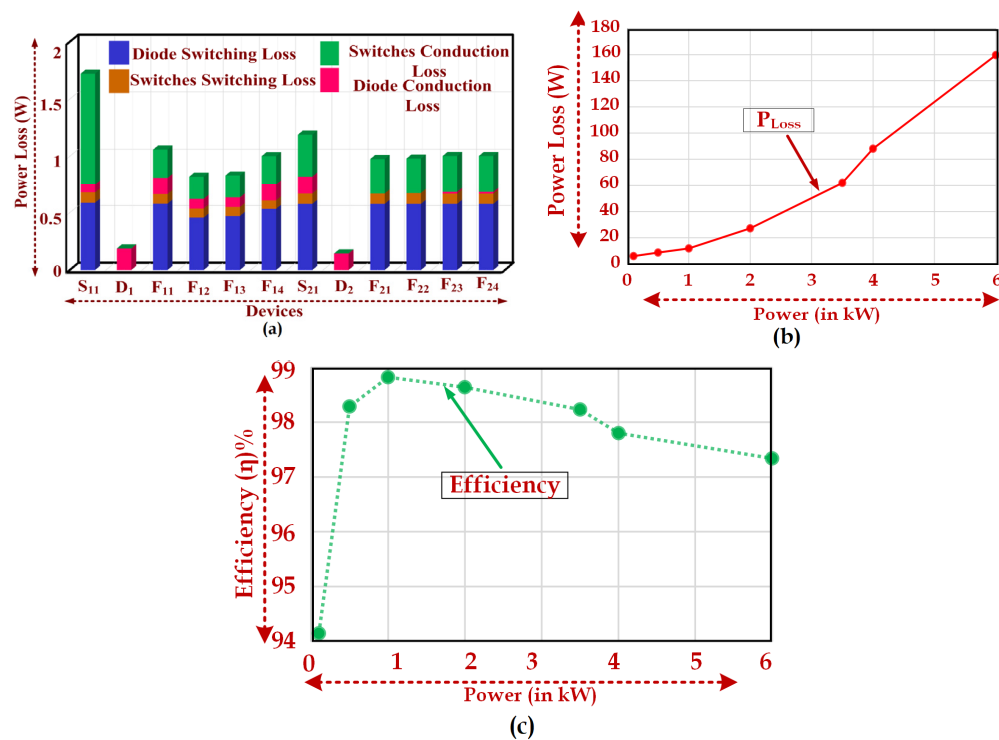


Figure 15. Plots (a) Various power loss for each device (b) Power loss versus power, (c) efficiency versus power.

8. Conclusions

A new cascaded diode half-bridge multilevel inverter topology is presented in symmetric, asymmetric, and cascaded structures. The symmetric topology is verified at 9-level output voltage and the results confirm the feasibility of the proposed topology. Similarly, asymmetric and cascaded topologies are verified for 17 L and 25 L. However, these topologies limit the high blocking voltage on the full bridge switches. Accordingly, a cascaded structure is proposed to reduce the blocking voltage and generate a higher number of output voltage levels. The cascaded topology is optimized for various parameters, and the results are compared with existing topologies. The prototype model was developed and tested for 130 W. The simulation and experimental results, as well as the comparative study, validate the robustness and effectiveness of the proposed cascaded topology in terms of the reduced power loss, cost, and the number of power electronic components. The maximum simulation efficiency of 98.6% is archived at ~130 W. Finally, the proposed converter is more suitable for distributed-power generation.

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