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A Curvature Compensation Technique for Low-Voltage Bandgap Reference

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Abstract: Based on the standard 40 nm Complementary Metal Oxide Semiconductor (CMOS) process, a curvature compensation technique is proposed. Two low-voltage, low-power, high-precision bandgap voltage reference circuits are designed at a 1.2 V power supply. By adding IPTAT (positive temperature coefficient current) and ICTAT (negative temperature coefficient current) to the output resistance, the first-order compensation bandgap voltages can be obtained. Meanwhile, the third high-order compensation current is also superimposed on the same resistance. We make use of the collector current of the bipolar transistor to compensate for the nonlinear term of V_{BE}. The simulation results show that TC (temperature coefficient) of the first circuit reference could be reduced from 29.1 × 10^{-6}/°C to 5.71 × 10^{-6}/°C over the temperature range of −25 to 125 °C after temperature compensation. The second one could be reduced from 17 × 10^{-6}/°C to 5.22 × 10^{-6}/°C.

Keywords: bandgap reference; curvature compensation; nonlinear current

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1. Introduction

Reference voltage source circuit is an important unit module in integrated circuit design, which is widely used in analog integrated circuits, digital integrated circuits, and hybrid integrated circuits. The ideal voltage reference has some requirements are as follows:

(1) Insensitive to temperature change;
(2) Insensitive to power fluctuations;
(3) Wide range of supply voltage;
(4) Adjustable output voltage;
(5) Low voltage and low power consumption.

Due to the advantages in the above aspects, the bandgap reference (BGR) is the mainstream reference source circuit at present. Nowadays, with the feature size of the integrated circuit is getting lower and lower, low-voltage, low power consumption, and high-precision bandgap reference circuits are necessary and have received widespread attention.

Many works [1–3] can achieve a high-precision reference voltage. Due to the limitation of the common-collector structure of the bipolar junction transistor, the reference voltage is higher than 1.2 V, and the minimum supply voltage must be higher than 1.4 V as well. To reduce the system voltage, researchers put forward various methods. H. Banba proposed the current mode structure [4] that could convert the sum of two currents to voltages, generate a temperature-independent reference, and also provide a practical pattern for the later low-voltage reference circuit.

The structure in the work of [5–8] achieves a sub-1 V voltage using the idea of [4]. K. J. Singh replaced the resistors of conventional bandgap voltage reference circuits with a stack of Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) [9], thus resulting

in the improvement in the area and low voltage. [10] CTAT voltage was divided, and PTAT voltage was multiplied to operate with a low input voltage. It was proposed that the circuit can generate a 0.8 V.

The temperature drift of the reference voltage has been another challenge in recent years. In order to reduce the temperature coefficient and improve the precision, many curvature compensation techniques have been presented. An exponential curvature compensation technique has been presented in the work of [11] by exploiting the temperature characteristics of the current gain ß of Bipolar Junction Transistors (BJTs). β changes with the temperature index, so a current that has a nonlinear relationship with the temperature can be obtained to compensate for the nonlinear term of the bandgap reference. However, the compensation in this work can only be applied for convex curves and is not suitable for concave curves. A piecewise-linear compensation was proposed in the work of [12]. The author divided the reference voltage curve into several parts within the whole temperature range and made a piecewise compensation for each part. In [13], a smoother reference voltage curve can be obtained by the superposition of two complementary reference voltages curves. The two paper have satisfactory compensation effects but double the layout area. Different kinds of resistors [14] have been incorporated into the compensation, aiming to cancel the nonlinear temperature dependence of the emitter-base voltage V_{EB}. The method in this work has a high requirement on the type of resistance.

This paper adopted the square curvature compensation technology and designed two reference voltage source circuits. The compensation method in this paper is suitable for both the convex curves and the concave curves. Meanwhile, the simple structure will not waste too much layout area. This circuit only increases 3 μA current on the original basis. The collector current of the transistor was used to perform a nonlinear order compensation to reduce the influences of the nonlinear term on V_{BE}. Compared with the first-order compensation reference voltage source, the power consumption of the new circuit only adds a few microwatts, which greatly reduces the temperature coefficient.

2. Principle of Bandgap Reference

The classical bandgap reference with the current mode structure is shown in Figure 1. The principle is to add two reverse temperature coefficient currents with different weights, getting a zero TC reference current at a certain temperature.

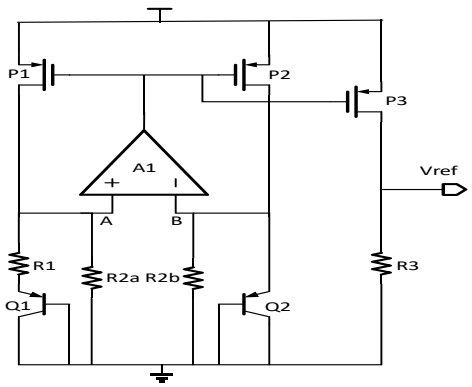


Figure 1. Bandgap reference with current mode structure. P represents PMOSFET; R represents resistance; Q represents transistor.

The base-emitter junction of the PNP tube has a V_{BE}-I_C relationship given by

$$V_{BE} = \frac{kT}{q} \ln \frac{I_C}{I_S} \quad (1)$$

where I_C is the collector current, and the saturation current I_S is proportional to the base-emitter area.

The CTAT current is generated by a single BJT tube [8]. The analytical form of V_{BE} is

$$V_{BE} = V_{g0}\left(1-\frac{T}{T_0}\right)+V_{BE0}\left(\frac{T}{T_0}\right)+\gamma V_T \ln\left(\frac{T}{T_0}\right)+V_T \ln\left(\frac{J_C}{J_{C0}}\right) \quad (2)$$

where T_0 is the reference temperature, V_{g0} is the bandgap voltage of silicon at T_0 and is 1.205 V at absolute temperature 0°, the temperature coefficient γ is approximately equal to 3, and J_C is collector current density of PNP.

The relationship between J_C and temperature can be expressed as

$$J_C = J_{C0}\left(\frac{T}{T_0}\right)^{\alpha} \quad (3)$$

Bring (3) into the previous Formula (2) to obtain the final expression of V_{BE}

$$V_{BE} = V_{g0}-(V_{g0}-V_{BE0})\frac{T}{T_0}+(\gamma-\alpha)V_T \ln\left(\frac{T}{T_0}\right) \quad (4)$$

where α is the order of the temperature behavior of the current.

In Equation (4), when V_{BE0} is approximately equal to 750 mV, T is 300 K, the value can be obtained by first-order partial derivative of V_{BE} to temperature and is about -1.5 mV/°C. The voltage is negatively correlated with temperature.

In the structure in Figure 1, nodes A and B are forced to be at equal potential because of the feedback loop from the operational amplifier A1. So the CTAT current flowing in R_{2a} is equal to the current flowing in R_{2b}, which can be described as

$$I_{CTAT} = \frac{V_{BE2}}{R_{2b}} \quad (5)$$

The PTAT current flowing through resistance R_1 can be described as

$$I_{PTAT} = \frac{\Delta V_{BE}}{R_1} = \frac{V_{BE1}-V_{BE2}}{R_1} = \frac{V_T}{R_1}\ln\frac{I_1}{I_2} = \frac{kT}{qR_1}\ln N \quad (6)$$

The first derivative of I_{PTAT} with respect to temperature can be obtained and is about $(0.086 \times \ln N)/R_1$ mV/°C. N is the ratio of the emitter area of two bipolar transistors generating positive TC voltage, and the voltage is proportional to temperature.

The low-voltage reference is generated by the sum of two currents, I_{PTAT} and I_{CTAT}, multiplied by the output resistor. I_{PTAT} is produced from ΔV_{BE}, and I_{CTAT} is produced from V_{BE}. The sum of I_{PTAT} and I_{CTAT} are copied from current mirrors P_1, P_2, and P_3 to the output resistor. The first-order reference voltage is written as

$$V_{REF} = R_3\left(\frac{V_{BE2}}{R_{2b}}+\frac{kT}{qR_1}\ln N\right) \quad (7)$$

N is the ratio of the emitter area of two bipolar transistors generating positive TC voltage. k is the Boltzmann constant, and q is the electric charger. V_{REF} in this structure is adjustable. This structure is suitable for low voltage.

The Formulas (4)–(7) show that ΔV_{BE} can only compensate for the linear term in V_{BE}, but the high-order term cannot be compensated. So the temperature coefficient of the bandgap source after first-order compensation will not be small, especially in low-voltage structure, the voltage deviation will be amplified, and we will obtain a worse temperature coefficient, usually more than 30×10^{-6}/°C. So other compensation ways are needed to obtain higher precision reference voltage.

A high-order compensation method was proposed in this article, and the principle is shown in Figure 2. The low-voltage reference is generated by three currents, namely, I_{PTAT}, I_{CTAT}, and I_{NL}, that are multiplied by the output resistor. I_{PTAT} is produced from ΔV_{BE},

and I_{CTAT} is produced from V_{BE}. The sum of these two opposite TC currents can present two typical curves, a convex curve, and a concave curve. The nonlinear compensation current I_{NL} from a nano-ampere curvature compensation module is to make a proper temperature compensation for different curvature curves, as illustrated in Figure 2. When the reference current forms a convex curve, the second derivative of its nonlinear term is less than zero. A current I^2_{PTAT} that is proportional to the square of temperature can make the compensation. By contrast, if the reference current forms a concave curve, the second derivative of its nonlinear term is greater than zero. The current $-I^2_{PTAT}$ that is inversely proportional to the square of temperature can make the compensation.

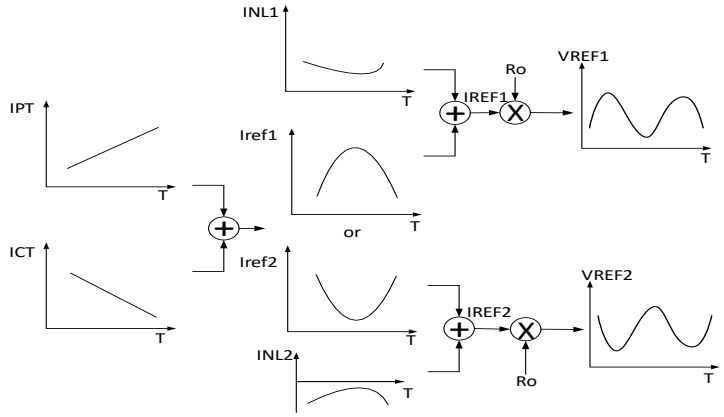


Figure 2. Square curvature compensation principle. IPT represents IPTAT; ICT represents ICTAT; Iref1,2 represent two typical current curves after first-order temperature compensation; INL1,2 represent two non-linear compensation current; Vref1,2 represent reference voltage after high-order temperature compensation.

After curvature compensation, we can obtain output reference current I_{REF} with:

$$I_{REF} = I_{g0} + k_1 T - k_2 T - k_3 T^2 + I_{NL} \quad (8)$$

Nonlinear compensation terms can be generated in different ways. In [11], I_{NL} is generated by the current difference between I_{PTTAT} and I_{VBE}, and the compensation current opens only at high temperatures. This reference circuit achieved a temperature drift of less than 20 ppm/°C at the temperature range of −15 to 90 °C. In [15], I_{NL} is generated by the base current of the bipolar transistor. However, the compensation is only used for convex curves.

3. Circuit Design

Two proposed low-voltage, high-precision bandgap circuit designs are shown in Figures 3 and 4. The two circuit structures are slightly different in the high-order compensation circuit. Theoretically, the second-order derivative of the nonlinear part of V_{BE} voltage is less than zero, and we obtain a downward V-T curve. However, in fact, because of the differences in current mirrors, bipolar transistors, op amps, or bias circuits, the second derivative of the nonlinear term of V_{REF} may be greater than zero, and the V-T curve may open upward [16,17]. In the second case, we need to reverse I_{NL} to compensate.

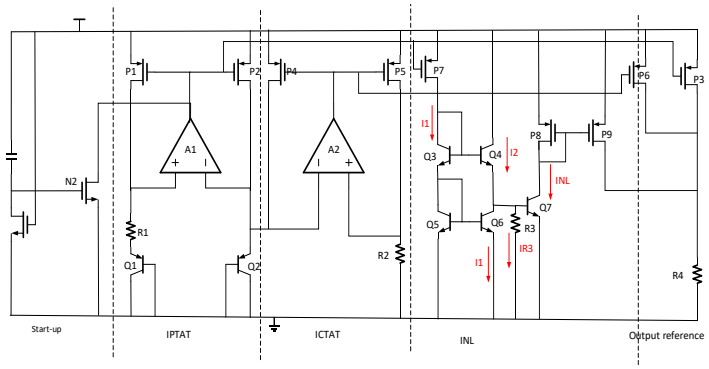


Figure 3. Proposed the first bandgap reference.

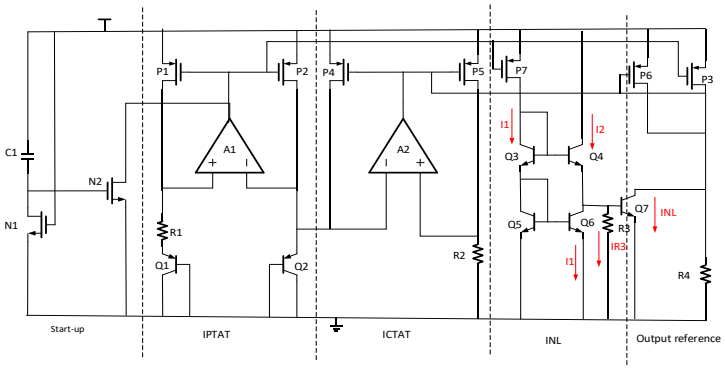


Figure 4. Proposed the second bandgap reference.

3.1. Start-Up Circuit

The purpose is to prevent the degenerate state that the output of the op-amp is high and the input is low. The degenerate state makes the circuit unable to work normally, and the output keeps a low level for a long time. Furthermore, the essence of the degeneracy state is a metastable state and requires an external force to break the balance. The start-up circuit is such an external force. When the circuit works normally, the start-up circuit must be disconnected to keep the circuit stable. On the other hand, the start-up circuit designed in this paper is very simple in a structure consisting of only two MOSFETs and one capacitor. Due to the capacitor characteristics, when it is just powered on, the gate of N_2 is high. After it is turned on, the gate voltage of P_1 and P_2 can be pulled down, and the two inputs of A_1 and A_2 amplifiers can be pulled up at the same time so that the circuit is out of degeneration. The gate of N_1 connects to the power supply in a continuous conduction state, which can provide a discharge path for the C_1 capacitor. After the discharge is completed, the gate of N_2 is pulled down, and the start-up circuit disconnects. Considering the low-voltage structure, $M_{3,4,9,}$ and M_{10} can work in the subthreshold region.

3.2. Operational Amplifier Design

The operational amplifier designed in this circuit is displayed in Figure 5, and it is a folded-cascode amplifier. The operational amplifiers in bandgap reference circuits are used to generate positive temperature currents by clamping the transistor base-emitter voltage, and two-stage structures are frequently applied. On the contrary, the current mirror connected to the two-stage amplifier output is equivalent to a common source stage, and the three-stage structure will bring some problems to the stability of the whole bandgap circuit. The one-stage operational amplifier can bring favorable effects on circuit stability, while insufficient gain will result in larger system offset voltage, which is out of the designer's expectations. For the advantages in sufficient gain, large output voltage swing, and suitable stability, the folded-cascode amplifier was used in our circuit.

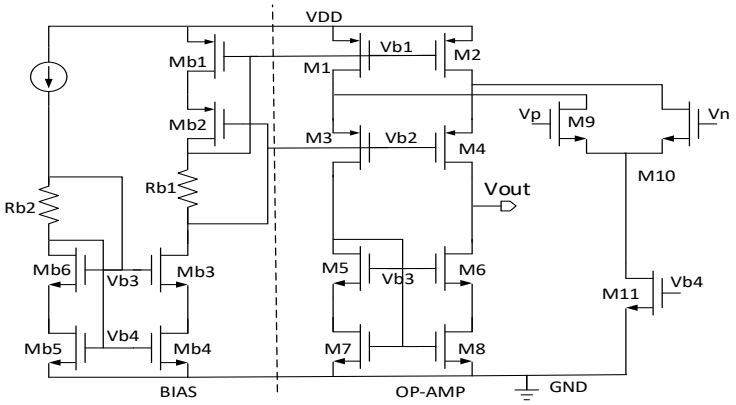


Figure 5. Operational amplifier design. M1–11, b1–b6 are MOSFETs; vb1–4 are bias voltage; vp, vn are inputs.

Under the same conditions, the mobility of N-Metal-Oxide-Semiconductor (NMOS) is higher than that of P-Metal-Oxide-Semiconductor (PMOS), which is conducive to improving the response speed, and then M9, M10 are used as NMOS differential input pairs that also match the emitter-base voltage of transistor Q2 better. In the temperature range of −25 to 125 °C, the voltage of Vp and Vn will vary from 0.65 to 0.8V, and the threshold of NMOS and PMOS transistor is V_{thn} = 0.65 V and V_{thp} = −0.75 V, respectively, in this process. If PMOSFETs are used as the differential input pairs, the current mirror M11 will be forced into the linear region. In Figure 5, M1 and M2 provide the bias current of the input device. M3, M4, M9, and M10 form a cascode device. M5, M6, M7, and M8 are the load tubes, which affect the output impedance.

The gain of the cascode operational amplifier can be approximately expressed as:

$$A = g_{m9,10}\{[(g_{m4} + g_{mb4})r_{o4}(r_{o10}||r_{o2})][(g_{m6} + g_{mb6})r_{o6}r_{o8}]\} \quad (9)$$

where g_{mi} is the transconductance of M_i, r_o is the output resistance.

The loop gain and phase simulation is shown in Figure 6. The proposed operational amplifier has a DC loop gain of 63.6 dB and a phase margin of 60 degrees at 1.2 V supply voltage.

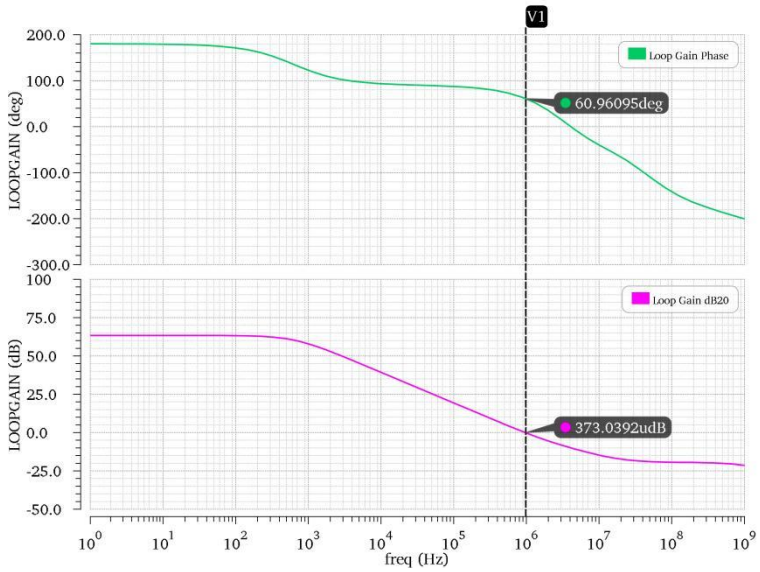


Figure 6. Simulated loop response in Figure 5: Phase response and gain response (VDD = 1.2 V).

3.3. First-Order Temperature Compensation Circuit

The first-order temperature compensation circuit is slightly modified on the basis of the Banba structure, separating the positive temperature current generating circuit and the negative temperature current generating circuit. The purpose is to obtain separate PTAT current preparing for high-order temperature compensation. The PTAT and CTAT current generating circuits are symmetrical in structures. The obtained current flows through the output resistance by two sets of current mirrors. When the proportional relationship between R_1 and R_2 is adjusted reasonably, we can obtain nice first-order temperature compensation. The principle of temperature compensation has been explained in detail in Section 2, and I will not repeat it here. In this circuit structure, we choose N = 8. After calculation and further simulation, the ratio of R_1 and R_2 can be trimmed.

After first-order temperature compensation, the output voltage can be expressed as:

$$V_{REF} = R_4\left(\frac{V_{BE2}}{R_2} + \frac{kT}{qR_1}\ln N\right) \tag{10}$$

The simulation of temperature coefficient at the range of −25–125 °C after first-order temperature compensation was shown in Figures 6–9.

3.4. High-Order Temperature Compensation Circuit

The high-order temperature compensation circuit in Figure 3 is composed of a resistor, five Negative-Positive-Negative (NPN) bipolar transistors, and three PMOSFETs; two PMOSFETs were removed from the circuit in Figure 4 in order to obtain the opposite compensation.

Take circuit in Figure 3 as an example. According to Kirchhoff's voltage law, $V_{BE,Q7}$ can be expressed as:

$$V_{BE,Q7} = V_{BE,Q5} + V_{BE,Q3} + V_{BE,Q4} \tag{11}$$

Collector currents of Q_3, Q_5, Q_6 copied from the current mirror are positive to temperature change (I_{PTAT}). The current flowing through R_3 is inversely proportional to the temperature (I_{CTAT}):

$$I_{R3} = \frac{V_{BE7}}{R_3} \tag{12}$$

The current flowing into Q_4 is calculated as:

$$I_{Q,4} = I_{Q,6} + I_{R,3} \tag{13}$$

We assumed that each BJT has the same size, substituting the base-emitter voltage from (1) and current Formulas (12) and (13) into Equation (11), we can obtain the following expression:

$$V_T \ln \frac{I_{NL}(I_{PTAT} + I_{CTAT})}{I_{PTAT} \times I_{CTAT}} = 0 \tag{14}$$

From Equation (14), we can obtain the current flowing in Q7:

$$I_{NL} = \frac{I^2{}_{PTAT}}{I_{PTAT} + I_{CTAT}} \tag{15}$$

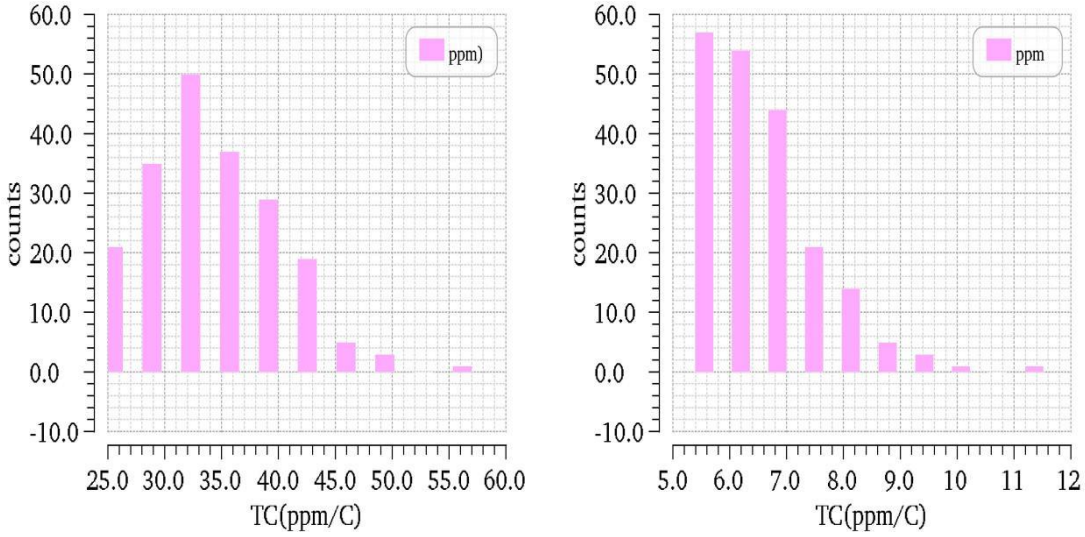
In order to make the TC of I_{NL} proportional to the square of the temperature, the denominator of formula (14) must be independent of temperature. We can adjust the ratio coefficient of R_3, R_2 to meet the requirements.

$$\frac{\partial V_{BE7}}{\partial T}\frac{1}{R_3} + \frac{k\ln N}{qR_2} = 0 \tag{16}$$

The output of the proposed design in Figures 2 and 3 can be expressed in the form of

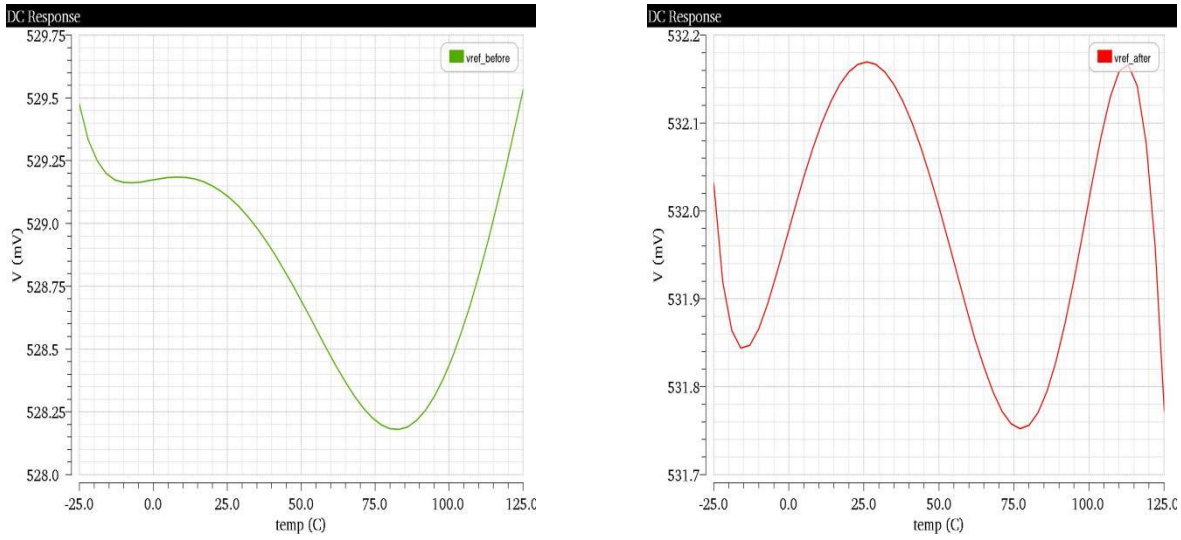
$$V_{REF} = R_4 \times \left(\frac{V_{BE2}}{R_2} + \frac{kT}{qR_1} \ln N + I_{NL} \right) \quad (17)$$

where the nonlinearities created by V_{BE} can be compensated by I_{NL}, which is given in Equation (15). In Figure 4, we reverse I_C and compensate for the high-order term of V_{REF}, whose second derivative is positive.



(**a**) (**b**)

Figure 7. In reference 1 (**a**) 200 Monte Carlo simulation results for TC after first-order temperature compensation; (**b**) 200 Monte Carlo simulation results for TC after high-order temperature compensation.



(**a**) (**b**)

Figure 8. In reference 2 (**a**) V-T curve after first-order temperature compensation; (**b**) V-T curve after high-order temperature compensation.

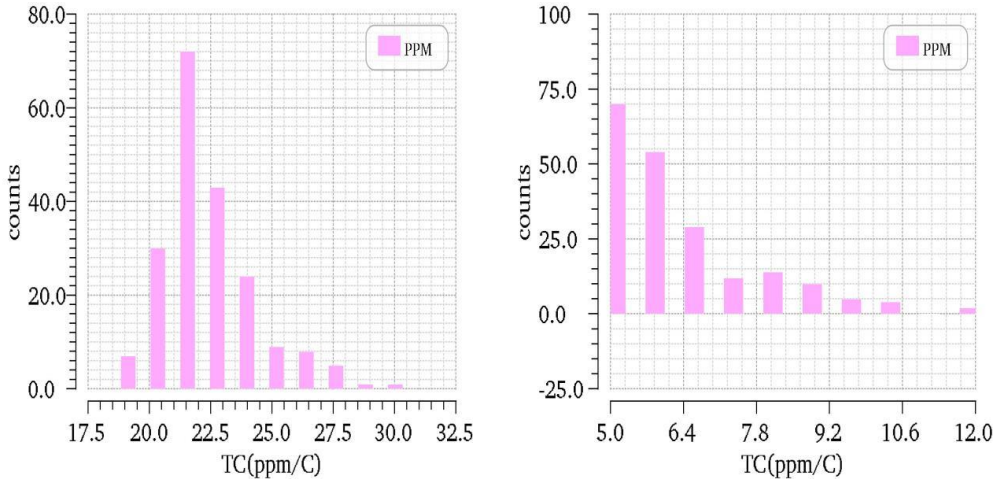


Figure 9. In reference 2 (**a**) 200 Monte Carlo simulation results for TC after first-order temperature compensation; (**b**) 200 Monte Carlo simulation results for TC after high-order temperature compensation.

4. Simulation Results

The simulation was carried out in candence software under the standard 40 nm CMOS process technology. The V-T curve of the structure in Figure 2 is exhibited in Figure 6. In a typical model, the power supply voltage is set to 1.2 V, the output voltage in reference 1 is 523 mV. When the temperature changes within the range of −25–125 °C, TC is 29.1 × 10^{-6}/°C after the first-order compensation and is 5.71 × 10^{-6}/°C after the second-order compensation. After the second-order compensation, the circuit power consumption only increases by a few microwatts and is only 30 uw, which meets the requirements of low voltage, low power consumption, and high precision. The output voltage in reference 2 is 533 mV. The V-T curve of the structure in Figure 3 is demonstrated in Figure 8. TC is reduced from 17 × 10^{-6}/°C to 5.22 × 10^{-6}/°C. Figures 7 and 9 show 200 Monte Carlo simulation results of the temperature coefficient distribution. The proposed BGR at 1.2 V. Monte Carlo simulation reflects a probability distribution. Therefore, the simulation results of Figures 6 and 8 are important examples of the results of Figures 7 and 9.

Figure 10 plots the output reference voltage with the corresponding supply voltage at different temperatures. The supply voltage changes from 0 to 2 V, at −25, 27 and 125 °C, respectively. The simulation results prove that the BGR has a suitable linear adjustment rate. The minimum power supply voltage is 1V, and in the voltage range from 1 to 2 V, the bandgap reference voltage is stable.

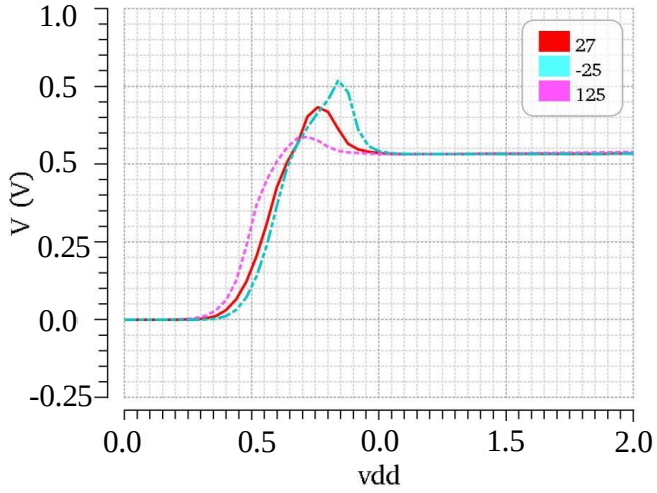


Figure 10. Reference voltage on the supply voltage in different operating temperatures (reference 2).

The simulation results of the bandgap reference voltage of −25 to 125 °C for various supply voltages are shown in Figure 11. The temperature coefficients at 1, 1.2, 1.4, 1.6, 1.8, and 2 V supply voltage are less than $10 \times 10^{-6}/°C$. In particular, the accuracy of BGR is the highest at 1.2 V voltage.

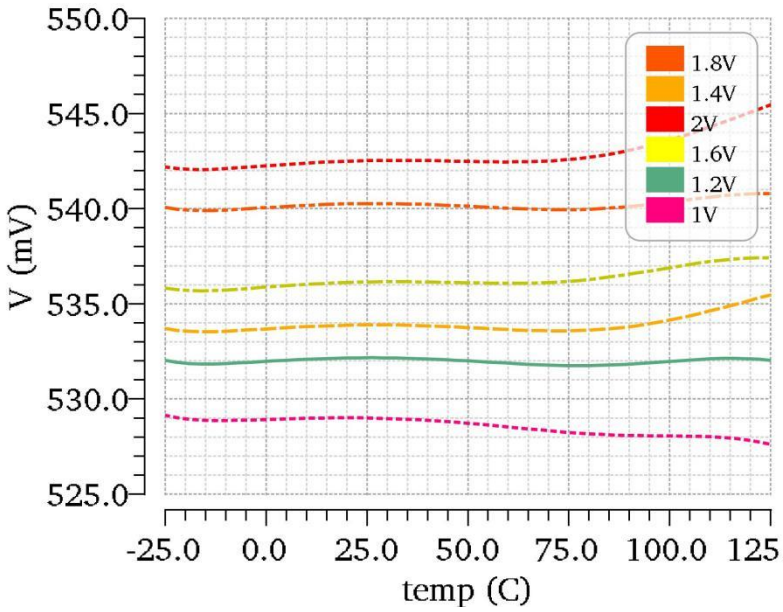


Figure 11. Reference voltage on the operating temperature in different supply voltage (reference 2).

Figure 12 shows that the reference circuit can start up normally in 3 us after the supply is turned on.

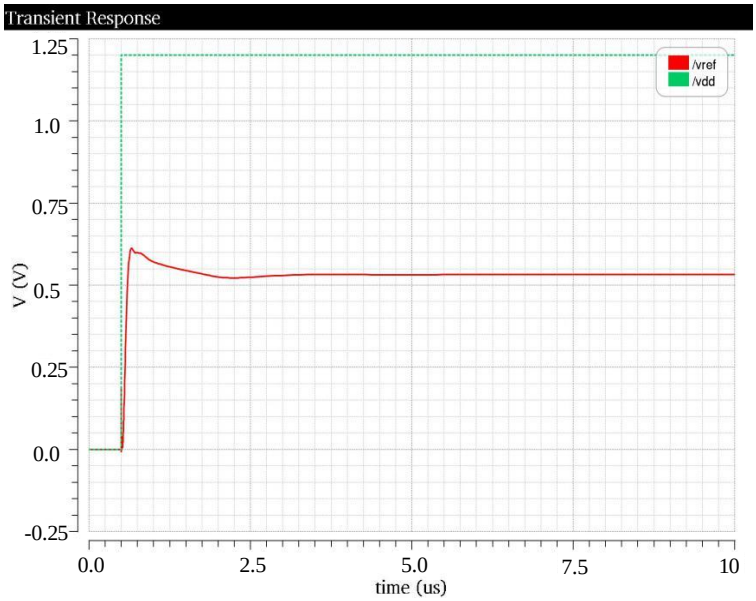


Figure 12. Start-up time (reference 2).

5. Conclusions

In this paper, two bandgap references have been designed and simulated under a standard 40 nm CMOS process at a 1.2 V power supply. On the base of the model in [4], first-order temperature compensation, a second-order temperature compensation circuit is achieved. The collector current of the bipolar transistor can be used to generate exponential curvature compensation. This compensation method has the advantages of

simple principle, suitable compensation effect, and strong applicability and can be used in low-voltage and low-power reference circuits. The simulation result shows that, at 1.2 V voltage, the two BGR achieve suitable TC of 5.71 × 10^{-6}/°C, 5.22 × 10^{-6}/°C when the temperature changes from −25 to 125 °C, and performs well under wide power supply variation. Table 1 lists the comparison of this work with designs reported in the work of [5–8]. Compared with other works, the proposed circuit has less temperature coefficient in a wide temperature range. The bandgap references designed in the paper have suitable properties of low-temperature coefficient and low power consumption, which is suitable for low-voltage, low-power, and high-precision circuits.

Table 1. Comparison of BGR in this article and previous work.

Parameter	5	6	7	8	This Work
Technology	90 nm	60 nm	65 nm	60 nm	40 nm
Supply voltage (V)	1.15	2–5	1.2	0.98	1–2
V_{REF} (mV)	720	389.8	730	603	530
TC (ppm/°C)	10.1	15	9.6	15	5.2
Temp range (°C)	10–80	0–100	−25–100	0–100	−25–125

Author Contributions: J.S. participated in methodology, software, validation, and writing original draft; H.C. participated in conceptualization, funding acquisition, and writing—review and editing; S.N. participated in investigation; and Z.S. participated in funding acquisition and project supervision. All authors have read and agreed to the published version of the manuscript.

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