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Design and Implementation of a New Cuk-Based Step-Up DC–DC Converter

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Abstract: This study proposes a novel modified Cuk converter. The proposed converter attempts to resolve the limitations of the conventional converters, such as voltage gain limitations of a canonical Cuk converter. Therefore, the mentioned improvement has made the proposed converters more compatible for renewable energy applications. Moreover, the increase of the voltage gain in the proposed converter has not impacted the efficiency or the voltage stress of the switches, which is common in other voltage boosting techniques, such as cascading methods. Furthermore, the advantages of a Cuk converter, such as continuity of the input current, have been maintained. The average voltage/current stresses of the semiconductor devices and various types of power losses have been calculated and compared with the existing topologies. Moreover, the non-ideal voltage gain of the proposed converters was compared with the other high step-up topologies. Eventually, the simulation results with PLECS, along with the experiments on an 120 W prototype, have been presented for validation.

Keywords: Cuk converter; modified Cuk converter; non-isolated DC–DC converters

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1. Introduction

A boost DC–DC converter is a DC–DC power converter that owns a continuous input current, one switch and diode, and is capable of increasing its input voltage level with respect to the duty cycle of the switch [1]. Several factors have made it a highly used and popular power electronics device, including its simple structure, low component count, and good efficiency [2]. However, this converter is not capable of providing a high voltage gain ratio [3]. According to the relation of the ideal voltage gain of the mentioned converter, when the duty cycle of the switch reaches the unity, the voltage gain ratio should reach infinity. However, the close value of the duty cycle to unity cannot result in a high value of the voltage gain, considering the parasitic effects in the equation of the voltage gain [4,5]. In other words, the parasitic components of the switches, inductors, and diodes cause different behavior of the voltage gain that swings from a rising region to a maximum point, then down to a falling region [6]. In Figure 1a, the expressed regions and points have been illustrated for the boost converter in 60 W as an example operating point. It is worth noting that the output power of the converter is another factor that affects these regions. In Figure 1b, the voltage gain of the non-ideal mode has been extracted for the different output power values. It can be seen that an increase in output power level decreases the maximum value of the voltage gains. To extract the mentioned figures, the non-ideal parasitic components of the inductors, switches, and diodes were considered, and all describing relations of the inductor voltages were extracted, besides the mentioned components. Consequently, the describing relations of Figure 1 can be extracted. It is

worth noting that the output current of the boost topology is not continuous. Therefore, the output capacitor must supply the load individually during the time interval that the diode is reverse-biased. As a result, the output capacitor must have a high value. Due to this, it is essential to use electrolyte capacitors with high capacitance. However, these capacitors have unavoidable equivalent series resistance (ESR). A high ESR can affect the efficiency. Moreover, such a capacitor's lifespan is shortened by its current stress.

Figure 1. Ideal and non-ideal voltage gains of the boost converter: (a) limits of the boost converter's voltage gain in non-ideal mode, (b) the behavior of the non-ideal voltage gain for different output powers.

The Cuk converter is another basic topology that has overcome some shortages of the boost converter [6]. The continuous input current in boost and Cuk topologies reduces the input filter capacitor value by reducing the input current stress on the capacitor [7]. Cuk topology ensures the continuity of the output current, as well. The voltage gain of the Cuk converter, in a way, allows it to be used for three different types of operation—step-up, step-down, and pass-through. Additionally, the duty cycle determines which mode of operation is used [8,9]. Basically, a Cuk converter operates by storing the input source energy in inductors and then, releasing it to the output. In other words, the energy is not transferred to the output directly. The optimal operation occurs when the stored and released energy are equal, which yields the duty cycle of the switch equivalent to 50 percent. The duty cycle of such a value causes a pass-through mode. Therefore, despite the advantages of Cuk topology, the voltage gain is low and insufficient.

A solution to resolve the low voltage gain can be found in quadratic topologies of DC–DC converters. In [10–14], a group of DC–DC converters has been suggested. A quadratic form of the Cuk's converter voltage gain can be found in all of the above topologies. The suggested topology of [10–14] suffers from the discontinuous input/output current. In addition, they operate as a Cuk converter when the duty cycle percentage reaches 50. In the topology proposed in [12], the input current is continuous, albeit with a high input current ripple. The quadratic topology of [11] suffers from the high voltage stress of the switches. The suggested topology of [14] has achieved continuous input/output current. However, different types of switches (NMOS and PMOS) have been used, which cause a difference in their gate-driver circuits. In [15–17], the other type of quadratic converter was recommended. In comparison with the first group, this kind of quadratic converter has a higher voltage gain. As a result, 50 percent of the duty cycle produces the same result as the boost converter in the converters mentioned above. The input current of the proposed converters is continuous. However, the output currents are discontinuous. The voltage stress of the second switch in the suggested topologies of [10–17] is higher than their output voltages, which may be seen as a significant drawback in high-voltage applications. In addition, both switches suffer from high current stress, which increases their switching losses.

In this paper, a quadratic DC–DC topology is suggested. The improvement of the topology increased the voltage gain in a way that, a 50 percent duty cycle caused a three-times voltage gain. In addition, the current stress of the switches in comparison with [10–17] was low. Consequently, it achieved a lower switch loss in comparison with the topologies of [10–17]. Moreover, the conduction loss of the inductors among the significant power loss types, became lower than [10–15,17]. Therefore, the efficiency of the converter achieved an acceptable value along with increasing the voltage gain.

2. Proposed Topology

2.1. Fundamental Concepts

According to Figure 2a, a combination of two switches, one inductor, one capacitor, and one diode is presented. The components were combined in a way that a switch is seen from both sides. Consequently, it can replace a low-side switch in a converter. As can be understood from Figure 2a, a Cuk converter has a low-side switch. As a result, the presented topology of Figure 2b is the modified topology of the Cuk converter. According to Figure 2c, the presented topology of Figure 2a was replaced by the switch of the Cuk converter. The modified structure maintains the advantages of the Cuk converter, such as continuity of the input/output current waveforms, and increases the voltage-gain ratio.

Figure 2. (a) Cuk converter and how it was modified; (b) the recommended design; (c) the procedure of its creation from the recommended structure and Cuk converter; (d) the equivalent circuit of the first mode; and (e) equivalent circuit of the second mode.

2.2. Operational Modes

Both switches are activated synchronously. During the activation time of the switches, all diodes are OFF. To explain the function of the converter, all of the components were considered ideal. In addition, the operation of the converter takes place in continuous conduction mode (CCM). Moreover, all capacitors are high-valued enough to keep their voltage constant. The activation of the switches causes the first operational mode. During this mode, the first and the last inductors are magnetized due to their applied positive voltage. The voltage of the second inductor is negative. Therefore, it becomes demagnetized. The capacitor currents become negative and make them discharged. The inactivation of the switches starts the second operational mode. During this mode, the diodes are ON and the switches become inactivated. The second inductor becomes magnetized due to its positive voltage. On the other hand, the remaining inductors become demagnetized. In addition, all of the capacitors become charged due to their positive currents. The circuits of both operation modes are illustrated in Figure 2d,e respectively. The steady state relations of the inductor voltages and capacitor currents are expressed as (1), while the state space equations have been investigated in the Appendix A.

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = D(v_{in} + v_{c1}) + (1-D)(v_{in} - v_{c2}) \\ L_2 \frac{di_{L2}}{dt} = D(-v_{c1}) + (1-D)(v_{c2} - v_{c1}) \\ L_3 \frac{di_{L3}}{dt} = D(v_{c1} + v_{c2} - v_o) + (1-D)(-v_o) \\ C_1 \frac{dv_{c1}}{dt} = D(i_{L2} - i_{L3} - i_{L1}) + (1-D)(i_{L2}) \\ C_2 \frac{dv_{c2}}{dt} = D(-i_{L3}) + (1-D)(i_{L1} - i_{L2}) \\ C_o \frac{dv_o}{dt} = D(i_{L3} - I_o) + (1-D)(i_{L3} - I_o) \end{cases} \quad (1)$$

2.3. Average Values of the Voltage/Current of the Energy Storage Components

Referring to the volt-second balance and charge-second balance, all the expressed equations in (1) can be equal to zero in the steady-state. In other words, the inductors become short-circuited due to their zero average voltage and the capacitors become open-circuited due to their zero average current. Thus, rearranging the equations concludes the average voltage of the capacitors and average current of the inductors as (2):

$$\begin{cases} V_{C1} = \frac{V_{in}}{1-D}, V_{C2} = \frac{V_{in}}{(1-D)^2}, V_o = \frac{D(2-D)}{(1-D)^2} V_{in} \\ I_{L1} = \frac{D(2-D)}{(1-D)^2} I_o, I_{L2} = \frac{D}{1-D} I_o, I_{L3} = I_o \end{cases} \quad (2)$$

2.4. Voltage/Current Stresses of Semiconductor-Based Components

By expressing the average value of the inductor currents and capacitor voltages, the current/voltage of the semi-conductor-based components can be expressed as (3):

$$\begin{cases} V_{S1} = V_{D1} = \frac{V_{in}}{1-D}, V_{S2} = \frac{V_{in}}{(1-D)^2}, V_{D2} = \frac{D(2-D)}{(1-D)^2} V_{in} \\ I_{S1} = \frac{D}{(1-D)^2} I_o, I_{S2} = I_{D1} = \frac{D}{1-D} I_o, I_{D2} = \frac{1}{1-D} I_o \end{cases} \quad (3)$$

2.5. Current Ripple of Inductors and Voltage Ripple of Capacitors

The current ripple of the inductors is defined as the difference between the maximum and minimum value of the inductor current waveforms. According to the voltage–current relation of the inductors in the integral form, the simplified form of the current ripple can be defined based on the applied voltage of the inductor in one of the operation modes. Similarly, the voltage ripple can be defined as the difference between the maximum and minimum value of the voltage waveform. Based on the integral form of the voltage–current relation of the capacitors, the simplified form of the voltage ripple can be defined according to the crossing currents from the capacitor in one of the operation modes. The mathematical expression of the explained concepts is as (4):

$$\begin{cases} \Delta i_{L1} = \frac{DV_{in}}{L_1 f_s}, \Delta i_{L2} = \frac{DV_{in}}{(1-D)L_2 f_s}, \Delta i_{L3} = \frac{(1-D)V_o}{L_3 f_s} \\ \Delta v_{c1} = \frac{DV_o}{(1-D)RC_1 f_s}, \Delta v_{c2} = \frac{DV_o}{RC_2 f_s}, \Delta v_o = \frac{(1-D)V_o}{8C_o f_s^2 L_3} \end{cases} \quad (4)$$

3. Discontinuous Conduction Mode

The inductor value affects the current ripple. In other words, a decrease in the inductor value increases the current ripple. A current ripple that is higher than twice the average current leads to DCM. Therefore, the minimum value of the inductors are expressed as (5):

$$L_1 \geq \frac{(1-D)^4 R}{2D(2-D)f_s}, L_2 \geq \frac{(1-D)^2 R}{2D(2-D)f_s}, L_3 \geq \frac{(1-D)R}{2f_s} \quad (5)$$

In addition to the inductor ripple current, the average value of the current also affects the operation mode. In other words, a lower average current that is lower than half of the current ripple, concludes the operation of the converter in DCM. In addition, the average current of the inductor depends on the average output current. Therefore, the operation region of the converter was extracted, as illustrated in Figure 3, based on the varying value of the duty cycle and the output current for both constant output/input voltage. The voltage gain of the converter has a different behavior in DCM. In other words, the ideal voltage gain of the converter depends on the duty cycle in CCM. However, such a concept is not true in DCM. The describing relations of the DCM voltage gain are as (6), where D , D_1 , & D_2 represents the time-intervals that the switches are on, diodes are on, and all the semiconductors are off, respectively.

$$D + D_1 + D_2 = 1, V_o = V_{in} \frac{D(D + 2D_1)}{D_1^2} \quad (6)$$

Figure 3. Operational region of the converter in CCM and DCM, while the frequency is 100 kHz, the last inductor is 1500 μ H, and (a) the output voltage is constant (90 V), (b) the input voltage is constant (30 V).

4. The Non-Ideal Mode

4.1. The Non-Ideal Voltage Gain

In the second section, the converter was investigated in the ideal mode. In other words, the expressed voltage gain was extracted by ignoring the resistance of the inductors (r_L), and the dynamic resistance of the switches and diodes (r_S, r_D). However, the expressed voltage gain in the second section cannot clearly describe the prototype's behavior. The voltage gain of the converter is expressed by the employment of the parasitic components, as (7):

$$\begin{cases} \frac{V_o}{V_{in}} = \frac{D(2-D)}{(1-D)^2} - G_{r_L}(D) - G_{r_S}(D) - G_{r_D}(D) \\ G_{r_L}(D) = \frac{r_L}{R} \frac{2D^4 - 4D^3}{(1-D)^5}, G_{r_S}(D) = \frac{r_S}{R} \frac{D^5 - 2D^4 - 2D^3 + 4D^2}{(1-D)^6}, G_{r_D}(D) = \frac{r_D}{R} \frac{-D^2 + 2D}{(1-D)^5} \end{cases} \quad (7)$$

The difference of the voltage gain, in both ideal and non-ideal modes, is illustrated in Figure 4a. According to Equation (7), the parasitic components of the circuit elements, as well as the load, affect the voltage gain. It is worth noting that the parasitic components of the circuit elements refer to the quality of the used equipment. In addition, the load value refers to the output power. As seen in Figure 4b, the voltage gain of the non-ideal mode was plotted for different values of the output power. It can be understood that an increase in the output power decreases the maximum value of the voltage gain. In addition, an increase in the output power level shortens the rising interval of the voltage gain versus duty cycle. As presented in Figure 4c, the behavior of the voltage gain in a non-ideal mode was plotted for both the varying duty cycles and output power. It can be understood that the value of the maximum gain and its corresponding duty cycle increases as the output decreases. In Figure 4d,e, the voltage gain of the proposed topology is compared with [10–17] in the non-ideal mode of the converters. According to Figure 4d, while the duty cycle varies from 0 to 50 percent, the voltage gain of [10–14] varies from 0 to unity. The voltage gain of [15–17] varies from 0 to 2 in this interval and the voltage gain of the proposed converter

varies from 0 to 3. In Figure 4e, where the duty cycle varies from 50 to 100, the voltage gain of the suggested converter varies from 3 to 16. Consequently, it can be deduced that this converter has a better and higher voltage gain in both ideal and non-ideal modes.

Figure 4. (a) Comparison of ideal and non-ideal voltage gain; (b) comparison of non-ideal voltage gain for different output powers; (c) behavior of the voltage gain with respect to the varying duty cycles and output power; (d) comparison of the voltage gain of the high gain converter for the varying duty cycles from 0 to 50 percent; (e) comparison of the voltage gain of high gain converter for the varying duty cycles from 50 to 85 percent.

4.2. Efficiency

To obtain the converter efficiency, the conduction loss of inductors, switches, and diodes, and the frequency loss of the switches, are explained here. It is worth noting that the magnetic loss, hysteresis loss, eddy current loss, and frequency loss of the inductors were neglected. Moreover, the use of MKT-type capacitors, which have extremely low equivalent series resistors (ESRs), made it possible to neglect the conduction loss of capacitors. Additionally, the parasitic inductance of the circuit components store energy by currents and discharges as voltage spikes during the transient inactivation [7]. The conduction loss of inductors, switches, and diodes, and the frequency loss of the switches, are expressed as (8), respectively:

$$\begin{cases} P_L = r_{L1} I_{rms1}^2 + r_{L2} I_{rms2}^2 + r_{L3} I_{rms3}^2 = \left(r_{L1} \frac{D^2(2-D)^2}{(1-D)^4} + r_{L2} \frac{D^2}{(1-D)^4} + r_{L3} \right) \frac{P_o}{R} \\ P_S = r_{DS1} I_{S1,rms}^2 + r_{DS2} I_{S2,rms}^2 = \left(r_{DS1} \frac{D}{(1-D)^2} + r_{DS2} \frac{D}{(1-D)^4} \right) \frac{P_o}{R} \\ P_D = V_{DF1} I_{D1} + V_{DF2} I_{D2} \left(V_{DF1} \frac{D}{1-D} + V_{DF2} \frac{1}{1-D} \right) I_o \\ P_{SS} = \frac{1}{2} (I_{S1} V_{S1} t_{OFF1} f_s + I_{S2} V_{S2} t_{OFF2} f_s) = \left(t_{off1} + t_{off2} \right) \frac{P_o f_s}{(1-D)(2-D)} \end{cases} \quad (8)$$

The expressed equations state is that the efficiency depends on the quality of the circuit components and output power. In Figure 5a,b, the efficiency graph is plotted for the different values of the output power for all values of the duty. According to Figure 5a, while the duty cycle varies from 0 to 50 percent, the efficiency of the converter is more than 96 percent for the considered output powers. Moreover, based on Figure 5b, while the duty cycle is lower than 70 percent, the efficiency is more than 80 percent for the considered output powers. By increasing the duty cycle to 72 percent, the efficiency becomes more than 80 percent only for output power levels of 30 to 90 W. In Figure 5c,d, the efficiency of the proposed topology and converters of [10–17] are compared. As seen in Figure 5c, the efficiency of the proposed converter is close to the other topologies—well above 97 percent—when the duty cycle varies from 0 to 50 percent. Based on Figure 5d, the efficiency of the proposed converter is approximately the same as the others, as the duty cycle varies from 50 percent to 75 percent.

Figure 5. (a) Efficiency of the converter for different output powers and the varying duty cycles from 0 to 50 percent; (b) efficiency of the converter for different output powers and the varying duty cycles from 50 to 100 percent; (c) comparison of the efficiencies of high gain converters for varying duty cycles from 0 to 50 percent; (d) comparison of the efficiencies of high gain converters for varying duty cycles from 50 to 100 percent.

5. Comparative Analysis with Other Topologies

In this section, different parameters are expressed for the recommended converter, besides the recently proposed converters. It is worth noting that the output voltage and input current were assumed as basic values for normalizing voltage/current stresses, respectively. Moreover, to calculate the different kinds of losses and voltage/current stress of semiconductors, a value of the duty cycle was used that concluded a three-time voltage gain in the mentioned topologies.

5.1. Different Kinds of Power Losses

In Table 1, the conduction loss of the inductors and switches is expressed and valued by the duty cycle that leads to the voltage gain of 3. The corresponding value of the duty cycle is reported in Table 2. It can be understood that the conduction loss of the inductors in the suggested converter is lower than [11–15,17]. In addition, the conduction loss of the switch in this converter is lower than all of the other converters, except [15,16].

Table 1. Comparison of power loss of inductors and switches (conduction) as the voltage gain ratio equals 3.

	Inductors Loss (W)	Switches Conduction Loss (W)
proposed converters	$P_o \frac{r_L}{R} \frac{2D^4 - 8D^3 + 11D^2 - 4D + 1}{(1-D)^4} = 0.63$	$P_o \frac{r_S}{R} \frac{D^3 - 2D^2 + 2D}{(1-D)^4} = 0.45$
[10]	$P_o \frac{r_L}{R} \frac{2D^4 - 6D^3 + 8D^2 - 4D + 1}{(1-D)^4} = 0.5$	$P_o \frac{r_S}{R} \frac{2D^3 - 2D^2 + D}{(1-D)^4} = 0.8$
[11]	$P_o \frac{r_L}{R} \frac{3D^4 - 5D^3 + 7D^2 - 4D + 1}{(1-D)^4} = 1.15$	$P_o \frac{r_S}{R} \frac{5D^3 - 4D^2 + D}{(1-D)^4} = 0.7$
[12]	$P_o \frac{r_L}{R} \frac{D^4 - 2D^3 + 3D^2 - 2D + 1}{(1-D)^4} = 1.41$	$P_o \frac{r_S}{R} \frac{2D^3 - 2D^2 + D}{(1-D)^4} = 0.8$
[13]	$P_o \frac{r_L}{R} \frac{2D^2 - 2D + 1}{(1-D)^4} = 1.28$	$P_o \frac{r_S}{R} \frac{2D^3 - 2D^2 + D}{(1-D)^4} = 0.8$
[14]	$P_o \frac{r_L}{R} \frac{2D^4 - 6D^3 + 8D^2 - 4D + 1}{(1-D)^4} = 1.12$	$P_o \frac{r_S}{R} \frac{2D^3 - 2D^2 + D}{(1-D)^4} = 0.8$
[15]	$P_o \frac{r_L}{R} \frac{3D^2 - 4D + 2}{(1-D)^4} = 0.91$	$P_o \frac{r_S}{R} \frac{2D^3 - 6D^2 + 5D}{(1-D)^4} = 0.8$
[16]	$P_o \frac{r_L}{R} \frac{2D^4 - 6D^3 + 8D^2 - 4D + 1}{(1-D)^4} = 0.55$	$P_o \frac{r_S}{R} \frac{2D^3 - 2D^2 + D}{(1-D)^4} = 0.4$
[17]	$P_o \frac{r_L}{R} \frac{D^2 - 2D + 2}{(1-D)^4} = 1.56$	$P_o \frac{r_S}{R} \frac{D^3 - 2D^2 + 2D}{(1-D)^4} = 0.88$

Table 2. Comparison of power loss in switches (switching) and diodes as the voltage gain ratio equals 3.

	Switching Loss of Switches (W)	Diodes Loss (W)	Duty Cycle	η
proposed converters	$\frac{f_s P_o t_{off}}{(1-D)(2-D)} = 0.013$	$\frac{V_{DF} I_o (1+D)}{1-D} = 1.5$	0.5	97.2
[10]	$\frac{f_s P_o t_{off}}{1-D} = 0.027$	$\frac{V_{DF} I_o}{1-D} = 1.35$	0.63	97.1
[11]	$\frac{f_s P_o t_{off} D}{(1-D)^2} = 0.046$	$\frac{V_{DF} I_o}{1-D} = 1.35$	0.63	96.5
[12]	$\frac{f_s P_o t_{off} (1+D)}{1-D} = 0.044$	$\frac{V_{DF} I_o}{1-D} = 1.35$	0.63	96.1
[13]	$\frac{f_s P_o t_{off}}{1-D} = 0.027$	$\frac{V_{DF} I_o}{1-D} = 1.35$	0.63	96.3
[14]	$\frac{f_s P_o t_{off}}{1-D} = 0.027$	$\frac{V_{DF} I_o}{1-D} = 1.35$	0.63	96.4
[15]	$\frac{f_s P_o t_{off} (1+D)}{1-D} = 0.036$	$\frac{V_{DF} I_o (1+D)}{1-D} = 1.82$	0.57	96.6
[16]	$\frac{f_s P_o t_{off} (1+D)}{1-D} = 0.036$	$\frac{V_{DF} I_o}{1-D} = 1.15$	0.57	97.7
[17]	$\frac{f_s P_o t_{off} (1+D)}{1-D} = 0.036$	$\frac{V_{DF} I_o (2-D)}{1-D} = 1.66$	0.57	95.6

In Table 2, the switching loss of the switch, the conduction loss of the diodes, the corresponding value of the duty cycle, and concluded efficiency are reported. It can be understood that the proposed converter has achieved the lowest value in comparison with [10–17]. In addition, the conduction loss of the diode is only lower than [15,17]. Moreover, the suggested converter uses the lowest value of the duty cycle to provide the voltage

gain of 3. In the last column of the second table, the efficiency is reported. As reported, the suggested converter has the highest efficiency among [10–15,17]. It is worth noting that the difference between the efficiency of the proposed converter and [16] is 0.5 percent.

5.2. The Comparison of the Current/Voltage Stress of the Switches and Diodes at the Operating Point

In Table 3, the normalized voltage stress of switches and diodes is valued by a percentage of the duty cycle, which provides the voltage gain of 3. Based on the mentioned table, the first switch and diode of this converter have achieved the lowest values among [10–17]. The voltage stress of the second switch is lower than [10,11,13–16]. However, the voltage stress of the second diode of this converter is more than the others.

Table 3. Comparison of the normalized voltage stress of semiconductors as the voltage gain ratio equals 3.

	$\frac{V_{S1}}{V_O}$	$\frac{V_{S2}}{V_O}$	$\frac{V_{D1}}{V_O}$	$\frac{V_{D2}}{V_O}$	D
proposed converter	$\frac{1-D}{D(2-D)} = 0.66$	$\frac{1}{D(2-D)} = 1.32$	$\frac{1-D}{D(2-D)} = 0.66$	$\frac{1}{D} = 2$	0.5
[12]	$\frac{1-D}{D^2} = 0.82$	1	$\frac{1-D}{D^2} = 0.82$	$\frac{1}{D} = 1.6$	0.63
[10]	$\frac{1-D}{D^2} = 0.82$	$\frac{1}{D} = 1.6$	$\frac{1-D}{D^2} = 0.82$	$\frac{1}{D} = 1.6$	0.63
[11]	$\frac{1}{D^2} = 2.56$	$\frac{1}{D} = 1.6$	$\frac{1-D}{D^2} = 0.82$	$\frac{1}{D} = 1.6$	0.63
[13]	$\frac{1-D}{D^2} = 0.82$	$\frac{1}{D} = 1.6$	$\frac{1-D}{D^2} = 0.82$	$\frac{1}{D} = 1.6$	0.63
[14]	$\frac{1-D}{D^2} = 0.82$	$\frac{1}{D} = 1.6$	$\frac{1-D}{D^2} = 0.82$	$\frac{1}{D} = 1.6$	0.63
[15]	$\frac{1-D}{D} = 0.75$	$\frac{2D-1}{D} = 0.24$	$\frac{1-D}{D} = 0.75$	1	0.57
[16]	$\frac{1-D}{D} = 0.75$	$\frac{1}{D} = 1.75$	$\frac{1-D}{D} = 0.75$	$\frac{1}{D} = 1.75$	0.57
[17]	$\frac{1-D}{D} = 0.75$	1	$\frac{1-D}{D} = 0.75$	1	0.57

In Table 4, the current stress of the switches and diodes are compared. As can be seen, the current stress of the first switch is lower than [10–15,17]. In addition, the current stress of the second switch and the first diode are the lowest values among [10–17]. However, the current stress of the second diode is more than the others. It is worth noting that interested readers can use the reported normalized values of the current/voltage stresses in Tables 4 and 5 to find the behavior of the normalized values for different values of the duty cycle.

5.3. The Comparison of the Component Numbers and Continuity of Input/Output Currents

In Table 5, the number of circuit components and the continuity of the input/output currents are compared among the proposed topology and suggested topologies of [10–17]. The number of inductors and capacitors is the same in the suggested topology and converters of [10,12,14–16]. In addition, the number of switches and diodes is the same in all converters. The input current of the suggested topology and proposed converters of [11,12,14–16] are continuous. In addition, the output current of the suggested design is continuous, the same as [11,14].

Table 4. Comparison of the normalized current stress of semiconductors as the voltage gain ratio equals 3.

	$\frac{I_{S1}}{I_{in}}$	$\frac{I_{S2}}{I_{in}}$	$\frac{I_{D1}}{I_{in}}$	$\frac{I_{D2}}{I_{in}}$	D	$\frac{V_o}{V_{in}}$
proposed converter	$\frac{1}{2-D} = 0.66$	$\frac{1-D}{2-D} = 0.33$	$\frac{1-D}{2-D} = 0.33$	$\frac{1-D}{D(2-D)} = 0.66$	0.5	$\frac{D(2-D)}{(1-D)^2} = 3$
[10]	1	$\frac{1-D}{D} = 0.59$	$\frac{1-D}{D} = 0.59$	$\left(\frac{1-D}{D}\right)^2 = 0.33$	0.63	$\left(\frac{D}{1-D}\right)^2 = 3$
[11]	1	$\frac{1-D}{D} = 0.59$	$\frac{1-D}{D} = 0.59$	$\left(\frac{1-D}{D}\right)^2 = 0.33$	0.63	$\left(\frac{D}{1-D}\right)^2 = 3$
[12]	1	$\frac{2D-1}{D} = 0.41$	$\frac{2D-1}{D} = 0.59$	$\left(\frac{1-D}{D}\right)^2 = 0.33$	0.63	$\left(\frac{D}{1-D}\right)^2 = 3$
[13]	1	$\frac{1-D}{D} = 0.59$	$\frac{1-D}{D} = 0.59$	$\left(\frac{1-D}{D}\right)^2 = 0.33$	0.63	$\left(\frac{D}{1-D}\right)^2 = 3$
[14]	1	$\frac{1-D}{D} = 0.59$	$\frac{1-D}{D} = 0.59$	$\left(\frac{1-D}{D}\right)^2 = 0.33$	0.63	$\left(\frac{D}{1-D}\right)^2 = 3$
[15]	$2-D = 1.43$	$1-D = 0.43$	$\frac{1-D}{D} = 0.75$	$\frac{(1-D)^2}{D} = 0.33$	0.57	$\frac{D}{(1-D)^2} = 3$
[16]	$D = 0.57$	$1-D = 0.43$	$1-D = 0.43$	$\frac{(1-D)^2}{D} = 0.33$	0.57	$\frac{D}{(1-D)^2} = 3$
[17]	1	$1-D = 0.57$	$\frac{1-D}{D} = 0.75$	$\frac{(1-D)^2}{D} = 0.33$	0.57	$\frac{D}{(1-D)^2} = 3$

Table 5. Comparison of component numbers and voltage gain.

	No. L	No. C	No. S	No. D	Total	Input Current	Output Current	Voltage Gain
proposed	3	3	2	2	10	Continuous	Continuous	$\left(\frac{D}{1-D}\right)^2$
[10]	2	2	2	2	8	Discontinuous	Discontinuous	$\left(\frac{D}{1-D}\right)^2$
[11]	3	3	2	2	10	Continuous	Continuous	$\left(\frac{D}{1-D}\right)^2$
[12]	3	3	2	2	10	Continuous	Discontinuous	$\left(\frac{D}{1-D}\right)^2$
[13]	2	2	2	2	8	Discontinuous	Discontinuous	$\left(\frac{D}{1-D}\right)^2$
[14]	3	3	2	2	10	Continuous	Continuous	$\left(\frac{D}{1-D}\right)^2$
[15]	3	3	2	2	10	Continuous	Discontinuous	$\frac{D}{(1-D)^2}$
[16]	3	3	2	2	10	Continuous	Discontinuous	$\frac{D}{(1-D)^2}$
[17]	2	2	2	2	8	Continuous	Discontinuous	$\frac{D}{(1-D)^2}$

6. Simulation Results

To verify the findings of the second section, the simulation results are discussed here. To find the suitable values of the inductors and capacitors, some parameters need to be considered. The voltage and current values need to follow the safety requirements and equipment limits. Therefore, the input voltage and output current have exceeded 30 V and 1 A, respectively. Due to the frequency limits of the inductor wire, switching frequency was set to 100 kHz. Moreover, according to the power quality considerations, the current ripple of the inductors and voltage ripple of the capacitors were considered 30 and 5 percent, respectively. The average value of the inductor currents and capacitor voltages are calculated by Equation (3). Consequently, the average inductor current and average capacitor voltage are expressed as (9).

$$I_{L1} = 3 \text{ A}, I_{L2} = I_{L3} = 1 \text{ A}, V_{C1} = 60 \text{ V}, V_{C2} = 120 \text{ V}, V_O = 90 \text{ V} \quad (9)$$

Based on the calculated values in (9), and the expressed relations of (4), the inductors and capacitors are expressed as (10):

$$L_1 = 160 \text{ } \mu\text{H}, L_2 = 1000 \text{ } \mu\text{H}, L_3 = 1500 \text{ } \mu\text{H}, C_1 = 3.34 \text{ } \mu\text{F}, C_2 = 0.83 \text{ } \mu\text{F}, C_o = 0.083 \text{ } \mu\text{F} \quad (10)$$

The simulation results were extracted by PLECS software. The voltage/current waveforms of all circuit components are presented in Figure 6. According to Figure 6a–f, the average value of the inductor current and capacitor voltage is as (11):

$$I_{L1} = 3 \text{ A}, I_{L2} = I_{L3} = 1 \text{ A}, V_{C1} = 59.5 \text{ V}, V_{C2} = 120 \text{ V}, V_O = 90 \text{ V} \quad (11)$$

A comparison between (11) and (9) confirms their compatibility. In addition, based on the extracted Figures 6g–l, the average voltage of the inductors and average current of the capacitors is zero and the extracted results are compatible with the voltage/current second balance. In Figures 6m–p, the current waveforms of semiconductors are presented. It is worth noting that the switches are activated synchronously. Moreover, during the activation of diodes, the switches are OFF. These concepts are compatible with the theoretical descriptions of the second section. In Figure 6q–t, the voltage waveforms of the semiconductors are presented. It can be understood that the voltage of the first capacitor was applied to the first switch and diode. Moreover, the applied voltage to the second switch is the second capacitor voltage, which is compatible with the extracted result in Figure 6r. Furthermore, the applied voltage to the second diode is the sum of the first and second capacitors, which is compatible with the extracted outcome.

Figure 6. (a) First inductor current; (b) second inductor current; (c) third inductor current; (d) first capacitor voltage; (e) second capacitor voltage; (f) output capacitor voltage; (g) first inductor voltage; (h) second inductor voltage; (i) third inductor voltage; (j) first capacitor current; (k) second capacitor current; (l) output capacitor current; (m) first switch current; (n) second switch current; (o) first diode current; (p) second diode current; (q) first switch voltage; (r) second switch voltage; (s) first diode voltage; (t) second diode voltage.

7. Experimental Results

In line with the simulation results, the current/voltage waveforms of all circuit components were extracted. Similar to the simulation results, the minimum values of the capacitor and inductors of the prototype follow the calculations of (10). Moreover, metallized polyester film capacitors with low ESR were used. In addition, for the inductor windings, litz wires were used. Moreover, IRF540 and 2015OCT were used as the MOSFET and diode in the prototype. Furthermore, IRF2110 was used as the driver of the MOSFET. The experimental results are presented in Figure 7. According to Figure 7a, the average current of the first, second, and third inductors is 3 A, 1 A, and 1 A, respectively. Moreover, based on Figure 7d, the voltage of the inductors is compatible with volt-second balance. It is worth noting that, in Figure 7b, the voltage waveform of the capacitors are illustrated. Additionally, the average value of the voltage is 59.5 V, 120 V, and 90 V for the first to third capacitors, respectively. Moreover, the charge-second balance can be understood from Figure 7e, due to the zero average value of the presented current waveforms. In Figure 7c,f, the current waveforms and voltage waveforms of the semiconductors are presented, respectively. According to Figure 7c, the operation of the semiconductor takes place asynchronously, which is compatible with the theoretical analysis of the paper, as well as the simulation results. Moreover, the applied voltages to the semiconductors during their OFF mode is compatible with the simulation results and the theoretical equations. It is worth noting that the prototype is shown in Figure 8a. Moreover, the detailed information of the MOSFET drivers are illustrated in Figure 8b,c for low-side and high-side switches, respectively. Additionally, other comparisons based on the experimental results are presented in Figure 9. In Figure 9a,b, the diagram of the non-ideal voltage gain is compared with the extracted results of the experiment for 90 W output power, 30 V input voltage, and varying duty cycles. It can be understood that, while the duty cycle varies from 20 to 50 percent, according to Figure 9a, the theoretical and experimental voltage gains will perfectly match. The same concept is true for the duty cycles ranging between 50 and 70 percent, as per Figure 9, but there is a difference between the theory and experiments in duty cycles greater than 70 percent, which was predictable due to the parasitic effects. In Figure 9c,d, the efficiency of the converter is compared based on the theoretical analysis and experiments. It can be understood that while the duty cycle varies from 20 percent to 50 percent in Figure 9c, the differences of the curves increase from 2 percent to 3 percent. Moreover, while the percentage of the duty cycle becomes 50 percent, the extracted efficiency from the theory and experiment is 97 percent and 93.6 percent, respectively. Furthermore, according to Figure 9d, the efficiency of the converter is higher than 80 percent for the percentage of the duty cycles lower than 71. However, this value is 73 percent in the theoretical result. Typically, the efficiency of the power converter declines as the duty cycle of the switch increases, due to the increase of the power loss over the components. However, it should be noted that the practical voltage gain in a transformer-less topology would not normally exhibit ultra-high voltage gains, due to the parasitic effect, which confirms the efficiency yield of over 80 percent for the practical gains in Figure 9. We should note that the experimental efficiency and different losses are expressed for the operating point in Figure 9e,f. The diode and inductor losses are the same at the operating point according to Figure 9f. Moreover, according to this figure, the switch loss is lower than the diode and inductor losses. In Figure 9g, the efficiency of the converter is extracted for the different output powers from the theory and experiment, while the duty cycle is 50 percent, and the output voltage is 90 V.

Figure 7. The experimental results: (a) inductors current; (b) capacitors voltage; (c) semiconductors current; (d) inductors voltage; (e) capacitors current; (f) semiconductors voltage.

Figure 8. (a) The prototype; (b) driver of the low side switch; (c) driver of the high-side switch.

Figure 9. Theoretical analysis vs. experiments: (a) the comparison of the theoretical and experimental voltage gain, while the duty cycle varies from 0 to 50 percent; (b) the comparison of the theoretical and experimental voltage gain, while the duty cycle varies from 50 to 100 percent; (c) the comparison of the theoretical and experimental efficiency, while the duty cycle varies from 0 to 50 percent; (d) the comparison of the theoretical and experimental efficiency, while the duty cycle varies from 50 to 100 percent; (e) pie chart of the efficiency and losses; (f) loss break down; (g) comparison of the theoretical and experimental efficiency for varying output power, from 30 to 180 W.

8. Conclusions

In this article, a high step-up DC-DC converter was proposed. The proposed converter was based on the Cuk converter. Therefore, the continuity of the input current was maintained. This feature makes this converter suitable for renewable energy applications. Moreover, the ideal model of the proposed converter was studied and explained in CCM and DCM. The average voltage of the capacitors, the voltage gain, the boundary value of the

inductors, and the CCM and DCM operation regions were studied. The relation of the non-ideal voltage ratio was extracted, which was then compared with the practical voltage ratio to validate its combustibility. Furthermore, the improvements of the proposed converter, in comparison with the conventional Cuk and the other converters, were discussed; it was deduced that the proposed converter has a higher voltage ratio by the lower value of the duty cycle. The mathematical equations of the efficiency and different power losses were expressed. Therefore, the advantages of the proposed converter were discussed in various aspects. Finally, the simulation and the experimental results were delivered and compared with the design assumptions based on the theoretical analysis. Finally, the compatibility of the simulation and experimental results with the theoretical relations validated the correctness of the mathematical analysis.

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Appendix A

The state equations of the proposed converter are as (A1).

$$\begin{cases} L_1 \frac{d \langle i_{L1} \rangle}{dt} = V_{in} + d \langle v_{c1} \rangle - (1-d) \langle v_{c2} \rangle \\ L_2 \frac{d \langle i_{L2} \rangle}{dt} = -d \langle v_{c1} \rangle + (1-d) \langle v_{c2} \rangle \\ L_3 \frac{d \langle i_{L3} \rangle}{dt} = d \langle v_{c1} + v_{c2} \rangle - \langle v_o \rangle \\ C_1 \frac{d \langle v_{c1} \rangle}{dt} = \langle i_{L2} \rangle - d \langle i_{L1} + i_{L3} \rangle \\ C_2 \frac{d \langle v_{c2} \rangle}{dt} = -d \langle i_{L3} \rangle + (1-d) \langle i_{L1} - i_{L2} \rangle \\ C_o \frac{d \langle v_o \rangle}{dt} = \langle i_{L3} \rangle - \frac{\langle v_o \rangle}{R} \end{cases} \quad (A1)$$

The required assumptions and neglecting are as (A2).

$$\begin{cases} i_{L1} = \hat{i}_{L1} + I_{L1}, i_{L2} = \hat{i}_{L2} + I_{L2}, i_{L3} = \hat{i}_{L3} + I_{L3}, v_{c1} = \hat{v}_{c1} + V_{c1}, v_{c2} = \hat{v}_{c2} + V_{c2}, v_o = \hat{v}_o + V_o \\ \hat{i}_{L1} \ll I_{L1}, \hat{i}_{L2} \ll I_{L2}, \hat{i}_{L3} \ll I_{L3}, \hat{v}_{c1} \ll V_{c1}, \hat{v}_{c2} \ll V_{c2}, \hat{v}_o \ll V_o \end{cases} \quad (A2)$$

The space state equations based on the state matrices are as (A3).

$$\dot{x} = Ax + Bu, y = Cx \quad (A3)$$

The mentioned matrices are as :

$$\begin{bmatrix} \frac{d\hat{i}_{L1}}{dt} \\ \frac{d\hat{i}_{L2}}{dt} \\ \frac{d\hat{i}_{L3}}{dt} \\ \frac{d\hat{v}_{C1}}{dt} \\ \frac{d\hat{v}_{C2}}{dt} \\ \frac{d\hat{v}_{C0}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{D}{L_1} & \frac{D-1}{L_1} & 0 \\ 0 & 0 & 0 & \frac{-D}{L_2} & \frac{1-D}{L_2} & 0 \\ \frac{-D}{C_1} & \frac{1}{C_1} & \frac{-D}{C_1} & 0 & 0 & 0 \\ \frac{1-D}{C_2} & \frac{1-D}{C_2} & \frac{-D}{C_2} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_o} & 0 & 0 & \frac{-1}{RC_o} \end{bmatrix} x + \begin{bmatrix} b_{11} \\ b_{12} \\ b_{13} \\ b_{14} \end{bmatrix} \hat{d}, y = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ -1 \end{bmatrix}^t d$$

Based on the expressed relations, the bode diagram of the converter is illustrated in Figure A1 for both before/after compensating. Additionally, gain and phase margins for both mentioned modes are expressed as (A4) and (A5).

$$G_m = -36 \text{ dB}, P_m = 173 \text{ deg} \quad (\text{A4})$$

$$G_m = 11.1 \text{ dB}, P_m = 64.8 \text{ deg} \quad (\text{A5})$$

The appropriate compensator for the mentioned converter was calculated by MATLAB as (A6).

$$-0.010318 * \frac{1 + 0.0099s}{s} \quad (\text{A6})$$

Figure A1. The bode diagram: (a) before compensating; (b) after compensating.

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