

Article

Transformer-Less Switched-Capacitor Quasi-Switched Boost DC-DC Converter

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Abstract: In this article, a quasi-switched boost converter based on the switched-capacitor technique with high step-up voltage capability is dealt with and analyzed. The proposed converter offers a simple structure and low voltage stress on the semiconductor elements with intrinsic small duty cycle. An inductor of the proposed converter is connected in series with the input voltage source; therefore, continuous input current ripple is attainable. In addition, the efficiency of the proposed converter is also improved. A detailed steady-state analysis is discussed to identify the salient features of the switched-capacitor-based quasi-switched boost DC-DC converter. The performance of the converter is compared against similar existing high boost DC-DC converters. Finally, the switched-capacitor-based quasi-switched boost DC-DC converter is investigated by experimental verification.

Keywords: switched-capacitor; quasi-switched boost; high step-up; duty cycle; power conversion



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1. Introduction

Nowadays, the deployment of the renewable energy sources includes photovoltaic, and fuel cells have grown significantly over the past decade. However, one of the main drawbacks of these sources are low output voltage. As a main part of the distributed generation technologies, the high-voltage boost DC-DC converters have emerged and been the main link to realize an energy transfer from the renewable energy sources [1,2]. Typical isolated converters have been developed to achieve a high voltage conversion with high turns ratio of the high-frequency transformer. Isolated converters including forward, flyback, half/full-bridge, and push-pull structures were presented in [3–6]. However, they offer problems such as leakage inductance occurred by the secondary side of the HF transformer, showing large voltage and current spikes on semiconductor devices. By contrast, the transformer-less high voltage gain DC-DC configurations are considering suitable solutions for achieving high conversion efficiency and decreasing the cost of system in the power distributed system due to omitting the galvanic isolation transformers. The coupled-inductor-based structures can also produce the solution to improve the voltage gain without galvanic isolation [7,8]. Nonetheless, these converters have to add a snubber-clamped circuitry to reduce leakage inductor energy recovery problems, which increases the cost of the converter.

For the transformer-less DC-DC structures, a conventional boost DC-DC converter is able to provide a boost ability. In the ideal case, the boost converter can realize very high voltage gain. However, the duty cycle is limited due to the non-idealities of the passive components, semiconductor devices, and loss considerations. Therefore, the conventional boost converter is not a suitable solution for high voltage gain applications. In such applications, the cascaded and quadratic boost converters were introduced to achieve

high voltage conversion [9,10]. In this case, two or more conventional boost converters are connected in series. The size and weight of these converters will be increased because many switches and gate drivers are required. Furthermore, the voltage conversion of the converter can also be improved by using the switched-inductor technology in [11–13]. In the conventional switched-inductor high step-up DC-DC converter, the voltage gain is limited and the semiconductor devices with high voltage ratings are needed, which significantly raises the cost and the size of the converter. The duty cycle of the mentioned conventional boost non-isolated DC-DC is operated in wide range, and the range of duty cycle is varied between 0 and 1. In this case, the high voltage gain can be obtained with large duty cycle value, which causes to produce power loss on power active switches. Moreover, to limit the range of duty cycle operated within (0, 0.5) and improve the voltage gain, the Z-source and quasi-Z source configurations are considered as good solutions [14–17]. The shortages of these topologies are discontinuous input current and complex topological structure. Instead of considering about adding passive components in the class of the Z-source and quasi-Z-source-based converters, a class of switched-boost and quasi-switched-boost converters were proposed in [18,19]. However, the voltage stress on the semiconductor devices of them is still high and equals to the output voltage. The aforementioned structures can realize high voltage conversion but share a similar problem, which is the requirement of a large number of additional devices. In addition, research of switched-capacitor-based technology has been proposed to produce the high voltage gain, as presented in [20–24]. The switched-capacitor structure has been known with merits such as small size, low-voltage rating on the semiconductor devices, and high voltage density. In [21], a boost DC-DC converter adopting the switched-boost network was introduced with high voltage conversion and low voltage rating on switches. However, the voltage and current stress of diodes are still high. In [22], an extended switched-boost DC-DC was proposed, which incorporated the switched-capacitor network and switched-boost converter with improved the voltage gain and low voltage stress on semiconductor devices [22]. Nevertheless, the input current is discontinuous and the voltage ratio is still not high. The dual-switch boost converter based on the switched-capacitor in [23] has used for one inductor structure, high boost gain, and low voltage stress. However, the input research in [24] has been proposed the solution for the high-step-up topology. By applying an additional diode and capacitor, the voltage charge pumping solution with integrating switched-boost and Z-source networks have been developed with high voltage gain and low voltage rating on components.

In this article, to enhance the practical high-voltage conversion and reduce the duty cycle ratio, a new transformer-less quasi-switched boost DC-DC converter with integrating switched-capacitor network will be determined. The proposed switched-capacitor switched-boost converter has the merit of enhancing voltage gain, achieve low voltage rating on the active switches and high efficiency. The remainder of this article is organized as follows. Section 2 presents the configuration and operating principle of the switched-capacitor quasi-switched boost converter in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM). In Section 3, the design guideline is explained. The comparison between proposed converter and other high gain topologies is provided in Section 4. Further, the experimental verifications are presented in Section 5. Finally, Section 6 concludes this article.

2. Operating Principle of Proposed SCQSBC

2.1. Power Circuit

The configuration of the proposed SCQSBC converter as depicted in Figure 1 incorporates the quasi-switched boost network and switched-capacitor cell. The converter is composed of two MOSFETs (S_1 and S_2), four diodes (D_0 to D_3), one inductor, and three capacitors (C_0 to C_2). Figure 2 presents the typical waveforms of the SCQSBC in CCM and DCM. In this case, it can be seen that S_1 is turned on 50% of the period, while S_2 is turned on with the duty cycle of D .

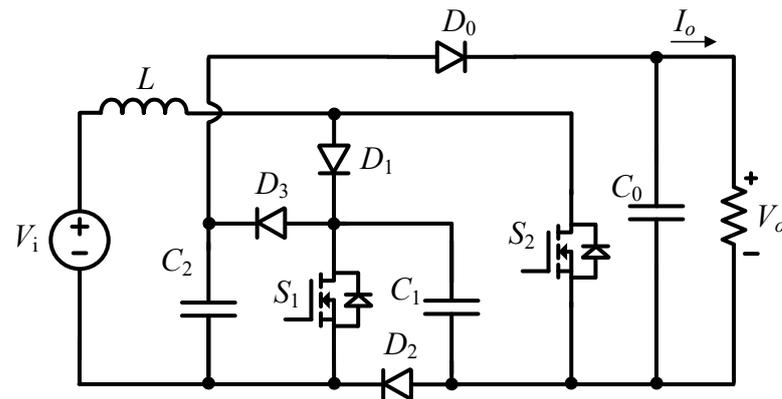


Figure 1. Proposed SCQSB converter.

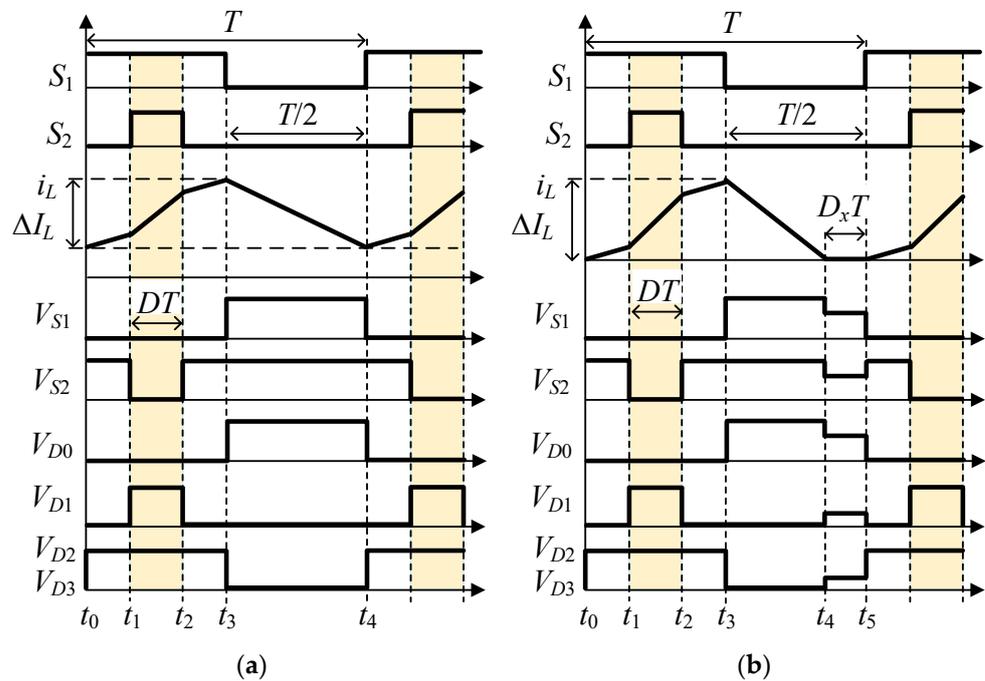


Figure 2. Typical waveform of proposed SCQSB for (a) CCM and (b) DCM.

2.2. Circuit Analysis in CCM

To determine the operating analysis of the SCQSB in the CCM, assume that (1) all power components are ideal; (2) capacitors C_0 , C_1 , and C_2 are enough to induce the constant voltage in one switching period; and (3) the current of an inductor is linear.

Mode I (t_0-t_1 and t_2-t_3): In this mode, the inductor is magnetized by input power supply. MOSFET S_1 is turned on while MOSFET S_2 is turned off. Capacitors C_1 and C_2 are discharged through the output C_0 capacitor. During this mode, diodes D_0 and D_1 are forward-biased, while diodes D_2 and D_3 are reverse-biased. The analysis circuitry of the SCQSB is depicted in Figure 3a. The following equations can be given:

$$\begin{cases} v_L = V_i \\ i_{C01} + i_{C11} = -I_o \end{cases} \quad (1)$$

Mode II (t_1-t_2): In this mode, the inductor is still magnetized by input power supply and capacitor C_1 . MOSFETs S_1 and S_2 are turned on. Capacitors C_1 and C_2 are also discharged through the output C_0 capacitor. During this mode, diode D_0 is forward-biased,

whereas diodes D_1 , D_2 and D_3 are reverse-biased. The circuitry of the SCQSBC is depicted in Figure 3b. The equations can be obtained:

$$\begin{cases} v_L = V_i + V_{C1} \\ i_{C02} + i_{C12} = -I_o \\ i_{C22} - i_{C12} = I_L \end{cases} \quad (2)$$

Mode III (t_3-t_4): In this mode, the inductor is discharged in series with the input voltage to charge two capacitors C_1 and C_2 , while MOSFETs S_1 and S_2 are turned off. During this mode, the diodes D_0 is reversed-bias, whereas diodes D_1 , D_2 and D_3 are forward-biased. Capacitor C_0 is transferred an energy through the resistive load. The circuitry of the SCQSBC is depicted in Figure 3c. The mentioned equations are given:

$$\begin{cases} v_L = V_i - V_{C1} \\ i_{C03} = -I_o \\ i_{C13} = I_L - i_{C23} \end{cases} \quad (3)$$

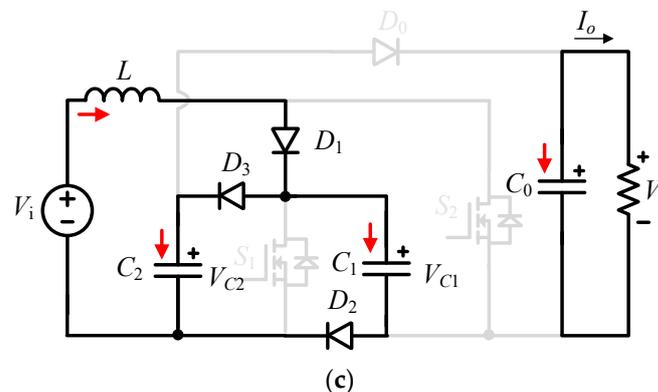
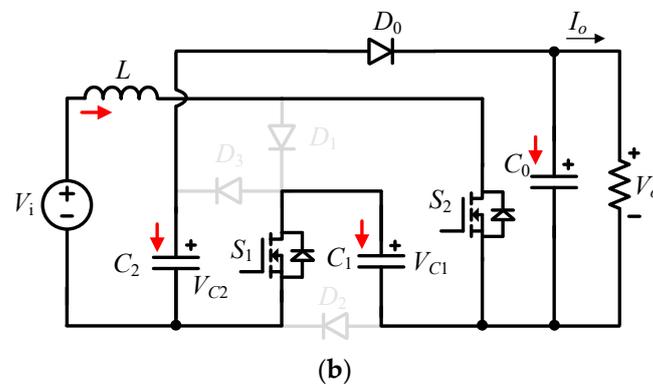
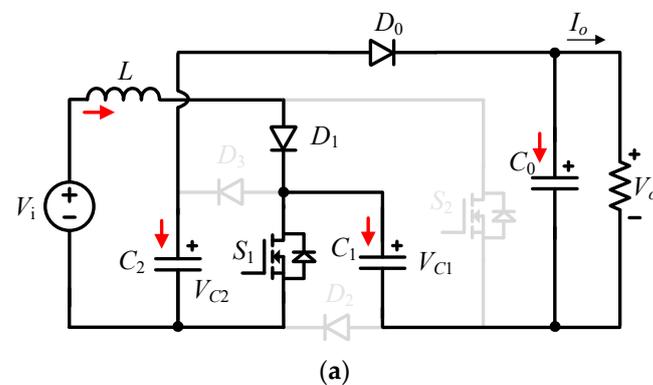
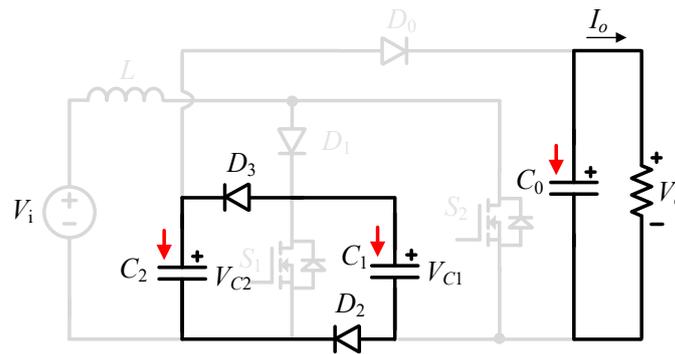


Figure 3. Cont.



(d)

Figure 3. Operating modes of proposed SCQSBC: (a) Mode I, (b) Mode II, (c) Mode III, and (d) Mode IV (DCM).

From (1) to (3), the average value of the inductor voltage can be obtained:

$$L \frac{di_L}{dt} = (0.5 - D)V_i + D(V_i + V_C) + 0.5(V_i - V_C) = 0 \tag{4}$$

Applying the DC variable equation to (4), the capacitors voltage and voltage gain of the proposed SCQSBC can be given as follows:

$$\begin{cases} V_{C1} = V_{C2} = V_C = \frac{2}{1-2D} V_i \\ G = \frac{V_o}{V_i} = \frac{4}{1-2D} \end{cases} \tag{5}$$

where D is the duty cycle.

An inductor of the proposed SCQSBC is connected directly with an input voltage source, and the expressions of the inductor current is:

$$I_L = \frac{4}{1-2D} I_o \tag{6}$$

From (1) to (3), the currents of capacitors C_0 , C_1 and C_2 in mode I, II and III are derived as follows, respectively.

$$\begin{cases} i_{C01} = \frac{I_o}{k_C - 1} \\ i_{C11} = i_{C21} = \frac{-k_C}{k_C - 1} I_o \end{cases} \tag{7}$$

$$\begin{cases} i_{C02} = \frac{k_C - 2 + 2D}{2D(k_C - 1)} I_o \\ i_{C12} = \frac{2 - k_C + 4D - 8k_C D + 4k_C D^2}{2D(k_C - 1)(1 - 2D)} I_o \\ i_{C22} = \frac{2 - k_C - 2D}{2D(k_C - 1)} I_o \end{cases} \tag{8}$$

$$\begin{cases} i_{C03} = -I_o \\ i_{C13} = \frac{2(1 + 2D)}{1 - 2D} I_o \\ i_{C23} = 2I_o \end{cases} \tag{9}$$

$$k_C = \frac{C_2 r_{C2} \%}{2C_0 r_{C0} \%} \tag{10}$$

where k_C , $r_{C0} \%$, and $r_{C2} \%$ are the ratio of capacitor C_2 and C_0 currents in mode I, voltage ripple of capacitors C_0 and C_2 , respectively.

In mode I, the capacitor C_2 and C_0 currents are determined as:

$$\begin{cases} i_{C03} = C_2 \frac{\Delta V_C}{(0.5-D)T} = C_2 \frac{r_{C2}\%V_C}{(0.5-D)T} \\ i_{C13} = i_{C23} = C_0 \frac{\Delta V_o}{(0.5-D)T} = C_0 \frac{r_{C0}\%V_o}{(0.5-D)T} \end{cases} \quad (11)$$

2.3. Circuit Analysis in DCM

The SCQSBC is operated in DCM when the light load of converter is applied. The operating of the proposed SCQSBC for DCM analysis is verified in four modes. First when switch S_1 is only turned on, second when S_1 and S_2 are on simultaneously, third when S_1 and S_2 are turned off and an inductor current is nonzero, and fourth when the S_1 and S_2 are turned off and an inductor current is zero. The inductor current reduces to zero at time t_4 . As shown in Figure 2b, intervals t_0-t_1 and t_2-t_3 are mode I, interval t_1-t_2 is mode II, interval t_3-t_4 is mode III, and interval t_4-t_5 is mode IV. Note that the converter is operated in CCM in mode I to mode III.

Mode I (t_0-t_1 and t_2-t_3): For this mode, the operating of the proposed SCQSBC and equivalent circuit are the same as CCM mode I and also depicted in Figure 3a. From the starting point of this mode (time t_0 and t_2-t_3), the inductor current increases linearly from zero and achieves the maximum value at t_3 . The current ripple of inductor in each mode is given:

$$\Delta I_1 = \Delta I_3 = \frac{V_i}{2L}(0.5-D)T \quad (12)$$

Mode II (t_1-t_2): For the mode, the operating of the proposed SCQSBC and circuitry is the CCM analysis mode II. The current ripple of inductor in this mode can be given:

$$\Delta I_2 = \left(\frac{V_i + V_C}{L} \right) DT \quad (13)$$

The maximum current through inductor can be given as follows:

$$I_{L,max} = \left(\frac{V_i/2 + DV_C}{L} \right) T \quad (14)$$

Mode III (t_3-t_4): For the mode, the operating of the proposed SCQSBC and equivalent circuit are the same as CCM mode III. The current ripple of inductor in this mode can be given:

$$\Delta I_4 = \left(\frac{V_i - V_C}{L} \right) D_x T \quad (15)$$

Mode IV (t_4-t_5): The equivalent circuit is depicted in Figure 3c. Switches S_1 and S_2 are remained off and inductor current is at zero level. The capacitor C_o is discharged through resistive load.

According to the condition of CCM/DCM boundary, we have:

$$\bar{I}_L < \Delta I_L / 2 \quad (16)$$

The result of the substitution of (6)–(9) into (11) is as follows:

$$k < k_{crit}(D) \quad (17)$$

where k is a normalized boundary of the converter in DCM, and $k = 36L/(RT)$, $k_{crit} = 1 - 4D^2$.

Figure 4 presents the relationship of k_{crit} and D ; the DCM and CCM boundary region is depicted. Then, the converter operates in CCM at the value $k > k_{crit}$.

Referring to Figure 2b, the average value of inductor current is given by:

$$\bar{I}_L = \Delta I_1 \left(\frac{1}{2} + 2D_x \right) + \Delta I_2 \left(\frac{1}{4} + \frac{D_x}{2} \right) \quad (18)$$

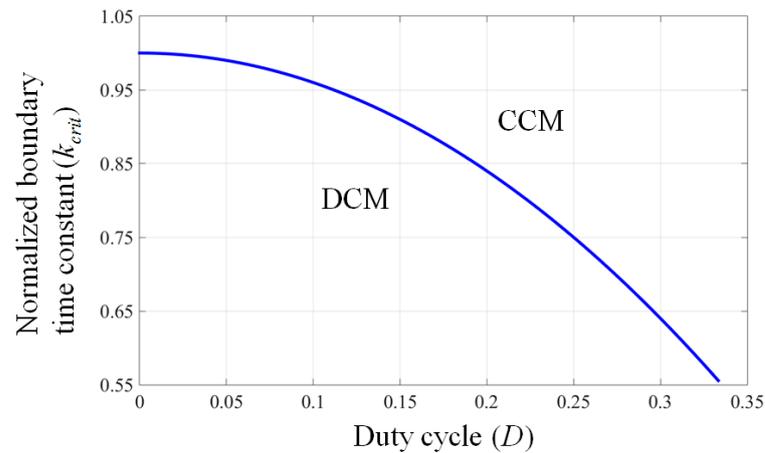


Figure 4. CCM/DCM boundary condition of the SCQSBC.

According to the volt-second balance property of inductor to (13), D_x is calculated:

$$D_x = \frac{V_i/2 + DV_C}{2(V_C - V_i)} \quad (19)$$

From (6), (18), and (19), the output voltage conversion of the SCQSBC in DCM can be verified by:

$$G = \frac{2k + 1 - 2D + \sqrt{4k^2 + (1 - 4D^2)^2}}{2[k - D(1 - 2D)(1 + D)]} \quad (20)$$

3. Designed Guideline

3.1. Selection of Inductor

The rated current of inductor can be determined as the input current and given by (6). The inductor value is selected such that the proposed SCQSBC operates in CCM. Considering the operating mode 2 shown in Figure 3c, the ripple current expression for inductor is given as:

$$\Delta I_L = \frac{V_C - V_i}{2L \cdot f_s} \quad (21)$$

Assuming from (4) and (5) that $\Delta I_L = r_L \% I_L$, inductance L in the function of inductor current ripple is:

$$L = \frac{(1 + 2D)V_i^2}{2(1 - 2D)r_L \% \cdot f_s \cdot P_o} \quad (22)$$

where $r_L \%$, T , and P_o are the inductor current ripple, period, and output power, respectively.

3.2. Selection of Capacitors

Like the parameter design guideline of the inductor, the design of the capacitors can be determined by the rated voltage and capacitance. The rated voltages of the capacitors can be determined from (5). The capacitors in the proposed SCQSBC are designed based on the differential equation of capacitors C_0 , C_1 , and C_2 .

$$\begin{cases} C_1 \frac{\Delta V_C}{0.5T} = \frac{2(1+2D)}{1-2D} I_o \\ C_2 \frac{\Delta V_C}{0.5T} = 2I_o \\ C_0 \frac{\Delta V_o}{0.5T} = I_o \end{cases} \quad (23)$$

By considering the maximum ripple voltages of the capacitors, the capacitances of C_1 , C_2 , and C_0 are determined to be:

$$\begin{cases} C_1 = \frac{2(1+2D)T}{(1-2D)RrC\%} \\ C_2 = \frac{2T}{RrC\%} \\ C_0 = \frac{T}{2RrC\%} \end{cases} \tag{24}$$

3.3. Selection of Switching Components

Generally, to select the parameter design of the switching components including power MOSFETs and diodes in operating safety range, the rated voltage and current of the components must be considered greater than the theoretical values. The voltage rating of the MOSFETs and diodes are presented in (25) and current stresses from (26) and (27), respectively.

$$\begin{cases} V_{S1} = V_{S2} = \frac{2}{1-2D} V_i \\ V_{D0} = V_{D1} = V_{D2} = V_{D3} = \frac{2}{1-2D} V_i \end{cases} \tag{25}$$

$$\begin{cases} I_{S1} = \frac{3-2D}{1-2D} I_o \\ I_{S2} = \frac{4}{1-2D} I_o \end{cases} \tag{26}$$

$$\begin{cases} I_{D0} = I_o \\ I_{D1} = \frac{4}{1-2D} I_o \\ I_{D2} = \frac{2(1+2D)}{1-2D} I_o \\ I_{D3} = 2I_o \end{cases} \tag{27}$$

3.4. Power Loss Analysis

In this section, the power loss of the proposed SCQSBC topology is investigated. The power loss calculation can be validated according to conducting time and conducting current of devices, as shown in Table 1. The power loss distribution is included the MOSFETs, diodes, inductor, and capacitors loss. The power loss of MOSFETs can be given:

$$\begin{aligned} P_M &= P_{Con_S1} + P_{Sw_S1} + P_{Con_S2} + P_{Sw_S2} \\ &= \frac{(9+20D+4D^2)}{2(1-2D)^2} \cdot I_o^2 \cdot R_{DSon} + \frac{(7-2D)}{(1-2D)^2} \cdot V_i \cdot I_o \cdot f_s \cdot (t_{on} + t_{off}) \end{aligned} \tag{28}$$

where R_{DSon} , f_s , t_{on} , and t_{off} are the on-state drain-source resistance, switching frequency, and the turn-on and turn-off times, respectively.

The diode power loss is included the conduction loss and the reverse recovery loss.

$$P_D = P_{Con_D} + P_{Sw_D} \tag{29}$$

The conduction loss of D_0, D_1, D_2 and D_3 diodes is calculated as:

$$\begin{aligned} P_{Con_D} &= \sum_{x=0}^3 P_{Con_Dx} = (u_D \cdot I_o + r_D \cdot I_o^2) \cdot 0.5 + \left[u_D \cdot \frac{4I_o}{1-2D} + r_D \cdot \left(\frac{4I_o}{1-2D} \right)^2 \right] \cdot 0.5 \\ &+ \left[u_D \cdot \frac{2(1+2D)I_o}{1-2D} + r_D \cdot \left(\frac{2(1+2D)I_o}{1-2D} \right)^2 \right] \cdot (1-D) + [u_D \cdot 2I_o + r_D \cdot 4I_o^2] \cdot 0.5 \end{aligned} \tag{30}$$

where u_D and r_D are the ON-state voltage and the ON-state resistance of diodes, respectively. The reverse recovery loss of diodes is given:

$$P_{Sw_D} = \sum_{x=0}^3 P_{Sw_Dx} = 4Q_{rr} \cdot \frac{2V_i}{1-2D} \cdot f_s \tag{31}$$

where Q_{rr} is the reverse recovery charge of diodes.

Table 1. Conducting current and period of devices.

Components	Conducting Current	Conducting Period
S_1	$\frac{3-2D}{1-2D} I_o$	$0.5 \times T$
S_2	$\frac{4}{1-2D} I_o$	$D \times T$
D_0	I_o	$0.5 \times T$
D_1	$\frac{4}{1-2D} I_o$	$(1 - D) \times T$
D_2	$\frac{2(1+2D)}{1-2D}$	$0.5 \times T$
D_3	$2I_o$	$0.5 \times T$
L	$\frac{4}{1-2D} I_o$	T
C_1	$\frac{I_o}{k_C-1}$	$D \times T$
	$\frac{-k_C}{k_C-1} I_o$	$(1 - D) \times T$
C_2	$\frac{k_C-2+2D}{2D(k_C-1)} I_o$	$(0.5 - D) \times T$
	$\frac{2-k_C+4D-8k_CD+4k_CD^2}{2(k_C-1)D(1-2D)} I_o$	$D \times T$
	$\frac{2-k_C-2D}{2D(k_C-1)} I_o$	$0.5 \times T$
C_o	$\frac{-I_o}{1-2D}$	$(0.5 - D) \times T$
	$\frac{2(1+2D)}{1-2D} I_o$	$D \times T$
	$2I_o$	$0.5 \times T$

Power loss of capacitors can be derived by:

$$P_C = r_{C0} \cdot i_{C0_rms}^2 + r_{C1} \cdot i_{C1_rms}^2 + r_{C2} \cdot i_{C2_rms}^2 \quad (32)$$

The RMS current of C_0 , C_1 and C_2 capacitors are derived as:

$$\left\{ \begin{array}{l} i_{C0_rms} = \sqrt{I_o^2 \cdot (0.5 - D) + \left[\frac{2(1+2D)I_o}{1-2D} \right]^2 \cdot D + 4I_o^2 \cdot 0.5} \\ i_{C1_rms} = \sqrt{\left(\frac{I_o}{k_C-1} \right)^2 \cdot D + \left(\frac{k_C}{k_C-1} I_o \right)^2 \cdot (1 - D)} \\ i_{C2_rms} = \sqrt{\left[\frac{(k_C-2+2D)I_o}{2D(k_C-1)} \right]^2 \cdot (0.5 - D) + \left[\frac{(2-k_C+4D-8k_CD+4k_CD^2)I_o}{2D(k_C-1)D(1-2D)} \right]^2 \cdot D + \left[\frac{(2-k_C-2D)I_o}{2D(k_C-1)} \right]^2 \cdot 0.5} \end{array} \right. \quad (33)$$

Power loss of inductor can be given by:

$$P_L = P_{fe} + P_{cu} = k \cdot B^\beta \cdot f_s^\alpha \cdot A_e \cdot l_e + r_L \cdot I_{L_RMS}^2 \quad (34)$$

where B is the AC magnetic flux; f_s is the frequency; A_e is the core cross-sectional area; l_e is the core mean magnetic path length; I_{L_rms} is RMS current of the inductor; and r_L is wire resistance. k , α , β can be found from the manufacturer's datasheet.

4. Comparison with Other High Gain DC-DC Converter

4.1. Voltage Gain and Count of Device Comparison

In this section, the comparison of the performance of the proposed SCQSBC with other high voltage gain converters is reported. Table 2 presents the comparison count of devices used in these converters. According to Table 2, it can be seen that the proposed SCQSBC has one less inductor than AQSC [21] and VPQBC [24], and two less inductors than 3-ZBC [17]. Moreover, it has two less capacitors than the AQSC [21]. Besides, the total number of devices of the proposed converter has the same with the ESBC [22], SCDSBC [23], VPQBC [24], and VPQSBC [24], and less than those of the 3-ZBC [17] and AQSC [21].

The expressions of the voltage gain comparison of the proposed SCQSBC and those of the other high gain converters are shown in Table 2 and also mentioned in Figure 5a. It can be found that the gain of proposed SCQSBC is the highest in compared with other converters through the whole duty cycle lower than 0.33.

Table 2. Comparison of the proposed SCQSCB topology with considered topologies.

	3-ZBC [17]	AQSC [21]	ESBC [22]	SCDSC [23]	VPQBC [24]	VP-QSBC [24]	Proposed SCQSCB
Inductor/Capacitor	4/2	2/4	1/3	1/3	2/3	1/3	1/3
Switch/Diode	1/9	2/4	2/4	2/4	1/4	2/4	2/4
Total of Devices	16	12	10	10	10	10	10
Voltage gain	$\left(\frac{1+D}{1-D}\right)^2$	$\frac{2(1-D)}{1-3D+D^2}$	$\frac{2(1-D)}{1-2D}$	$\frac{3-2D}{1-2D}$	$\frac{2-D}{(1-D)^2}$	$\frac{2}{1-2D}$	$\frac{4}{1-2D}$
Normalized capacitor voltage stress (V_C/V_i)	$\frac{1+D}{1-D}$ $\left(\frac{1+D}{1-D}\right)^2$	$\frac{D}{1-3D+D^2}$ $\frac{1-D}{1-3D+D^2}$ $\frac{2(1-D)}{1-3D+D^2}$	$\frac{D}{1-2D}$ $\frac{1-D}{1-2D}$ $\frac{2(1-D)}{1-2D}$	$\frac{1}{1-2D}$ $\frac{3-2D}{1-2D}$	$\frac{1}{1-D}$ $\frac{1}{(1-D)^2}$ $\frac{2-D}{(1-D)^2}$	$\frac{1}{1-2D}$ $\frac{2}{1-2D}$	$\frac{2}{1-2D}$ $\frac{4}{1-2D}$
Normalized switch voltage stress (V_S/V_i)	$\left(\frac{1+D}{1-D}\right)^2$	$\frac{D}{1-3D+D^2}$ $\frac{1-D}{1-3D+D^2}$	$\frac{D}{1-2D}$ $\frac{1-D}{1-2D}$	$\frac{1}{1-2D}$	$\frac{1}{(1-D)^2}$	$\frac{1}{1-2D}$	$\frac{2}{1-2D}$
Normalized diode voltage stress (V_D/V_i)	$\frac{D}{1-D}$ $\frac{1}{2D(1+D)/(1-D)^2}$ $\frac{1}{(1+D)/(1-D)}$ $\frac{1}{D(1+D)/(1-D)^2}$ $\frac{1}{(1+D)^2/(1-D)^2}$	$\frac{1}{1-3D+D^2}$ $\frac{1-D}{1-3D+D^2}$	$\frac{1-D}{1-2D}$ $\frac{D}{1-2D}$	$\frac{2}{1-2D}$ $\frac{1}{1-2D}$	$\frac{1}{(1-D)^2}$ $\frac{1}{1-D}$ $\frac{D}{(1-D)^2}$	$\frac{1}{1-2D}$	$\frac{2}{1-2D}$
Switch current stress (I_S/I_o)	$\frac{4D}{(1-D)^2}$	$\frac{2}{1-3D+D^2}$ $\frac{1+D-D^2}{D(1-3D+D^2)}$	$\frac{2}{1-2D}$ $\frac{1}{D(1-2D)}$	$\frac{1}{D(1-2D)}$	$\frac{1+D-D^2}{D(1-D)^2}$	$\frac{2}{1-2D}$ $\frac{1}{D(1-2D)}$	$\frac{3-2D}{1-2D}$ $\frac{4}{1-2D}$
Diode current stress (I_D/I_o)	$\frac{D(1+D)/(1-D)^2}{(1+D)/(1-D)}$ $\frac{2D(1+D)/(1-D)^2}{D/(1-D)}$ $\frac{1}{1}$	$\frac{1/D}{1-3D+D^2}$ $\frac{2}{1-D}$	$\frac{1/D}{1-3D+2D^2}$ $\frac{1}{1-D}$ $\frac{2}{1-2D}$	$\frac{1/D}{1-D}$ $\frac{2}{1-2D}$ $\frac{1}{(1-D)(1-2D)}$	$\frac{1/D}{2-D}$ $\frac{2-D}{(1-D)^2}$ $\frac{1}{1-D}$	$\frac{1/D}{(1-D)(1-2D)}$ $\frac{D}{1-2D}$	$\frac{1}{4}$ $\frac{1-2D}{1-2D}$ $\frac{2(1+2D)}{1-2D}$ $\frac{2}{1-2D}$
Inductances	$\frac{D(1+D)k_L}{D(1+D)^3 k_L}$ $\frac{D(1+D)^3 k_L}{(1-D)^2}$	$\frac{2D(1-D)^2 k_L}{1-3D+D^2}$	$\frac{D(1-D)^2 k_L}{1-2D}$	$\frac{D(1-D)(3-2D) k_L}{1-2D}$	$\frac{D(2-D) k_L}{1-D}$ $\frac{D(2-D) k_L}{D k_L}$	$\frac{2D(1-D) k_L}{1-2D}$	$\frac{1+2D}{2(1-2D)} k_L$
Input current ripple	High	Low	High	High	Low	Low	Very low

 k_L is coefficient of inductor.

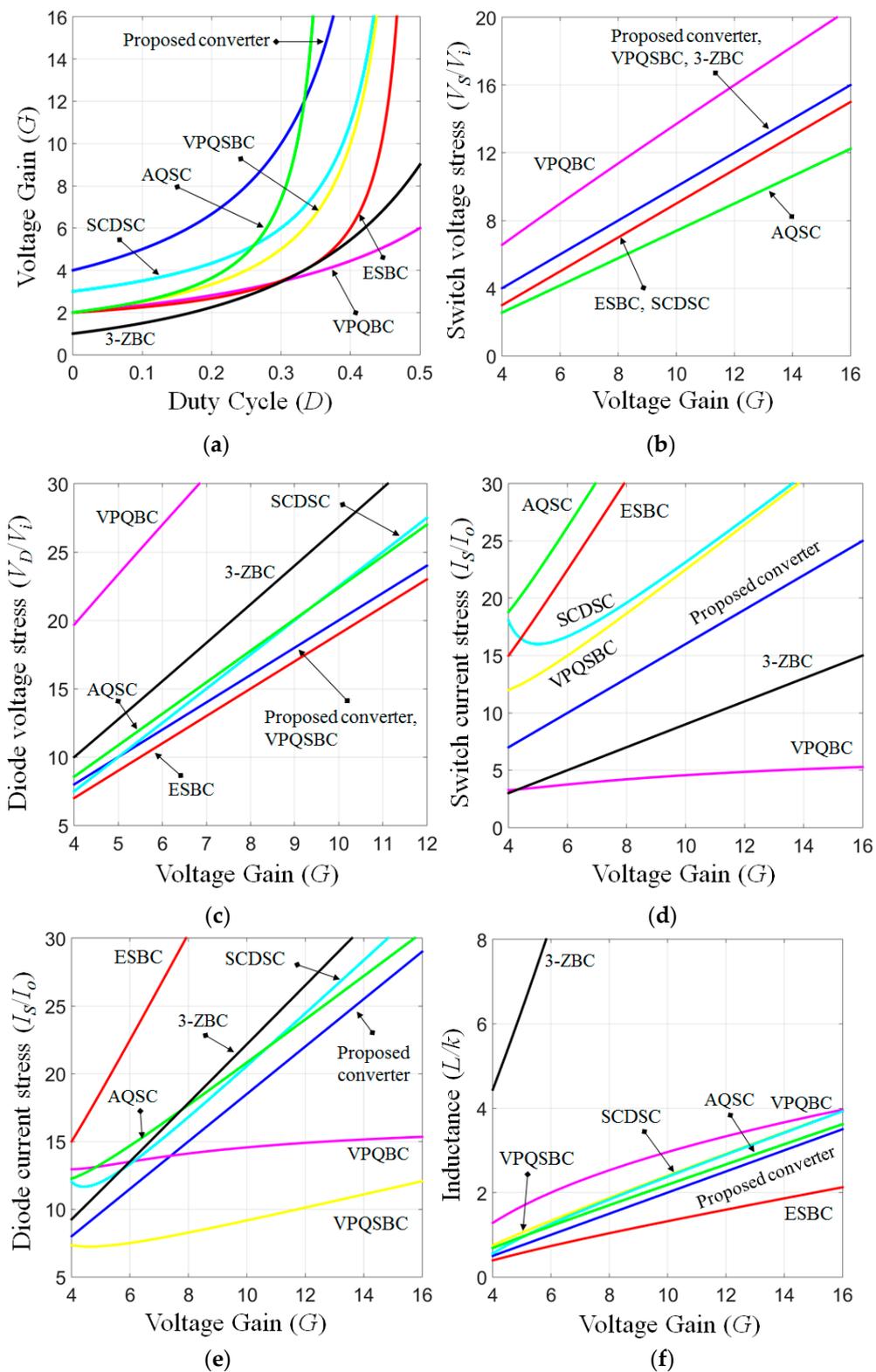


Figure 5. Comparison between the proposed converter and other converters: (a) Voltage gains versus duty cycle, (b) Total voltage rating of switches, (c) Total voltage rating of diodes, (d) Total current rating of switches, (e) Total current rating of diodes, and (f) Inductance.

4.2. Voltage and Current Stress Comparison

The detailed voltage and current rating of the proposed SCQSBC and other converters have been shown in Table 2 to make the comparison. It can be seen that the total normalized voltage and current stress of semiconductor devices have been depicted in Figure 5b,c. From Figure 5b, the switch voltage stress of the proposed SCQSBC is the same as those of the VPQSBC [24] and 3-ZBC [17]. Besides this, it is lower than the switch voltage stress of the VPQBC [24] and higher than those of the ESBC [22], SCDSC [23], and AQSC [21]. Moreover, the diode voltage stress of the proposed SCQSBC and VPQSBC is higher than ESBC [22] and lower than those of other converters.

Figure 5d,e depict the plots of the current stress of switches and diode with other converters. It can be seen that the switch current stress of the proposed SCQSBC is lower than that of the AQSC [21], ESBC [22], SCDSC [23], and VPQSBC [24]. However, the SCQSBC has higher switch current stress than that of the 3-ZBC [17] and VPQBC [24]. This is because they only used one switch. In the diode current stress comparison, the diode current stress of VPQSBC is the lowest. Moreover, the SCQSBC is lower than that of the 3-ZBC [17] and AQSC [21]. AQSC [21], ESBC [22], SCDSC [23], and VPQBC [24] in the whole voltage gain from 0 to 7.4.

4.3. Input Current and Inductor Current Ripple Comparison

Based on Table 2, Figure 5f draws the inductance value curves versus output voltage gain among the mentioned converters. It can be noticed that the inductance of the proposed SCQSBC is lower than that of the 3-ZBC, VPQBC, SCDSC, VPQBC, and AQSC. This makes the size of the magnetic element of the proposed SCQSBC small. Note that the inductance comparison was calculated with applying the same operating condition of input voltage, output power, switching frequency, and inductor current ripple. As summarized in Table 2, the input current ripple is considered for comparison. The diode and capacitor are directly connected to the input voltage source in the 3-ZBC, ESBC, and SCDSC, leading to the occurrence of very high input current ripple in these topologies. In the remaining converters, the input current is equal to the inductor current, so it can be observed that the input current ripple of the proposed SCQSBC is the lowest.

5. Simulation and Experimental Results

In order to verify the precision of the operating capability of SCQSBC, some simulation and experiments have been conducted. For simulation verification, a simulation is built for the SCQSBC parameters are follows: $V_i = 20$ V ($D = 0.3$) and $V_i = 50$ V ($D = 0$), $V_o = 200$ V, $P_o = 250$ W, $L = 0.5$ mH, $C_1 = C_2 = 10$ μ F, $C_0 = 110$ μ F, and all semiconductor devices are ideal. The switching frequencies are 20 kHz and 50 kHz have been tested in the simulation. In two cases, output voltage V_o is 200 V and the voltage stresses across all semiconductor devices and average value of capacitors voltage are half of the output voltage, as shown in Figures 6 and 7. However, the peak-to-peak values of inductor L current and capacitors C_1 , C_2 voltage are increased when the switching frequency is reduced, which are consistent with the calculations obtained in (22) and (24).

The experimental prototype was also designed and shown in Figure 8. The key parameters for the experiment are presented in Table 3. Two power MOSFETs of IRFP4668PbF with low values of r_{DSon} and four Schottky STPS60SM200C diodes were considered to use for the laboratory prototype. The experimental results with the input voltage of 50 V are depicted in Figure 9a,c,e. The obtained waveforms of PWM signals and drain-source of switches S_1 and S_2 are shown in Figure 9a. The switch S_1 has 50% on-state and off-state, while switch S_2 is turned off. In this case, the duty cycle D is zero. The average and peak values of the voltage across switch S_1 are 52 V and 100 V, respectively. The switch S_2 is always off with the peak voltage stress of 100 V. The measured output voltage, capacitor C_1 , C_2 voltage, and input current are 201 V, 100.5 V, 101 V, and 4.3 A, respectively. It can be observed that the input current is continuous with a small ripple, and the peak-to-peak inductor current ripple is 0.85 A. The slope of the input current is magnetizing and demag-

netizing due to the on-state of switch S_1 . The waveform of voltage across the D_0 , D_2 and D_3 diodes are reversed-bias with the peak value of 100 V, while the D_1 diode is always forward-bias, as depicted in Figure 9e. In another case, the converter has been tested with 20 V DC input voltage and the duty cycle is set 0.3, as shown in Figure 9b,d,f. The PWM control signals for S_1 and S_2 are also observed and depicted in Figure 9b, where switch S_1 is still 50% on-state and off-state. However, switch S_2 is turned on with a duty cycle of 0.3. The average and peak values of the voltage rated switch S_1 are 52 V and 101 V, respectively. For switch S_2 , the obtained average and peak values of the voltage across switch S_2 are 72 V and 100 V, respectively. It can be obtained that 200.5 V output voltage is produced and the input current is also continuous with the peak-to-peak inductor current ripple of 1.83 A, and the inductor is just demagnetized due to the off-state of switch S_1 . As depicted in Figure 9f, the voltage stress of the D_0 , D_1 , D_2 , and D_3 diodes are 100 V.

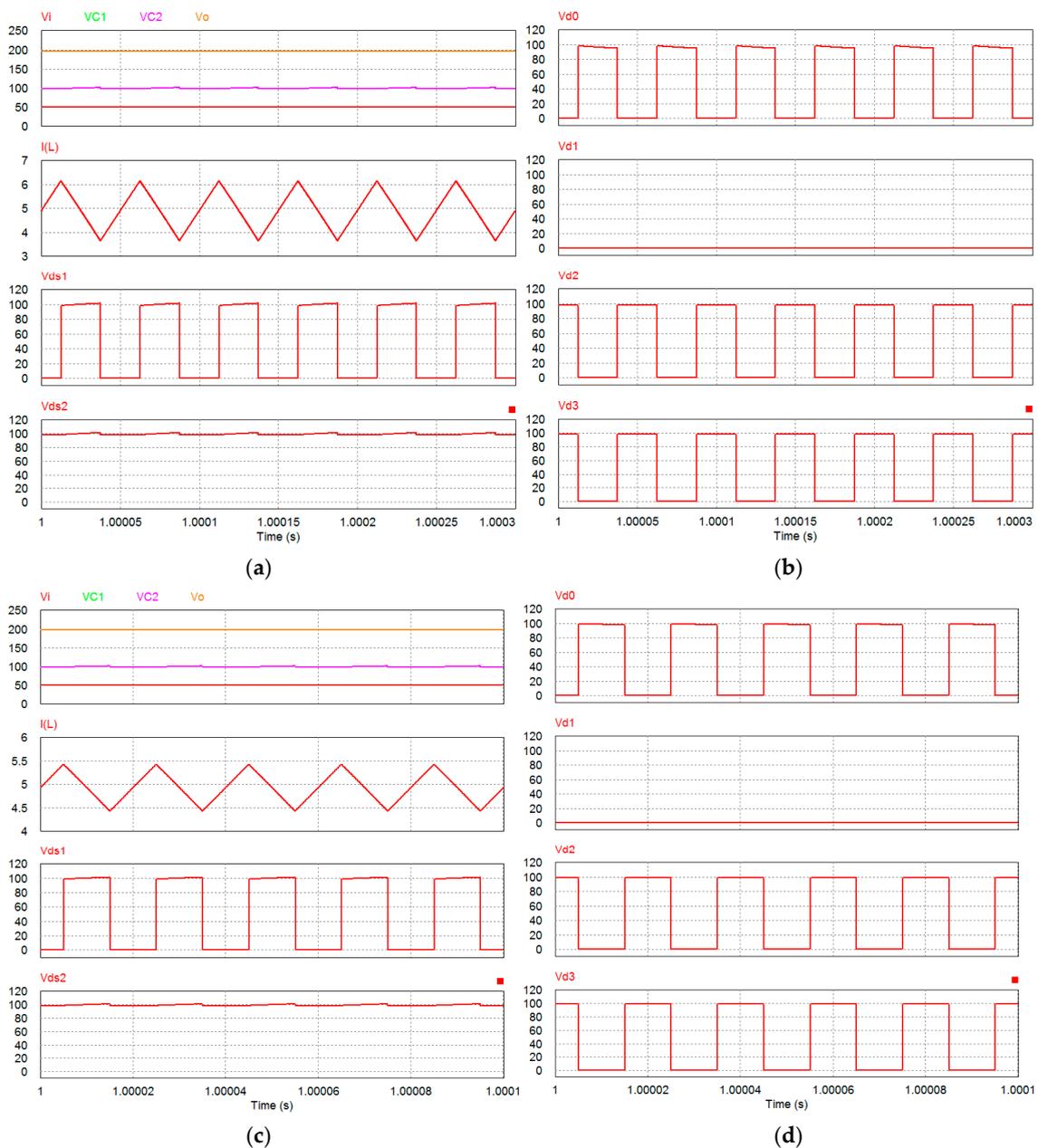


Figure 6. Simulation results with $V_i = 50$ V: (a,b) $f_s = 20$ kHz and (c,d) $f_s = 50$ kHz. From top to bottom: input voltage, output voltage, capacitors C_1 , C_2 voltage; inductor current; the drain-source of switch S_1 and S_2 ; diodes D_0 , D_1 , D_2 and D_3 voltage stress.

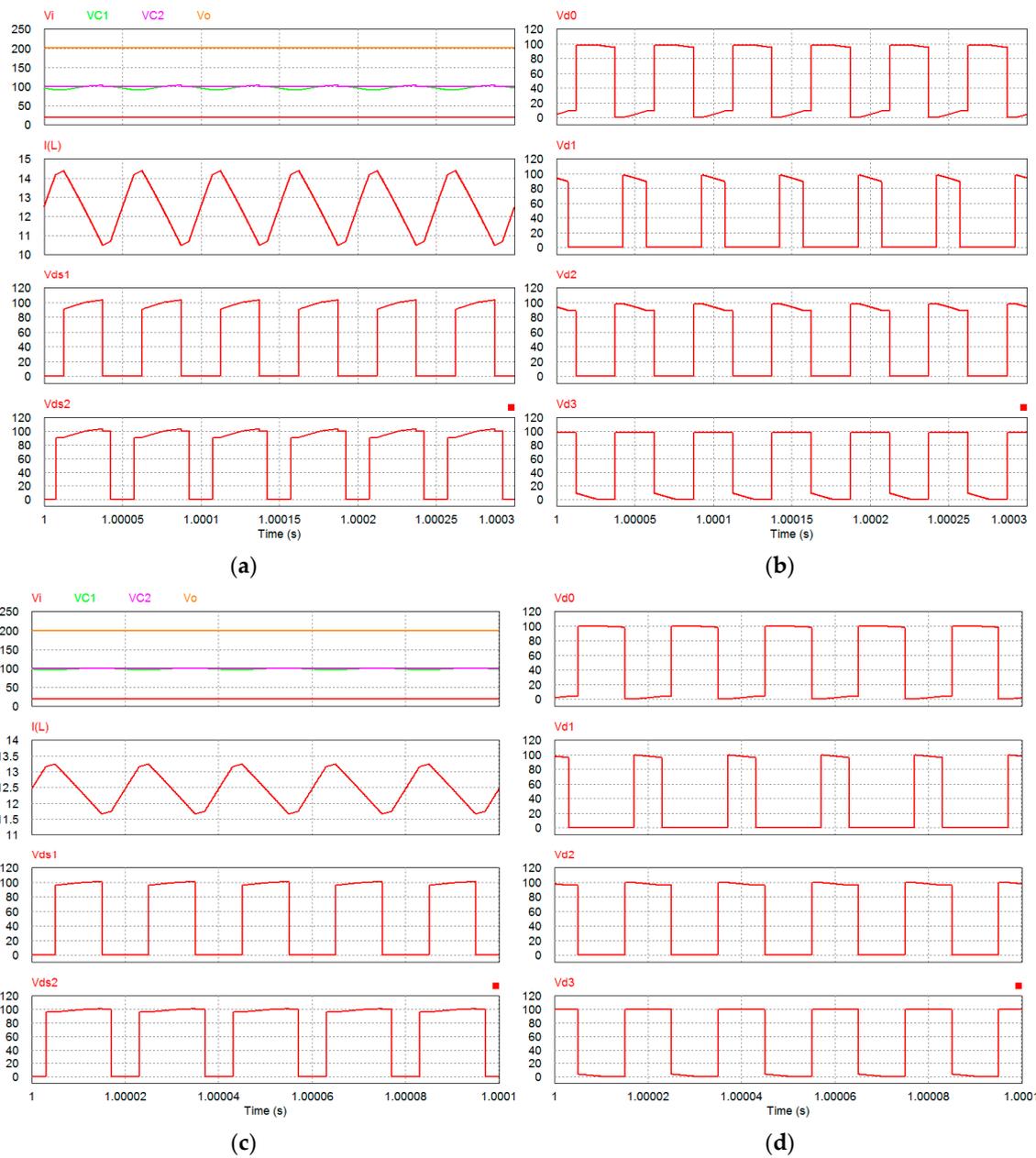


Figure 7. Simulation results with $V_i = 20$ V: (a,b) $f_s = 20$ kHz and (c,d) $f_s = 50$ kHz. From top to bottom: input voltage, output voltage, capacitors C_1 , C_2 voltage; inductor current; the drain-source of switch S_1 and S_2 ; diodes D_0 , D_1 , D_2 and D_3 voltage stress.

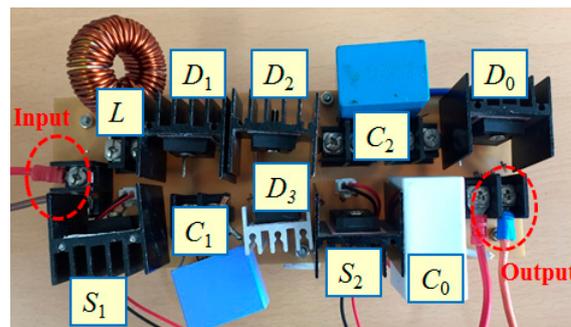


Figure 8. Prototype of proposed SCQSBC.

Table 3. Experimental parameters.

Parameter	Values
Input voltage range	20 V to 50 V
Output voltage	200 V
Power rating	250 W
Inductor (L)	0.5 mH
Capacitors	10 μ F/160 V for C_1, C_2 110 μ F/450 V for C_0
Switching frequency	50 kHz
MOSFETs	IRFP4668PbF
Diodes	STPS60SM200C

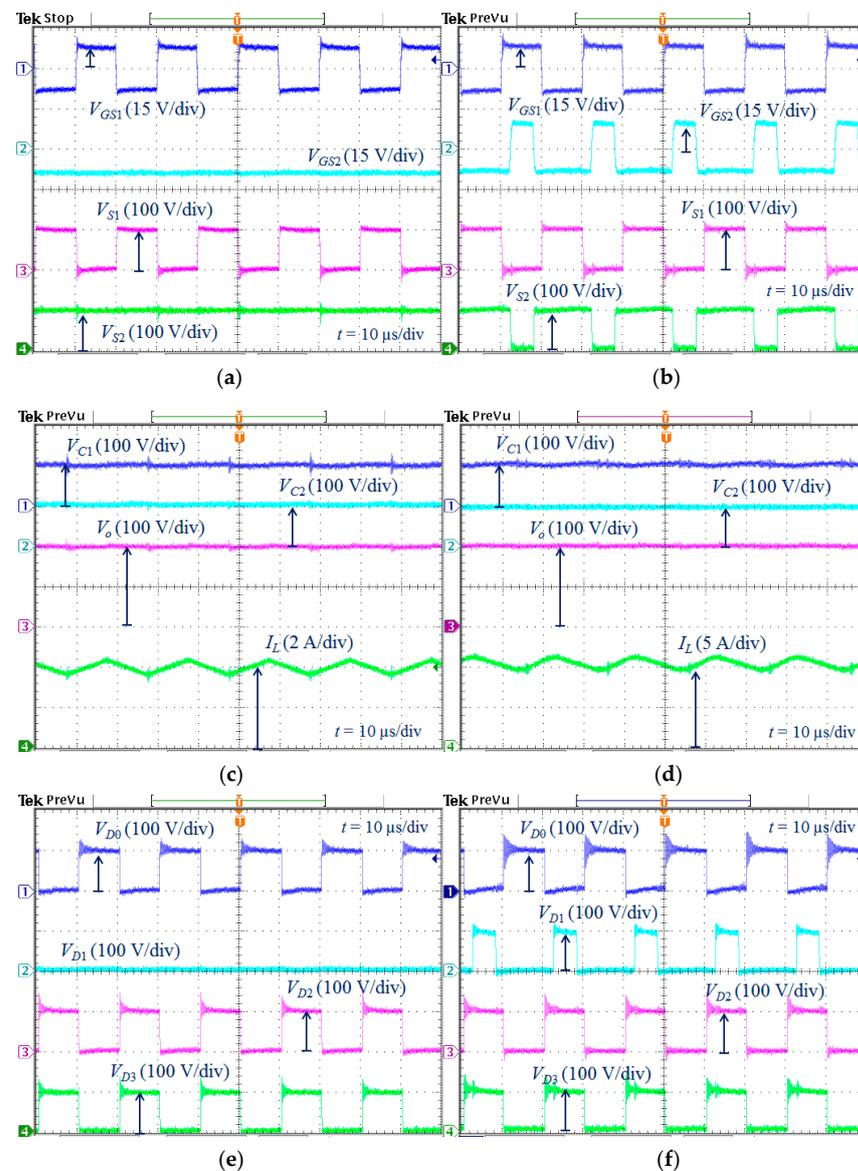


Figure 9. Experimental results with $V_i = 50$ V (left side) and 20 V (right side). (a,b) Bottom to top: The drain-source and gate-source voltage of switch S_1 and S_2 ; (c,d) output voltage, capacitors C_1, C_2 voltage, inductor current; (e,f) diode D_3, D_2, D_1 and D_0 voltage stress.

Based the analysis in Section 3.4 and the parameters in Table 4, the power loss calculation of the proposed SCQSBC is validated. The power loss distribution is depicted in Figure 10 with the input voltages are 20 V and 50 V. It can be observed that the duty cycle is large when $V_i = 20$ V leads to decrease the efficiency of the converter. When the input voltage with 50 V is applied, the efficiency is significantly increased. As shown in Figure 10, the power loss of the diode is highest in the loss distribution; this is because the four diodes were used in the proposed SCQSBC. Table 5 shows the measurement current input ripple and peak-to-peak inductor current ripple and efficiency the proposed SCQSBC and other switched-capacitor-based converters in [24]. In this experiment, the input voltage and output power rating are tested in 20 V and 200 W. It can be seen that the peak-to-peak inductor current ripple of the proposed converter is the lowest. Furthermore, the proposed converter can reduce the size of the inductor of the design when compared with other converters. The input current ripple of the proposed converter is also the lowest.

Table 4. Parameters for power loss analysis.

Parameters		Values
Inductor	Core	CM777125 (142 nH/N ²)
	Copper-wire	0.04 Ω
Capacitors	C_1, C_2	3.2 m Ω
	C_o	4 m Ω
Power switches		IRFP4668PbF (200 V, 130 A, $R_{DSon} = 8$ m Ω)
Power diodes		STPS60SM200C (200V, 30A, $U_D = 0.7$ V)

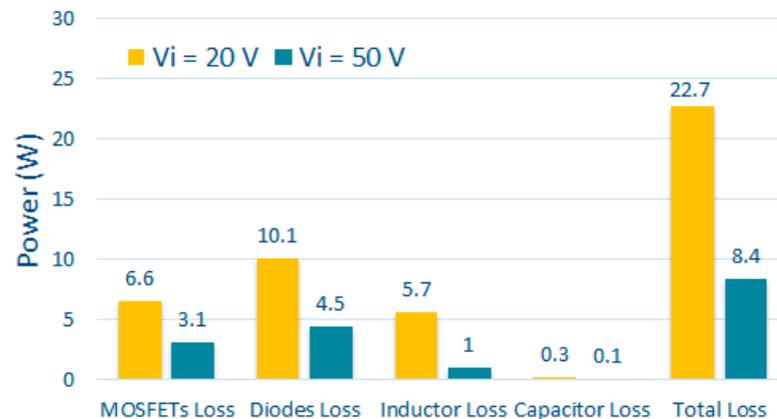


Figure 10. Power loss distribution.

Table 5. Input current ripple and efficiency of VPQBC, VPQSBC, and proposed SCQSBC at $V_i = 20$ V and $P_o = 250$ W.

Converter	VPQBC	VPQSBC	Proposed SCQSBC
ΔI_{in}	1.3 A	1.2 A	0.8 A
Efficiency	91.1%	90.9%	91.8%

The measured efficiencies of ESBC [22], SCDSC [23], and VPQBC–VPQSBC [24] are highlighted compared with the proposed SCQSBC because they used the same number of components with the proposed SCQSBC. To validate the measured efficiency, the experimental parameters in Table 3 are used for specification of the ESBC [22], SCDSC [23], VPQBC–VPQSBC [24], and the proposed SCQSBC. The plot of measurement efficiency versus output power of the proposed converter and other converters are shown in Figure 11

when the input voltages are 20 V and 50 V. In this case, the output power is measured from 80 W to 250 W. When $V_i = 50$ V, the proposed SCQSBC achieves the highest efficiency of 97%. When the input voltage is reduced to 20 V, the efficiency of the proposed converter is greater than that of other converters in comparison.

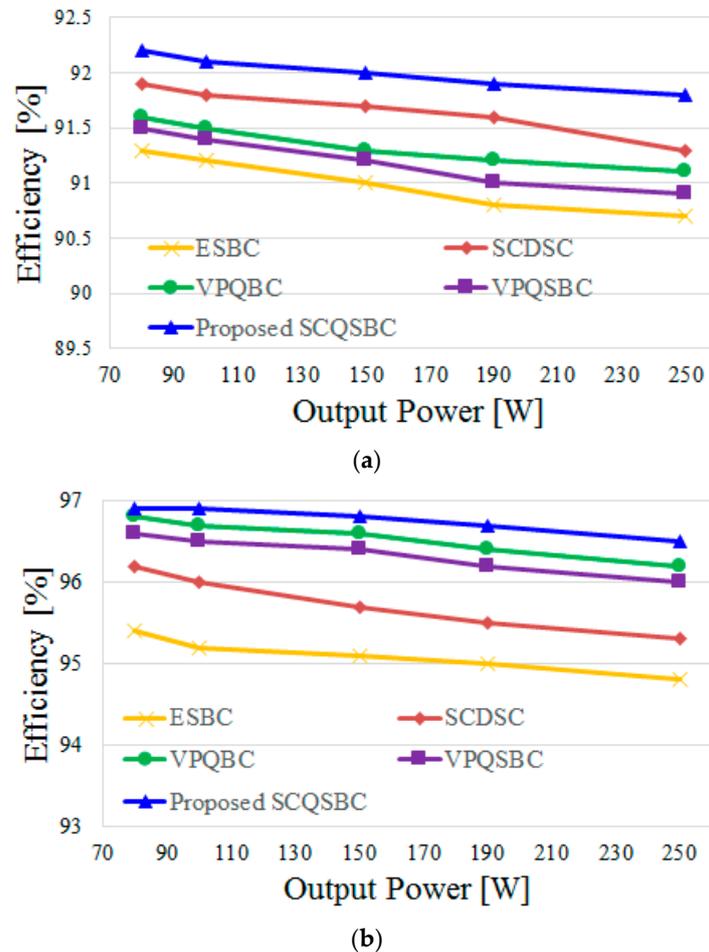


Figure 11. Measured efficiency comparison at (a) $V_i = 20$ V, and (b) $V_i = 50$ V.

The simple PI controller for output voltage loop has been determined to generate the output voltage is 200 V, as shown in Figure 12. The experimental results are shown under the load transient between light load and full load while input and output voltage are 20 V and 200 V, respectively. Moreover, the input voltage adjustment is also considered from 20 V to 50 V. In this case, the output voltage and power are set at 200 V and 200 W, respectively. As depicted in Figure 13, it can be observed that the output voltage of the proposed SCQSBC is insensitive to the load in Figure 13a or input voltage variation in Figure 13b, and settling time of the converter is approximately 0.1 s.

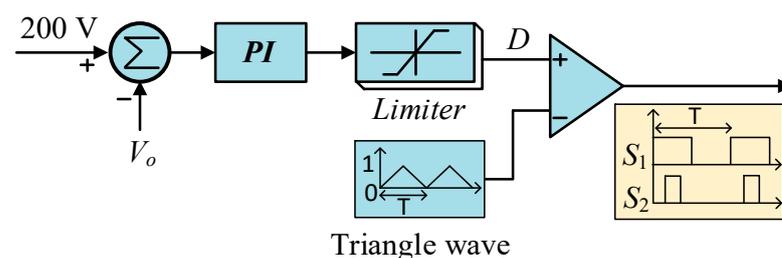


Figure 12. Simple PI controller for the proposed SCQSBC.

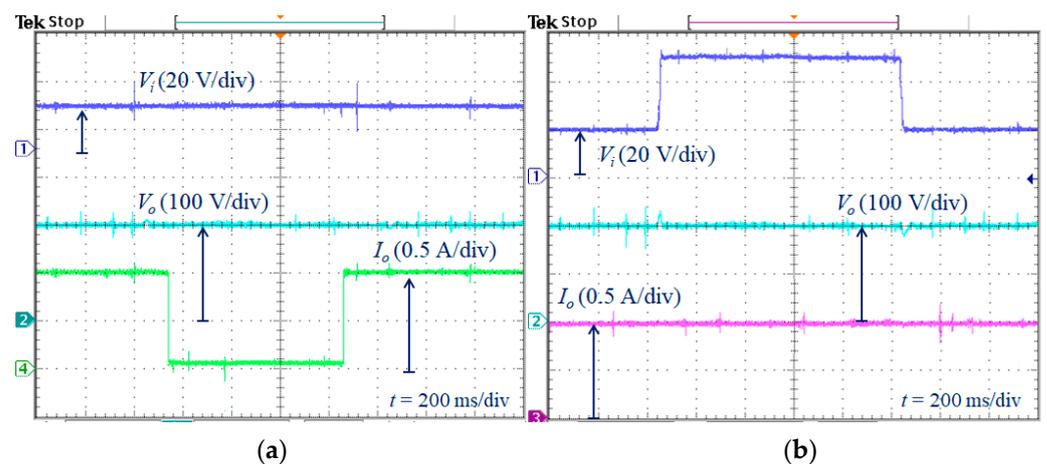


Figure 13. Experimental results with closed-loop control. (a) The load change and (b) Input voltage change.

6. Conclusions

A switched-capacitor-based quasi-switched boost DC-DC converter is presented in this article for low power and high step-up voltage conversion applications. The contributions of the SCQSBC include: providing a high voltage capability with small duty cycle, thereby improving the efficiency of the converter; and a simple topological structure. Moreover, the low input current ripple of the SCQSBC can maintain the lifetime of the power DC sources in renewable energy systems. The theoretical analysis in CCM/DCM boundary condition and parameters design are determined in detail. What is more, the performance comparisons with other transformer-less high gain structures and an experimental verification with single closed-loop controller are provided to demonstrate the characteristics of the proposed SCQSBC. The proposed SCQSBC was suitable for interfacing fuel cells and photovoltaic applications, which required high voltage gain.

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References

- Loana, M.P.C.; Septimiu, L.; Sorin, P.; Dan, L.; Loan, L.; Radu, M. A New Hybrid Inductor-Based Boost DC-DC Converter Suitable for Applications in Photovoltaic Systems. *Energies* **2019**, *12*, 252.
- Abdulaziz, A.; Khairy, S.; Naif, A.; Ahmed, G.A.K.; Hedra, S. Multi-Port PWM DC-DC Power Converter for Renewable Energy Applications. *Energies* **2021**, *14*, 3490.
- Nguyen, M.K.; Duong, T.D.; Lim, Y.C.; Kim, Y.J. Isolated boost DC-DC converter with three switches. *IEEE Trans. Power Electron.* **2018**, *33*, 1389–1398.
- Bin, G.; Jason, D.; Lai, J.S.; Zheng, Z.; Chuang, L. High boost ratio hybrid transformer DC-DC converter for photovoltaic module applications. *IEEE Trans. Power Electron.* **2013**, *28*, 2048–2058.

5. Nguyen, M.K.; Lim, Y.C.; Choi, J.H.; Cho, G.B. Isolated High Step-up DC-DC Converter Based on Quasi-Switched-Boost Network. *IEEE Trans. Ind. Electron.* **2016**, *63*, 7553–7562. [[CrossRef](#)]
6. Francois, F.; Thiery, A.M.; Eric, L.; Bertrand, G.; Jean, J.H.; Julia, C.B. An isolated multicell intercell transformer converter for applications with a high step-up ratio. *IEEE Trans. Power Electron.* **2013**, *28*, 1107–1119.
7. Gang, W.; Xinbo, R.; Zhihong, Y. High step-up DC-DC converter based on switched capacitor and couple inductor. *IEEE Trans. Ind. Electron.* **2018**, *65*, 5572–5579.
8. Yam, P.S.; Frede, B.; Poh, C.L. Quasi-Y-source boost DC-DC converter. *IEEE Trans. Power Electron.* **2015**, *30*, 6514–6519.
9. Hossein, G.; Reza, S.S.; Mir, R.H.; Ebrahim, A.; Gorji, S.A. Design and Implementation a Single-Switch Step-Up DC-DC Converter Based on Cascaded Boost and Luo Converters. *Energies* **2021**, *14*, 3584.
10. Lee, S.W.; Do, H.L. Quadratic Boost DC-DC Converter with High Voltage Gain and Reduced Voltage Stresses. *IEEE Trans. Power Electron.* **2019**, *34*, 2397–2404. [[CrossRef](#)]
11. Javed, A.; Mohammad, Z.; Adil, S.; Lin, C.H.; Mohammed, A.; Raj, K.Y.; Mohd, T.; Kuntal, S.; Basem, A. A New High-Gain DC-DC Converter with Continuous Input Current for DC Microgrid Applications. *Energies* **2021**, *14*, 3629.
12. Ahmad, A.; Pourya, S.; Mehdi, F. Interleaved Multistage Step-Up Topologies with Voltage Multiplier Cells. *Energies* **2020**, *13*, 5990.
13. Ebrahim, B.; Hamed, M.M.; Mehran, S.; Seyed, H.H. Extendable Nonisolated High Gain DC-DC Converter Based on Active–Passive Inductor Cells. *IEEE Trans. Ind. Electron.* **2018**, *65*, 9478–9487.
14. Sajad, R.; Vahid, A.; Frede, B. Implementation of a common grounded Z-source dc-dc converter with improved operation factors. *IET Power Electron.* **2019**, *12*, 2245–2255.
15. Veda, P.G.; Marian, K.K. Analysis of PWM Z-source dc-dc converter in CCM for steady state. *IEEE Trans. Circuits Syst. I Reg. Pap.* **2012**, *59*, 854–863.
16. Punit, K.; Mummadi, V. Z-network plus switched-capacitor boost dc-dc converters. *IEEE J. Emerg. Sel. Top. Power Electron.* **2021**, *9*, 791–803.
17. Guidong, Z.; Bo, Z.; Zhong, L.; Dongyuan, Q.; Liqiang, Y.; Wolfgang, A.H. A 3-Z-network boost converter. *IEEE Trans. Ind. Electron.* **2015**, *62*, 278–288.
18. Santanu, M.; Ravindranath, A.; Avinash, J. Inverse Watkins-Johnson topology based inverter. *IEEE Trans. Power Electron.* **2012**, *27*, 1066–1070.
19. Nguyen, M.K.; Le, T.V.; Park, S.J.; Lim, Y.C. A class of quasi-switched boost inverters. *IEEE Trans. Ind. Electron.* **2015**, *62*, 1526–1536. [[CrossRef](#)]
20. Alencar, F.D.S.; Fernando, L.T.; Enio, R.R. Switched Capacitor DC-DC Converters: A Survey on the Main Topologies, Design Characteristics, and Applications. *Energies* **2021**, *14*, 2231.
21. Xiaoquan, Z.; Bo, Z.; Ke, J. Hybrid nonisolated active quasi-switched DC-DC converter for high step-up voltage conversion applications. *IEEE Access* **2020**, *8*, 222584–222598.
22. Xiaoquan, Z.; Bo, Z.; Zhong, L.; Hong, L.; Li, R. Extended switched-boost DC-DC converters adopting switched-capacitor cells for high step-up conversion. *IEEE J. Emerg. Sel. Topics Power Electron.* **2017**, *5*, 1020–1030.
23. Nguyen, M.K.; Duong, T.D.; Lim, L.C. Switched-capacitor-based dual-switch high-boost dc-dc converter. *IEEE Trans. Power Electron.* **2018**, *33*, 4181–4189. [[CrossRef](#)]
24. Guidong, Z.; Zhiyang, W.; Samson, S.Y.; Si, Z.C.; Bo, Z.; Herbert, H.C.I.; Yun, Z. A generalized additional voltage pumping solution (GAVPS) for high-step-up converters. *IEEE Trans. Power Electron.* **2019**, *34*, 6456–6467.