Article

Distortion Due to the Zero Current Detection Circuit in High Power Factor Quasi-Resonant Flybacks

Claudio Adragna ¹, Giovanni Gritti ¹, Santi Agatino Rizzo ^{2,*} and Giovanni Susinni ²

¹ Industrial and Power Conversion Division Application Laboratory, STMicroelectronics S.R.L., 20864 Agrate Brianza, Italy; claudio.adragna@st.com (C.A.); giovanni.gritti@st.com (G.G.)

² Department of Electrical, Electronic and Computer Engineering, University of Catania, 95125 Catania, Italy; giovanni.susinni@unict.it

* Correspondence: santi.rizzo@unict.it; Tel.: +39-09-5738-2308

Abstract: In a high-power factor quasi-resonant Flyback, an ideal zero current detection (ZCD) circuit and control circuitry enable the power switch turn-on in the exact instant a zero ringing current is reached after demagnetization. A nonzero current at the turn-on instant affects the input current shape and; consequently, affects its Total Harmonic Distortion (THD). This paper firstly deeply analyzes the effect on the distortion due to a nonideal ZCD circuit. After, some typical implementations of the ZCD circuit and their effect on the THD are analyzed, identifying their pros and cons. Finally, some experimental results are obtained to validate the analytical investigation.

Keywords: converter control; power factor correction; total harmonic distortion; flyback; solid-state lighting

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1. Introduction

The Flyback topology circuit represents one of the most attractive dc-dc converters used for low and medium power applications. To date, the Flyback converters have been widely employed as USB chargers for cell phones, notebooks, LCD TVs, and LED drivers [1–6]. The key factors that make this solution very popular are related to the simple design of the conversion stage, high efficiency, inexpensive cost of the components, possible multiple isolated output stages, and high output voltage.

It is worth remembering that the Flyback topology has been widely studied in the literature, where several advantageous results with respect to other converter topologies have been pointed out. In this perspective, the authors in [7] have compared the performance between a flyback, a buck-boost, and a hybrid solution [8–14] in terms of some key factors (e.g., cost, efficiency, step-down ability, etc.). The comparison has highlighted the superior performance of the flyback converter, which makes it the preferred choice for countless dc-dc power applications.

The flyback converter can be summarized into two different operating modes. When the current in the secondary windings goes to zero before the OFF time of the power switch, the Flyback operates in discontinuous conduction mode (DCM). On the other hand, when the current in the primary windings is greater than zero before the OFF time is complete, the converter operates in the continuous conduction mode (CCM) [15].

In many applications, the flyback converter can be used with a feedback control loop, with the aim to sense the voltage and current variations of the output. Generally, an optocoupler is used to sense the output voltage and in addition, it provides electrical isolation (SSR—secondary side regulation). Nevertheless, the use of an optocoupler presents a few disadvantages [16]. Indeed, the current transfer ratio may be subjected to variation due to the temperature, and furthermore, the optocoupler introduces an undesired pole in the feedback loop, which may lead to an instability of the converter.

On the other hand, the adoption of the constant-current primary sensing regulation (CC-PSR) technique [3,4], the feedback loop at the output(secondary) side is not used and consequentially, the output voltage can be adjusted by using only the control method of the electrical quantities in the primary side. This leads to a save cost and the power losses are strongly reduced. More specifically, in this configuration, only the auxiliary winding is used to sense the output voltage. It is worth underlining that this approach brings greater safety and reliability. As a disadvantage, the primary-side control may result in less accuracy in comparison to the feedback conventional method.

The high-power-factor (Hi-PF) flyback converter is one of the most popular topologies used in low-medium power applications (e.g., LED drivers that feed from the ac power line [17–20]). It has been widely used due to its low input current distortion (low THD) and it guarantees high safety isolation. Furthermore, it is easily suitable for CC-PSR operation [21–23]. The Hi-PF flyback converters can be used with a fixed switching frequency and in the DCM mode (FF-DCM) [24,25]. This mode operation is theoretically able to obtain unity power factor and zero THD.

Furthermore, the Hi-PF flyback converters can also be used in the Quasi-Resonant (QR) mode, where the switching period depends on transformer demagnetization. It presents several advantages compared to FF-DCM such as valley-switching, (almost zero-voltage switching, ZVS) and low EMI emissions. However, its standard implementation guarantees a sinusoidal envelope of the peaks of the primary current. This cannot achieve a very low THD of the input current, as widely discussed in [22–27]. However, more recently, an enhanced QR control method [28] able to provide Hi-PF QR flyback converters with the ability to ideally get a sinusoidal input current has been disclosed.

In this paper, the contribution to the distortion of the input current in a Hi-PF Flyback converter due to a nonzero current at the turn-on instant of the power switch in a switching cycle has been discussed in depth.

Firstly, the general trend of the impact of a nonzero current at the turn-on instant on the input current shape and, ultimately, on its THD is analyzed with both the traditional (QR) method and the enhanced QR (EQR) method. Secondly, this impact is analyzed more in detail with reference to some typical implementations of the zero current detectors (ZCD) circuit responsible for determining the turn-on instant of the power switch.

It is worth underlining that both the quantitative and the qualitative effects of a nonzero initial current due to the implementation of the zero-current detection circuit have not been yet documented in the literature.

Finally, several experimental results showing the aforementioned contributions in a couple of prototypes of Hi-PF Flyback converter controlled with both the traditional QR method and the enhanced QR method are presented.

2. Review of the Hi-PF QR Flyback Converter and Its Control Methods

A flyback converter (whether Hi-PF or not) is said to be QR-operated when the turn-on of the power switch (usually a MOSFET) is synchronized to the instant when the transformer demagnetizes (i.e., as the secondary current becomes zero), normally after an appropriate delay. In this way, the turn-on can be commanded on the valley of the drain voltage ringing that follows the demagnetization, thus with minimum turn-on losses. For this reason, this operation is often termed “valley-switching”.

A Hi-PF QR flyback converter, whose principle schematic and relevant key waveforms are shown in Figures 1 and 2 respectively, is powered from the ac power line with no energy reservoir capacitor after the input bridge rectifier (C_{in} serves as a high-frequency smoothing filter). Thus, its input voltage is essentially a rectified sinusoid ($V_{IN}(\theta) = V_{PK} |\sin(\theta)|$) and the current $I_{AC}(\theta)$ drawn from the power line is sinusoidal-like (the rectified input current $I_{IN}(\theta)$ downstream the bridge is $|I_{AC}(\theta)|$). In these expressions and in the following discussion, V_{PK} is the peak line voltage, $\theta = 2\pi f_L t$ is the instantaneous phase angle of the line voltage, f_L is the line frequency. Note also that uppercase subscripts will refer to quantities considered on a line cycle time scale, lowercase subscripts to quantities

considered on a switching cycle time scale. Circuit parameters have a lowercase subscript, dc quantities do not have subscripts.

Figure 1. Principle schematic of a Hi-PF QR flyback converter.

Figure 2. Key waveforms of the circuit in Figure 1; switching cycle time scale (a), line cycle time scale (b). In the second diagram from top on the right-hand side, black and blue shapes are the envelopes of primary and secondary current with EQR control; light grey and dark grey shapes are the same with QR control.

With no loss of generality, whichever type of feedback -SSR or PSR- is used, it is possible to assume that the error signal is processed producing a control voltage V_c that controls the input-to-output power flow. Being a Hi-PF system, the open-loop bandwidth

of the overall control loop is very narrow—typically below 20 Hz—and under steady-state operation, V_c can be regarded as a dc level, at least to a first approximation.

Considering peak current mode control, the turn-off of the power switch is determined by the current sense signal reaching the value programmed by the control loop that regulates V_{out} or I_{out} via V_c . This value is set by the reference $V_{csREF}(\theta)$ output by the “Current reference generator” block that receives at its inputs the control voltage V_c , the voltage $V_{MULT}(\theta)$ —a scaled-down image of the input voltage $V_{IN}(\theta)$ that serves as a sinusoidal template—and, in case, the output Q of the PWM latch.

In fact, $V_{csREF}(\theta)$ is fed into the inverting input of the PWM comparator that receives the voltage $V_{cs}(t, \theta)$ on the other input. $V_{cs}(t, \theta)$ is sensed across the sense resistor R_s , which is proportional to the instantaneous current $I_p(t, \theta)$ flowing through the primary winding L_p and the power switch M when this is in the on state. Assuming that the PWM latch is set (and M turned on) at $t = 0$, the current $I_p(t, \theta)$ will be ramping up linearly and so will do $V_{cs}(t, \theta)$; at the instant $t = T_{ON}$, when $V_{cs}(T_{ON}, \theta) = V_{csREF}(\theta)$, i.e., $I_p(T_{ON}, \theta) = V_{csREF}(\theta)/R_s$, the PWM comparator resets the PWM latch, thus switching off M .

As M is switched off, most of the energy stored in L_p is transferred to the secondary winding L_s so that current starts flowing through L_s and D , dumping this energy into the output capacitor C_{out} and the load. As L_s is completely demagnetized (i.e., the current through L_s zeroes) the diode D opens. The drain voltage V_{ds} , which was fixed at $V_{IN}(\theta) + V_R$ ($V_R = nV_{out}$) while D was conducting, starts oscillating around the instantaneous line voltage $V_{IN}(\theta)$ due to the resonance of the parasitic capacitance of the drain node (C_{ds}) with L_p . The quick drain voltage fall that marks the onset of this ringing is coupled to the ZCD block in the controller through the auxiliary winding L_{aux} and the resistor R_{zcd} . The ZCD block releases a pulse as it detects the negative-going edge and this pulse sets the PWM latch and turns on the power switch M , starting a new switching cycle.

Therefore, the shape of $V_{csREF}(\theta)$ determines the shape of the envelope of the peak primary current $I_{pPK}(\theta) = I_p(T_{ON}, \theta) = V_{csREF}(\theta)/R_s$ and, in turn, that of the average inductor current, i.e., the rectified input current $I_{IN}(\theta)$ and ultimately the current $I_{AC}(\theta)$ drawn from the power line. The way the “Current reference generator” block combines the input signals V_c and $V_{MULT}(\theta)$ (and, in case, Q) to produce the reference $V_{csREF}(\theta)$ defines the control method.

With the traditional control method [27], which in the following discussion will be referred to as the “QR method”, the reference $V_{csREF}(\theta)$ is defined by the relationship:

$$V_{csREF}(\theta) = K_M V_c V_{MULT}(\theta) \quad (1)$$

where K_M is a constant (multiplier gain, dimensionally $1/V$). Being V_c a dc level and $V_{MULT}(\theta)$ a rectified sinusoid, the peaks of the primary current will be enveloped by a sinusoid:

$$I_{pPK}(\theta) = \frac{V_{csREF}(\theta)}{R_s} = I_{PPK} \sin \theta, \quad (2)$$

where I_{PPK} is the peak value of the envelope $I_{pPK}(\theta)$. With this method there is an inherent distortion in the input current because the input current flows only during the on-time T_{ON} of the power switch M . Assuming that the turn-on of the power switch is commanded in the instant when the transformer demagnetizes (i.e., assuming $T_V = 0$, see Figure 2 right-hand side), T_{ON} is constant along a line cycle whereas the switching period T is not [27]. The rectified input current is, therefore:

$$I_{IN}(\theta) = I_{PPK} \frac{T_{ON}}{T(\theta)} \sin \theta \quad (3)$$

In [28] an enhanced control method was proposed that produces a reference $V_{csREF}(\theta)$ related to the input signals by the relationship:

$$V_{csREF}(\theta) = K_M V_c V_{MULT}(\theta) \frac{T(\theta)}{T_{ON}(\theta)} \quad (4)$$

In this way, the peak primary current envelope will not be sinusoidal:

$$I_{pPK}(\theta) = \frac{V_{CSREF}(\theta)}{R_s} = I_{PPK} \frac{T(\theta)}{T_{ON}(\theta)} \sin \theta \quad (5)$$

but, considering again the approximation $T_V = 0$, the rectified input current will be:

$$I_{IN}(\theta) = I_{PPK} \sin \theta, \quad (6)$$

so that, in this case, I_{PPK} coincides with the peak value I_{PK} of both $I_{IN}(\theta)$ and $I_{AC}(\theta)$. As previously mentioned, we will refer to this enhanced method as the “EQR method”.

3. Input Current Distortion Due to Power Processing: A Closer Look

The simplification $T_V = 0$ used to determine the shape of the rectified input current $I_{in}(\theta)$ described by (3) for the QR method and (6) for the EQR method leads to neglecting the contribution to $I_{IN}(\theta)$ provided by the negative inductor current that flows during this time interval.

The distortion caused by this negative current is discussed in [7], where the analysis has been carried out based on the equivalent circuit depicted in Figure 3. This has been done under the simplifying assumption that the primary current in the instant when M is turned on to start a new switching cycle is zero (Zero-current switching at turn-on, ZCS), as shown in the timing diagrams of Figure 4. Notice that this is equivalent to saying that M is turned on with ZVS (Zero-voltage switching) if $V_{IN} \leq V_R$ and with valley-switching if $V_{IN} > V_R$.

Figure 3. Simplified equivalent circuit of primary side after transformer’s demagnetization.

Figure 4. Key waveforms of the circuit in Figure 2 with $V_{IN} \leq V_R$ and zero-current switching (left); with $V_{IN} > V_R$ and valley switching (right). DCM waveforms (dotted lines) are shown for reference.

Assuming that $t = 0$ is the instant when the transformer demagnetizes (i.e., when secondary current zeroes and ringing starts) and t_{ON} the instant when the power switch is turned on, this condition can be labeled as $t_{ON} = T_{neg}$. The results of the analysis, as well as the definition of the relevant timing and electrical quantities, are summarized in Table 1.

Table 1. Timings and primary current characteristics of Hi-PF QR flyback converters assuming that current in the turn-on instant of power switch M is zero ($t_{ON} = T_{neg}$).

Symbol	Definition	Expression
T_{ON}	Duration of ON-time of power switch M	$\frac{L_p I_{ppk}}{V_{IN}}$
T_{FW}	Time needed for secondary current I_s to ramp linearly from I_{spk} down to zero	$\frac{L_s I_{spk}}{V_{out}} = \frac{L_p I_{ppk}}{V_R}$
T	Switching period	$T_{pos} + T_{FW} + T_{neg}$
T_r	Period of drain voltage ringing after demagnetization	$2\pi \sqrt{L_p C_{ds}}$
T_{pos}	Duration of positive portion of primary current I_p .	T_{ON}
T_z	Time needed for drain voltage V_{ds} to fall to zero when $V_{IN} \leq V_R$ or to a minimum when $V_{IN} > V_R$	$\begin{cases} V_{IN} \leq V_R & \frac{T_r}{2} \left(1 - \frac{1}{\pi} \cos^{-1} \frac{V_{IN}}{V_R}\right) \\ V_{IN} > V_R & \frac{T_r}{2} \end{cases}$
T_{zz}	Time needed for primary current I_p to ramp linearly from $I_p(T_z)$ to zero when $V_{IN} \leq V_R$. To be considered equal to zero when $V_{IN} > V_R$	$\begin{cases} V_{IN} \leq V_R & \frac{T_r}{2\pi} \frac{V_R}{V_{IN}} \sqrt{1 - \left(\frac{V_{IN}}{V_R}\right)^2} \\ V_{IN} > V_R & 0 \end{cases}$
T_{neg}	Duration of negative portion of primary current I_p	$\begin{cases} V_{IN} \leq V_R & T_z + T_{zz} \\ V_{IN} > V_R & \frac{T_r}{2} \end{cases}$
Q_{pos}	Positive charge taken from input source during T_{pos} in a switching cycle	$\frac{I_{pk} T_{pos}}{2}$
Q_{neg}	Negative charge returned to input source during T_{neg} in a switching cycle	$-\frac{C_{ds}}{2} \frac{(V_{IN} + V_R)^2}{V_{IN}}$
$\langle I_p \rangle^*$	Average input current in a switching cycle	$\frac{Q_{pos} + Q_{neg}}{T}$

The ZCS assumption is not always true in practice, because the control circuit that initiates a new switching cycle upon detecting the transformer's demagnetization (ZCD circuit) is not always realized in such a way that the power switch M can be always turned on in the exact instant when the ringing current after demagnetization zeroes.

3.1. Effects of a Nonzero Current at the Turn-on Instant of the Power Switch M

A nonzero current at the turn-on instant will alter the Q_{pos} and/or the Q_{neg} contribution in a switching cycle and this, in turn, will have an impact on the input current shape and, ultimately, on its THD. Both the quantitative and the qualitative effects of this impact have not been analyzed in the existing literature and will be addressed in this section.

The impact is different depending on whether one analyzes the open-loop operation (i.e., with assigned input and output voltages and a profile of the peak primary current $I_{pPK}(\theta)$ having a fixed amplitude) or the closed-loop operation. In this second case, the input voltage is assigned but the amplitude of the profile of the peak primary current $I_{pPK}(\theta)$ is determined by the control loop to deliver the average power demanded by the load in a line cycle with a regulated output voltage or current.

The analysis carried out in this section refers to the open-loop operation.

In the following analysis, the definitions of the quantities considered in Table 1 do not change. To distinguish the quantities related to the $t_{ON} \neq T_{neg}$ case from those related to the $t_{ON} = T_{neg}$ case, the former ones will have an "*" superscript.

It is worth reminding that instantaneous values of all time-varying quantities are considered a function of the phase angle $\theta = 2\pi f_L t$ when considering their evolution on a line cycle time scale. Instantaneous values of those quantities that vary within a switching cycle as well are a function of both phase angle and time, being intended that time extends over a single switching cycle, during which the phase angle can be considered constant. To simplify the notation, these dependences will not be explicitly indicated.

We will consider two fundamental cases.

- Case I: $0 < t_{ON} < T_{neg}$ (refer to Figure 5)

In this hypothesis, the initial current $I_p(t_{ON})$ is negative and $T_{ON} > T_{pos}$. Q_{neg} may be affected by the t_{ON} value; considering an open-loop operation, Q_{pos} and T_{pos} will not be affected, in closed-loop operation they will be: a different Q_{neg} value due to a different t_{ON} value needs to be compensated by an opposite change in Q_{pos} so that the input current to the converter is such that the average power delivered to the load in a line cycle does not change. T_{pos} will need to change accordingly.

Figure 5. Close-up of primary current with $t_{ON} < T_{neg}$. Dashed lines, which refer to the case $t_{ON} = T_{neg}$, are shown for reference. The diagonally striped area marks the interval where T_{neg}^* and Q_{neg}^* are not affected by t_{ON} position (subsubcase I a2).

We need to distinguish two subcases.

- Subcase I(a): $V_{IN} \leq V_R$.

We need to distinguish two further subdivisions.

- Subsubcase I(a1): $0 < t_{ON} \leq T_z$.

In this case, the sinusoidal portion of the negative current will be truncated by the turn-on of the power switch before the drain voltage touches zero. Turn-on will not be exactly ZVS (Zero-voltage switching). The duration of the negative portion of the primary current will be reduced ($T_{neg}^* < T_{neg}$) and so will be Q_{neg}^* .

- Subsubcase I(a2): $T_z < t_{ON} \leq T_{neg}$.

In this case, the turn-on of the power switch occurs while the primary current, though negative, is already ramping up linearly as if the power switch were turned on at $t = T_z$. Turn-on will still be exactly ZVS. Both T_{neg}^* and Q_{neg}^* will be unaffected ($T_{neg}^* = T_{neg}$, $Q_{neg}^* = Q_{neg}$).

- Subcase I(b): $V_{IN} > V_R$.

The situation becomes similar to that when $V_{IN} \leq V_R$: current is sinusoidal until $t = t_{ON}$, after that it is a linear ramp. Turn-on will occur before the drain voltage reaches the valley, so valley switching will be lost. Both T_{neg}^* and Q_{neg}^* will be reduced.

The results of this analysis are summarized in Table 2, where T_z is that defined in Table 1 (it is unaffected by t_{ON} and is not shown).

The diagrams in Figure 6 show how T_{neg}^* and Q_{neg}^* vary as a function of the ratio V_{IN}/V_R for different values of t_{ON} . Values are normalized to those for $V_{IN} > V_R$ ($T_r/2$ and $2 V_R C_{ds}$ respectively). The diagrams in Figure 7 show how T_{neg}^* and Q_{neg}^* vary with t_{ON} for different values of the ratio V_{IN}/V_R . Values are normalized in the same manner.

- Case II: $T_{neg} < t_{ON} < T_{neg} + T_r/2$ (refer to Figure 8)

In this case, the initial current $I_p(t_{ON})$ is positive and $T_{ON} < T_{pos}$. Q_{pos} and T_{pos} will be affected, whereas Q_{neg} and T_{neg} will not: Q_{neg} depends on voltages only and not on the power circulating in the converter. Regardless of whether V_{IN} is greater or less than V_R , turn-on occurs on the positive wave of the drain voltage ringing and with the positive current if $t_{ON} < T_r$. However, we need to distinguish two subcases.

- Subcase II(a): $V_{IN} \leq V_R$.

In this case, due to the charge not transferred from L_p to C_{ds} while the drain voltage is clamped in the interval $T_z \leq t \leq T_{neg}$, the ringing occurring after T_{neg} has a peak amplitude reduced from V_R to V_{IN} in voltage and from $V_R Y_L$ to $V_{IN} Y_L$ in current:

$$\begin{aligned} V_{ds}(t) &= V_{IN} \left[1 - \cos\left(2\pi \frac{t - T_{neg}}{T_r}\right) \right] \\ I_p(t) &= Y_L V_{IN} \sin\left(2\pi \frac{t - T_{neg}}{T_r}\right) \end{aligned} \quad (7)$$

Table 2. Timings and input current characteristics of Hi-PF QR flyback converters assuming current in the turn-on instant of power switch M is negative ($t_{ON} < T_{neg}$).

Symbol	Definition	Expression
T_{pos}^*	Duration of Positive Portion of Primary Current I_p .	$\frac{L_p I_{ppk}}{V_{IN}}$
T_{ON}^*	Duration of ON-time of power switch M	$T_{pos}^* + T_{neg}^* - t_{ON}$
T_{FW}^*	Time needed for secondary current I_s to ramp linearly from I_{spk} down to zero	$\frac{L_s I_{spk}}{V_{out}} = \frac{L_p I_{ppk}}{V_R}$
T^*	Switching period	$T_{pos}^* + T_{FW}^* + T_{neg}^*$
T_{zz}^*	Time needed for primary current I_p to ramp linearly to zero starting from $I_p(t_{ON})$	$\frac{1}{2\pi} T_r \frac{V_R}{V_{IN}} \sin\left(2\pi \frac{t_{ON}}{T_r}\right)$
T_{neg}^*	Duration of negative portion of primary current I_p	$\begin{cases} V_{IN} \leq V_R, & 0 \leq t_{ON} < T_z & t_{ON} + T_{zz}^* \\ V_{IN} \leq V_R, & T_z \leq t_{ON} \leq T_{neg} & T_{neg} \\ V_{IN} > V_R & & t_{ON} + T_{zz}^* \end{cases}$
Q_{pos}^*	Positive charge taken from input source during T_{pos}^* in a switching cycle	$\frac{1}{2} I_{ppk} T_{pos}^*$
Q_{neg}^*	Negative charge returned to input source during T_{neg}^* in a switching cycle	$\begin{cases} V_{IN} \leq V_R, & 0 \leq t_{ON} < T_z & V_R C_{ds} \left[\cos\left(2\pi \frac{t_{ON}}{T_r}\right) + \right. \\ & & \left. - \frac{1}{2} \frac{V_R}{V_{IN}} \sin^2\left(2\pi \frac{t_{ON}}{T_r}\right) - 1 \right] \\ V_{IN} \leq V_R, & T_z \leq t_{ON} \leq T_{neg} & Q_{neg} \\ V_{IN} > V_R & & V_R C_{ds} \left[\cos\left(2\pi \frac{t_{ON}}{T_r}\right) + \right. \\ & & \left. - \frac{1}{2} \frac{V_R}{V_{IN}} \sin^2\left(2\pi \frac{t_{ON}}{T_r}\right) - 1 \right] \end{cases}$
$I_p(t_{ON})$	Primary current at turn-on instant	$\begin{cases} V_{IN} \leq V_R, & 0 \leq t_{ON} < T_z & -Y_L V_R \sin\left(2\pi \frac{t_{ON}}{T_r}\right) \\ V_{IN} \leq V_R, & T_z \leq t_{ON} \leq T_{neg} & \frac{V_{IN}}{L_p} (t_{ON} - T_{neg}) \\ V_{IN} > V_R & & -Y_L V_R \sin\left(2\pi \frac{t_{ON}}{T_r}\right) \end{cases}$
$\langle I_p \rangle^*$	Average input current in a switching cycle	$\frac{Q_{pos}^* + Q_{neg}^*}{T^*}$

Figure 6. Normalized values of T_{neg}^* and Q_{neg}^* as a function of the V_{IN}/V_R ratio for different turn-on instants t_{ON} , with $t_{ON} \leq T_{neg}$.

Figure 7. Normalized values of T_{neg}^* and Q_{neg}^* as a function of the turn-on instant t_{ON} , with $t_{ON} \leq T_{neg}$, for different V_{IN}/V_R ratios.

Figure 8. Close-up of primary current with $t_{ON} > T_{neg}$. Dashed lines, which refer to the case $t_{ON} = T_{neg}$, are shown for reference. Dotted lines show primary current ringing continuation.

- Subcase II(b): $V_{IN} \leq V_R$.

In this case, the exchange of electric charge between L_p and C_{ds} is unaffected, and there is no change in the ringing occurring after $T_r/2$.

The results of this analysis are summarized in Table 3, where T_z and T_{zz} (which are those defined in Table 1) are not shown because not relevant and unaffected by t_{ON} .

The diagrams in Figure 9 show how T_{pos}^* and Q_{pos}^* vary as a function of the ratio V_{IN}/V_R for different values of t_{ON} . Values are normalized to those of T_{pos} and Q_{pos} when $t_{ON} = T_{neg}$. The diagrams in Figure 10 show how T_{neg}^* and Q_{neg}^* vary with t_{ON} for different values of the ratio V_{IN}/V_R . Values are normalized in the same manner.

Figure 9. Normalized values of T_{pos}^* and Q_{pos}^* as a function of the V_{IN}/V_R ratio for different turn-on instants t_{ON} , with $t_{ON} \geq T_{neg}$.

Figure 10. Normalized values of T_{pos}^* and Q_{pos}^* as a function of the turn-on instant t_{ON} , with $t_{ON} \geq T_{neg}$, for different V_{IN}/V_R ratios.

Table 3. Timings and input current characteristics of Hi-PF QR flyback converters assuming current in the turn-on instant of power switch M is positive ($t_{ON} > T_{neg}$).

Symbol	Definition	Expression
T_{pos}^*	Duration of positive portion of primary current I_p .	$T_{ON}^* + t_{ON}$
T_{ON}^*	Duration of ON-time of power switch M	$\begin{cases} V_{IN} \leq V_R \\ V_{IN} > V_R \end{cases} \quad \frac{L_p}{V_{IN}} I_{ppk} - \frac{1}{2\pi} T_r \sin\left(2\pi \frac{t_{ON}}{T_r}\right)$
T_{FW}^*	Time needed for secondary current I_s to ramp linearly from I_{spk} down to zero	$\frac{L_s I_{spk}}{V_{out}} = \frac{L_p I_{ppk}}{V_R}$
T^*	Switching period	$T_{pos}^* + T_{FW}^* + T_{neg}^*$
T_{neg}^*	Duration of negative portion of primary current I_p	T_{neg}
Q_{neg}^*	Negative charge returned to input source during T_{neg}^* in a switching cycle	Q_{neg}
Q_{pos}^*	Positive charge taken from input source during T_{pos}^* in a switching cycle	$\begin{cases} V_{IN} \leq V_R \\ V_{IN} > V_R \end{cases} \quad \frac{1}{2} \left[I_{ppk} + V_{IN} Y_L \sin\left(2\pi \frac{t_{ON}}{T_r}\right) \right] T_{ON}^*$
$I_p(t_{ON})$	Primary current at turn-on instant	$\begin{cases} V_{IN} \leq V_R \\ V_{IN} > V_R \end{cases} \quad \begin{aligned} &Y_L V_{IN} \sin\left(2\pi \frac{t_{ON}}{T_r}\right) \\ &Y_L V_R \sin\left(2\pi \frac{t_{ON}}{T_r}\right) \end{aligned}$
$\langle I_p \rangle^*$	Average input current in a switching cycle	$\frac{Q_{pos}^* + Q_{neg}^*}{T^*}$

3.2. Comments on Previous Analysis

It is worth reminding that this analysis contains simplifications that impact the quantitative aspect. Especially noteworthy is the one concerning the C_{oss} of the power switch M, a strongly nonlinear capacitance that in the latest MOSFET generations increases dramatically (a hundred times or more) when the drain-source voltage falls below few ten volts. This capacitance has been considered constant or, at least, not significantly impacting the overall C_{ds} .

Another simplification is that the ringing has been assumed to be undamped. Actually, the ringing current flowing through the primary winding of the transformer encounters the ac resistance of that winding at the ringing frequency (typically, some hundred kHz). Because of skin and proximity effects, and depending on the construction of the transformer, its value may be even significantly high and provide significant damping of the ringing. In the context of the present analysis, the most significant consequence of the damping is that the amplitude of the ringing, even considering the first valley, will be lower than V_R . Therefore, the valley of the drain voltage will touch zero at an input voltage lower than V_R .

Another simplification concerns what happens when the ac line voltage $V_{AC}(\theta)$ approaches zero.

The present analysis points out the existence of a time interval around zero crossings of $V_{AC}(\theta)$ (often termed dead zone) where the input current to the converter $I_{AC}(\theta) = 0$, although $V_{AC}(\theta) \neq 0$, originating the so-called crossover distortion. This happens when the peak current in a switching cycle becomes so small that $Q_{pos} < |Q_{neg}|$ and the rectified input current $I_{IN}(\theta)$ becomes negative. The physical interpretation of being $I_{IN}(\theta) < 0$ and

$I_{AC}(\theta) = 0$ around the zero-crossings is: when $I_{IN}(\theta) < 0$ it actually charges back the input capacitor (C_{in} in Figure 1) so that $V_{IN}(\theta)$ becomes larger than $V_{AC}(\theta)$, the input bridge is reverse-biased and, consequently, $I_{AC}(\theta)$ is zero.

The situation is even more complicated because of the residual voltage across the input capacitance C_{in} and the possible interactions with the input EMI filter due to the drastic reduction of the switching frequency that occurs near the zero-crossings. Additionally, there is another dead zone around the line voltage zero-crossings where no primary-to-secondary energy transfer takes place that interacts with that determined by the average inductor current $I_{IN}(\theta)$ being negative. All these aspects are expanded in [7].

For the completeness of the analysis, it is worth mentioning another minor effect that makes the task of an accurate description of the behavior near the zero crossings even tougher.

As reported in [7], the previously mentioned region around the line voltage zero crossings where there is no input-to-output energy transfer occurs when the inductor peak current is so low that the energy stored in L_p during the on-time T_{ON} of the power switch M is not enough to charge C_{ds} up to $V_{IN}(\theta) + V_R$ when the power switch turns off.

As illustrated in Figure 11, the drain waveform is a sinusoidal arc going from zero to a peak value $V_Y < V_R$ and then back to zero. The situation is significantly different as compared to that considered during the previous analysis and shown in Figure 4: V_Y is not large enough for the voltage on the secondary side of the transformer to forward bias the rectifier and have current circulating, thus the T_{FW} interval disappears and no energy is delivered to the output.

Figure 11. Simplified equivalent circuit after power switch turn-off in the no input-to-output energy transfer region around the line voltage zero-crossings and relevant key waveforms.

Assuming as $t = 0$ the instant when the drain voltage peaks, the interval T_z needed for it to fall to zero is essentially the same as that needed to reach the peak after turn-off. Both the rise and fall times are then in the range of $T_f/4$. The rise time of the drain voltage, which

has always been assumed to be negligible, in this case, is not so short but the duration of the switching period is largely dominated by the interval $T_{zz} + T_{pos}$ because of the very low input voltage, then its effect on the switching frequency can still be neglected.

The equations shown in Figure 2 and that have been used to derive those in Tables 1–3 are no longer valid and should be modified by substituting V_R with V_Y .

3.3. Quantitative Aspects of a Nonzero Current at the Turn-on Instant of the Power Switch M

To provide a quantitative idea of the impact of a nonzero current at the turn-on instant in the closed-loop operation, the analysis done so far will be applied to a pair of exemplary cases.

The first exemplary case is a Hi-PF QR flyback converter whose main electrical specification is detailed in Table 4 and that is controlled with the traditional QR method, where the peak primary current is enveloped by a rectified sinusoid as expressed by (2).

Table 4. Main characteristics of Hi-PF QR flyback converter with the QR control method used as a first reference.

Parameter	Symbol	Value	Unit
Line voltage range	$V_{ACmin}-V_{ACmax}$	90–265	Vac
Line frequency range	f_L	47–63	Hz
Regulated output voltage	V_{out}	48	V
Rated dc output current	I_{out}	730	mA
Expected full-load efficiency	η	90	%
Reflected voltage	V_R	180	V
Transformer primary inductance	L_p	550	μ H
Output capacitance	C_{out}	2000	μ F
Input capacitance	C_{in}	220	nF
Drain node total capacitance	C_{ds}	140	pF
Switching frequency range (@ line voltage peaks)	$f_{swmin}-f_{swmax}$	$\approx$ 64–150	kHz

This control method provides a rectified input current to the converter, $I_{IN}(\theta)$, which is given by the sequence of $\langle I_p \rangle$ along each line half-cycle, that is expressed by:

$$I_{IN}(\theta) = \begin{cases} \frac{1}{2} I_{PPK} \frac{T_{pos}(\theta)}{T(\theta)} \sin\theta - \frac{2}{T(\theta)} V_R C_{ds} & V_{IN}(\theta) > V_R \\ \frac{1}{2} I_{PPK} \frac{T_{pos}(\theta)}{T(\theta)} \sin\theta - \frac{1}{2T(\theta)} \frac{[V_{IN}(\theta) + V_R]^2}{V_{IN}(\theta)} C_{ds} & V_{IN}(\theta) \leq V_R \end{cases} \quad (8)$$

In this converter the turn-on instant t_{ON} has been swept in the interval $0 \leq t_{ON} \leq T_r$, considering operation at low line voltage (115 Vac) and high line voltage (230 Vac) at full load. The results are shown in the diagram in Figure 12.

Figure 12. Total harmonic distortion (THD) of the input current $I_{AC}(\theta)$ of the converter specified in Table 4, controlled with the QR control method, upon varying the turn-on instant t_{ON} of the power switch in the interval $0 \leq t_{ON} \leq T_r$.

Notice that in a large region around $t_{ON} = T_r/2$, the one of greater practical interest, the distortion is nearly independent of t_{ON} , especially at the low line. Based on this observation, it is possible to conclude that with the QR control method the distortion of the input current is essentially insensitive to the way the ZCD circuit is realized and to the statistical spread of its parameters.

The second exemplary case is a Hi-PF QR flyback converter whose main electrical specification is detailed in Table 5 and that is controlled with the EQR method, where the envelope of the peak primary current is given by (5).

Table 5. Main characteristics of Hi-PF QR flyback converter with the EQR control method used as a second reference.

Parameter	Symbol	Value	Unit
Line voltage range	$V_{ACmin}-V_{ACmax}$	90–265	Vac
Line frequency range	f_L	47–63	Hz
Rated output voltage (14 LED string @ 100% load)	V_{out}	48	V
Regulated dc output current	I_{out}	730	mA
Expected full-load efficiency	η	90	%
Reflected voltage	V_R	120	V
Transformer primary inductance	L_p	500	μ H
Output capacitance	C_{out}	1360	μ F
Input capacitance	C_{in}	470	nF
Drain node total capacitance	C_{ds}	220	pF
Switching frequency range (@ line voltage peaks)	$f_{swmin}-f_{swmax}$	$\approx 44-88$	kHz

This control method provides a rectified input current to the converter, $I_{IN}(\theta)$, expressed by:

$$I_{IN}(\theta) = \begin{cases} \frac{1}{2} I_{PPK} \frac{T_{pos}(\theta)}{T_{ON}(\theta)} \sin\theta - \frac{2}{T(\theta)} V_R C_{ds} & V_{IN}(\theta) > V_R \\ \frac{1}{2} I_{PPK} \frac{T_{pos}(\theta)}{T_{ON}(\theta)} \sin\theta - \frac{1}{2T(\theta)} \frac{[V_{IN}(\theta) + V_R]^2}{V_{IN}(\theta)} C_{ds} & V_{IN}(\theta) \leq V_R \end{cases} \quad (9)$$

In this converter too the turn-on instant t_{ON} has been swept in the interval $0 \leq t_{ON} \leq T_r$ considering operation at 115 Vac and 230 Vac at full load. The results are shown in the diagram in Figure 13.

Figure 13. Total harmonic distortion (THD) of the input current $I_{AC}(\theta)$ of the converter specified in Table 5, controlled with the EQR control method, upon varying the turn-on instant t_{ON} of the power switch in the interval $0 \leq t_{ON} \leq T_r$.

Notice that in this case in the region around $t_{ON} = T_r/2$, at the low line the distortion is a little dependent on t_{ON} , whereas at the high line the dependence is significantly higher.

In both cases, the distortion becomes smaller as t_{ON} is delayed. Based on this observation, it is possible to conclude that with the EQR control method the distortion of the input current, though lower as compared to the QR method, is more sensitive to t_{ON} and, then, to the way the ZCD circuit is realized and to the statistical spread of its parameters.

Notice that in the positive terms in (5), the ratio $T_{pos}(\theta)/T_{ON}(\theta)$ expresses the effect that the current in the turn-on instant of the power switch M has on the shape of the input current. In fact, in the case $T_{pos}(\theta) \neq T_{ON}(\theta)$, since in general, they are not proportional to one another, the positive term contains a distortion term that adds up to the distortion caused by the negative one. This explains why the EQR method is more sensitive to t_{ON} and to the implementation of the ZCD circuit.

3.4. Notes on the THD Calculation Method

The THD of $I_{AC}(\theta)$ vs. t_{ON} plots of Figures 12 and 13 have been derived determining the expressions of $I_{IN}(\theta)$, Equation (8) for the QR method and Equation (9) for the EQR method, and then extending them over the interval $(0, 2\pi)$. In these equations I_{PPK} , which is related to the power delivered by the converter, is the unknown parameter, t_{ON} is the independent variable, the others are those in Tables 2 and 3.

Notice that the quantity I_{PPK} in these tables is given by Equation (2) for the QR method and Equation (5) for the EQR method. To prevent the singularity when $V_{IN} = 0$ in the expressions related to $V_{IN} \leq V_R$ where V_{IN} appears at the denominator, a voltage drop $V_F = 0.7$ V across the body diode of the power switch has been assumed. Hence, in all formulas in Table 2 where $V_{IN} \leq V_R$ it is actually $V_{IN} = V_{PK} \sin \theta + V_F$.

In closed-loop operation, for a given V_{AC} , the average value of the product $V_{IN}(\theta) \cdot I_{IN}(\theta)$ over a line half-cycle (i.e., the integral of the product in $(0, \pi)$ divided by π) must be equal to the dc input power to the converter $P_{in} = V_{out} I_{out}/h$. This equation is solved by iteration for the unknown parameter I_{PPK} with a given value of t_{ON} , thus completely defining Equations (8) and (9).

As previously said, the Fourier coefficients (i.e., the peak amplitudes of each harmonic) of $I_{AC}(\theta)$ are computed by extending Equations (8) and (9) over the interval $(0, 2\pi)$. Being $I_{AC}(\theta)$ an odd function, there are only sine terms. Because of its rotational symmetry ($I_{AC}(\theta + \pi) = -I_{AC}(\theta)$) there are only odd harmonics.

The THD is computed as the ratio between the square root of the sum of squares of the peak amplitudes of the higher order harmonics (from 3rd up to 39th) and the peak amplitude of the fundamental one.

Finally, all these calculations are repeated sweeping t_{ON} from 0 to T_r . This has been done with the help of Mathcad®, engineering math software.

4. Impact of ZCD Circuit Operation on Input Current Shaping

The impact of a nonzero current as the power switch M turns on, causing $T_{pos}(\theta) \neq T_{ON}(\theta)$, will be now analyzed more in detail with reference to some typical implementations of the ZCD circuit that determines the turn-on instant t_{ON} of the power switch M. Some results, referred to the exemplary converter specified in Table 5 and controlled with the EQR method will be presented to provide the reader with some quantitative information. No investigation will be done on the converter specified in Table 4 and controlled with the QR method, since the previous analysis has shown its substantial insensitivity to the position of t_{ON} and, then, to the operation of the ZCD circuit.

The calculation method used to obtain the results that are shown in the following sections is the same as that described in Section 3.4.

4.1. Optimal ZCD Circuit

An optimal ZCD circuit ensures that the turn-on of the power switch always occurs with zero initial current ($t_{ON} = T_{neg}$), so that it is always $T_{pos} = T_{ON}$ and, as stated by Equation (9), no distortion is introduced in the positive terms all over the V_{IN} range:

$$I_{IN}(\theta) = \begin{cases} \frac{1}{2} I_{PPK} \sin \theta - \frac{2}{T(\theta)} V_R C_{ds} & V_{IN}(\theta) > V_R \\ \frac{1}{2} I_{PPK} \sin \theta - \frac{1}{2T(\theta)} \frac{[V_{IN}(\theta) + V_R]^2}{V_{IN}(\theta)} C_{ds} & V_{IN}(\theta) \leq V_R \end{cases} \quad (10)$$

The principle circuit shown in Figure 14 along with its key waveforms may fulfill this task. The auxiliary winding L_{aux} is coupled to the primary winding of the transformer in such a way that its voltage V_{aux} and the drain voltage V_{ds} are in-phase. More specifically, V_{aux} is a replica of the drain voltage V_{ds} scaled down by the turn ratio and centered on zero.

Figure 14. Principle schematic of an optimal ZCD circuit and relevant key waveforms.

V_{aux} , which is negative during the on-time of the power switch M, is positive during the off-time, as long as the current circulates on the secondary winding; when this current zeroes (demagnetization), V_{ds} starts ringing with a negative-going sinusoidal arc and the same falling arc appears on V_{aux} .

L_{aux} is coupled to the ZCD pin of the control IC via the resistor R_{zcd} : since the voltage V_{zcd} on the ZCD pin is top and bottom clamped, R_{zcd} limits the current sunk/sourced by the clamps.

A comparator (ZCD comparator) with the noninverting input referred to a slightly positive threshold V_{th} (e.g., 100 mV) senses V_{zcd} on its inverting input. Another comparator (CS comparator), whose inverting input is referred to as a negative threshold $-V_{th1}$ very close to zero (e.g., -20 mV) senses the voltage on the current sense input V_{CS} on its noninverting input. The PWM latch is edge-sensitive and its set input S is driven by the AND gate that receives the outputs of the two comparators. With this circuit arrangement, the output Q of the PWM latch goes high causing the power switch M to turn on both conditions, $V_{zcd} < V_{th}$ and $V_{CS} > -V_{th1}$, are met.

When the secondary current zeroes, V_{aux} collapses and, as it goes below the upper clamp value, also V_{zcd} starts collapsing. As V_{zcd} falls below V_{th} the output of the ZCD comparator goes high. Being V_{th} close to zero, this occurs about $T_r/4$ after the secondary current zeroes. The primary current I_p is ringing too (in quadrature to V_{aux}), so in that instant, I_p is close to its negative peak, it is $V_{CS} < -V_{th1}$ and the output of the CS comparator is low. As long as I_p is negative and it is $V_{CS} < -V_{th1}$, the output of the CS comparator stays low. Only when V_{CS} exceeds $-V_{th1}$ (either because of ringing when $V_{IN} > V_R$, or because I_p is ramping up linearly when $V_{IN} \leq V_R$), the output of the CS comparator and the output of the AND gate go high too. The PWM latch is then set, its output Q goes high and turns on the gate driver and the power switch M, starting a new switching cycle.

The diagrams of Figure 15 provide some exemplary quantitative results for the converter specified in Table 5. The diagrams on the left-hand side show the shape of the input current to the converter $I_{AC}(\theta)$ (in red) along with a black sinusoid for reference and, below, its harmonic contents at full load and $V_{ac} = 115$ V. The diagrams on the right-hand side show the same at $V_{ac} = 230$ V.

Figure 15. Optimal ZCD circuit: input current shape (a,b) and its harmonic content (c,d) for converter specified in Table 5 at 115 Vac (a,c) and 230 Vac (b,d).

The horizontal red dotted lines in the upper diagrams mark the points where $|V_{IN}| = V_R$, i.e., the transition from the region ($|V_{IN}| > V_R$), where the negative charge Q_{neg} depends on V_R only, to the region ($|V_{IN}| < V_R$) of $I_{IN}(\theta)$ and then, of $I_{AC}(\theta)$ where Q_{neg} depends on V_{IN} too.

Note that the shape of $I_{AC}(\theta)$ shows the crossover distortion, highlighted by the blue circle, i.e., the dead zone corresponding to a negative $I_{IN}(\theta)$ around the zero crossings of the instantaneous line voltage $V_{AC}(\theta)$, which makes $I_{AC}(\theta) = 0$, although $V_{AC}(\theta) \neq 0$ as previously explained.

The dead zone in $I_{AC}(\theta)$ predicted by (10) lies in the interval $-3.2^\circ < \theta < 3.2^\circ$ at 115 Vac and in the interval $-5.8^\circ < \theta < 5.8^\circ$ at 230 Vac. As discussed in Section 3.2, the accuracy of the model Equation (10) around line voltage zero-crossings is impaired by the existence of other distortion causes (above all else the input capacitor C_{in}). Therefore, these data on the dead zone amplitude are ballpark figures that can be used only for comparison with other ZCD circuits by isolating their contribution alone.

4.2. Differentiator-Based ZCD Circuit

The principle schematic of this circuit and its key waveforms are shown in Figure 16. Both the external circuit connected to the ZCD pin and its operation are exactly the same as with the optimal ZCD circuit, except that in this case the pin is directly connected to L_{aux} .

Internally, the voltage on the ZCD pin is unclamped; as to the differentiator, it is assumed that it is $R_d C_d \ll T_r/2$. The current I_d (and, then, the voltage $V_d = I_d R_d$) is zero as long as V_{aux} is on either level and is nonzero when V_{aux} transitions from one level to the other. The voltage V_d is sensed by a comparator whose inverting input is referred to a negative threshold $-V_{th}$ close to zero, e.g., -100 mV.

When the secondary current zeroes and the negative-going edge of V_{aux} starts, the voltage V_d applied to the noninverting input of the comparator becomes much negative, thus its output goes low. When the negative-going edge ends I_d zeroes and so does V_d too: as it exceeds $-V_{th}$ the output of the comparator has a low-to-high transition. The PWM

latch, edge-sensitive, is then set, its output Q goes high turning on the gate driver and the power switch M and starting a new switching cycle.

Figure 16. Principle schematic of a differentiator-based ZCD circuit and relevant key waveforms.

With this circuit, if $V_{IN} > V_R$ the turn-on of the power switch M occurs on the valley of the V_{ds} ringing ($t_{ON} = T_r/2$, when its derivative is zero): zero derivative means zero ringing currents and, then, zero initial current and $T_{pos} = T_{ON}$. No distortion is associated with the corresponding positive term in Equation (9). When $V_{IN} \leq V_R$ the turn-on is commanded as the drain voltage touches zero, i.e., $t_{ON} = T_z$ given in Table 1 when the ringing current is still negative. In this case, based on Table 2, T_{ON} is expressed as:

$$T_{ON} = T_{pos} + T_{zz} \quad (11)$$

and (5), neglecting the contribution of the ringing current as previously stated, becomes:

$$I_{IN}(\theta) = \begin{cases} \frac{1}{2} I_{PPK} \sin \theta - \frac{2}{T(\theta)} V_R C_{ds} & V_{IN}(\theta) > V_R \\ \frac{1}{2} I_{PPK} \sin \theta - \frac{1}{2} I_{PPK} \frac{T_{zz}(\theta)}{T_{ON}(\theta)} \sin \theta - \frac{1}{2T(\theta)} \frac{[V_{IN}(\theta) + V_R]^2}{V_{IN}(\theta)} C_{ds} & V_{IN}(\theta) \leq V_R \end{cases} \quad (12)$$

As a conclusion, the differentiator-based ZCD circuit does not introduce any distortion as long as $V_{IN} > V_R$ (condition fulfilled along most of the rectified sinusoid at the high line, e.g., with the European mains); conversely, it introduces a distortion term when $V_{IN} \leq V_R$, a condition that is fulfilled along most of the rectified sinusoid at the low line, i.e., with US or Japan mains). The amplitude of this distortion is related to the ratio T_{zz}/T_{ON} and a Fourier analysis of Equation (12) shows that the distortion term creates a component at the fundamental frequency and odd harmonics, all in phase opposition to the fundamental component.

With reference again to the converter specified in Table 5, the diagrams of Figure 17 provide the same exemplary quantitative results as those shown in Figure 15 with the optimal ZCD circuit. Note that the harmonic contents have a distribution not too different from that provided by the optimal ZCD circuit, but with a slightly larger amplitude. This results in a slightly higher THD: +1% at 115 Vac and +1.3% at 230 Vac.

In this case the crossover distortion due to the positive term in Equation (12) becoming smaller than the negative term is slightly wider: the dead zone in $I_{AC}(\theta)$ occurs in the interval $-3.4^\circ < \theta < 3.4^\circ$ at 115 Vac and in $-6.7^\circ < \theta < 6.7^\circ$ at 230 Vac. The external circuit connected to the ZCD pin and its operation are the same as the optimal ZCD circuit. Internally, the voltage V_{zcd} on the ZCD pin is top and bottom clamped and there is the same ZCD comparator with the noninverting input referred to as a slightly positive threshold V_{th} (e.g., 100 mV) that senses V_{zcd} on its inverting input as seen in the optimal ZCD circuit. The output X of the ZCD comparator goes through a delay block T_d , ideally tuned to slightly less than $T_r/4$, after that it reaches the set input of the edge-sensitive PWM latch.

Figure 17. Differentiator-based ZCD circuit: input current shape (upper) and its harmonic content (lower) for converter specified in Table 1 at 115 Vac (left) and 230 Vac (right).

4.3. Comparator-plus-Delay ZCD Circuit

The principle schematic of this circuit and its key waveforms are shown in Figure 18.

Figure 18. Principle schematic of a comparator-plus-delay ZCD circuit and relevant key waveforms.

When the secondary current zeroes, V_{aux} collapses and, as it goes below the upper clamp value, V_{zcd} also starts collapsing. As V_{zcd} falls below V_{th} the output X of the comparator has a low-to-high transition. After a delay T_d the PWM latch is set, its output Q goes high and turns on the gate driver and the power switch M , starting a new switching cycle.

Note that, being V_{th} close to zero, the negative edge is detected about $T_r/4$ after the secondary current zeroes. Note also that the resistor R_{zcd} , along with the parasitic capacitance of the internal clamp plus some external stray contributors (which are anyhow well defined once the layout of the external circuit is defined), form an RC low-pass filter that delays V_{zcd} with respect to V_{aux} . This delay adds up to T_d and can be fine-tuned by adjusting R_{zcd} (or even adding a small external capacitor between the ZCD pin and ground) so that the overall delay equals $T_r/2$ and it is $t_{ON} = T_r/2$ both with $V_{IN} > V_R$ and $V_{IN} \leq V_R$.

With this circuit, therefore, when $V_{IN} > V_R$ turn-on occurs on the valley of the V_{ds} ringing, the initial current is zero, $T_{pos} = T_{ON}$, and no distortion is introduced. When $V_{IN} \leq V_R$ the ringing current at $t = T_r/2$ is ramping up linearly but is still negative. In this case, based on Table 2, T_{ON} is given by:

$$T_{ON} = T_{pos} + T_{neg} - \frac{T_r}{2} \quad (13)$$

and (9) becomes:

$$I_{IN}(\theta) = \begin{cases} \frac{1}{2} I_{PPK} \sin \theta - \frac{2}{T(\theta)} V_R C_{ds} & V_{IN}(\theta) > V_R \\ \frac{1}{2} I_{PPK} \sin \theta - \frac{1}{2} I_{PPK} \frac{T_{neg}(\theta) - \frac{T_r}{2}}{T_{ON}(\theta)} \sin \theta - \frac{1}{2T(\theta)} \frac{[V_{IN}(\theta) + V_R]^2}{V_{IN}(\theta)} C_{ds} & V_{IN}(\theta) \leq V_R \end{cases} \quad (14)$$

Once more with reference to the converter specified in Table 5, the diagrams of Figure 19 provide the same results as those shown in Figures 15 and 17, with the comparator-plus-delay ZCD circuit. Note that the harmonic contents is lower in amplitude as compared to that of the differentiator-based ZCD circuit and quite close to that of the optimal ZCD circuit: the THD values are only 0.4% at 115 Vac and 0.3% at 230 Vac larger.

Figure 19. Comparator-plus-delay ZCD circuit: input current shape (a,b) and its harmonic content (c,d) for converter in Table 1 at 115 Vac (a,c) and 230 Vac (b,d).

Compared to the previous case, the dead zone in $I_{AC}(\theta)$ is slightly narrower at high line: it occurs in the interval $-3.4^\circ < \theta < 3.4^\circ$ at 115 Vac and in $-6.2^\circ < \theta < 6.2^\circ$ at 230 Vac. To summarize:

- The optimal ZCD circuit does not alter the shape of the input current determined by the control mechanism but its implementation in a control IC requires a high level of silicon use.
- The differentiator-based ZCD circuit provides the highest THD values and its implementation in a control IC, though simple, requires silicon consuming structures able to withstand relatively large positive and negative voltages.
- The comparator-plus-delay ZCD circuit performs only slightly worse than the optimal ZCD circuit, provides the fine-tuning capability, and compared to the other two solutions, is less silicon consuming.

It is worth noticing that all the three ZCD circuit implementation do not alter the shape of the input current in the region $V_{IN} > V_R$; their difference in THD performance comes from the different behavior in the $V_{IN} \leq V_R$ region. A significant portion of this

difference is in the amplitude of the dead-zone in $I_{AC}(\theta)$ that is generated. The diagram of Figure 20 shows how the total amplitude of the dead-zone changes as a function of the parameter $Kv = V_{PK}/V_R$ for various implementations of the ZCD circuit.

Figure 20. Dead-zone amplitude with various types of ZCD circuit as a function of the V_{PK}/V_R ratio.

It has been shown that the detrimental effect of the ZCD circuit on the input current shape is caused by a negative current in the turn-on instant of the power switch M that makes $T_{pos}(\theta) < T_{ON}(\theta)$. If we artificially delay the turn-on instant beyond $T_r/2$ after demagnetization, the initial current will be positive, thus making $T_{pos}(\theta) > T_{ON}(\theta)$. This will create a positive term (increasing with the extra delay) that will partly compensate for the negative term due to the ringing current and is expected to result in a lower THD of the input current. Actually, this is shown in the diagram of Figure 13 and is consistent with the reduction of the dead-zone amplitude and the resulting crossover distortion shown in Figure 20 with an increasing delay.

In conclusion, the comparator-plus-delay ZCD circuit seems to be the best practical choice, due to its fine-tuning capability, good performance, and simplicity. The comparator-plus-delay ZCD circuit might even outperform the optimal ZCD circuit when $T_{pos}(\theta) > T_{ON}(\theta)$. Anyway, any improvement in the THD attempted in this way should be traded off against the consequences of a long delay in restarting a new switching cycle: losing exact valley switching (higher turn-on losses and electromagnetic noise) and pushing the operation more deeply into DCM (worsening of current form factor, higher conduction losses).

5. Experimental Verifications

A pair of test benches have been set up to experimentally assess the impact of a nonzero current at turn-on on the THD of the input current to verify the theoretical predictions outlined in Section 4.

The first test bench was based on the reference Hi-PF QR flyback converter specified in Table 4 and whose picture is shown in Figure 21 on the left-hand side. The converter is an old design based on the L6562A, a PFC IC from STMicroelectronics primarily intended for boost-based PFC converters, that implements the QR control method.

The second test bench was based on the reference Hi-PF QR flyback converter specified in Table 5 and whose picture is shown in Figure 21 on the right-hand side. The converter is a newly developed design based on the HVLED007, a PFC IC from STMicroelectronics specific for flyback topology that implements the EQR control method.

The instrumentation used to set up the test benches included an ac source Chroma 61501 and an e-load Chroma 6314A + 63108A set in constant current mode (both converters provide a regulated output voltage); voltage waveforms acquisitions and time measurements were done with the oscilloscope Tektronix DPO 7054C; the THD was measured with a power meter Yokogawa WT210.

Figure 21. 35 W Hi-PF QR flyback controlled with QR method by the L6562A IC (a); 35 W Hi-PF QR flyback controlled with EQR method by the HVLED007 IC (b).

Both controllers have a comparator-plus-delay ZCD circuit onboard and in both cases, the delay from the transformer's demagnetization instant to the turn-on instant of the power switch M has been adjusted by acting on the external interface circuit between the auxiliary winding and the ZCD input pin, as shown in Figure 22.

Figure 22. External circuits are used to adjust the delay between the transformer's demagnetization instant to turn-on instant of the power switch M. Upper circuit delays turn-on, lower circuit brings it forward.

It is worth reminding that the experimental data will provide the total result of all the concurrent causes of distortion and it is not generally possible to isolate each of them. Additionally, they are interacting with each other, thus a change in one of them may affect the amount of distortion caused by another one in a way that may be either detrimental or ameliorative. The objective is, therefore, to possibly capture a trend.

Experiments have been carried out at full load, where the contribution of other distortion causes (primarily, C_{in}) is expected to be at a minimum, at 115 Vac and 230 Vac.

Figure 23 shows a few key waveforms (drain-source voltage V_{ds} , auxiliary winding voltage V_{aux} and the gate-drive output V_{gs}) at the lower and upper ends of the adjustment

range in the converter specified in Table 4 and controlled by the L6562A control IC with the QR method.

Figure 23. Key waveforms at the ends of the adjustment range of the turn-on instant t_{ON} for the converter specified in Table 4 and controlled by the L6562A control IC with the QR method.

The period of the ringing after demagnetization is $1.72 \mu\text{s}$, then $T_r/2 = 860 \text{ ns}$ and the explored range (730 ns to $1.16 \mu\text{s}$) includes both conditions $t_{ON} < T_{neg}$ and $t_{ON} > T_{neg}$ for $V_{IN} > V_R$.

Figure 24 shows (round markers connected by solid lines) the measured THD values of the input current $I_{AC}(\theta)$ as a function of different t_{ON} instants, obtained by varying C_{adj} , at both 115 Vac and 230 Vac and 100% load. For comparison, the plot shows also the corresponding values obtained by calculation (rhomboid markers connected by dotted lines) shown in the plot of Figure 12.

Figure 24. Plot of THD of the input current I_{AC} for different values of the delay between transformer's demagnetization instant to the turn-on instant t_{ON} of the power switch M for the converter specified in Table 4 and controlled by the L6562A control IC with the QR method. Theoretical values are shown for reference.

The experimental data confirm the “flat” trend of THD vs. t_{ON} predicted by the theoretical analysis, even though there is some discrepancy, a sort of offset, in the predicted values. The reasons for this difference have not been investigated but they might be explained by the presence of other distortion causes (e.g., C_{in} , or a negative input offset of the PWM comparator).

Figure 25 shows the same key waveforms (V_{ds} , V_{aux} , and V_{gs}) as in Figure 23 at the lower and upper ends of the adjustment range in the converter specified in Table 5 and controlled by the HVLED007 control IC with the EQR method.

Figure 25. Key waveforms at the ends of the adjustment range of the turn-on instant t_{ON} for the converter specified in Table 5 and controlled by the HVLED007 control IC with the EQR method.

The period of the ringing after demagnetization is $2.07 \mu\text{s}$, then $T_r/2 = 1.035 \mu\text{s}$ and the explored range (550 ns to $1.22 \mu\text{s}$) includes both conditions $t_{ON} < T_{neg}$ and $t_{ON} > T_{neg}$ for $V_{IN} > V_R$.

Figure 26 shows (round markers connected by solid lines) the measured THD values of the input current $I_{AC}(\theta)$ as a function of different t_{ON} instants, obtained by varying C_{adj} , at both 115 Vac and 230 Vac and 100% load. For comparison, the plot shows also the corresponding values obtained by calculation (rhomboid markers connected by dotted lines) reported in the plot of Figure 13.

Figure 26. Plot of THD of the input current I_{AC} for different values of the delay between transformer's demagnetization instant to the turn-on instant t_{ON} of the power switch M for the converter specified in Table 5 and controlled by the HVLED007 control IC with the EQR method. Theoretical values are shown for reference.

The experimental data at low line are very well aligned to those calculated, except for the longest delay where the actual THD trend and the predicted one seem to diverge. At the high line, surprisingly, the measured values are lower than the calculated ones. However, the trend is the same except for the shortest delay, where the two values are much closer to one another. This difference is compatible with a positive offset of the PWM comparator, which increases the positive contribution of the per-cycle charge Q_{pos} and then, tends to reduce the THD.

To complete the experimental analysis, it is worth measuring the impact of t_{ON} on converter's efficiency ($\eta = P_{out}/P_{in}$). With valley switching ($t_{ON} = T_r/2$ when $V_{IN} > V_R$) the per-cycle energy lost at turn-on is at a minimum and increases as t_{ON} moves in either direction. However, with a shorter t_{ON} the switching frequency increases slightly (so do capacitive and switching losses) but operation gets closer to transition and the current form factor improves slightly (so conduction losses are a bit lower). With a longer t_{ON} there are

the opposite changes in power losses. Additionally, a positive initial current causes a small amount of switching losses at turn-on, as if the converter worked in slight CCM.

Figure 27 shows the measured efficiency values of the converter specified in Table 4 and controlled by the L6562A control IC with the QR method as a function of different t_{ON} instants, the same as those considered in the plot of Figure 24, at 115 Vac and 230 Vac, 100% and 50% load.

Figure 27. Plot of the measured efficiency for different values of the delay between transformer's demagnetization instant to the turn-on instant t_{ON} of the power switch M for the converter specified in Table 4 and controlled by the L6562A control IC with the QR method.

Figure 28 shows the measured efficiency values of the converter specified in Table 5 and controlled by the HVLED007 control IC with the EQR method as a function of different t_{ON} instants, the same as those considered in the plot of Figure 26, at 115 Vac and 230 Vac, 100% and 50% load.

Figure 28. Plot of the measured efficiency for different values of the delay between transformer's demagnetization instant to the turn-on instant t_{ON} of the power switch M for the converter specified in Table 5 and controlled by the HVLED007 control IC with the EQR method.

In both cases it is possible to observe that the efficiency at low line is essentially insensitive to t_{ON} , which is a benign characteristic: since at low line the full load efficiency is at a minimum, i.e., power losses are at a maximum, the thermal design of the converter will be unaffected by the ZCD circuit, its setting, and its tolerances. This makes sense since under these conditions, conduction losses dominate.

At high line, where capacitive and switching losses dominate, the efficiency has a peak in the neighborhood of $t_{ON} = Tr/2$, meaning that capacitive losses are actually dominant. At 50% load this trend becomes more visible at low line as well.

These observations suggest a few system-level design guidelines. In converters controlled with the QR method, since t_{ON} has essentially no impact on the THD of the input current, it makes sense to set the ZCD circuit to target $t_{ON} = Tr/2$ to optimize their efficiency.

In converters controlled with the EQR method one can aim to minimize the THD of the input current by setting the ZCD circuit to target $t_{ON} > Tr/2$ with no impact on the thermal design. However, by doing so the drop in efficiency at high line and/or lighter load will be more pronounced. This fact should be kept in mind in designs where the electrical specification sets efficiency targets at high line and/or light load as well.

6. Conclusions

Hi-PF QR Flyback is the preferred converter different application thanks to the related high benefit/cost ratio. Although, one can implement an optimal control there are some inherent causes of distortion due to the nonideality of the components. In this work, the distortion due to the actual ZCD circuit has been qualitatively and quantitatively investigated. Moreover, a comparison among three ZCD has been performed. An optimal ZCD circuit does not negatively affect the input current but requires much silicon for implementing the control IC. A differentiator-based ZCD is the worst in terms of THD and, similarly to the previous case, it is silicon consuming. The comparator-plus-delay ZCD circuit enables the best trade-off between performance (only slightly worse than the optimal ZCD circuit) and silicon consumption (the lowest one). Two test benches have been used to experimentally assess the impact of a nonzero current at turn-on on the THD of the input current and verify the aforesaid theoretical predictions, finding a good agreement especially as far as the trend is concerned. The impact of a nonzero current at turn-on on efficiency has been assessed too.

As a conclusion, it is possible to state that the impact of the ZCD circuit on the THD of the input current in Hi-PF QR flyback converters is essentially negligible with the traditional QR method and low with the enhanced QR method. In other words, the detection method, as well as the quality and the performance of the semiconductor components utilized for the ZCD circuit, only slightly affect the THD of the input current or the efficiency of the converter. Therefore, utilizing more sophisticated and/or costly detection circuits does not necessarily provide significant improvement. Rather, it appears that the low-cost comparator-plus-delay ZCD circuit in use in the control ICs considered for the experiments is all in all the best choice.

The experiments have shown also that with the traditional QR method it is possible to set the comparator-plus-delay ZCD circuit to target the maximum conversion efficiency with no impact on the THD of the input current by setting $t_{ON} = Tr/2$. With the enhanced QR method it is possible to have a slight improvement of the THD by setting the ZCD circuit so as to have $t_{ON} > Tr/2$, with no penalty on the thermal design but with a higher deterioration rate of the efficiency at high line and/or light load.

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