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Optimized Modulation Method for Common-Mode Voltage Reduction in H7 Inverter

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Abstract: The three-phase H7 inverter topology installs an additional power semiconductor switch to the positive or negative node of the DC-link for reducing the common-mode voltage (CMV) by disconnecting the inverter from the DC source during the zero-voltage vectors. The conventional CMV reduction method for the three-phase H7 inverter uses modified discontinuous pulse width modulation (MDPWM) and generates a switching signal for the additional switch using logical operations. However, the conventional method is unable to eliminate the CMV for the entire dwell time of the zero-voltage vectors. It only has the effect of reducing the CMV in a limited area of the space vector where the V_7 zero voltage vector is applied. Therefore, this paper proposes an optimized modulation method that can reduce the CMV during the entire dwell time of zero-voltage vectors. The proposed method moves the switching patterns by adding an offset voltage to guarantee that only one kind of zero-voltage vector, V_7 , is applied in the system. It then turns off the seventh switch only during the zero-voltage vector to disconnect the inverter from the DC source. As a result, the CMV and the leakage current are attenuated for the entire dwell time of the zero-voltage vector. Simulation and experimental results confirm the validity of the proposed method.

Keywords: common-mode voltage; zero-voltage vector; H7 inverter; PMSM

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1. Introduction

Common-mode voltage (CMV) is one of the main issues that need to be dealt with in pulse width modulation (PWM) inverters using high-frequency semiconductor devices. In three-phase AC motor drives, the CMV is defined as the voltage difference between the DC-side neutral point and the motor-side neutral point [1]. Due to the high-frequency operation of switches, the fluctuation of the CMV causes various problems such as electromagnetic interference (EMI) noise, common-mode current (CMC), bearing current, and leakage current. The CMC, bearing current, and leakage current cause damage to the physical system and malfunction of devices dedicated to communication and protection operation. Hence, the CMV plays a vital role in reducing the durability of the entire AC motor drive system [2–10].

To address these concerns caused by the CMV, much research for reducing the CMV has been conducted. The general approach for reducing the CMV is to install additional hardware devices to the PWM inverter, such as an isolated transformer and a passive filter [5,11–14]. The passive filter, which is configured as a common-mode (CM) choke and inductor–capacitor–resistor (LCR) circuit, is added to the output side of the PWM inverter. It is effective in minimizing the leakage current and EMI noise. However, the design of the filter varies according to the applications because the parameters of the equivalent circuit for the common-mode voltage vary with switching frequency, length of the electric line,

grounding technique, and motor parameters. In addition, this approach increases the cost and size of the overall system [15].

As an alternative hardware approach, the active filter method has also been widely investigated [16–21]. It measures the noise from the PWM inverter through a sensor and injects a corresponding compensation signal back to the inverter system. To generate the compensation signal, an operational amplifier (OP-Amp) [18–20] or a push–pull emitter follower (PPEF) circuit [21] is applied. However, this approach increases the cost and weight of the overall system in the same way that the passive filter method does. Additionally, the design of the active filter is complex and depends on the specific application of the inverter system. The active filter needs to be redesigned whenever the application of the system changes for optimal operation [22].

The additional cost and weight caused by the hardware approach motivates researchers to devise a PWM scheme that minimizes the CMV without an external hardware device [22–27]. The main advantage of the PWM methods is that no external devices are required for CMV reduction. Among the various PWM methods for CMV reduction are remote-state PWM (RSPWM), near-state PWM (NSPWM) and active zero-state PWM (AZSPWM) [25,26,28]. For the PWM inverter with a space vector modulation (SVM), the PWM methods utilize a combination of voltage vectors, which generate no CMV or minimum CMV among the available voltage vectors of the PWM inverter. However, the excessive use of these voltage vectors for CMV reduction decreases the linear modulation region and degrades the performance of the output waveform.

The hardware and PWM methods explained above have their drawbacks. In addition to the complexity of the design of the active and passive filters in hardware-based CMV reduction, the size and cost of the overall system are significantly affected. On the other hand, the PWM techniques used for CMV reduction significantly increase the THD of the three-phase current. To achieve CMV reduction while maintaining low THD in the three-phase current and simple additional hardware, a combination of both a PWM technique and a novel PWM inverter topology with an additional power semiconductor switch connected to the DC-link of the three-phase two-level inverter is used. An H7 inverter, which has a seventh power switch (S_7) at the positive node of the DC-link, as shown in Figure 1a, has been introduced [29,30]. As shown in Figure 1a, the H7 inverter topology uses only one additional switch, which does not require a complex hardware design procedure. The authors in [29] proposed a modified discontinuous PWM (MDPWM) method. Since the proposed MDPWM is based on a 60-degree discontinuous PWM (DPWM) method, the switching pattern in each switching period consists of two zero-voltage vectors V_0 and V_7 . The MDPWM uses a logical operation that generates a turn-off signal for the seventh switch (S_7) during only the dwell time of the V_7 zero-voltage vector to disconnect the motor from the DC source. Therefore, it reduces the CMV magnitude from $V_{dc}/2$ to $V_{dc}/4$ only in the regions where the V_7 zero-voltage vector is applied. However, this algorithm is unable to reduce the CMV magnitude in the regions where the other zero-voltage vector, V_0 , is generated from the DPWM method because the seventh switch is kept turn-on by logical operations of the MDPWM algorithm. Therefore, the MDPWM cannot reduce the CMV in all sectors of the space vector.

Figure 1. H7 inverter topology for three-phase AC motor drive. (a) Switch (S_7) connected to the positive DC-link node. (b) Switch (S_7) connected to the negative DC-link node.

This paper adopts the H7 inverter and proposes an optimized modulation strategy for CMV reduction. The proposed modulation method utilizes only one zero-voltage vector, V_7 , in all sectors and keeps the seventh switch in the off state for the entire zero-voltage vector duration. Unlike [29] (MDPWM), which turns off the seventh switch only during half of the dwell time of the zero-voltage vectors, the proposed algorithm turns off the seventh switch for the entire zero-voltage vector duration. While [29] reduces the CMV only for half of the dwell time of the zero-voltage vector, the modulation strategy proposed in this paper reduces the CMV for the entire dwell time of the zero-voltage vector. The performance of the proposed algorithm is verified by a simulation and an experiment performed on a three-phase AC motor drive system. The CMV, leakage current, total harmonic distortion (THD), and efficiency of the proposed algorithm are compared with those of the other modulation methods. The H7 inverter topology can also be configured, as shown in Figure 1b, where the seventh power switch (S_7) is connected to the negative node of the DC-link.

The rest of the paper is organized as follows. In Section 2, the CMV is analyzed and defined for the common three-phase two-level inverter and H7 inverter system. Section 3 covers the proposed CMV reduction method for the H7 inverter system. The simulation and experimental results for the proposed and conventional algorithms are given in Sections 4 and 5, respectively. Finally, Section 6 states the conclusion. Since the basic idea of the proposed modulation strategy is similar for both H7 inverter topologies in Figure 1a,b, most of the analysis in this paper is based on the circuit configuration of Figure 1a.

2. Analysis of Common-Mode Voltage in H7 Inverter

2.1. Common-Mode Voltage Analysis in Three-Phase Two-Level Inverter

The CMV of the AC motor drive system using the three-phase two-level inverter shown in Figure 2 is defined as the potential difference, v_{sn} , between the load neutral point, s , and the DC-link neutral node, n , and is expressed by Equation (1) [1].

$$v_{cm} = v_{sn} = \frac{1}{3} (v_{an} + v_{bn} + v_{cn}), \quad (1)$$

where v_{an} , v_{bn} , and v_{cn} are phase A, B, and C pole voltages, respectively. The upper and lower switches of each phase are complementary, and the respective switching function is defined as

$$S_x + \bar{S}_x = 1, \quad (2)$$

where S_x and $\bar{S}_x$ are 1 in the turn-on state and 0 in the turn-off state, and the subscript, x , denotes phases a, b, and c. The pole voltage for each phase is defined as Equation (3).

$$v_{xn} = \frac{V_{dc}}{2} (S_x - \bar{S}_x), \quad (3)$$

Figure 2. Three-phase two-level inverter topology for AC motor drive.

Substituting Equations (2) and (3) into Equation (1), the CMV is rewritten as a function of the switching states and the DC-link voltage.

$$v_{cm} = \frac{V_{dc}}{3} (S_a + S_b + S_c) - \frac{V_{dc}}{2}, \quad (4)$$

In the space vector, the reference voltage vector can be represented as

$$V^* = \frac{2}{3} (v_{as}^* + a v_{bs}^* + a^2 v_{cs}^*), \quad (5)$$

where the asterisk represents the reference value, and v_{as}^* , v_{bs}^* , and v_{cs}^* are the reference voltage of phases A, B, and C, respectively [25]. From Equation (5) and the switching states of the three-phase inverter, the six active voltage vectors (V_1 – V_6) and two zero-voltage vectors (V_0 and V_7) are defined, and the space vector can be divided into six sectors (A_1 – A_6), as shown in Figure 3. Based on Equation (4), the voltage vectors V_0 to V_7 generate a CMV of $-V_{dc}/2$, $-V_{dc}/6$, $V_{dc}/6$, $-V_{dc}/6$, $V_{dc}/6$, $-V_{dc}/6$, $V_{dc}/6$, and $V_{dc}/2$, respectively.

Figure 3. Voltage vectors and sectors on the space vector.

2.2. Common-Mode Voltage in H7 Inverter

The PWM inverter is fed by the DC source during the duration of the active voltage vectors. Therefore, CMV reduction of the H7 inverter is realized by turning off the S_7 switch during the dwell time of one of the zero-voltage vectors and disconnecting the inverter from the DC source. The equivalent circuit for the H7 inverter topology of Figure 1a with an off-state S_7 switch and the V_7 zero-voltage vector are shown in Figure 4a. Assuming the on state and off state of the switch to be short circuit and high resistance (R_{off}) respectively, the voltages between P and the poles of phases a, b, and c are represented as

$$v_{Pa} = v_{Pb} = v_{Pc} = \left(\frac{R_{off}}{R_{off} + \frac{R_{off}}{3}} V_{dc} \right) = \frac{3}{4} V_{dc}, \quad (6)$$

Figure 4. Equivalent circuit of H7 inverter during zero-voltage vectors with S_7 switch turned off (a); S_7 switch connected to positive DC-link node. (b) S_7 switch connected to negative DC-link node.

Since the voltage across P and n, V_{Pn} , is $V_{dc}/2$, the pole voltage of one phase is given by Equation (7).

$$v_{xn, H7(P), V_7} = -v_{Px} + v_{Pn} = -\frac{1}{4} V_{dc}, \quad (7)$$

where the subscript, x, denotes phases a, b, and c. Using Equations (1) and (7), the CMV is calculated to be $-V_{dc}/4$.

On the other hand, for the H_7 inverter topology of Figure 1b, the CMV is reduced by turning off the S_7 switch during the V_0 zero-voltage vector. The equivalent circuit for this case is shown in Figure 4b, and the voltages, v_{Na} , v_{Nb} , and v_{Nc} , are given by Equation (8).

$$v_{Na} = v_{Nb} = v_{Nc} = -\frac{3}{4} V_{dc}, \quad (8)$$

Since the voltage V_{Nn} is $-V_{dc}/2$, the pole voltage of each phase is represented as

$$v_{xn, H7(N), V_0} = -v_{Nx} + v_{Nn} = \frac{1}{4}V_{dc}, \quad (9)$$

From Equations (1) and (9), the CMV is calculated to be $V_{dc}/4$. Therefore, for the H7 inverter, the CMV can be reduced to half of the conventional magnitude during the dwell time of one of the zero-voltage vectors. Table 1 summarizes the CMV according to the voltage vector and the circuit configuration.

Table 1. Common-mode voltage according to the voltage vector and circuit configuration.

	2-Level Inverter (Figure 2)	H7 Inverter (P) (Figure 1a)	H7 Inverter (N) (Figure 1b)
V_0 (000)	$-V_{dc}/2$	$-V_{dc}/2$	$V_{dc}/4$
V_1 (100)	$-V_{dc}/6$	$-V_{dc}/6$	$-V_{dc}/6$
V_2 (110)	$V_{dc}/6$	$V_{dc}/6$	$V_{dc}/6$
V_3 (010)	$-V_{dc}/6$	$-V_{dc}/6$	$-V_{dc}/6$
V_4 (011)	$V_{dc}/6$	$V_{dc}/6$	$V_{dc}/6$
V_5 (001)	$-V_{dc}/6$	$-V_{dc}/6$	$-V_{dc}/6$
V_6 (101)	$V_{dc}/6$	$V_{dc}/6$	$V_{dc}/6$
V_7 (111)	$V_{dc}/2$	$-V_{dc}/4$	$V_{dc}/2$

3. Proposed Modulation Method for Common-Mode Voltage Reduction in H7 Inverter

3.1. Modulation Strategy of Three-Phase Reference Voltages

As explained in Section 2, the two circuit configurations of the H7 inverter system reduce the CMV only for the duration of one of the zero-voltage vectors. The topology in Figure 1a,b achieves CMV reduction only for the V_7 and V_0 zero-voltage vectors, respectively. Therefore, to achieve CMV reduction in all regions, the reference voltages should be manipulated to have only one kind of zero-voltage vector in the switching patterns. Figure 5 shows the switching pattern of the conventional and proposed modulation methods for the H7 inverter structure of Figure 1a. As shown in Figure 5a, the reference voltages are sorted in descending order as $v_{s,max}^*$, $v_{s,mid}^*$, and $v_{s,min}^*$, and the duration of the two zero-voltage vectors (V_0 , and V_7) is determined by $v_{s,max}^*$ and $v_{s,min}^*$, respectively. If a similar offset voltage is added to the three-phase reference voltages of the H7 inverter of Figure 1a, the V_0 zero-voltage vector is removed from the switching pattern, as shown in Figure 5b. The offset voltage for removing the V_0 zero-voltage vector from the switching pattern is defined by Equation (10).

$$v_{offset} = \frac{V_{dc}}{2} - v_{s,max}^*, \quad (10)$$

Using the offset voltage in Equation (10), the three-phase reference voltages are modified as Equations (11)–(13).

$$v_{an}^* = v_{as}^* + v_{offset}, \quad (11)$$

$$v_{bn}^* = v_{bs}^* + v_{offset}, \quad (12)$$

$$v_{cn}^* = v_{cs}^* + v_{offset}, \quad (13)$$

The maximum of the modified reference voltages, $v_{n,max}^*$, sticks to $V_{dc}/2$, and only one zero-voltage vector, V_7 , remains in the switching pattern, as shown in Figure 5b. Since only the duration of the zero-voltage vectors is changed, the duty cycle of the active voltages remains the same, and the linear modulation range is preserved during the switching period.

Figure 5. Switching pattern of the H7 inverter topology of Figure 1a: (a) without proposed algorithm; (b) with proposed algorithm.

The H7 inverter in Figure 1b is required to remove the V_7 zero-voltage vector for CMV reduction. For this topology, the offset voltage is defined by Equation (14). The minimum of the modified reference voltages, $v_{n,min}^*$, sticks to $-V_{dc}/2$, and the zero-voltage vector, V_0 , remains in the switching pattern while V_7 is eliminated.

$$v_{offset} = -\frac{V_{dc}}{2} - v_{s,min}^* \quad (14)$$

3.2. Switching Method of the Seventh Switch in H7 Inverter

The switching of the seventh switch is determined by the manipulated zero-voltage vector. As shown in Figure 5b, the S_7 switch is kept in the on state during the dwell time of the active voltage vectors and is only turned off during the dwell time of the zero-voltage vector. Therefore, the minimum of the modified reference voltages is utilized to generate the switching signal of the S_7 switch [31].

3.3. Implementation of the Proposed Algorithm

Figure 6 shows the overall block diagram of the proposed algorithm for the H7 inverter of Figure 1a. The reference voltages are manipulated by the offset voltage given in Equation (10). The switching signals are generated by comparing the three-phase reference voltages with a carrier. For the operation of the S_7 switch, the minimum of the reference voltages is detected and also compared with the same carrier. The proposed algorithm can be easily realized because it only requires calculation of the offset voltage and comparison operation for the minimum of the reference voltage with the carrier.

In Figure 7, the switching patterns are shown for all sectors. Since each sector has only one zero-voltage vector, V_7 , the proposed algorithm can reduce the CMV in all sectors of the space vector.

Figure 6. Implementation of proposed algorithm.

Figure 7. Switching pattern of the H7 inverter topology of Figure 1a: (a) Sector A1; (b) Sector A2; (c) Sector A3; (d) Sector A4; (e) Sector A5; (f) Sector A6.

4. Simulation Result

A computer simulation using the MATLAB/Simulink platform was used to validate the performance of the proposed algorithm, as shown in Figure 8. Table 2 shows the system specifications used in the simulation. All the simulations were performed on an H7 inverter topology where the seventh switch is installed at the positive node of the DC-link.

Figure 8. MATLAB/Simulink model of proposed algorithm.

Table 2. Specification of the H7 inverter drive system.

	Parameter	Value
DC-Link	DC voltage	300 V
	DC capacitor	4700 uF
Motor	Rated active power	1.8 kW
	Rated rotational speed	1500 rpm
	Rated torque	11.5 N·m
	Rated rms line current	14.8 A
	Pole pair	4
	Rotor inertia	0.0064 kg m ²
Controller	Switching frequency	100 KHz

Figure 9 shows the simulation results of the CMV for the three modulation methods (SVPWM [32], MDPWM [29], and the proposed algorithm) at MI = 0.3 and a 50% load torque.

The SVPWM is implemented for the H7 inverter by always turning on the seventh switch, and the resulting CMV has a value that ranges from -150 V ($-V_{dc}/2$) to 150 V ($V_{dc}/2$), as shown in Figure 9a. The number of changes of the CMV is six times during one switching period, as shown in Figure 9b. The results of the MDPWM method, [29], shown in Figure 9c prove that the peak value of the CMV is reduced to -75 V ($-V_{dc}/4$) from -150 V ($-V_{dc}/2$) in the region where the V_7 zero-voltage vector is applied. However, despite changing the V_0 zero-voltage vector generated by the DPWM to the V_7 zero-voltage vector, the conventional MDPWM algorithm does not turn off the seventh switch in the region where the V_0 zero-voltage vector is generated by the DPWM method. This causes the magnitude of the CMV during the V_0 zero-voltage vector to be 150 V ($V_{dc}/2$), which is similar to the SVPWM method in [32]. The change in the CMV happens four times during one switching period, as shown in Figure 9d. The result in Figure 9e shows that the proposed algorithm reduces the CMV to -75 V ($-V_{dc}/4$) from -150 V ($-V_{dc}/2$) in all sectors. The CMV does not exceed 50 V ($V_{dc}/6$) because the injection of the offset voltage given in Equation (10) makes sure that only one zero-voltage vector, V_7 , is included in the switching pattern, and the seventh switch of the H7 inverter is turned off for the duration

of the V_7 zero-voltage vector. As can be seen from the simulation results, the proposed algorithm reduces the peak-to-peak value of the CMV by 58% and 44% compared to the SVPWM and MDPWM methods, respectively. The number of changes of the CMV is four times in every switching period, which is similar to the MDPWM method. Figure 10 shows the CMV characteristic of the H7 inverter with the proposed method according to the MI. When the MI is changed, the switching pattern is different, but the peak-to-peak value of the CMV still varies from -75 V to 50 V.

Figure 9. CMV at MI = 0.3 and 50% load torque: (a) SVPWM [32]; (b) enlarged waveform with SVPWM [32]; (c) MDPWM [29]; (d) enlarged waveform with MDPWM [29]; (e) proposed algorithm; (f) enlarged waveform with proposed algorithm.

Figure 10. Simulation results of CMV with proposed algorithm with 50% load torque: (a) MI = 0.6; (b) enlarged waveform at MI = 0.6; (c) MI = 0.9; (d) enlarged waveform at MI = 0.9.

5. Experimental Result

An experiment was performed to verify the validity of the proposed algorithm using the laboratory test setup shown in Figure 11. The overall experimental system was configured using DSP (TMS320C28377D), an A/D converter (AD7864), a DC-link capacitor, a current sensor (LEM LA-25P), a D/A converter (DAC8803), an H7 inverter, and a motor-generator (MG) set, which uses HIGEN FMATF20-AB00 as both the motor and generator. The inverter system is designed using the GaN switch (GS66508T), and the seventh switch is connected to the positive node of the DC-link. The same parameters listed in Table 2 were used for the experiment.

Figure 11. Experimental setup for H7 inverter drive system: (a) H₇ inverter control system hardware; (b) MG set.

Figure 12 shows the comparison of the results of the SVPWM [32], conventional MDPWM [29], and proposed algorithm at 50% load torque and a modulation index of 0.3. The results in Figure 12 show that the proposed algorithm significantly reduces the CMV and leakage current compared with the SVPWM and conventional MDPWM methods.

Figure 12. Experimental result of the conventional and proposed algorithms at 50% load torque and MI = 0.3: (a) SVPWM [32]; (b) enlarged waveform with SVPWM [32]; (c) MDPWM [29]; (d) enlarged waveform with MDPWM [29]; (e) proposed algorithm; (f) enlarged waveform with proposed algorithm.

The performance of the proposed algorithm is verified for various MIs at different load torques, as shown in Figures 13 and 14. Figure 13 shows the results of the proposed algorithm at no load with MIs of 0.3, 0.6, and 0.9. The results confirm that the CMV ranges from -75 V ($-V_{dc}/4$) to 50 V ($V_{dc}/6$), which verifies the analysis in Section 2. As the MI increases, the duration of the active voltage vector increases, but the peak-to-peak value of the CMV remains the same. However, due to the need to use dead time in the physical system, a glitch in the CMV that resides beyond the expected peak-to-peak range happens once in a while. The leakage current that flows between the neutral points of the motor and DC-link is reduced in all conditions compared to the conventional methods. The proposed

algorithm attenuates the leakage current by 73% and 40% compared to the SVPM and MDPWM methods, respectively. In Figure 14, the results of the CMV are shown under the condition of 5.75 Nm (50%) load torque for various MIs. The switching patterns of the CMV are changed, but the CMV is still within the same range as the results under the no-load condition. The leakage currents also are similar at the different MIs and load torques.

Figure 13. Experimental result of the proposed algorithm according to MI in no-load condition: (a) MI = 0.3; (b) enlarged waveform at MI = 0.3; (c) MI = 0.6; (d) enlarged waveform at MI = 0.6; (e) MI = 0.9; (f) enlarged waveform at MI = 0.9.

Figure 14. Experimental result of the proposed algorithm according to MI with 50% load torque: (a) MI = 0.3; (b) enlarged waveform at MI = 0.3; (c) MI = 0.6; (d) enlarged waveform at MI = 0.6; (e) MI = 0.9; (f) enlarged waveform at MI = 0.9.

The efficiency and THD of the three modulation methods are shown in Figure 15. The proposed method has a slightly higher THD compared to the SVPWM method but has almost a similar THD compared to the MDPWM method. In terms of efficiency, the three modulation methods have similar performance, as shown in Figure 15. The three-phase line current waveform for the proposed algorithm is given in Figure 16. The comparison of the SVPWM, MDPWM, and proposed algorithm with respect to various aspects is given in Table 3.

Figure 15. System efficiency and THD of three-phase current: (a) SVPWM; (b) MDPWM; (c) proposed algorithm.

Figure 16. Three-phase current for the proposed algorithm.

Table 3. Performance comparison of various PWM methods.

	SVPWM	MDPWM	Proposed Method
Switching frequency	100KHz	100KHz	100KHz
Modulation index	0.3	0.3	0.3
Phase current (rms)	7.4A	7.4A	7.4A
Leakage current (peak to peak)	800mA	360mA	216mA
CMV	$-\frac{V_{dc}}{2}$ to $\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{4}$ to $\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{4}$ to $\frac{V_{dc}}{6}$
Efficiency (%)	92.357	91.856	92.028
Current THD (%)	0.745	1.108	1.110

6. Conclusions

The H7 inverter topology deploys an additional seventh switch to the two-level inverter to further reduce the peak-to-peak value of the CMV. In the H7 inverter topology, the SVPWM method does not use the off state of the seventh switch and generates a CMV having a similar magnitude to the CMV of the common two-level PWM inverter. However, as the proposed algorithm turns off the seventh switch during the entire dwell time of the zero-voltage vector, and the MDPWM turns off the seventh switch only for half of the dwell time of the zero-voltage vectors, the proposed algorithm results in the lowest peak-to-peak value of the CMV and leakage current. The proposed algorithm is easy to

implement. It modifies the three-phase reference voltages by adding an offset voltage to guarantee the use of only one zero-voltage vector in the switching pattern. During the zero-voltage vector, the seventh switch is always turned off regardless of the sector in the space vector, the MI, and the load torque. As a result, the peak-to-peak value of the CMV is reduced by 58% and 44% compared with the SVPWM and MDPWM methods, respectively. It also attenuates the leakage current by 73% and 40% compared to the SVPWM and MDPWM methods, respectively.

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