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A Novel Single-Switch High Step-Up DC–DC Converter with Three-Winding Coupled Inductor

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Abstract: This paper introduces a single-switch, high step-up DC–DC converter for photovoltaic applications such as power optimizers and microinverters. The proposed converter employs two voltage multipliers cells with switched capacitor and magnetic coupling techniques to achieve high voltage gain. This feature, along with a passive clamp circuit, reduces the voltage stress across the switch, allowing for the employment of low R_{DSon} MOSFET. This leads to low conduction loss of the switch. The diodes operate with zero-current switching at their turn-off transition, eliminating the reverse recovery losses. Additionally, the switch turns on with zero-current switching, leading to insignificant switching loss associated with its turn-on transition. The operation principle and steady-state analysis are presented and validated through experimental results obtained from a 140 W prototype of the proposed converter.

Keywords: high step-up DC–DC converters; zero current switching; three-winding coupled inductor; photovoltaic energy

1. Introduction

The development of technologies to improve the performance of architectures with distributed maximum power point tacking (MPPT) are fundamental to raise grid-utilitydistributed generation systems from photovoltaic (PV) solar sources in large urban centers, mainly for residential applications. Although architectures with PV module-integrated converters (MICs) and parallel connected power optimizers have maximum power point tracking (MPPT) per PV module capability, these configurations are different: architectures with MICs, shown in Figure 1a, convert the PV module DC voltage directly to AC, since MICs are composed of two power conversion stages (DC–DC followed by DC–AC); on the other hand, in architectures with parallel-connected power optimizers, shown in Figure 1b, the output DC voltage of the power optimizer is converted into AC by a central inverter [1,2].

Due to the low voltage and efficiency of PV modules, high-gain DC–DC converters are necessary in MICs and power optimizers to boost the DC bus voltage of the DC–AC converter above the minimum value necessary while tracking the maximum power of PV modules. A classical boost converter is normally used as the DC–DC stage despite its limitations for high static gain. The voltage stress of the main switch is equal to its output voltage, which results in high conduction losses. Furthermore, an outstandingly high duty cycle causes large conduction losses and reverse recovery problems. As a consequence, the conventional boost converter would not be adequate for high step-up voltage gain applications [2–5].

There are some techniques that can be used to increase the DC–DC converter output voltage in order to solve the high gain problem described above. In addition, it is essential



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Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). to reduce losses related to semiconductor switches. Within the literature, there is a consistent demand for new converters with high efficiency, high reliability and high voltage gain characteristics.



Figure 1. Architectures with distributed MPPT. (a) MICs, (b) parallel-connected power optimizers.

The literature presents several review articles that characterize different voltageboosting techniques. Among them, the following techniques stand out: multi-stage (multilevel, interleaved, cascaded); voltage multiplier cells (VMCs); magnetic coupling (with or without coupled inductors) and switched capacitors (SCs). Each technique has its own features and should be selected based on the application and its requirements [5–11].

In order to reduce the input current ripple, an interleaved structure is used. This technique allows current sharing between parallel modules which operate alternately. The main disadvantage of this technique is the required number of cells to achieve higher gain. In [12–15], VMCs are added to increase the voltage gain, while the converter presented in [16] uses SCs for extra voltage gain.

VMCs are usually cell-based structures, presented after the main switch to decrease its voltage stress. Due to the arrangements of semiconductors, capacitors and inductors, VMCs are able to provide high voltage gain with a low component count, as presented in [17–20]. Due to their modular structure, various VMCs can be cascaded to achieve a higher gain [12,21]. This combination can improve advantages or reduce negative traits. Nevertheless, more components are required for extremely high gain, leading to complex circuits with higher costs.

In the literature, DC–DC converters based on SCs have been proposed to provide high voltage gain in modular schemes [22–24]. This technique is employed by inserting semiconductor and capacitor structures. The voltage gain is obtained due to the capacitive energy transfer, but at the cost of a high number of components. Moreover, SCs can be used along with coupled inductors to further increase the static gain [18,25–30].

Coupled inductors are valuable components of magnetic coupling techniques. As many applications do not require electrical isolation, this element is an interesting alternative to boost voltage gain. Furthermore, it can reduce the reverse recovery losses of diodes due to hard switching. Soft-switching conditions are found in [18,31,32], where the semiconductor components operate with ZCS.

Various magnetically coupled impedance networks have been presented in the recent literature [7–9]. In [33], a Y-source impedance network is presented to allow more design degrees of freedom. Furthermore, to achieve flexible topological structures and to reduce the voltage stress of rectifier diodes, multi-winding coupled-inductors are employed. Since higher voltage conversion is necessary, a three-winding coupled-inductor (TWCI) can be useful. However, the cost and volume may increase because of the complexity in the design of TWCI.

Recent studies in [13,19] concluded that an interleaved coupled-inductor converter can be used to develop a DC–DC boost topology based on a three-winding coupled-inductor. This method has the advantage of adopting a single switch while obtaining high efficiency conversion, high step-up and high power density.

Considering the limitations of high-gain boost converters and the aspects described above, a novel single-switch high step-up DC–DC converter suitable for high power conversion is proposed in this paper. The new topology is characterized by a three-winding coupled-inductor and two symmetrical modules. SC cells are placed in the middle of the circuits to increase the output voltage level with low voltage stress across all components, allowing the use of low $R_{DS_{on}}$ semiconductors. In addition, the coupled inductor has a dominant boost feature, providing a even higher voltage gain. Due to the utilization of the magnetic coupling, special considerations for recycling the leakage energy are implied. Thus, a passive clamp circuit is used to absorb the energy of the leakage inductance and to improve the converter's efficiency. Additionally, the diodes operate with zero-current switching at their turn-off transition, eliminating the reverse recovery losses. Furthermore, the MOSFET's switching loss associated with its turn-on transition is minimized as a consequence of zero-current switching.

In this paper, a novel single-switch high step-up DC–DC converter with TWCI is presented and a 140 W prototype is used to corroborate the theoretical analysis. The circuit description and operating principles are discussed in detail in Section 2. The steady-state analysis of the proposed topology is approached in Section 3, where the static voltage gain and the voltage stress values on power devices are obtained. It is followed by the selection of parameters in Section 4. In addition, the performance comparison with existing high step-up DC–DC converters is presented in Section 5. In order to validate the theoretical analysis, the experimental results are shown in Section 6. Finally, conclusions are presented in Section 7.

2. Operational Principle and Analysis

The equivalent circuit of the proposed topology is shown in Figure 2, where the assumed voltage polarities and current directions are also given. The components in the circuit are defined as:

- N_1 , N_2 and N_3 are the primary and the two secondary turn numbers, respectively, in which $n = \frac{N_2}{N_1} = \frac{N_3}{N_1}$;
- *L_k* is the leakage inductance of the coupled inductor;
- *L_m* is the magnetizing inductance of the coupled inductor;
- *S* is the single switch;
- *D*₁ and *D*₄ are the clamper circuit diodes;
- *D*₂ and *D*₃ are the switched capacitors' diodes;
- *C*₁ and *C*₄ are the clamper circuit capacitors;
- *C*₂ and *C*₃ are the switched capacitors;
- *C*_o is the output capacitor;
- *C_{in}* is the input capacitor.

Operating States

Figure 3 introduces the key waveforms of the proposed converter, where T and D are the period of the switching waveform and the duty cycle, respectively. Based on the waveforms, four main operating stages can be observed when analyzing the proposed converter in the CCM (continuous conduction mode) operation, and are described as follows:



Figure 2. The equivalent circuit of the proposed converter.



Figure 3. Key waveform of the proposed single-switch three-winding coupled-inductor converter.

State 1 ($t_0 - t_1$, shown in Figure 4a): the switch is turned on with zero current switching at $t = t_0$. The leakage inductance, L_k , is charged by the input capacitor, C_{in} ; at the same time, the magnetizing inductance, L_m , is discharged with voltage, V_{in} . The difference between the currents on L_k and the current on L_m flows through the primary winding, N_1 , decaying until it reaches zero. During this interval, the current is transferred through the secondary windings, N_2 and N_3 , and through switched capacitors' diodes, D_2 and D_3 . All the remaining diodes are turned off. This interval is is proportional to the leakage inductance. This stage ends when the leakage current, i_{L_k} , become equal in value to the magnetizing current, i_{L_m} at $t = t_1$. The following equations are obtained:

$$i_{L_m}(t) = i_{L_m}(t_0) - \frac{V_{in}}{L_m}(t - t_1),$$
(1)

$$i_{L_k}(t) = i_{L_k}(t_0) + \frac{V_{C_2} - V_{C_1}}{nL_k}(t - t_1),$$
(2)

$$i_{D_2}(t) = i_{D_3}(t) = \frac{i_{L_k}(t) + i_{L_m}(t)}{2n}.$$
 (3)

State 2 ($t_1 - t_2$, shown in Figure 4b): from the time $t = t_1$, the current i_{L_k} remains equal to the current, i_{L_m} . This causes the currents through primary and secondary windings to maintain zero, which subsequently causes diodes D_3 and D_2 to turn off with zero current switching. The magnetizing inductance, L_m , and leakage inductor, L_k , are charged by the input capacitor. Thus, i_{L_m} and i_{L_k} are increased linearly. Meanwhile, all capacitors release energy to the output. This state is responsible for the high voltage gain. The following equations are written:

$$i_{L_m}(t) = i_{L_m}(t_1) + \frac{V_{in}}{L_m}(t - t_2),$$
(4)

$$i_{L_k}(t) = i_{L_m}(t). \tag{5}$$

State 3 ($t_2 - t_3$, shown in Figure 4c): at the time $t = t_2$, the converter's switch is turned off. The clamper diodes D_4 and D_1 become forward biased and capacitors C_1 and C_4 start to be charged. Furthermore, the switched capacitors are charged through the diodes D_3 and D_2 . The energy of leakage inductance is recycled. This results in the i_{L_k} discharging with voltage $\frac{V_{C_2} - V_{C_1}}{n}$; hence, the current decays linearly. The current i_{L_k} values become smaller than i_{L_m} , which change the primary winding current direction. As a result, i_{N_1} increases linearly. The followings equation are obtained:

i

$$i_{L_m}(t) = i_{L_m}(t_2) + \frac{V_{in} - V_{C_1}}{L_m}(t - t_3),$$
(6)

$$i_{L_k}(t) = i_{L_k}(t_2) - \frac{V_{C_2} - V_{C_1}}{nL_k}(t - t_3).$$
⁽⁷⁾

State 4 $(t_3 - t_4)$, shown in Figure 4d): at this state, the switch remain turned off. The current i_{N_1} surpasses i_{L_m} at instant t_3 . This causes the current i_{L_k} to reach a slightly negative value. Furthermore, the diodes D_1 and D_4 to turn off with zero current switching. This state ends when *S* begins to conduct at t_4 , restarting the cycle. The following equations describe this interval:

$$i_{L_m}(t) = i_{Lm}(t_3) - \frac{V_{in} - V_{C_1}}{L_m}(t - t_4),$$
(8)

$$i_{L_k}(t) = \frac{V_{C_2} - V_{C_1}}{nL_k}(t - t_4),$$
(9)

$$i_{D_2}(t) = i_{D_3}(t) = \frac{i_{L_k}(t) + i_{L_m}(t)}{2n}.$$
 (10)



Figure 4. Topological states of the proposed converter. (a) State 1, (b) state 2, (c) state 3, (d) state 4.

3. Steady-State Analysis

To simplify the process of theoretical analysis, the following assumptions were made:

- All components are ideal;
- $n = \frac{N_2}{N_1} = \frac{N_3}{N_1};$
- The capacitance values of the switched capacitors are the same;
- The capacitance values of the clamper circuit capacitors are the same;
- Capacitors are large enough to reasonably neglect the voltage ripples.

Since the leakage inductance impact is not considered, state 1 and 4 are contemplated in the analysis performed in this section. This occurs because of these stages are mainly associated with the charge and discharge of this inductance, respectively.

3.1. Voltage Gain Derivation

By applying the volt-second balance to the magnetizing inductor, L_m , during the turn on and off states of the switch, the voltage over the clamp capacitors C_1 and C_4 can be achieved by the equation below.

$$V_{C_1} = V_{C_4} = \frac{V_{in}}{1 - D}.$$
(11)

By applying the Kirchhoff's Voltage Law in state 3, the voltage stress across the capacitors C_2 and C_3 can be derived as:

$$V_{C_2} = V_{C_3} = V_{N_{2,off}} + V_{C_1} = (1 + nD)\frac{V_{in}}{1 - D}.$$
(12)

The output voltage, V_o , and the converter's voltage gain are:

$$V_o = V_{C_o} = V_{C_2} + V_{C_3} - V_{in}.$$
(13)

$$G = \frac{V_o}{V_{in}} = \frac{1 + 2nD + D}{1 - D}.$$
 (14)

In Figure 5, the voltage gain is illustrated for different turn ratio values. As it is illustrated, the proposed converter achieves high voltage gain without needing an extremely large duty cycle or needing to operate at elevated turn ratios.



Figure 5. Duty cycle versus voltage gain for distinct turn ratios.

3.2. Semiconductors' Voltage Stress

From the steady-state analysis of the proposed converter, it is observed that the voltage over the power switch during state 3 is equal to the voltage of the capacitors C_1 and C_4 . Thus, from Equation (11), the maximum voltage across the switch is defined as:

$$V_S = V_{C_1} = \frac{V_{in}}{1 - D}.$$
 (15)

Thus, low drain source on the resistance switch can be used to reduce conduction losses on this device.

By using Kirchhoff's voltage law in the proposed converter operating intervals and from Equations (11) and (12), the maximum voltage over the diodes are:

$$V_{D_1} = V_{D_4} = V_{C_1} = \frac{V_{in}}{1 - D},$$
(16)

$$V_{D_2} = V_{D_3} = V_{C_2} - V_{C_1} = nD\frac{V_{in}}{1-D}.$$
(17)

It can be noted that the voltage stresses of the diodes D_1 and D_4 are lower than the voltage stresses of the diodes D_2 and D_3 . Additionally, the MOSFET losses and the switching losses of all diodes can be reduced due to ZCS operation. Hence, the efficiency is improved in this topology.

3.3. Average Current Stresses

The average currents through the magnetizing inductance and semiconductors in a switching cycle can be obtained by analyzing Figure 2. Thus, those can be described as follows:

$$\bar{I}_{Lm} = I_{in} + I_o = (G+1)I_o,$$
(18)

$$\bar{I}_{D1} = \bar{I}_{D4} = \bar{I}_{D2} = \bar{I}_{D3} = I_o, \tag{19}$$

$$I_S = I_{in} - 2I_o = (G - 2)I_o.$$
⁽²⁰⁾

3.4. Maximum Current Stresses

The peak current of magnetizing inductance is equal to half of the total ripple plus its average value. Thus, from (4) and (18), the equation is given by:

$$\widehat{I}_{Lm} = \overline{I}_{Lm} + \frac{\Delta I_{Lm}}{2} = \frac{2 + 2nD}{1 - D} I_o + \frac{TDV_{in}}{2L_m}.$$
(21)

The maximum current on the diodes D_1 and D_4 happens at t_2 , as shown in Figure 3. Its value is equal to half of the magnetizing current at the same time. Hence, it can be expressed as shown below:

$$\hat{I}_{D1} = \hat{I}_{D4} = \frac{\hat{I}_{Lm}}{2}.$$
(22)

From Figure 3, it is observed that the peak current on the diodes D_2 and D_3 happens at t_3 and is equal to the secondary winding current at the same instant. Thus, the peal current on these components is given by:

$$\widehat{I}_{D2} = \widehat{I}_{D3} = \frac{\widehat{I}_{N1}}{2n}.$$
 (23)

The maximum value of the current on the switch can be found at t_2 , as seen in Figure 3. It is noted that this maximum value is equal to the magnetizing current minus the output current at the same moment. Thus, it can be calculated as:

$$\widehat{I}_S = \widehat{I}_{Lm} + I_o. \tag{24}$$

4. Design Considerations

4.1. Turns Ratio Selection

The turns ratio of the coupled inductor is essential for the voltage and current stresses of power devices and duty cycle. Figure 5 illustrates the influence of the turns ratio on the voltage gain. Thus, using Equation (14), it can be calculated as:

$$n = \frac{G - 1 - D(G + 1)}{2D}.$$
(25)

4.2. Magnetizing Inductance Selection

The inductance is selected by using the current ripple of the magnetizing inductor. From the state 2 analysis in Figure 4b and Equation (4), it can be determined that:

$$L_m = \frac{TDV_{in}}{\Delta I_{L_m}}.$$
(26)

To operate in the CCM, the following condition must be satisfied:

$$\overline{I}_{L_m} - \frac{\Delta I_{L_m}}{2} > 0. \tag{27}$$

Thus, substituting Equations (21), (26) and (27):

$$L_{mB} = \frac{TDR_o}{2G(G+1)}.$$
(28)

The proposed converters operates in CCM if L_m is higher than L_{mB} . On the other hand, the discontinuous conduction mode occurs when the L_m is smaller.

4.3. Capacitance Selection

In order to suppress the capacitors' voltage ripple to an acceptable range, the minimum capacitance should be determined. To simplify the considerations of the capacitor design, it

is considered $C_1 = C_4$ and $C_2 = C_3$. According to (11) and (12), the voltages of capacitors for the proposed topology are calculated. The charge absorbed or produced by the capacitors are derived as:

$$\Delta V_c = \frac{\Delta Q}{C_i},\tag{29}$$

where i = 1, 2, o.

The maximum tolerant voltage ripple $\left(\frac{V_{C_i}}{\Delta V_{C_i}}\right)$ is usually set at 1%. The suitable values of the capacitors can be determined as follows:

$$C_1 \ge \frac{(1-D)^2 T G}{R_o} \frac{V_{C_1}}{\Delta V_{C_1}},$$
 (30)

$$C_2 \ge \frac{(1-D)^2 T G}{n D R_o} \frac{V_{C_2}}{\Delta V_{C_2}},$$
(31)

$$C_o \geqslant \frac{TD}{R_o} \frac{V_o}{\Delta V_{C_o}}.$$
(32)

4.4. Semiconductor Devices Selection

Two factors are determinant when seleting the proper semiconductor devices: (i) their voltage stress; and (ii) their current stress. The voltage stress can be obtained from Equations (15)–(17). The average and peak current stresses are determined by Equations (19), (20), and (22)–(24). Therefore, the chosen semiconductor devices' characteristics are normally larger than the determined values.

5. Performance Comparison

For demonstrating the performance of the proposed converter, it is compared with other related converters presented in [12,14,16,18,25,27,32–35]. In this study, the turns ratio is considered $n = \frac{N_2}{N_1} = \frac{N_3}{N_1} = 1$. Thus, the topologies in [18,27,33] are excluded due to their limitations.

The comprehensive comparison between the proposed topology and the recent studies from the literature is summarized in Table 1. Their main characteristics, such as voltage gain, maximum voltage stresses on switches, diodes and capacitors and the total number of components, have been compared.

For a deeper comprehension, this analysis is also illustrated in Figure 6. The topologies in [12,14,16] use interleaved strategies with two switches. For that reason, the continuous conduction of both is considered, with switches operating at a duty cycle higher than 0.5. Therefore, values for duty cycle lower than 0.5 are not desired and not plotted for them. Furthermore, the topology in [34] has a duty cycle limitation. Thus, values for duty cycle higher than 0.5 are not plotted for this converter.

As demonstrated in this table, the proposed converter has the lowest number of semiconductors components. However, the developed topology has a higher number of capacitors than the converters presented in [14,35]. Additionally, the suggested converter has a small component number. Thus, the cost, weight and size of the proposed converter are acceptable.

Despite the fact that the number of coupled inductors in [16] is double the proposed topology, its voltage gain is lower for a duty cycle higher than 0.65. It is noteworthy that the voltage gain of the converters suggested in [14,32,35] is lower than the proposed topology with more numbers of power components, even though the component count of the converters presented in [35] is slightly lower.



Figure 6. Comparison of the main circuit features. (a) Voltage gain, (b) total voltage stress of switch, (c) total voltage stress of diode, (d) total voltage stress of capacitor.

Ref.	Number of Components					Vallage Cair (C)	Maximum Voltage Stress		
	I	CI	С	D/S	Total	voltage Gain (G)	V _S /Vin	V _D /Vin	V _C /Vin
[12]	0	1	6	6/2	15	$\frac{5n+1}{1-D}$	$\frac{G}{5n+1}$	$\frac{2nG}{5n+1}$	$\frac{(3n+1)G}{5n+1}$
[14]	1	1	3	4/2	11	$\frac{1+n}{1-D}$	$\frac{G}{1+n}$	$\frac{nG}{1+n}$	$\frac{nG}{1+n}$
[16]	0	1	5	6/2	15	$n + \frac{2+2nD-D}{1-D}$	$\frac{G}{2+nD+n-D}$	$\frac{(1+n)G}{2+nD+n-D}$	$n + \frac{(2-D)G}{2+nD+n-D}$
[25]	0	1	5	5/1	12	$\frac{3+3n}{1-D}$	$\frac{G}{3+3n}$	$\frac{(1+2n)G}{3+3n}$	$\frac{G(1+n)}{3+3n}$
[32]	1	1	6	5/1	14	$2n + \frac{2nD+1}{1-D}$	$\frac{G}{2n+1}$	$\frac{nDG}{2n+1}$	$\frac{G(1+n-nD)}{2n+1}$
[34]	0	1	6	5/1	13	$\frac{2+n(2-D)}{1-2D}$	$\frac{2G-n}{4+3n}$	$\tfrac{(2G-n)(1+n)}{4+3n}$	$\frac{(1+2n-nD)G}{2+2n-nD}$
[35]	0	1	4	4/1	10	$n + \frac{2-D+n}{1-D}$	$\frac{G}{2+2n-D(1+n)}$	$\tfrac{(1+n)G}{2+2n-D(1+n)}$	$2+n+\tfrac{DG}{2+2n-D(1+n)}$
Prop.	0	1	5	4/1	11	$\frac{1+2nD+D}{1-D}$	$\frac{G}{1+2nD+D}$	$\frac{nG}{1+2nD+D}$	G
I inductors CI coupled inductors C capacitors D/S diadas/switches Prop proposed converter									

Table 1. Performance comparison of similar converters.

I—inductors. CI—coupled inductors. C—capacitors. D/S—diodes/switches. Prop.—proposed converter.

Since the suggested converter achieves high voltage gain using a low turn ratio and duty cycle, it is a promising solution. For better understanding, Figure 6a provides information about the comparison of voltage gain versus duty cycle. It is worth noting that the presented topology has a greater voltage gain than the converters suggested in [14,16,32,35] for a duty cycle higher than 0.7.

The voltage stress on the switch of these eight converters is shown in Figure 6b. It can be noted that the proposed converter has a lower total voltage stress when analyzing the others converters. This makes viable the use of semiconductors with small parasitic components, minimizing conduction losses.

As illustrated in Figure 6c, to achieve the same output voltage gain, the suggested topology produces the lowest total switching voltage stress on diodes almost overall. This feature is a result of diodes ZCS operation at their turn-off transition. Though, from Figure 6d, it can be seen that the proposed topology has the highest total capacitors voltage stress. This drawback is caused by the higher number of capacitor in this topology.

6. Experimental Results

In this section, the effectiveness of the proposed topology is evaluated in order to corroborate the theoretical analysis and performance; the model is designed with output voltage and input voltage set to 220 V and 14.8 V, respectively. The switching frequency used in the prototype is 100 kHz, with a load power of 140 W. The experimental prototype is illustrated in Figure 7 and the specifications of the prototype circuit are listed in Table 2. The current and voltage waveforms were obtained using an Yokogawa's DL850 Oscillo-scope.



Figure 7. Photograph of the experimental prototype.

Table 2. Operational specifications used on the prototype.

Specifications	Value
Output Power	140 W
Input Voltage	14.8 V
Output Voltage	220 V
Switching Frequency	100 KHz
C_1, C_2, C_3, C_4, C_o	10 μF/250 V
Magnetizing Inductance L _m	15 μΗ
Leakage Inductance L_k	1 µH
Turns Ratio	1:2:2, C055071A2
Power Switch	IPP048N12N3, $R_{DS_{on}} = 4.8 \text{ m}\Omega$
Diodes D_1 and D_4	STTH1202, $V_{F_{(typ)}} = 0.82 \text{ V}$
Diodes D_2 and D_3	STTH802, $V_{F_{(typ)}} = 0.8$ V

Figure 8 illustrates the switch gate signal, input and output voltages. It is noted that the voltage gain is almost fifteen times larger for a duty cycle that is not extremely large, about 0.72 in agreement with Equation (14).



Figure 8. Top window : gate signal V_g (5 V/div); bottom window: output voltage V_o (50 V/div) and input voltage V_{in} (5 V/div).

The switch voltage and current are shown in Figure 9. The switch turns on at the ZCS condition with low voltage stress, around 50 V. It can be seen that the voltage stress is less than a quarter of the output voltage. Besides, the conduction losses can be reduced by employing low on-resistance MOSFET. These results validate Equations (15) and (24).



Figure 9. Switch voltage $V_S(10 \text{ V/div})$ and current $i_S(5 \text{ A/div})$.

Figure 10 exhibits the voltage stresses on clamper diodes as well as currents through them. The peak voltages are about 50 V, which is in accordance with Equation (16). From Figure 11, it can be seen that the voltage stresses on diodes D_2 and D_3 are around 70 V, as defined in Equation (17). Moreover, one can see that all diode currents fall to zero when the diodes are turned off. This means that all converter diodes operate with ZCS at turn off time. Hence, the diode reverse recovery losses are eliminated. The experimental results obtained using the prototype are consistent with the operating analysis illustrated in Figure 4c,d.



Figure 10. Top window : diode D_1 voltage V_{D_1} (10 V/div) and current i_{D_1} (1 A/div); bottom window: diode D_4 voltage V_{D_4} (10 V/div) and current i_{D_4} (1 A/div).



Figure 11. Top window : diode D_2 voltage V_{D_2} (20 V/div) and current i_{D_2} (0.5 A/div); bottom window: diode D_3 voltage V_{D_3} (20 V/div) and current i_{D_3} (0.5 A/div).

The magnetic component's currents are represented in Figure 12. i_{L_m} illustrates the converter operation in the continuous conduction mode, corroborating with Equation (28). It can be noted that the leakage inductor current i_{L_k} equals i_{L_m} in state 2 in accordance with Figure 4b. Additionally, the primary winding current i_{N_1} surpasses i_{L_m} , which is in agreement with the operating analysis in state 4, shown in Figure 4d. As a result, i_{L_k} reaches a slightly negative value. Hence, the currents waveform are in good agreement with Figure 3, validating the steady-state analysis.



Figure 12. Primary winding N_1 current i_{N_1} (5 A/div), leakage inductance L_k current i_{L_k} (5 A/div) and magnetizing inductance L_m current i_{L_m} (5 A/div).

Finally, the Yokogawa WT1800 power analyzer was utilized to measure the power conversion efficiency. Figure 13 summarizes the efficiency curve of the built prototype. The duty cycle is variable, while the output voltage and the load power are constant. The highest efficiency obtained is 93.77% at 51.27 W, while at full load, the efficiency is 91.84% at 140 W.



Figure 13. Efficiency test results for distinct duty cycle.

7. Conclusions

This study proposed a single-switch high step-up DC–DC converter. This element reduces the voltage stress on power devices, enabling the use of low $R_{DS_{on}}$ MOSFET. Additionally, the proposed topology can minimize reverse recovery losses through the diodes due to zero-current switching at their turn-off transition. The simulation results demonstrated that the proposed converter achieves high voltage gain and exhibits acceptable performance. Moreover, comprehensive analysis between the proposed converter and

other similar high step-up DC–DC topologies was carried out. This comparison emphasized the advantages and disadvantages of the presented converter. To complement this study, a 140 W prototype was built to validate the proposed solution. The experimental results corroborate the good performance of the proposed converter.

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Abbreviations

The abbreviations presented below are used in this paper:

AC	Alternating current
CCM	Conntinuous Conduction Mode
DC	Direct current
ESR	Equivalent Series Resistance
IPOS	Input-parallel Output-series
MOSFET	Metal-oxide-semiconductor field effect
MPPT	Maximum Power Point Trackers
PV	Photovoltaic
RES	Renewable Energy Sources
RMS	Root Mean Square
SC	Switched Capacitors
TWCI	Three-winding coupled-inductor
VMC	Voltage Multiplier Cells
VSI	Voltage Source Inverter
ZCS	Zero-Current Switching
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