energies

MDPI

Article

A Novel Single-Inductor Bipolar-Output DC/DC Boost Converter for OLED Microdisplays

Ingrid Casallas [1], Robert Urbina [1], Carlos-Ivan Paez-Rueda [1], Carlos Adrián Correa-Flórez [1], José Vuelvas [1], Manuel Parraga [1,2], Abdel-Karim Hay [1], Arturo Fajardo [1,*] and Gabriel Perilla [1]

[1] Department of Electronic Engineering, Pontificia Universidad Javeriana, Bogotá 110311, Colombia; ingrid.casallas@javeriana.edu.co (I.C.); r_urbina@javeriana.edu.co (R.U.); paez.carlos@javeriana.edu.co (C.-I.P.-R.); carlosa-correaf@javeriana.edu.co (C.A.C.-F.); vuelvasj@javeriana.edu.co (J.V.); manuel.parraga@javeriana.edu.co (M.P.); karim.hay@javeriana.edu.co (A.-K.H.); gabriel.perilla@javeriana.edu.co (G.P.)

[2] Faculty of Mechanical, Electronic and Biomedical Engineering, Universidad Antonio Nariño, Bogotá 111321, Colombia; manuelparraga@uan.edu.co

* Correspondence: fajardoa@javeriana.edu.co

Abstract: In this paper, a novel SIBO (Single-Inductor Bipolar-Output) DC/DC Boost converter is proposed to power OLED (Organic Light-Emitting Diode) microdisplays. The proposed topology merges a conventional SISO (Single-Inductor Single-Output) DC/DC Boost converter and a switched capacitor inverter to produce a SIBO converter without both the cross-regulation effect and the unbalanced output voltages. Moreover, its control circuit and efficiency are almost the same as the conventional SISO Boost converter. Therefore, the novel converter maintains the power density, the small form factor, and the high efficiency of its conventional counterpart. The proposed converter was analyzed under continuous-conduction mode operation using the moving average operator and charge conservation principle. As a result, the authors proposed an equation set with the main averages and ripples of the circuit variables expressed as analytical functions of the circuit components, the input voltage, and the duty cycle. Both the functionality of the proposed converter and the accuracy of the developed equation set were analyzed by extensive simulations. The simulation performed using ideal components was characterized by a mean absolute percentage error of 0.774% with a standard deviation of 1.566%. These results confirm the high accuracy of the proposed equation set. Furthermore, the non-ideal model simulation confirms the functionality of the proposed converter in "real" operation conditions. Under simulation with non-ideal components, the result statistics were a mean absolute percentage error of 7.36% with a standard deviation of 6.91%. Therefore, the converter design using the proposed ideal model could be a good start point of a converter optimization process based on more complex component models and assisted by computer-aided design tools.

Keywords: bipolar boost converter; SIBO DC/DC converter; SIMO DC/DC converter; voltage unbalance elimination

Citation: Casallas, I.; Urbina, R.; Paez-Rueda, C.I.; Correa-Flórez, C.A.; Vuelvas, J.; Parraga, M.; Hay, A.K.; Fajardo, A.; Perilla, G. A Novel Single-Inductor Bipolar-Output DC/DC Boost Converter for OLED Microdisplays. *Energies* **2021**, *14*, 6220. https://doi.org/10.3390/en14196220

Academic Editor: Adolfo Dannier

Received: 31 July 2021
Accepted: 16 September 2021
Published: 29 September 2021

1. Introduction

The display technologies are being used in several electronic devices such as smartphones, tablets, computer monitors, televisions, and IP phones [1,2]. These technologies are recognized as indispensable to adopt technological paradigms such as the internet of things [3]. Currently, liquid crystal displays are the dominant technology [1,4]. However, the market of the organic light-emitting diode (OLED) and the inorganic mini-LEDs (mLED) has grown rapidly, especially in the low-cost and small-sized display applications [1,4]. This market is estimated to grow to USD $1.2 billion by 2030 [3]. In particular, the OLED displays are used in portable electronic devices because of their high screen quality (i.e., high-contrast, high-speed, wide viewing angles, wider color gamut, and higher brightness), low cost, and low power consumption [1,4,5].

The power consumption of the OLED displays is determined by the efficiency of the power chain composed of the display driver, the Active Matrix OLED (AMOLED), and its optical system [4]. In recent years, progress in OLED materials has greatly improved AMOLED efficiency [6]. Therefore, the driver efficiency became very significant in the system power chain and its design become a critical step in the design of OLED microdisplays (i.e., integrated on a silicon wafer) [7–10]. Along with high efficiency, the AMOLED driver should provide the positive and negative output voltages (with low ripple) required to turn on the AMOLED pixels without light fluctuation [8,11–13]. Furthermore, this power manager unit must be characterized by its small form factor and low-complexity control to simplify its integration [8,13]. The regulation specifications of the voltages are different because only the positive voltage directly affects the pixel luminance of the OLED microdisplays [8], a more detailed discussion on this topic can be found in [14].

The bipolar input voltage required by the AMOLED of the microdisplay can be generated by a power manager unit composed of two parallel DC-DC converters [15], two DC-DC converters in cascade [14,16–19], or a Single-Inductor Bipolar-Output (SIBO) switched converter topology [7,8,12,20–24]. The first approach is typically used because it is easy to design and suitable for time-to-market [24]. However, its main limitation is the need for two inductors and their impact on form factor and cost of the microdisplay [7]. The goal of the second approach is to reduce the cost and the area of the microdisplay by removing one inductor [14]. In this approach, the power manager unit is composed of a single-inductor converter and an inductor-less converter (see Figure 1a), which can be implemented with a linear regulator or a switched capacitor converter. In the linear regulator implementation, both the efficiency and the chip active area are significantly reduced [24]. Therefore, system designers only use linear implementation for lighter loads [25]. On contrary, in the switched capacitor implementation, the efficiency is not dramatically affected and the chip active area is larger than the one used by the linear regulator solution because the secondary converter control required a complex logic circuit [24]. Finally, the conventional SIBO approach provides high efficiency with a decrease of the die area by using a single time-shared inductor [26].

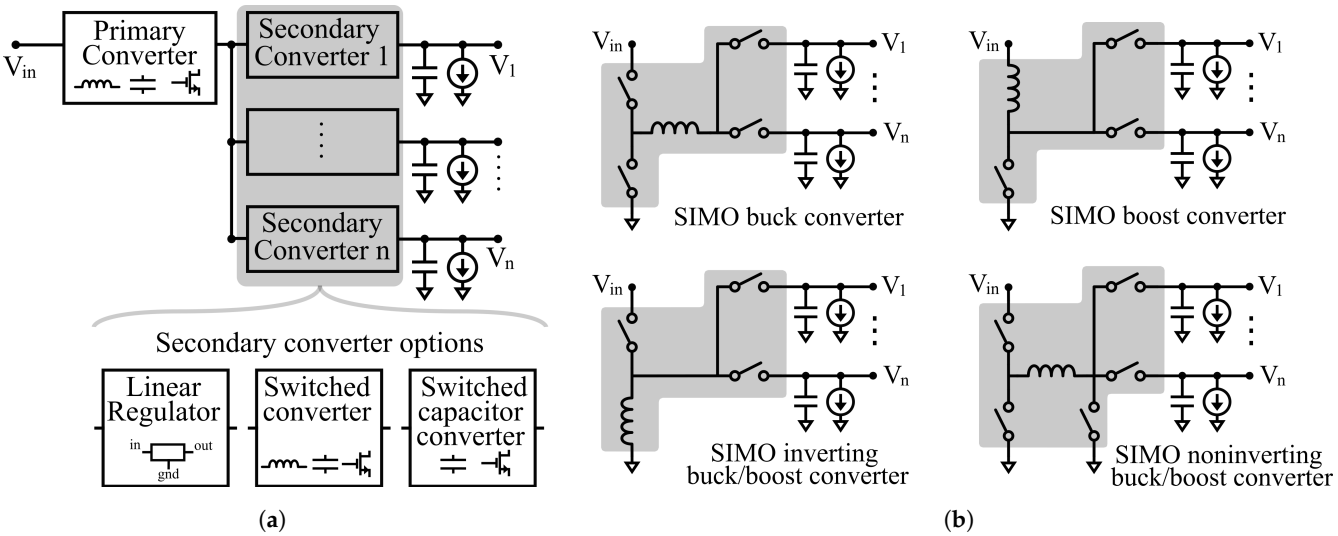

Figure 1. Topology of used DC/DC converters. (**a**) Cascade converters; (**b**) Conventional SIMO converters.

The conventional SIBO converter is part of the conventional Single-Inductor Multiple-Output (SIMO) switching converter family [23], which basic topology is depicted in Figure 1b. Topologically, conventional SIMO converters are circuit extrapolations of the corresponding Single-Inductor Single-Output (SISO) converters, except that energy flow and feedback control are more complex [26]. Furthermore, a voltage variation in one output affects the other ones because they share a common inductor [23,27]. In particular, the conventional SIBO converters generate a significant disparity in their outputs because of

the cross-regulation effect [12,23]. Some examples of conventional SIBO for OLED microdisplays can be found in [8]. Although many researchers have explored non-conventional SIBO converters to overcome the cross-regulation for OLED microdisplays, they are mainly focused on converter design and its control schemes [7,14,24]. However, its application scope is limited by either a lack of load flexibility or the complexity of the converter and its control circuits [25]. For instance, in [14] a SIBO Boost converter is implemented for OLED microdisplays. The positive output voltage is regulated by a modified comparator control, and the negative output voltage is regulated by a charge-pump operation with a proportional-integral control. The authors proposed a SIBO converter operating in both Discontinuous Conduction Mode (DCM) and Continuous-Conduction Mode (CCM). In [8], a power-efficient SIBO converter is proposed for microdisplays used in virtual reality applications. The authors proposed a converter that regulates its negative output voltage using hysteretic skipping control and regulates the positive output voltage with higher priority than the negative one to increase its power efficiency and decrease the pixel luminance variations. In [24], the author developed and tested a non-conventional SIBO topology under DCM for AMOLED displays that overcome the cross-regulation effect using the voltage mode control technique and only five switches. Moreover, in [7] the authors propose a non-conventional SIBO topology to improve the display quality by achieving a near-zero voltage ripple by the use of floating negative output and low-power shunt regulators. As the last example, in [13], the authors propose a simultaneous energy transferring SIBO converter which operates with two phases. The resulting converter uses a flying capacitor to reduce the inductor ripple and the conduction loss. Finally, and to the best of the authors' knowledge, it is important to notice that in the state-of-the-art analyzed, there is an acknowledged gap in the optimizing of SISO converter and a capacitive switched converter in a cascade connection to generate a non-conventional SIBO converter with the main advantage of the absence of the cross-regulation effect due to its working principle.

In this paper, a novel SIBO Boost converter is proposed. Furthermore, this converter eliminates both the cross-regulation effect and the output voltage imbalance (under unbalanced loads) without a dedicated control system. The novel topology results from an optimized combination of a conventional SISO Boost Converter and a switched capacitor voltage inverter, as is illustrated in Figure 2. Additionally, an analytical equation set was proposed, which predicts the steady-state behaviors of the converter under CCM operation. The converter functionality and the equation set accuracy were analyzed by extensive simulations. The simulation performed using ideal components was characterized by a mean absolute percentage error of 0.774% with a standard deviation of 1.566%. These results confirm the high accuracy of the proposed equation set. Furthermore, simulation with non-ideal components confirms the functionality of the proposed converter in "real" operation conditions. The resulting statistics were a Mean Absolute Percentage Error (MAPE) of 7.36% with a Standard Deviation (SD) of 6.91%. Therefore, the converter design using the proposed ideal model could be a good start point of a converter optimization process assisted by computer-aided design tools and more complex component models. The rest of the article is divided as follows. Section 2 is dedicated to the topological derivation of the novel converter. In Section 3 is presented the development of the analytical equations set, which is composed of expressions for the average and ripple values of voltages and currents in the capacitors and inductance, respectively. In Section 4 is presented the verification of the equations set by parametric simulations. Finally, in Section 5, the conclusions and future works are summarized.

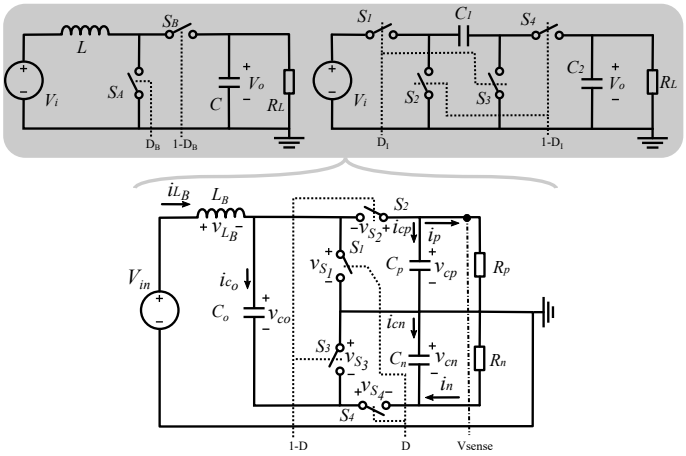

Figure 2. Topology of the proposed SIBO Boost converter.

2. Topology Derivation

The proposed topology is derived from two converters connected in a cascade configuration. The primary converter is a conventional SISO Boost, and the secondary one is a conventional switched capacitor inverter, as is shown in Figure 3a. As the switched capacitor inverter can operate with any duty cycle (D), the control circuits are integrated as shown in Figure 3b. As the switches S_{I1} and S_{B2} are redundant, they can be replaced by a single switch. Following the same approach, switches S_{I2} and S_{B1} are simplified too. Furthermore, the capacitor C_o can be connected directly with the inductor L_B because this connection point has the same signal voltage as the original one if the ripple is neglected. After these changes, the switches S_{I1} and S_{I2} are unnecessary, and they are removed. The resulting topology is shown in Figure 3c. As the input of the converter control, the designer could sense the positive or negative load voltages. This selection is closely related to the design requirements. For instance, the design can sense the input voltage of the critical load, which typically is the one that had the most restricted dynamic range. In Figure 3c,d, the critical load was assumed as R_p and R_n, respectively. Finally, in Figure 2 the switches are renamed and the notation of each voltage is indicated to simplify the analysis in the rest of the paper. Furthermore, in this figure, the control circuit senses the positive voltage because these voltages are directly related to the AMOLED pixel illumination quality.

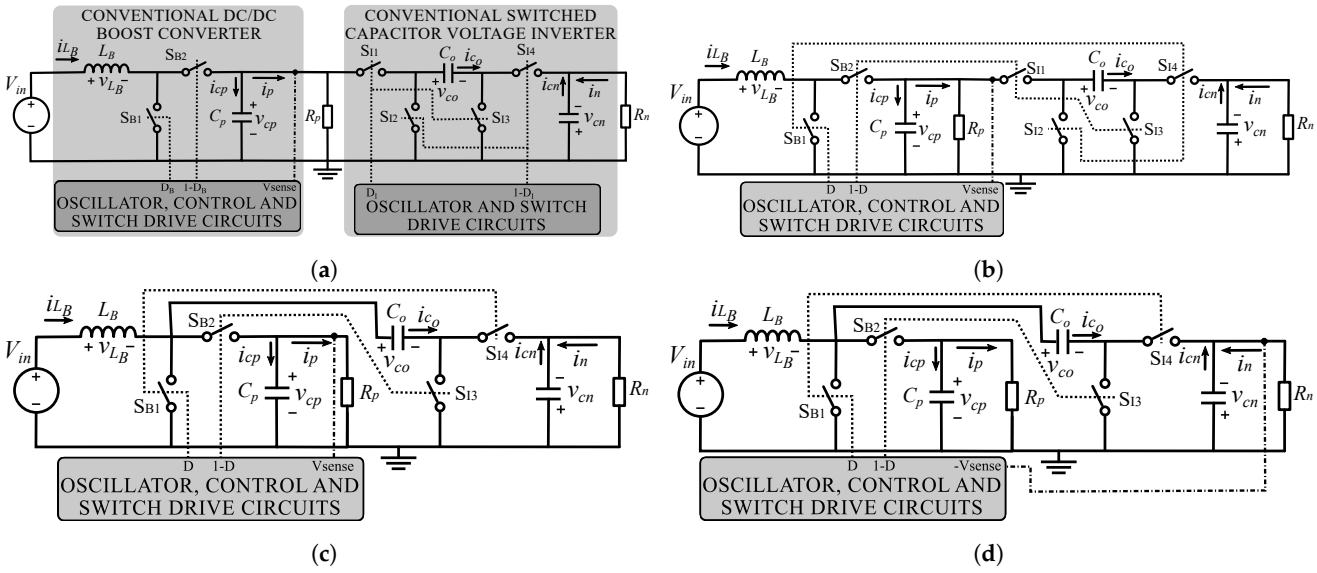

Figure 3. Optimization of the proposed cascade converters. (**a**) Step 0; (**b**) Step 1; (**c**) Step 2; (**d**) Step 3.

3. CCM Operation of the Proposed Topology

To analyze the operating principle of this converter in steady-state, two switching intervals derived from Figure 2 are considered. On one hand, in the first interval (i.e., $0 < t < DT_s$) the switches S_1 and S_4 are simultaneously on, and S_2 and S_3 are off. On the other hand, in the second interval (i.e., $DT_s < t < T_s$) the overall switches commuted to the contrary state, the resulting equivalent circuits are shown in Figure 4. In the first interval, the capacitors C_o and C_n are connected in parallel and they supply the energy demanded by R_n. Moreover, at the starting of the interval, the capacitors instantly matched their voltages and generated a current impulse. Simultaneously, the inductance is charged by the input voltage and the energy demand of R_p is supplied by the capacitor C_p. In the second interval, the capacitors C_o and C_p are connected in parallel and they supply the energy demanded by R_p. Furthermore, at the starting of the interval, the capacitors instantly matched their voltages and generated a current impulse. Simultaneously, the inductance L_B delivers the stored energy to the capacitors C_o, C_p, and the energy demand of R_n is supplied by the capacitor C_n.

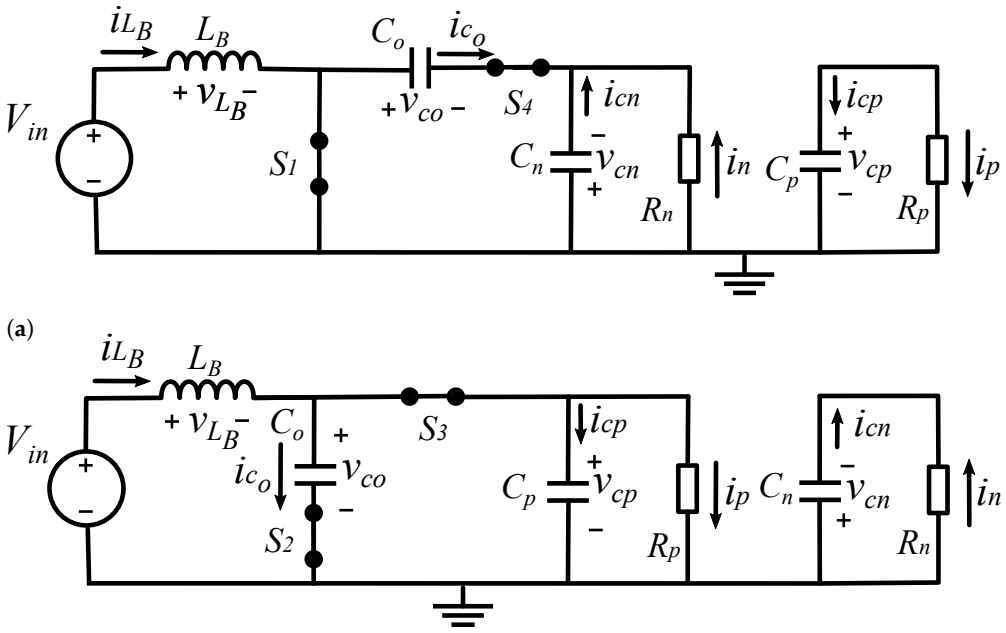

Figure 4. Equivalent circuits of the converter in steady-state. (**a**) Interval 1: $0 < t < DT_s$; (**b**) Interval 2: $DT_s < t < T_s$.

Assuming CCM operation for the converter, small ripple approximation [28], and ideal current sources as converter loads, the main converter waveforms are estimated and plotted in Figure 5. In these figures, the impulse currents are plotted as gray arrows, the slopes as blue triangles, and the average function values as a dashed line.

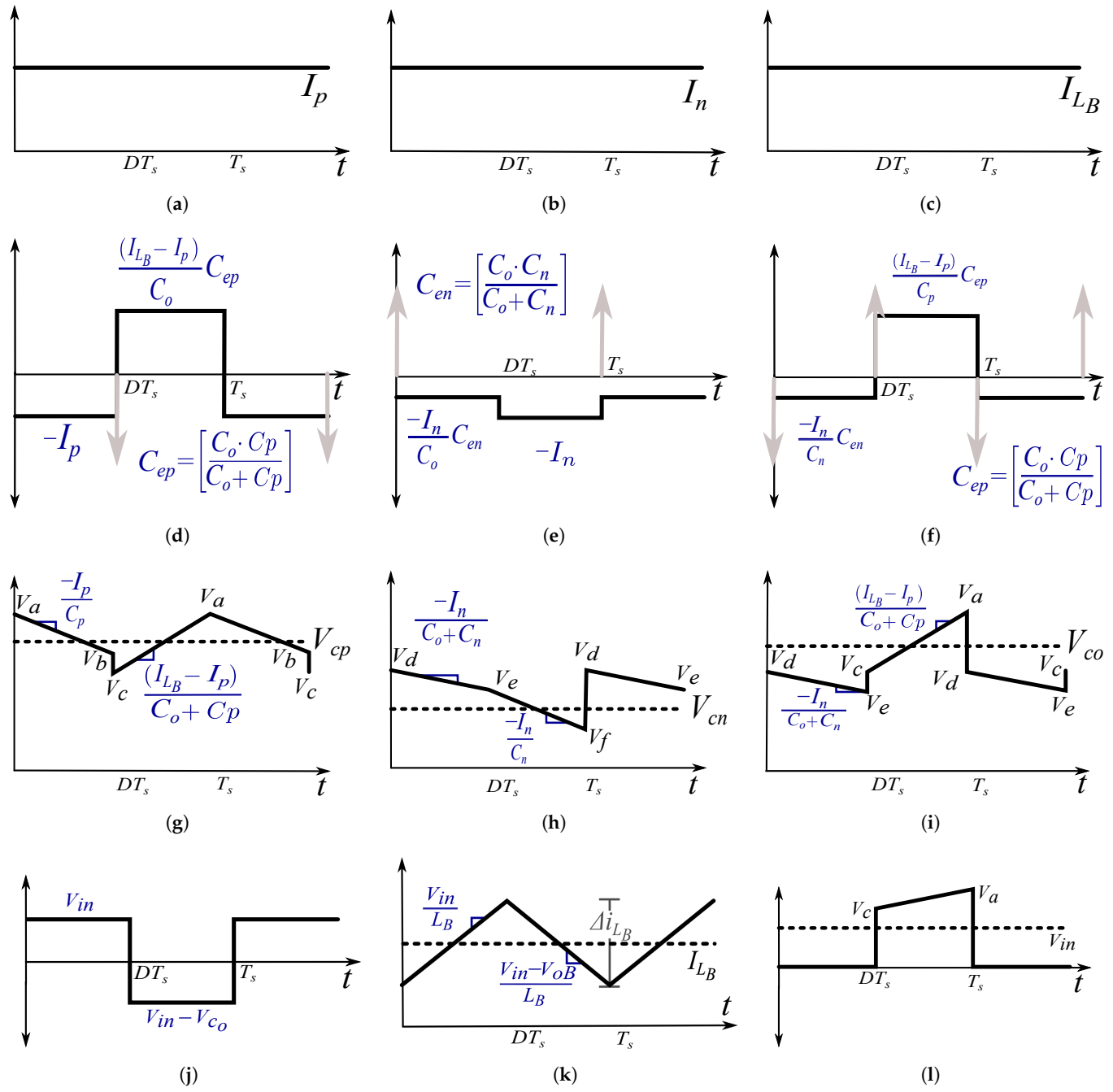

Figure 5. Main current and voltage waveforms of the converter in steady-state using small ripple approximation. (**a**) $i_p(t)$, (**b**) $i_n(t)$, (**c**) $i_{L_B}(t)$ with small ripple approximation. (**d**) $i_{cp}(t)$, (**e**) $i_{cn}(t)$, (**f**) $i_{co}(t)$, (**g**) $v_{cp}(t)$, (**h**) $v_{cn}(t)$, (**i**) $v_{co}(t)$, (**j**) $v_{L_B}(t)$, (**k**) $i_{L_B}(t)$ without small ripple approximation. (**l**) $v_{S_1}(t)$.

The average values and the ripple of the main circuit variables of the converter (i.e., V_{cp}, V_{cn}, V_{co}, and I_{L_B}) were calculated based on the waveform summarized in Figure 2. The resulting analytical equations are given by

$$V_{cp} = \frac{V_a + V_b}{2} D + V_{in} \quad (1)$$

$$V_{cn} = \frac{V_d + V_e}{2} D + \frac{V_e + V_f}{2}(1 - D) \quad (2)$$

$$V_{co} = \frac{V_d + V_e}{2} D + \frac{V_c + V_a}{2}(1 - D) \quad (3)$$

$$I_{L_B} = \frac{I_p + I_n}{1 - D} \quad (4)$$

$$\Delta v_{cp} = V_a - min(V_c, V_b) = V_a - V_b + \frac{V_b - V_c}{2} + \left| \frac{V_b - V_c}{2} \right| \quad (5)$$

$$\Delta v_{cn} = V_d - V_f \quad (6)$$

$$\Delta v_{co} = V_a - min(V_e, V_c) = V_a - V_c + \frac{V_c - V_e}{2} + \left| \frac{V_c - V_e}{2} \right| \quad (7)$$

$$\Delta i_{L_B} = \frac{V_{in}}{L_B} D T_s \quad (8)$$

Considering the linear discharge of the capacitors (see Figure 5g–i) were found some relationship between the variables used to describe the converter voltage waveforms (i.e., V_a, V_b, V_c, V_d, V_e, and V_f), which are given by

$$V_b = V_a - \frac{I_p}{C_p} D T_s \quad (9)$$

$$V_a = V_c + \frac{I_{L_B} - I_p}{C_o + C_p}(1 - D) T_s \quad (10)$$

$$V_e = V_d - \frac{I_n}{C_o + C_n} D T_s \quad (11)$$

$$V_f = V_e - \frac{I_n}{C_n}(1 - D) T_s \quad (12)$$

An additional equation set with the relationship between the variables used to describe the converter voltage waveforms were obtained using the charge conservation principle (i.e., the total amount of electric charge in a system does not change with time) [28]. Furthermore, the Equations (13) and (14) results from applying this principle to the circuit analysis at $t = DT_s$ and $t = T_s$, respectively.

$$V_b C_p + V_e C_o = V_c (C_p + C_o) \quad (13)$$

$$V_f C_n + V_a C_o = V_d (C_n + C_o) \quad (14)$$

Replacing (13) and (14) in the Equations (9)–(12) and before some mathematical manipulation, the Equations (9)–(12) could be rewritten as

$$V_c = V_a - \frac{I_n T_s}{C_o + C_p} \left[\frac{I_p}{I_n} D + 1 \right] \quad (15)$$

$$V_d = V_a - \frac{I_n T_s}{C_o} \left[\frac{C_n}{C_o + C_n} D + (1 - D) \right] \quad (16)$$

$$V_e = V_a - \frac{I_n T_s}{C_o} \quad (17)$$

$$V_f = V_a - \frac{I_n T_s}{C_o} \left[1 + \frac{C_o}{C_n}(1 - D) \right] \quad (18)$$

In addition, applying Kirchhoff's voltage law to the mesh composed of the input voltage source, the inductor, and the switch S1. The S1 voltage was found as

$$v_{s1} = v_{in} - v_{L_B} \tag{19}$$

Assuming steady-state and the moving average operator (i.e. $\frac{1}{T}\int_0^T x(t)\,dt$, where T is the fundamental period of the function $x(t)$ [28]), the Equation (19) is rewritten as

$$\frac{1}{T_s}\int_0^{T_s} v_{s1}(t)\,dt = \frac{1}{T_s}\int_0^{T_s} v_{in}(t)\,dt - \frac{1}{T_s}\int_0^{T_s} v_{L_B}(t)\,dt = V_{in} \tag{20}$$

Calculating the left side of the (20), a relation between the input voltage and the variables used to describe the converter voltage waveforms (see Figure 5l), which is given by

$$V_{in} = \frac{V_c + V_a}{2}(1 - D) \tag{21}$$

Finally, from (21) and (10), V_a is given by

$$V_a = \frac{V_{in}}{(1-D)} + \frac{I_n T_s}{2(C_0 + C_p)}\left[\frac{I_P}{I_n}D + 1\right] \tag{22}$$

Assuming $C_p = C_n = C_o = C$, $I_p = I_n = 0.5 \cdot I_x$ (i.e., balanced load), and replacing (15)–(18) and (22) in (1)–(7), the average values and the ripple of the main converter components can be rewritten as

$$V_{cp} = V_{oB} - \Delta V_x\left(D^2 - D\right) \tag{23}$$
$$V_{cn} = V_{oB} - \Delta V_x\left(D^2 - 5D + 5\right) \tag{24}$$
$$V_{co} = V_{oB} + \Delta V_x\left(2D^2 - 3D\right) \tag{25}$$
$$I_{L_B} = \frac{I_x}{1-D} \tag{26}$$
$$\Delta v_{cp} = \Delta V_x\left(1 + 3D + |D-1|\right) \tag{27}$$
$$\Delta v_{cn} = \Delta V_x\left(4 - 2D\right) \tag{28}$$
$$\Delta v_{co} = \Delta V_x\left(3 + D + |D-1|\right) \tag{29}$$

where ΔV_x is the common voltage ripple and V_{oB} is the conventional output voltage of the Boost converter, given by

$$\Delta V_x = \frac{I_x T_s}{8\,C} \tag{30}$$
$$V_{oB} = \frac{V_{in}}{1-D} \tag{31}$$

4. Evaluation of the Converter

The operation of the proposed topology and the accuracy of the expressions reported in Section 3 were validated by the simulation of twelve case studies, which circuit values are summarized in Table 1. The DC/DC converters 1 and 2 operate with low and high output voltage ripples (i.e., Δv_{cn} and Δv_{cp}), respectively. In the cases from 3 to 7, the duty

cycle was swept from 10% to 90% with steps of 20%. Finally, in the 8 to 12 converters, the input voltage was swept from 6 V to 10 V with steps of 1 V.

Table 1. Circuit values of the proposed converters.

Variable	Case Study	V_{in} [V]	C [µF]	L [mH]	I_x [A]	D [%]	T_s [µs]
Ripple	1	5.0	100	37	1.0	50	50
	2	5.0	10.0	3.7	1.0	50	50
Duty cycle	3	3.0	10.0	3.7	0.2	10	50
	4	3.0	10.0	3.7	0.2	30	50
	5	3.0	10.0	3.7	0.2	50	50
	6	3.0	10.0	3.7	0.2	70	50
	7	3.0	10.0	3.7	0.2	90	50
Input voltage	8	6.0	10.0	3.7	1.0	50	50
	9	7.0	10.0	3.7	1.0	50	50
	10	8.0	10.0	3.7	1.0	50	50
	11	9.0	10.0	3.7	1.0	50	50
	12	10	10.0	3.7	1.0	50	50

All the simulations use a voltage-controlled switch with off-resistance of 10 MΩ, on-resistance of 10 mΩ, and zero rise and fall commutation times. Furthermore, it uses ideal components (i.e., inductors and capacitors with infinite quality factor), whose initial conditions are configured using the values calculated from Equations (23)–(26) and Table 1. The overall simulations were carry-out on the same computer (Windows 10 of 64-bits, Intel® Core™ i7-6700T CPU @ 2.80 GHz, and RAM @ 8.00 GB) with the software PSIM (named as S3 in tables and figures), using the transient analysis with a maximum time step of 2 ns. Furthermore, the converters were simulated until they achieved their steady-state, which is quantitatively checked using the difference between the low-peak values of the slowest signal (i.e., the V_f in Figure 5h) in two consecutive periods (ΔV_f). Specifically, the numerical criterion is a value lower than 0.04% of the ratio of ΔV_f and the average value of the voltage V_{cn}. In addition, to compare the performance of this simulator with other available simulation tools, case studies 1 and 2 were simulated in OrCAD PSpice Designer (named as S1 in tables and figures) and LTspice (named as S2 in tables and figures) too. The time spent by each simulator is summarized in Table 2, the fastest simulator was PSIM.

Table 2. Times of the circuit simulations of converter 1 and 2.

Case Study	Ripple	Simulation Time [min]		
		OrCAD	LTspice	PSIM
1	Low	542.9	399.6	4.500
2	High	8.500	6.900	4.700

For case studies 1 and 2, the comparison between the theoretical values (i.e., calculated using Equations (8) and (23)–(29)) and the simulated results are shown in Table 3, Figures 6 and 7. The simulations converged, with consistent results between the three simulators, confirming that the steady-state behaviors of the waveforms are represented correctly by the proposed analytical equations. On one hand, the highest percentage error (Error [%]) is presented in the ΔV_{cp} parameter, which has a value close to zero. On the other hand, the lowest error is (Error [mA]) presented in the ΔI_{L_B} parameter. The statistical results of the evaluated parameters in these converters are shown in Table 4. The MAPE and its SD were calculated for each parameter with the results of the three simulators. The average voltages (V_{cp}, V_{cn}, and V_{co}) are characterized by a MAPE of 0.573% and 0.751% with an SD of 0.497% and 0.496% in the low and high ripple cases, respectively. Additionally, the ripple of these voltages had a MAPE of 6.447% and 1.001% with an SD of 5.230%

and 0.843% in the low and high ripple cases, respectively. The overall reported parameters (voltages and currents) are characterized by a MAPE of 2.650% and 0.760% with an SD of 4.321% and 0.698%, respectively. As the main conclusion, the accuracy of the analytical equation is high.

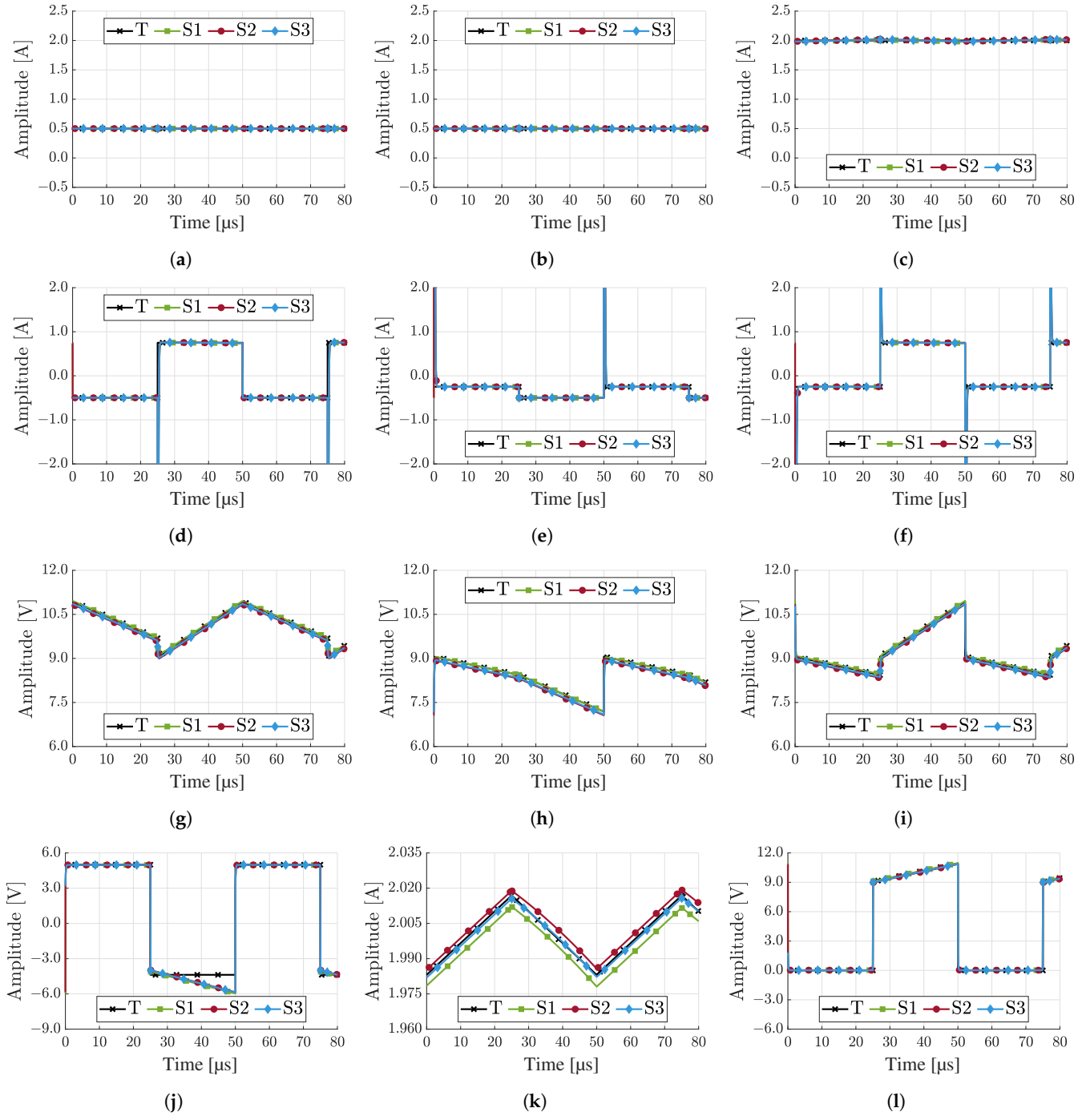

Figure 6. Waveforms validated in simulation for High ripple case. **(a)** $i_p(t)$; **(b)** $i_n(t)$; **(c)** $i_{L_B}(t)$ with small ripple approximation. **(d)** $i_{cp}(t)$; **(e)** $i_{cn}(t)$; **(f)** $i_{co}(t)$; **(g)** $v_{cp}(t)$; **(h)** $v_{cn}(t)$; **(i)** $v_{co}(t)$; **(j)** $v_{L_B}(t)$; **(k)** $i_{L_B}(t)$ without small ripple approximation. **(l)** $v_{S_1}(t)$; In this figure, the theoretical impulse currents were omitted intentionally to simplify the graphs. However, the simulated impulses are consistent with the theoretical ones.

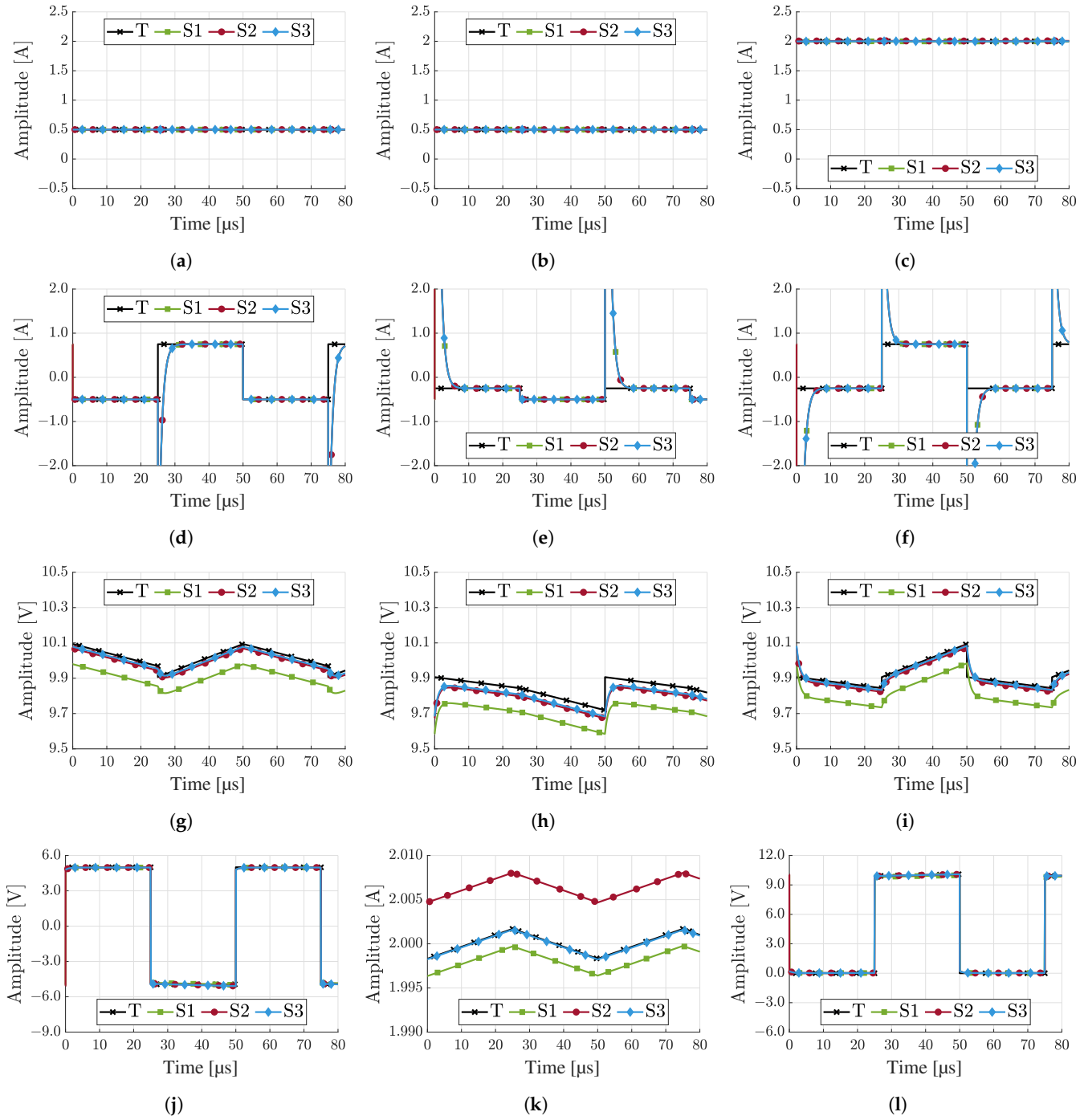

Figure 7. Waveforms validated in simulation for Low ripple case. **(a)** $i_p(t)$; **(b)** $i_n(t)$; **(c)** $i_{L_B}(t)$ with small ripple approximation. **(d)** $i_{cp}(t)$; **(e)** $i_{cn}(t)$; **(f)** $i_{co}(t)$; **(g)** $v_{cp}(t)$; **(h)** $v_{cn}(t)$; **(i)** $v_{co}(t)$; **(j)** $v_{L_B}(t)$; **(k)** $i_{L_B}(t)$ without small ripple approximation. **(l)** $v_{S_1}(t)$; In this figure, the theoretical impulse currents were omitted intentionally to simplify the graphs. However, the simulated impulses are consistent with the theoretical ones.

Table 3. Theoretical and simulated values of the converter with Ripple variation.

Case Study	Ripple	Simulator	V_{cp} [V]	V_{cn} [V]	V_{co} [V]	I_{L_B} [A]	Δv_{cp} [V]	Δv_{cn} [V]	Δv_{co} [V]	Δi_{L_B} [A]	Max. Error Parameter
1	Low	T [a]	10.02	9.828	9.938	2.000	0.188	0.188	0.250	0.003	
		S1 [b]	9.903	9.690	9.831	1.998	0.164	0.174	0.250	0.003	Δv_{cp}
		S2 [c]	9.992	9.779	9.920	2.006	0.165	0.175	0.252	0.003	Δv_{cp}
		S3 [d]	10.00	9.789	9.929	2.000	0.164	0.174	0.250	0.003	Δv_{cp}
		Error [mA] o [mV]	113.1	137.9	106.7	6.400	23.40	13.30	1.600	0.000	
		Error [%]	1.129	1.403	1.074	0.320	12.48	7.093	0.640	0.000	
2	High	T	10.16	8.281	9.375	2.000	1.875	1.875	2.500	0.034	
		S1	10.18	8.280	9.404	1.996	1.836	1.859	2.500	0.034	Δv_{cp}
		S2	10.06	8.154	9.283	2.003	1.841	1.861	2.509	0.034	Δv_{cp}
		S3	10.08	8.179	9.305	1.999	1.834	1.856	2.500	0.034	Δv_{cp}
		Error [mA] o [mV]	97.30	127.1	92.30	4.500	40.90	18.80	8.500	0.600	
		Error [%]	0.958	1.535	0.985	0.225	2.181	1.003	0.340	1.775	

[a] Theoretical. [b] OrCAD PSpice Designer. [c] LTspice. [d] PSIM.

Table 4. Percentage error statistical results of the proposed converter with Ripple variation.

Ripple	V_{cp}		V_{cn}		V_{co}		I_{L_B}		Δv_{cp}		Δv_{cn}		Δv_{co}		Δi_{L_B}	
	MAPE [%]	SD [%]	MAPE [%]	SD [%]	MAPE [%]	SD [%]	MAPE [%]	SD [%]	MAPE [%]	SD [%]	MAPE [%]	SD [%]	MAPE [%]	SD [%]	MAPE [%]	SD [%]
Low	0.504	0.544	0.769	0.551	0.445	0.547	0.142	0.160	12.25	0.355	6.880	0.282	0.213	0.370	0.000	0.000
High	0.640	0.384	0.931	0.804	0.681	0.340	0.133	0.098	2.020	0.199	0.862	0.132	0.120	0.191	0.690	0.951

The theoretical values and the results obtained by simulation for study cases 3 to 7 are shown in Table 5. These case studies analyze the accuracy of the proposed expressions regarding the duty cycle variable. According to the simulated results, the highest error is presented in case study 7 (D = 90%), and the lowest error in case study 3 (D = 10%). The waveforms of the case study with the highest error are shown in Figure 8. Additionally, the statistical results of the overall duty cycle sweeps are shown in Table 6. The MAPE and its SD were calculated for each parameter with the results of the five case studies. The average voltages (V_{cp}, V_{cn}, and V_{co}) are characterized by a MAPE of 0.289% with an SD of 0.228%. Moreover, the voltage ripples obtained a MAPE of 1.172% with an SD of 1.180%. These five case studies have an error of less than 4% in the evaluated voltages and currents. According to the results, the accuracy of the proposed analytical equations decreases if the duty cycle increases.

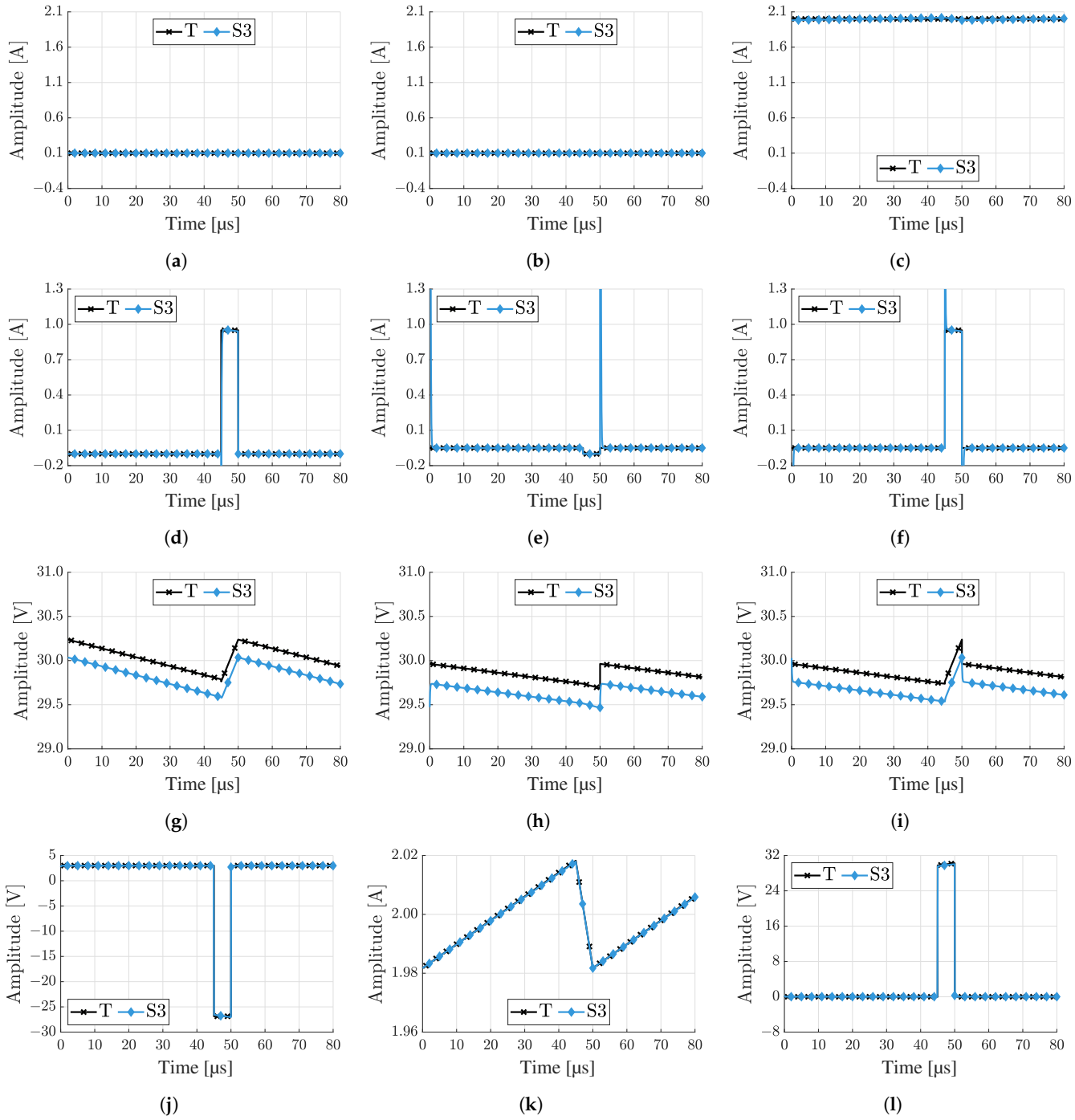

Figure 8. Waveforms validated in simulation for duty cycle of 90%. **(a)** $i_p(t)$; **(b)** $i_n(t)$; **(c)** $i_{L_B}(t)$ with small ripple approximation. **(d)** $i_{cp}(t)$; **(e)** $i_{cn}(t)$; **(f)** $i_{co}(t)$; **(g)** $v_{cp}(t)$; **(h)** $v_{cn}(t)$; **(i)** $v_{co}(t)$; **(j)** $v_{L_B}(t)$; **(k)** $i_{L_B}(t)$ without small ripple approximation. **(l)** $v_{S_1}(t)$; In this figure, the theoretical impulse currents were omitted intentionally to simplify the graphs. However, the simulated impulses are consistent with the theoretical ones.

Table 5. Theoretical and simulated values of the converter with Duty cycle variation.

Case Study	D [%]	Simulator	V_{cp} [V]	V_{cn} [V]	V_{co} [V]	I_{L_B} [A]	Δv_{cp} [V]	Δv_{cn} [V]	Δv_{co} [V]	Δi_{L_B} [A]	Max. Error Parameter
3	10	T [a]	3.345	2.770	3.298	0.222	0.275	0.475	0.500	0.004	Δv_{cp}
		S3 [b]	3.342	2.763	3.297	0.222	0.271	0.471	0.500	0.004	
		Error [mA] o [mV]	2.605	6.916	1.556	0.027	4.274	3.913	0.003	0.017	
		Error [%]	0.078	0.250	0.047	0.012	1.554	0.824	0.001	0.409	
4	30	T	4.312	3.837	4.196	0.286	0.325	0.425	0.500	0.012	Δv_{cp}
		S3	4.307	3.827	4.192	0.286	0.319	0.421	0.500	0.012	
		Error [mA] o [mV]	4.772	10.11	3.634	0.077	5.949	3.819	0.001	0.025	
		Error [%]	0.111	0.263	0.087	0.027	1.830	0.899	0.000	0.208	
5	50	T	6.031	5.656	5.875	0.400	0.375	0.375	0.500	0.020	Δv_{cp}
		S3	6.021	5.640	5.866	0.400	0.367	0.371	0.500	0.020	
		Error [mA] o [mV]	10.24	16.35	9.013	0.115	8.361	3.703	0.010	0.037	
		Error [%]	0.170	0.289	0.153	0.029	2.230	0.987	0.002	0.184	
6	70	T	10.03	9.751	9.860	0.667	0.425	0.325	0.500	0.028	Δv_{cp}
		S3	10.00	9.719	9.837	0.667	0.413	0.321	0.500	0.028	
		Error [mA] o [mV]	23.83	31.91	22.53	0.096	12.36	3.606	0.016	0.078	
		Error [%]	0.238	0.327	0.229	0.014	2.908	1.110	0.003	0.275	
7	90	T	30.01	29.84	29.87	2.000	0.475	0.275	0.500	0.036	Δv_{cp}
		S3	29.81	29.61	29.66	2.000	0.456	0.272	0.500	0.036	
		Error [mA] o [mV]	202.5	223.2	201.1	0.147	18.79	3.455	0.102	0.259	
		Error [%]	0.675	0.748	0.673	0.007	3.955	1.256	0.020	0.709	

[a] Theoretical. [b] PSIM.

Table 6. Percentage error statistical results of the proposed converter with Duty cycle variation.

Case Study	V_{cp}		V_{cn}		V_{co}		I_{L_B}		Δv_{cp}		Δv_{cn}		Δv_{co}		Δi_{L_B}	
	MAPE [%]	SD [%]	MAPE [%]	SD [%]	MAPE [%]	SD [%]	MAPE [%]	SD [%]	MAPE [%]	SD [%]	MAPE [%]	SD [%]	MAPE [%]	SD [%]	MAPE [%]	SD [%]
3 to 7	0.254	0.243	0.376	0.210	0.238	0.253	0.018	0.009	2.496	0.962	1.015	0.172	0.005	0.009	0.357	0.215

Finally, the results of the DC/DC converters 8 to 12 are summarized in Table 7. These case studies analyze the accuracy of the proposed expressions regarding the input voltage variable. The highest error is presented in the case study 8 (V_{in} = 6 V), and the lowest error in the case study 12 (V_{in} = 10 V). These five case studies have an error of less than 2.3% in the evaluated voltages and currents. The waveforms of the case study with the highest average error are illustrated in Figure 9. Additionally, the statistical results of the overall input voltage sweeps are shown in Table 8. The average voltages (V_{cp}, V_{cn}, and V_{co}) are characterized by a total MAPE of 0.365% with an SD of 0.147%, and the voltage ripples had a MAPE of 1.072% with an SD of 0.936%. According to the evaluated DC/DC converters, the accuracy of the proposed expression increase with the input voltage increment.

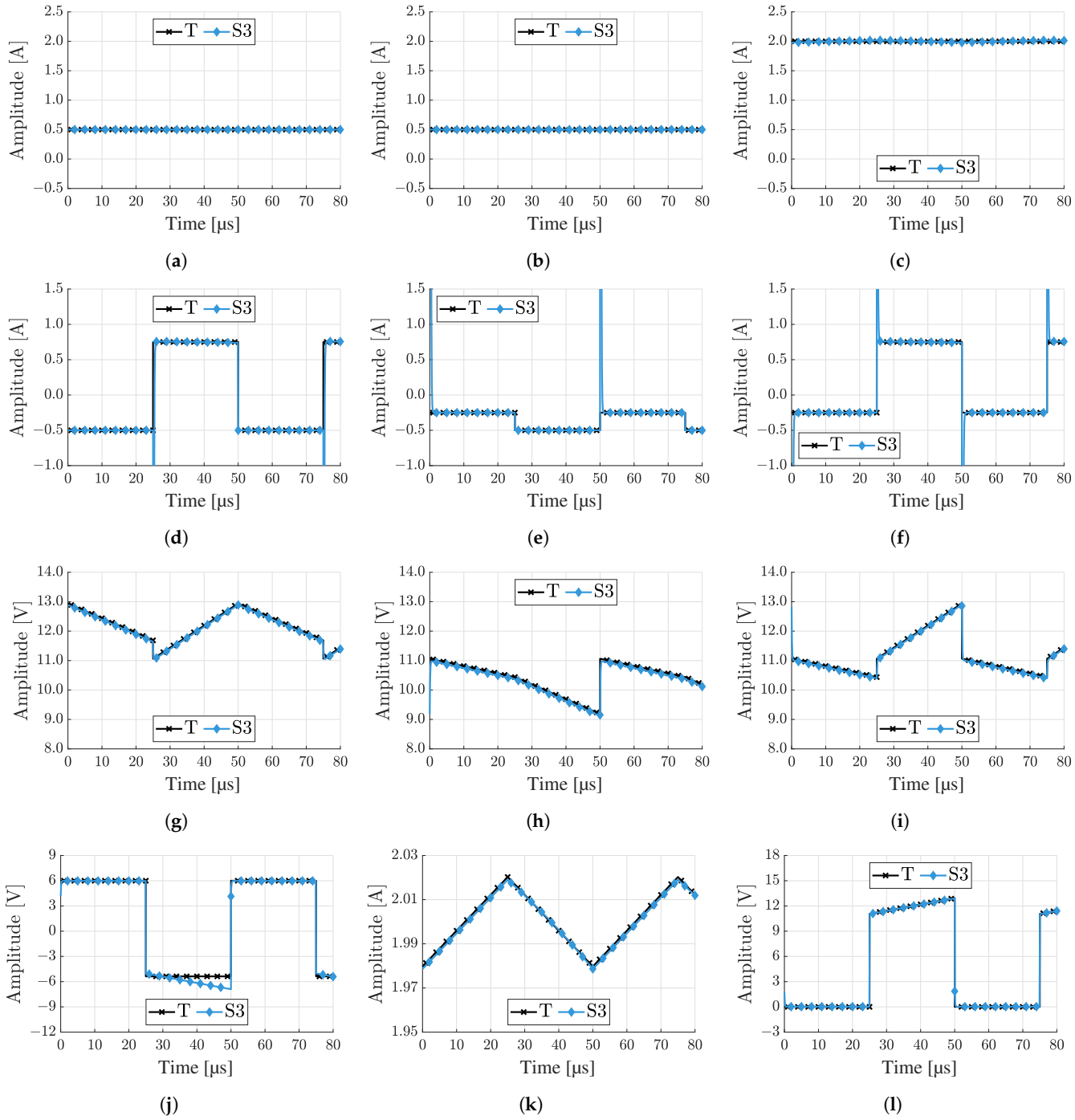

Figure 9. Waveforms validated in simulation for V_{in} 6 V. **(a)** $i_p(t)$. **(b)** $i_n(t)$. **(c)** $i_{L_B}(t)$ with small ripple approximation. **(d)** $i_{cp}(t)$. **(e)** $i_{cn}(t)$. **(f)** $i_{co}(t)$. **(g)** $v_{cp}(t)$. **(h)** $v_{cn}(t)$. **(i)** $v_{co}(t)$. **(j)** $v_{L_B}(t)$. **(k)** $i_{L_B}(t)$ without small ripple approximation. **(l)** $v_{S_1}(t)$. In this figure, the theoretical impulse currents were omitted intentionally to simplify the graphs. However, the simulated impulses are consistent with the theoretical ones.

Table 7. Theoretical and simulated values of the converter with Input voltage variation.

Case Study	V_{in} [V]	Simulator	V_{cp} [V]	V_{cn} [V]	V_{co} [V]	I_{L_B} [A]	Δv_{cp} [V]	Δv_{cn} [V]	Δv_{co} [V]	Δi_{L_B} [A]	Max. Error Parameter
8	6	T [a]	12.16	10.28	11.38	2.000	1.875	1.875	2.500	0.041	Δv_{cp}
		S3 [b]	12.11	10.21	11.34	1.999	1.834	1.856	2.500	0.040	
		Error [mA] o [mV]	45.98	73.03	39.74	0.679	41.19	18.74	0.132	0.190	
		Error [%]	0.378	0.710	0.349	0.034	2.197	1.000	0.005	0.469	
9	7	T	14.16	12.28	13.38	2.000	1.875	1.875	2.500	0.047	Δv_{cp}
		S3	14.11	12.21	13.34	1.999	1.834	1.856	2.500	0.047	
		Error [mA] o [mV]	43.89	71.45	37.72	0.555	41.21	18.82	0.026	0.203	
		Error [%]	0.310	0.582	0.282	0.028	2.198	1.004	0.001	0.430	
10	8	T	16.16	14.28	15.38	2.000	1.875	1.875	2.500	0.054	Δv_{cp}
		S3	16.11	14.21	15.34	1.999	1.834	1.856	2.500	0.054	
		Error [mA] o [mV]	44.26	72.20	38.10	0.554	41.28	18.79	0.026	0.204	
		Error [%]	0.274	0.506	0.248	0.028	2.202	1.002	0.001	0.377	
11	9	T	18.16	16.28	17.38	2.000	1.875	1.875	2.500	0.061	Δv_{cp}
		S3	18.11	16.21	17.34	1.999	1.834	1.856	2.500	0.061	
		Error [mA] o [mV]	44.64	72.95	38.48	0.554	41.36	18.76	0.025	0.204	
		Error [%]	0.246	0.448	0.221	0.028	2.206	1.000	0.001	0.335	
12	10	T	20.16	18.28	19.38	2.000	1.875	1.875	2.500	0.068	Δv_{cp}
		S3	20.11	18.21	19.34	1.999	1.834	1.856	2.500	0.067	
		Error [mA] o [mV]	45.01	73.70	38.86	0.553	41.43	18.72	0.024	0.204	
		Error [%]	0.223	0.403	0.201	0.028	2.210	0.999	0.001	0.301	

[a] Theoretical. [b] PSIM.

Table 8. Percentage error statistical results of the proposed converter with an input voltage variation.

Case Study	V_{cp}		V_{cn}		V_{co}		I_{L_B}		Δv_{cp}		Δv_{cn}		Δv_{co}		Δi_{L_B}	
	MAPE [%]	SD [%]	MAPE [%]	SD [%]	MAPE [%]	SD [%]	MAPE [%]	SD [%]	MAPE [%]	SD [%]	MAPE [%]	SD [%]	MAPE [%]	SD [%]	MAPE [%]	SD [%]
8 to 12	0.291	0.055	0.540	0.109	0.265	0.053	0.029	0.003	2.212	0.027	1.003	0.004	0.002	0.002	0.389	0.059

The percentages of statistical error grouped by cases are summarized in Table 9. The results indicate that the error is greater in the ripple variables than in the average variables, this difference is because the ripple values are magnitudes closer to zero. (e.g., Δv_{cp}), which generates a higher percentage of error with smaller variations. The results of the simulation (based on ideal models of the converter components) were consistent with the modeling approach. Furthermore, all the results of the 12 case studies, showing a low error between the theoretical calculations and the simulation results with a total MAPE of 0.774% with an SD of 1.566%.

As an initial evaluation of the accuracy of the proposed expressions in "real" operation, case study 10 was simulated using non-ideal components, the schematic of the resulting converter is shown in Figure 10. As summarized in this figure, the bidirectional converter switches were simulated in PSIM using the level 2 model of a commercial power MOSFET (i.e., IRF7380), wich parameter values were extracted from the device datasheet [29] and its Pspice model [30] provided by the manufacturer. Moreover, the commercial power

MOSFETS were driven by ideal pulsed voltage sources (i.e., v_1, v_2, v_3, and v_4 in Figure 10a) and a series resistor, which limits the current peak provided by the driver to less than 2 A. Furthermore, these switching control signals were implemented as ideal square waveforms with a dead-time (i.e., 274 ns), as shown in Figure 10c. Additionally, the energy storage components were simulated using wide-band circuit models, which were illustrated in Figures 10d,e. On one hand, the capacitor model used one ideal capacitor, one ideal inductor, and two ideal resistors, which values were fitted from experimental results by the capacitors' manufacturer and it is available in [31,32]. On the other hand, the inductor model used one ideal inductor, one ideal capacitor, and an ideal resistor. The resistor (i.e., DC resistance value) and inductor (i.e., the inductance value at low-frequencies, L_o) were extracted from the inductor datasheet [33,34]. However, the capacitor value (C_L) was estimated from the Self-Resonance Frequency (SRF), which is available in the inductor datasheet. Its value was calculated as

$$C_L = \frac{1}{(2\pi SRF)^2 L_o} \tag{32}$$

Table 9. Percentage error statistical results of the proposed converter with PSIM simulator.

Case Study	V_{cp} V_{cn} V_{co} I_{L_B}		Δv_{cp} Δv_{cn} Δv_{co} Δi_{L_B}		All Variables	
	MAPE [%]	SD [%]	MAPE [%]	SD [%]	MAPE [%]	SD [%]
1 to 2	0.425	0.447	2.929	4.529	1.677	3.367
3 to 7	0.221	0.230	0.968	1.081	0.595	0.859
8 to 12	0.281	0.195	0.902	0.859	0.591	0.690
All cases	0.280	0.267	1.267	1.267	0.774	1.566

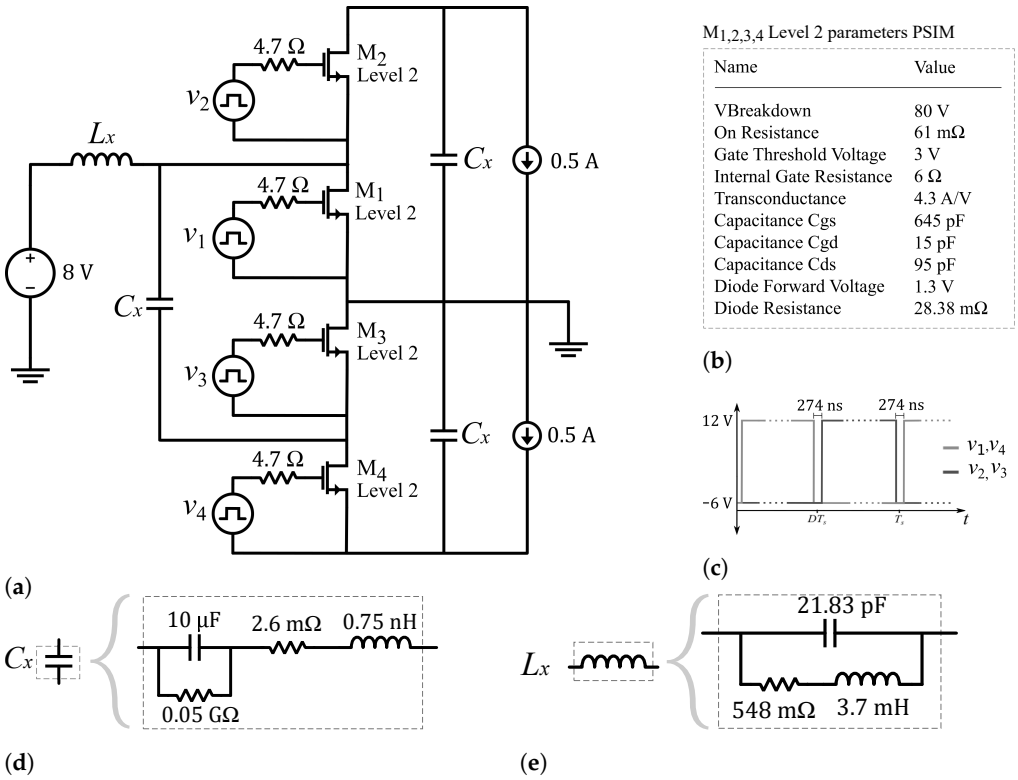

Figure 10. Simulation with real approximation of components. (**a**) Schematic; (**b**) Parameters mosfet IRF7380; (**c**) Gate control signal; (**d**) Capacitor approximation model; (**e**) Inductor approximation model.

To quantitatively evaluate the accuracy of the proposed expression in a non-ideal converter, three different simulations (of study case 10) were performed in PSIM with a simulation step of 2 ns. In the first simulation (SR1), the converter inductance and capacitors were simulated using its ideal circuit models. Contrary, the converter switches were simulated using a level 2 MOSFET model of PSIM with driving signals with dead time. In the second simulation (SR2), the converter switches were simulated using the ideal switch model and driving signals with dead time. Contrary, converter inductance and capacitors were simulated using its non-ideal models. Finally, in the third simulation (SR3) all the converter components were simulated with its non-ideal models. The resulting steady-state waveforms are shown in Figure 11. Moreover, Table 10 summarizes the main converter voltages and currents (average and ripple values).

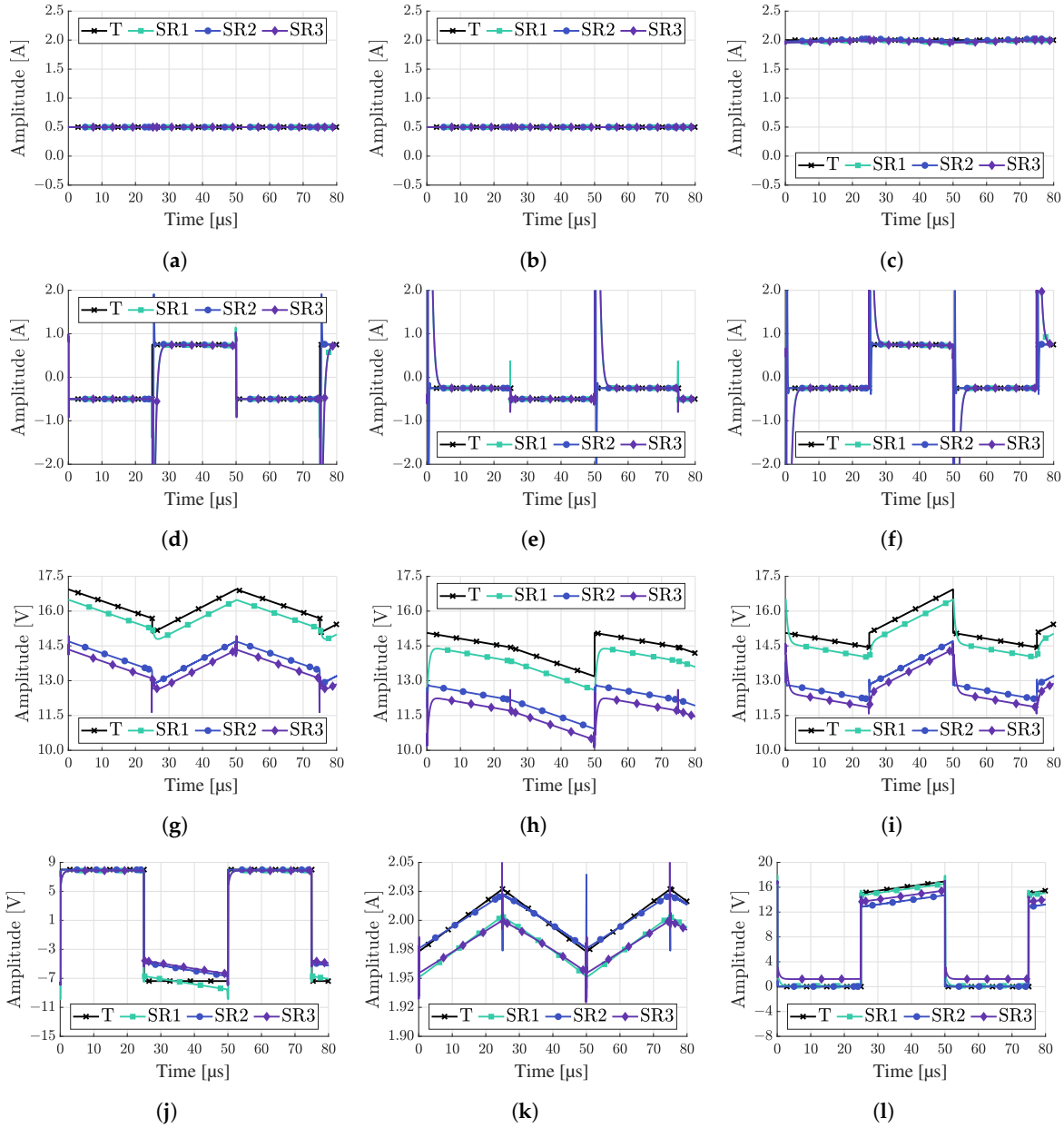

Figure 11. Waveforms validated in simulation with real approximation of components. (**a**) $i_p(t)$; (**b**) $i_n(t)$; (**c**) $i_{L_B}(t)$ with small ripple approximation. (**d**) $i_{cp}(t)$; (**e**) $i_{cn}(t)$; (**f**) $i_{co}(t)$; (**g**) $v_{cp}(t)$; (**h**) $v_{cn}(t)$; (**i**) $v_{co}(t)$; (**j**) $v_{L_B}(t)$; (**k**) $i_{L_B}(t)$ without small ripple approximation. (**l**) $v_{S_1}(t)$; In this figure, the theoretical impulse currents were omitted intentionally to simplify the graphs. However, the simulated impulses are consistent with the theoretical ones.

Table 10. Theoretical and simulated with real approximation of components.

Case Study	Simulation Type	V_{cp} [V]	V_{cn} [V]	V_{co} [V]	I_{L_B} [A]	Δv_{cp} [V]	Δv_{cn} [V]	Δv_{co} [V]	Δi_{L_B} [A]	Max. Error Parameter
	T [a]	16.16	14.28	15.38	2.000	1.875	1.875	2.500	0.054	
10	SR1 [b]	15.72	13.66	14.97	1.978	1.689	1.795	2.500	0.052	
	Error [mA] o [mV]	439.4	618.3	409.7	22.19	186.1	80.32	0.050	1.817	Δv_{cp}
	Error [%]	2.720	4.330	2.665	1.109	9.928	4.284	0.002	3.362	
	SR2 [c]	13.92	12.02	13.14	2.000	1.851	1.898	2.503	0.047	
	Error [mA] o [mV]	2237	2266	2230	0.497	24.48	23.27	2.563	7.416	V_{cn}
	Error [%]	13.85	15.87	14.51	0.025	1.305	1.241	0.103	13.72	
	SR3 [d]	13.57	11.52	12.82	1.978	1.680	1.780	2.490	0.044	
	Error [mA] o [mV]	2584	2763	2554	22.16	195.0	95.00	10.00	10.05	V_{cn}
	Error [%]	15.99	19.35	16.61	1.108	10.40	5.067	0.400	18.60	

[a] Theoretical. [b] PSIM with ideal L and C & real switches. [c] PSIM with real L and C & ideal switches. [d] PSIM with real L and C & real switches.

The simulation result of the converter in "real" operation shown good agreement between the proposed ideal modeling approach and the operation with non-ideal component models. The main differences between this model appear because of the equivalent series resistance of the inductor, which produces significant losses in the converter and limits its capacity to produce the ideal bipolar output (a well-known effect in SISO Boost converter [28]). Additionally, the simulated waveforms showed that the current pulses are within the typical ranges of switched converters. Therefore, the appropriate snubber networks must be analyzed in future research work. The resulting statistics were a MAPE of 7.36% with an SD of 6.91%. Therefore, the converter design using the proposed ideal model could be a good start point of a converter optimization process based on more complex component models and assisted by computer-aided design tools.

5. Conclusions

This paper presented a novel Single-Inductor and Bipolar-Output DC/DC Boost converter topology. The proposed topology allows controlling the output voltage balance under an unbalanced load without a specific control loop and it is not affected by the cross-regulation effect. The proposed converter was analyzed under CCM operation using the moving average operator and charge conservation principle. As a result, the authors proposed an equation set with the main averages and ripples of the circuit variables expressed as analytical functions of the circuit components, the input voltage, and the duty cycle. The functionality of the proposed converter was verified by extensive simulations in three commercial circuit simulators. Furthermore, the simulated and theoretical results were consistent. On the other hand, the accuracy of the proposed equation set was analyzed by parametric simulation of some converter variables using ideal models of the components. The swept variables were the capacitances and inductance values, the duty cycle, and the input voltage. As the main conclusion, the prediction error of the proposed equations is high. However, it increases and decreases with the increment and decrement of the ripple (and duty cycle) and the input voltage, respectively. Quantitatively, this accuracy was analyzed, the proposed equations were characterized by a mean absolute percentage error of 0.774% with a standard deviation of 1.566%. Furthermore, the non-ideal model simulation confirms the functionality of the proposed converter in "real" operation conditions. These simulations were characterized by a MAPE of 7.36% with an SD of 6.91%. Therefore, the converter design using the proposed ideal model could be a good start point of a converter optimization process based on more complex component models and assisted by computer-aided design tools.

This paper presents the results of one of the first milestones reached under the framework of the research projects entitled "Low cost and low complexity solar generator to support production processes in peace communities in Colombia". In future work, we will validate experimentally the proposed topology and explore the modeling of the converter in DCM operation. The future next step is to embed this topology in photovoltaic applications.

Author Contributions: Conceptualization, G.P., A.-K.H., and A.F.; methodology, G.P., A.-K.H., A.F., M.P., R.U., and I.C.; software, G.P., A.F., M.P., I.C., and R.U.; validation, G.P., A.-K.H., A.F., I.C., and R.U.; formal analysis, G.P., A.-K.H., A.F., and M.P.; resources, G.P., A.F., J.V., C.A.C.-F., and C.-I.P.-R.; writing—original draft preparation, all authors; writing—review and editing, all authors; visualization, G.P., A.F., I.C., and R.U.; supervision, G.P., A.-K.H., A.F., M.P., J.V., C.A.C.-F., and C.-I.P.-R.; funding acquisition, G.P., A.F., J.V., C.A.C.-F., and C.-I.P.-R. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by Pontificia Universidad Javeriana through the research project titled "Low cost and low complexity solar generator to support production processes in peace communities in Colombia" identified with ID 20292. The APC was funded by the Pontificia Universidad Javeriana.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: The data presented in this study are available on request from the corresponding author.

Acknowledgments: This research was funded by Pontificia Universidad Javeriana through the research project "Low cost and low complexity solar generator to support production processes in peace communities in Colombia" identified with ID 20292. The APC was funded by the Pontificia Universidad Javeriana too. Additionally, the authors would like to thank the Electronics Department and Electronics laboratory of the Pontificia Universidad Javeriana, for providing the resources required to conduct this study.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

SIBO	Single-Inductor Bipolar-Output
DC	Direct Current
SISO	Single-Inductor Single-Output
SIMO	Single-Inductor Multiple-Output
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
MAPE	Mean Absolute Percentage Error
SD	Standard Deviation

References

1. Chen, H.W.; Lee, J.H.; Lin, B.Y.; Chen, S.; Wu, S.T. Liquid crystal display and organic light-emitting diode display: Present status and future perspectives. *Light. Sci. Appl.* **2018**, *7*, 17168–17168.
2. Vaidya, V.; Soggs, S.; Kim, J.; Haldi, A.; Haddock, J.N.; Kippelen, B.; Wilson, D.M. Comparison of Pentacene and Amorphous Silicon AMOLED Display Driver Circuits. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2008**, *55*, 1177–1184, doi:10.1109/TCSI.2008.916548.
3. Dyson, M.J. *57-1: Trends in Low-Cost Displays for Emerging Applications*; SID Symposium Digest of Technical Papers; Wiley Online Library: Hoboken, NJ, USA, 2021; Volume 52, pp. 799–801.
4. Huang, Y.; Hsiang, E.L.; Deng, M.Y.; Wu, S.T. Mini-LED, Micro-LED and OLED displays: Present status and future perspectives. *Light. Sci. Appl.* **2020**, *9*, 1–16.
5. Virey, E.H.; Baron, N.; Bouhamri, Z. *30-4: MicroLED Display Technology Trends and Intellectual Property Landscape*; SID Symposium Digest of Technical Papers; Wiley Online Library: Hoboken, NJ, USA, 2020; Volume 51, pp. 436–439.
6. Lin, Z.R.; Chiu, H.J. Design and Implementation of Solar OLED Lighting Driver Circuit with Frequency Modulation Control. *Energies* **2020**, *13*, 5608.

7. Mao, F.; Lu, Y.; Bonizzoni, E.; Boera, F.; Huang, M.; Maloberti, F.; Martins, R.P. A Hybrid Single-Inductor Bipolar-Output DC-DC Converter With Floating Negative Output for AMOLED Displays. *IEEE J. Solid-State Circuits* **2021**, *56*, 2760–2769.
8. Kwak, B.C.; Hong, S.K.; Kwon, O.K. A Highly Power-Efficient Single-Inductor Bipolar-Output DC–DC Converter Using Hysteretic Skipping Control for OLED-on-Silicon Microdisplays. *IEEE Trans. Circuits Syst. II Express Briefs* **2018**, *65*, 2017–2021.
9. Shin, H.J.; Kim, T.W. Ultra-High-Image-Density, Large-Size Organic Light-Emitting Device Panels Based on Highly Reliable Gate Driver Circuits Integrated by Using InGaZnO Thin-Film Transistors. *IEEE J. Electron Devices Soc.* **2019**, *7*, 1109–1113, doi:10.1109/JEDS.2019.2947557.
10. Shin, H.J.; Kim, T.W. Decreased Motion Blur in Large-Size, Organic, Light-Emitting Device Panels Due to Integrated Gate Driver Circuits With a Moving-Picture Response-Time-Reduction Method. *IEEE J. Electron Devices Soc.* **2020**, *8*, 326–330, doi:10.1109/JEDS.2020.2981725.
11. Dongsheng, M.; Wing, H.K.; Mok, P.K.T.; Chi-Ying, T. Single-inductor multiple-output switching converters with bipolar outputs. In Proceedings of the ISCAS 2001 IEEE International Symposium on Circuits and Systems (Cat. No. 01CH37196), Sydney, NSW, Australia, 6–9 May 2001; Volume 3, pp. 301–304.
12. Kobayashi, H.; Nabeshima, T. *Handbook of Power Management Circuits*; Pan Stanford: Singapore, 2016.
13. Hong, S.W. 11.6 A 1.46 mm^2 Simultaneous Energy-Transferring Single-Inductor Bipolar-Output Converter with a Flying Capacitor for Highly Efficient AMOLED Display in 0.5 µm CMOS. In Proceedings of the 2020 IEEE International Solid-State Circuits Conference-(ISSCC), San Francisco, CA, USA, 16–20 February 2020; pp. 200–202, doi:10.1109/ISSCC19947.2020.9063141.
14. Chae, C.S.; Le, H.P.; Lee, K.C.; Cho, G.H.; Cho, G.H. A single-inductor step-up DC-DC switching converter with bipolar outputs for active matrix OLED mobile display panels. *IEEE J. Solid-State Circuits* **2009**, *44*, 509–524.
15. Lee, S.; Yoon, J.; Kim, J.; Lee, C.; Jung, H.; Lee, J.; Choi, J. High-capacity DC-DC converters for active matrix OLED display. In Proceedings of the 2010 IEEE Asia Pacific Conference on Circuits and Systems, Kuala Lumpur, Malaysia, 6–9 December 2010; pp. 480–483.
16. Moon, Y.; Roh, Y.; Gong, J.; Yoo, C. Load-Independent Current Control Technique of a Single-Inductor Multiple-Output Switching DC/DC converter. *IEEE Trans. Circuits Syst. II Express Briefs* **2012**, *59*, 50–54.
17. Le, H.; Chae, C.; Lee, K.; Wang, S.; Cho, G.; Cho, G. A Single-Inductor Switching DC/DC Converter With Five Outputs and Ordered Power-Distributive Control. *IEEE J. Solid-State Circuits* **2007**, *42*, 2706–2714.
18. Berkovich, Y.; Axelrod, B.; Shoshani, D.; Beck, Y. DC-DC converter based on the bipolar boost converter and Dickson voltage multiplier. In Proceedings of the 2018 IEEE International Energy Conference (ENERGYCON), Limassol, Cyprus, 3–7 June 2018; pp. 1–6.
19. Jeon, S.K.; Lee, H.J.; Choi, H.Y. Design of Highly Integrated 3-Channel DC-DC Converter Using PTWS for Wearable AMOLED. *J. IKEEE* **2019**, *23*, 1061–1067.
20. Ko, Y.H.; Jang, Y.S.; Han, S.K.; Lee, S.G. Non-load-balance-dependent high efficiency single-inductor multiple-output (SIMO) DC-DC converters. In Proceedings of the IEEE 2012 Custom Integrated Circuits Conference, San Jose, CA, USA, 9–12 September 2012; pp. 1–4.
21. Woo, Y.; Le, H.; Cho, G.; Cho, G.; Kim, S. Load-Independent Control of Switching DC-DC Converters With Freewheeling Current Feedback. *IEEE J. Solid-State Circuits* **2008**, *43*, 2798–2808.
22. Huang, M.; Chen, K. Single-Inductor Multi-Output (SIMO) DC-DC Converters With High Light-Load Efficiency and Minimized Cross-Regulation for Portable Devices. *IEEE J. Solid-State Circuits* **2009**, *44*, 1099–1111.
23. Dongsheng, M.; Wing-Hung, K.; Chi-Ying, T. A pseudo-CCM/DCM SIMO switching converter with freewheel switching. In Proceedings of the 2002 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (Cat. No. 02CH37315), San Francisco, CA, USA, 3–7 February 2002; Volume 1, pp. 390–476.
24. Boera, F.; Salimath, A.; Bonizzoni, E.; Maloberti, F. Design of a SIBO DC-DC Converter for AMOLED Display Driving. In Proceedings of the 2018 14th Conference on Ph. D. Research in Microelectronics and Electronics (PRIME), Prague, Czech Republic, 2–5 July 2018; pp. 109–112.
25. Goh, T.Y.; Ng, W.T. Single Discharge Control for Single-Inductor Multiple-Output DC–DC Buck Converters. *IEEE Trans. Power Electron.* **2018**, *33*, 2307–2316, doi:10.1109/TPEL.2017.2700483.
26. Kwon, D.; Rincon-Mora, G.A. Single-Inductor–Multiple-Output Switching DC–DC Converters. *IEEE Trans. Circuits Syst. II Express Briefs* **2009**, *56*, 614–618, doi:10.1109/TCSII.2009.2025629.
27. Zhou, S.; Zhou, G.; Wang, Y.; Liu, X.; Xu, S. Bifurcation analysis and operation region estimation of current-mode-controlled SIDO boost converter. *IET Power Electron.* **2017**, *10*, 846–853, doi:10.1049/iet-pel.2016.0539.
28. Erickson, R.W.; Maksimovic, D. *Fundamentals of Power Electronics*; Springer: Berlin/Heidelberg, Germany, 2007.
29. IRF7380PbF HEXFET Power MOSFET. 2004. Available online: https://www.infineon.com/dgdl/Infineon-IRF7380-DataSheet-v01_01-EN.pdf?fileId=5546d462533600a4015355f9da901b89 (accessed on 20 September 2021).
30. Spice Model–IRF7380. Simulation Models. 2002. Available online: https://www.infineon.com/cms/en/product/power/mosfet/n-channel/irf7380/?redirId=148013#!simulation (accessed on 20 September 2021).
31. Ceramic, M.; Capacitors, C. TDK Equivalent Circuit Model Library TDK Equivalent Circuit Model Library Multilayer Ceramic Chip Capacitors; 2020. Available online: https://product.tdk.com/system/files/dam/technicalsupport/tvcl/pdf/mlcc_commercial_general_c3216_ecm.pdf (accessed on 20 September 2021).
32. Tohgoh, T.; Tsuda, N. Multilayer ceramic chip capacitors. *Natl. Tech. Rep.* **1989**, *35*, 22–29.

33. Max, A. Vishay Dale Filter Inductors, High Current , Axial Leaded. 2014. pp. 1–5. Available online: https://www.vishay.com/docs/34015/ihb.pdf (accessed on 20 September 2021).
34. Dmt, T. Output Power Chokes—Toroid Styles Output Power Chokes—Toroid Styles. 2010. pp. 3–4. Available online: https://www.coilcraft.com/getmedia/41fe41f7-5d27-436f-943d-7ed00be2b2aa/dmt.pdf (accessed on 20 September 2021).