



# Article DC-Link Capacitor Voltage Balancing Control of a Five-Level Regenerative AC Electronic Load Using One-Cycle Control<sup>+</sup>

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Abstract: High voltage electric power equipment requires rigorous regulation testing to specific standards which ensure proper and safe operation in the grid. Manufacturers conduct these tests in order to prove standard compliance and product liability. Variable linear or nonlinear loads are necessary for testing medium voltage (MV) high power AC power converters. Generally, those AC power converters or power supplies require performance validation, burn-in and/or lifetime testing under different load conditions, defined by the end-user or standards for the given applications. For flexible and efficient MV verification testing, this paper presents a five-level multilevel converter-based MV regenerative AC electronic load with one-cycle control (OCC), which is based on five-level diode-clamped multilevel converters with back-to-back structure and can emulate any impedance load. In this paper, especially the dc-link capacitor voltage balance of the proposed multilevel MV regenerative AC load is deeply analyzed. Simulation and experimental results are presented to verify the dc-link voltage balance performance of the proposed multilevel MV regenerative AC electronic load.

**Keywords:** alternating current electronic load; one-cycle control; back-to-back five-level multilevel converter; dc-link voltage balance

# 1. Introduction

For utility companies the reliability of their power transmission and distribution equipment installed in the power grid is vital. The manufacturers of the high voltage power equipment can prove that their products have been tested according to international standards—IEC 62271, 61869, 60044 and 60076 standards, meet end-user specifications and relevant safety regulations. For this purpose, various loads are required to validate the performance, to carry on burn-in and to conduct lifetime testing of power conversion equipment, including uninterruptible power supplies, AC motors, turbine generators, inverters and power system equipment. Traditionally, high power load banks provide a practical solution for the manufacturers of the high-power equipment, but they are typically large, bulky and energy-consuming. Many load banks use a combination of resistors, inductors, capacitors and/or diode rectifiers to emulate various load conditions. When a different load parameter is required, reconnection of the load bank is necessary, which can be labor-intensive and time-consuming. This situation has led to the commercialization of some electronic loads that feature manual dial-in or automatic load adjustment, suitable for convenient and fast product testing. However, these electronic loads are limited in terms of both voltage and power rating. At present, these types of electronic loads are only available at low voltage, 400 V and low power level, 20 kVA per phase [1].

For MV verification, the testing equipment is generally not regenerative and still burns 100% testing energy. Energy consumption for power equipment testing is a serious problem, especially for high power MV applications. To recycle the testing energy, high voltage multilevel power electronic converters with back-to-back structure play an essential



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**Copyright:** © 2021 by the author. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). role in high voltage and medium voltage (MV) power applications. For high power MV applications, three-level or five-level diode-clamped multilevel converters (DCMCs) have been widely adopted in high power back-to-back systems. To obtain sinusoidal waveforms and reduce harmonic components, five-level DCMC-based back-to-back configuration has been receiving more attention recently [2]. However, the primary obstacle of the five-level DCMC-based back-to-back structure is control complexity to control 48 switching devices for the three-phase and achieve charge balance of four dc-link capacitors, for example, by using a modified space vector pulse width modulation (SVPWM) and a capacitor current prediction algorithm with or without an auxiliary hardware circuit that increases the complexity and the cost of the power conversion multilevel converters. There are commonly two types of the PWM methods to balance the dc-link capacitor voltages of the five-level DCMCs with or without back-to-back structure: (1) modified carrier-based SPWM [2–5] and (2) modified SVPWM [6–10]. Generally, the carrier-based SPWM technique is much simpler than the SVPWM method. As far as the implementation of the

SVPWM technique is concerned, it is computationally very difficult to realize. In [2], a MV adjustable-speed motor drive system based on two five-level DCMCs with back-to-back structure was proposed with 3 kHz four level-shifted carrier signals and four buck-boost choppers for achieving voltage balancing between four dc-link capacitors. The additional buck-boost choppers increase the complexity, the size and the cost of the proposed MV motor drive system. An auxiliary capacitor-based dc-link balancing approach was presented in [3] to equalize the dc-link capacitor voltages of the five-level DCMC by utilizing the auxiliary capacitor as an equalizer between the capacitors of different voltages. The proposed balancing hardware circuit-based method can be applied to both the carrierbased SPWM and the SVPWM but requires additional circuits and control, which would increase hardware complexity and system failure. A new carrier-based SPWM method with voltage balancing capability was proposed for the five-level DCMCs with back-toback structure in [4]. For the back-to-back configuration, the unbalance tendencies of both sides (a rectifier and an inverter) have a potential to compensate each other because of the symmetry. By controlling proper offset voltages on both rectifier and inverter sides, the average current flowing into the inner junction can be adjusted to be equal to that flowing out from it. Then, the voltage balancing of the inner junction can be achieved. In addition, the switch angles cannot be directly controlled in the proposed SPWM control. Instead, the offset voltage of each inner junction should be calculated and added to the phase voltage reference, which is not the sinusoidal reference. Therefore, the proposed carrier-based SPWM method requires complicated calculation of all the switching angles and is only applicable when both modulation indexes of the rectifier and the inverter are less than 0.5. In [5], a closed-loop dc-link voltage balancing algorithm was introduced with regular level-shifted carriers for a four-level DCMC. The proposed approach is based on redundant level modulation, which utilizes one additional voltage level in one switching cycle to obtain extra controllability of the dc-link capacitor voltages without distorting the fundamental frequency output voltage. However, the proposed dc-link voltage balancing method requires complicated control reference waveforms with the help of a digital signal processor (DSP) and makes additional switching transitions in one switching cycle, which increase the switching loss of the four-level DCMC.

A SVPWM-based switching strategy was proposed in [6] for a five-level DCMC by using redundant switching vectors based on the minimum energy property of the balanced five-level DCMC. However, the proposed SVPWM method has limited operation under distorted ac current condition and only evaluated by MATLAB simulation without experimental verification. In [7], a modified inner-hexagon-vector-decomposition-based space vector modulation method was introduced for a five-level DCMC in order to obtain the capacitor voltage balancing with high modulation index and high-power factor by introducing six new vector sequences to each triangle and applying a new vector selection rule. However, the proposed SVPWM method has two drawbacks in practice. First, the power factor is very small when the proposed five-level DCMC works as an active power filter, which brings little challenge to the voltage balancing control. Second, since an error exists between the reference vector and the actual synthesized vector, the magnitude and phase errors increase with the increasing dwelling time of transitional vectors. A new hybrid voltage balance method was proposed for five-level DCMCs in [8], where additional flyingcapacitor-based auxiliary circuits were used to balance the upper or lower two capacitors, along with a zero-sequence injection method to balance the midpoint voltage. Based on the proposed hybrid approach, the voltage stresses of power devices can be equalized, and the current ripples of the inductors can also be suppressed. However, the proposed hybrid voltage balance method requires the auxiliary circuits to balance the upper or lower two capacitors, which need two flying capacitors and inductors, and eight insulated gate bipolar transistors (IGBTs) with freewheeling diodes for each phase. The SVPWM-based switching strategy in [6] was extended to a HVDC converter system in [9] with back-to-back five-level DCMCs by using redundant switching vectors based on online minimization of the energy cost function, associated with the voltage deviations of the dc-link capacitors. The proposed SVPWM method was mostly evaluated by PSCAD/EMTDC time domain simulation with limited experimental verification, which was not enough to prove the proposed SVPWM and the energy cost function approach. In [10], a SVPWM-based dc-link voltage strategy was proposed for five-level multipoint DCMCs with back-to-back configuration by using redundant switching vectors and reactive power exchange between the grid-side LCL filter and the front end five-level DCMC. Therefore, the proposed dc-link voltage balance is only guaranteed while the grid-side LCL filter is fully dimensioned to provide the 100% required reactive power of the front end five-level DCMC instead of 2-5% of the required reactive power. This is one of the disadvantages of the proposed SVPWM method with reactive power exchange.

Regenerative AC loads (Regen-Load) have been recently proposed to recycle the testing energy of the high voltage power equipment. Regen-Loads shall be capable of emulating various load conditions within the test ranges and recycling the testing energy back to the power grid. Relevant research on low voltage AC electronic loads was found based on standard H-bridge converters with state feedback control or state-space average model control using DSPs [11–13], which require real time complicated calculation and some complex circuitry to implement the main controllers. Since the maximum blocking voltage of modern power semiconductor switches is about 6.5 kV, the H-bridge-based Regen-Loads are not ready to handle high power MV equipment testing. In this case, multilevel converter-based Regen-Loads will be necessary to overcome the voltage and current limits of the power semiconductor switches.

One-cycle control (OCC) technique has established a large-signal nonlinear PWM control method that features a simple circuit, high performance and universal applications. OCC has been successfully implemented in many sectors of power electronics including dc/dc converters, dc/ac inverters, power factor correction (PFC) rectifiers and active power filters (APFs) in both single-phase and three-phase configuration [14–17]. In [14], a single-phase APF with OCC control was presented based on a full-bridge power converter under unipolar operation. The proposed OCC control method in [14] can be only applicable for single-phase full-bridge type converters with the unity power factor. A three-phase PFC rectifier with OCC control was proposed based on a full-bridge power converter under vector operation. The proposed OCC method in [15] was also applicable for only three-phase full-bridge type converters with the unity power factor. In [16], a universal OCC vector controller was described for four-quadrant three-phase full-bridge type power converters, including PFC rectifiers and APFs. Finally, a first carrier level-shifted OCC PWM control method was proposed in [17] for five-level DCMCs, but the dc-link capacitor voltage balancing theory was not presented in details.

This paper presents a five-level DCMC-based MV regenerative AC electronic load (MV Regen-Load) with four-carrier level-shifted OCC control based on back-to-back configuration targeted towards high power MV applications, with the capability of emulating various impedance loads. A small-scale prototype of 1 kVA 120 Vac five-level OCC MV Regen-Load was designed and tested to verify the performance of the proposed five-level OCC MV Regen-Load. The regenerative feature of the proposed MV Regen-Load provides an effective energy saving solution for MV power equipment testing since the testing energy is fed back to the grid instead of being dissipated as heat during operation. In this paper, especially the dc-link voltage balancing control of the proposed five-level MV Regen-Load by using the simple level-shifted OCC is deeply analyzed. Compared to the conventional level-shifted SPWM control, the proposed level-shifted OCC of the five-level DCMC-based MV Regen-Load has the variable amplitudes of four carrier signals instead of the fixed amplitudes. With variable amplitude control of the four carrier signals, the dc-link capacitor voltages automatically become balanced and equal to the reference voltage ( $V_{DC}/4$ ). The most important merit of the proposed multilevel OCC method is to reduce a heavy computing burden. Simulation and experiments were performed using small-scale five-level DCMCs to verify the proposed multilevel MV Regen-Load performance.

#### 2. Multilevel OCC MV Regenerative Load Configuration

Figure 1 shows the diagram of the proposed single-phase multilevel MV Regen-Load. It is composed of a multilevel input rectifier, a multilevel output inverter, an OCC controller, a current reference generator and a graphical user interface (GUI). The equipment under test (EUT) is connected to the multilevel input rectifier, which is connected to the multilevel output inverter in a back-to-back configuration to realize energy regeneration to the power grid. The current reference generator produces the current reference signal for the proposed OCC controller to emulate the user-defined linear or nonlinear load. The GUI helps the user set up any load condition and provides the user-defined modeling option for complicated or dynamic loads.



Figure 1. Multilevel OCC MV Regen-Load implementation.

The power stage topology of the single-phase five-level MV Regen-Load is shown in Figure 2. The five-level input rectifier emulates the specified impedance while the fivelevel output inverter sends the absorbed energy back to the utility grid with unit power factor. The multilevel OCC MV Regen-Load is capable of emulating a specified load for the EUT by controlling the amplitude and phase of the input current of the multilevel MV Regen-Load. In addition, the proposed multilevel MV Regen-Load can be used in dynamic load emulation with fast and accurate response, due to the inherent characteristics of the OCC. Theoretically, when all components are ideal, the OCC MV Regen-load has no loss. Practically, certain percentage of energy is lost as conduction loss and switching



loss. Typically, the loss will be round 5%, which is a significant improvement over the conventional 100% loss.

Figure 2. Single-phase five-level OCC MV Regen-Load power stage configuration.

#### 3. OCC Control of Five-Level Regen-Load

As shown in Figure 2, the five-level DCMC is comprised of eight active switches  $(S_{A1}-S_{A'4})$ , 12 clamping diodes, four dc-link capacitors and an input inductor  $(L_S)$ . Voltage sharing between the main switches is achieved by the clamping diodes. It has been a major challenge to balance the dc-link capacitor voltages in a multilevel converter, especially as the number of levels increases. Traditionally two types of balancing methods were reported: using the redundant switching states and using the auxiliary balancing circuits.

With the SVPWM control, a number of redundant switching states can be used to help balance the dc-link capacitor voltages. This approach may minimize or eliminate the need for auxiliary balancing circuits. However, for five or higher-level multilevel converters, the SVPWM control is computation intensive and not commonly used in industrial applications. For example, a five-level multilevel converter has  $5^3 = 125$  switching states, for which the computation burden may require high-speed DSPs, limit the maximum switching frequency or slow down control response. In addition, the use of redundant switching states increases the switching frequency and the switching loss which is undesired for practical applications.

On the other hand, the traditional carrier-based SPWM control of the DCMCs produces unbalanced dc-link capacitor voltages. Thus, a balancing circuit is generally required, which significantly increases the complexity of the multilevel converter circuits or systems.

The proposed level-shifted OCC method provides a simple approach to balance the dclink capacitor voltages for multilevel converters without involving any auxiliary balancing circuit. For the five-level DCMC, four-carrier level-shifted SPWM with variable carrieramplitude control is employed as shown in Figure 3a. In general, the four carriers can be arranged in different forms: phase disposition (PD), phase opposition disposition (POD) and alternative phase opposition disposition (APOD). Among the above carrier forms, the PD technique, where all carriers are in phase, provides the lowest harmonic distortion.



**Figure 3.** Single-phase five-level OCC MV Regen-Load PWM waveforms. (**a**) Control reference  $(R_S \cdot I_S + V_{Iref})$  and four carrier signals; (**b**) Gate signals of four upper switches  $(S_{A1}-S_{A4})$ .

Based on the level-shifted PD SPWM control, the four carrier signals (Vcr1-Vcr4) of the proposed five-level OCC MV Regen-Load have the same phase but different amplitudes, depending on each dc-link capacitor voltage ( $V_{DC1}, \ldots, V_{DC4}$ ).

Figure 3 shows the single-phase OCC MV Regen-Load PWM waveforms of the fivelevel DCMC input rectifier. In Figure 3a, a sinusoidal reference ( $R_S \cdot I_S + V_{Iref}$ ) is compared with the four carrier signals (Vcr1-Vcr4) to determine the switched voltage levels:  $+V_{DC}/2$ ( $+V_{DC1} + V_{DC2}$ ),  $+V_{DC}/4$  ( $+V_{DC2}$ ), 0,  $-V_{DC}/4$  ( $-V_{DC3}$ ) and  $-V_{DC}/2$  ( $-V_{DC3} - V_{DC4}$ ). The line period is divided into four operation regions, according to where the reference signal lands, named as I, II, III and IV. The five-level DCMC input rectifier assumes different equivalent circuits and switching states in a different operation region.

Table 1 shows the five-level DCMC input rectifier voltages (*Vrec* or *Vrec–N*) and their switching states. The eight active switches are controlled as complementary pairs  $(S_{A1}, S_{A'1}, \text{etc.})$ . In region I in Figure 3a, the input rectifier voltage is switched between  $V_{DC1} + V_{DC2}$  and  $V_{DC2}$  by the first upper switch  $S_{A1}$  and its complementary switch  $S_{A'1}$ . As shown in Figure 3b, the other upper switches ( $S_{A2}-S_{A4}$ ) are kept on in region I. Similarly, in region II, the second upper switch  $S_{A2}$  and its complementary switch  $S_{A'2}$  are switched to provide the input rectifier voltage between  $V_{DC2}$  and 0. In this region, the first upper switch  $S_{A1}$  is turned off, and the other two upper switches ( $S_{A3}, S_{A4}$ ) are always turned on to provide the neutral point connection (0 or N) in Figure 2. For region III and IV, the same switching approach is applied to produce the negative input rectifier voltages.

 Table 1. Switching states and five-level DCMC input rectifier voltages.

	<i>S</i> <sub><i>A</i>1</sub>	S <sub>A2</sub>	S <sub>A3</sub>	<i>SA</i> 4	<i>S</i> <sub><i>A</i>′1</sub>	<i>S</i> <sub><i>A</i>′2</sub>	<i>S</i> <sub><i>A</i>′3</sub>	S <sub>A'4</sub> –	Vrec	
									PWM-ON	PWM-OFF
Ι	PWM	ON	ON	ON	<b>PWM</b>	OFF	OFF	OFF	$+V_{DC1} + V_{DC2}$	$+V_{DC2}$
II	OFF	PWM	ON	ON	ON	$\overline{\text{PWM}}$	OFF	OFF	$+V_{DC2}$	0
III	OFF	OFF	PWM	ON	ON	ON	<b>PWM</b>	OFF	0	$-V_{DC3}$
IV	OFF	OFF	OFF	PWM	ON	ON	ON	PWM	$-V_{DC3}$	$-V_{DC3} - V_{DC4}$

Assuming that the proposed OCC MV Regen-Load operates in continuous conduction mode, the equivalent circuits and the OCC control equations can be found for four operation regions. Figure 4 shows the simplified equivalent circuit of the five-level OCC MV Regen-Load in region I. By applying the volt-second balance rule to the input inductor ( $L_S$ ), the conversion gain equation for the equivalent circuit in Figure 4 can be derived by (1):

$$V_{S} = V_{DC2} + V_{DC1} \cdot d_{SA1} \approx \frac{V_{DC}}{4} (1 + d_{SA1})$$
(1)

where  $d_{SA1}$  is the duty ratio of the first upper switch  $S_{A1}$ .



Figure 4. Simplified equivalent circuit of the OCC MV Regen-Load in region I.

Then, the control goal of the OCC MV Regen-Load is for the input current ( $i_S$ ) to track the current reference signal ( $V_{Iref}$ ). According to this condition, the control goal can be defined by the Norton equivalent circuit as follows:

$$V_S = R_E \cdot \left( i_S + I_{Sref} \right) \tag{2}$$

where  $R_E$  is the emulated resistance of the input rectifier and  $I_{Sref}$  is the input current reference.

By combining the conversion gain Equation (1) and the control goal (2), the control key equation for the OCC MV Regen-Load in region I can be derived by the Thévenin equivalent circuit as follows:

$$R_{S} \cdot i_{S} + V_{Iref} = V_{m2} + V_{m1} \cdot d_{SA1} \tag{3}$$

where  $R_S$  is the sensing resistance of the input current,  $V_{Iref}$  is the current reference signal,  $V_{m1}-V_{m2}$  are the carrier amplitudes,  $V_{Iref} = R_S \cdot I_{Sref}$ ,  $V_{m1} = \frac{V_{DC1} \cdot R_S}{R_E}$  and  $V_{m2} = \frac{V_{DC2} \cdot R_S}{R_E}$ . With a similar procedure, the control key equations for the other operation regions

can be derived in Table 2.

To implement all the control key equations, an OCC level-shifted PWM control circuit is proposed shown in Figure 5, using a clock signal (CLK), four integrators, four comparators, four RS flip-flops and four reset switches for PWM generation. The OCC level-shifted PWM control circuit of the five-level OCC MV Regen-Load consists of four voltage compensators and OCC level-shifted PWM generators for the eight gate signals ( $S_{A1}-S_{A'4}$ ). The four identical voltage compensators determine the carrier amplitudes ( $V_{m1}-V_{m4}$ ), depending on deviation of each dc-link capacitor voltage ( $V_{DC1}-V_{DC4}$ ) from the reference voltage  $V_{DC}^*$  (=  $V_{DC}/4$ ). Using four integrators and three adders, the level-shifted carrier signals (*Vcr*1–*Vcr*4) are generated with the different amplitudes and dc-level shifts. By comparing the control reference ( $R_S \cdot I_S + V_{Iref}$ ) with the four carrier signals (*Vcr*1–*Vcr*4), the actual gate signals are produced by the RS flip-flops. When both the input signals of each comparator approach one another, the comparator changes its state, which in turn resets the RS flip-flop through its '*R*' input terminal and its integrator to zero. The next clock signal (CLK) sets the RS flip-flop through its '*S*' input terminal and the output terminal '*Q*' of the RS flip-flop is also set, which turns on its gate signal ( $S_{A1}$ – $S_{A4}$ ). With variable amplitude control of the four carrier signals, the dc-link capacitor voltages can become balanced and equal to the reference voltage ( $V_{DC}/4$ ) even under different dc-link capacitances ( $C_1$ – $C_4$ ).

	Switching State I	Switching State II	Switching State III	Switching State IV
Control Key Equations	$R_{S} \cdot I_{S} + V_{Iref}$ $= V_{m2} + V_{m1} \cdot d_{SA1}$	$R_{S} \cdot I_{S} + V_{Iref}$ $= V_{m2} \cdot d_{SA2}$	$R_{S} \cdot I_{S} + V_{Iref}$ $= -V_{m3} + V_{m3} \cdot d_{SA3}$	$R_S \cdot I_S + V_{Iref}$ = $-(V_{m3} + V_{m4}) + V_{m4} \cdot d_{SA4}$
Region Selections	$V_{m2} \leq R_S \cdot I_S + V_{Iref} \\ \leq (V_{m1} + V_{m2})$	$0 \le R_S \cdot I_S + V_{Iref} \\ < V_{m2}$	$-V_{m3} \le R_S \cdot i_S + V_{Iref} < 0$	$-(V_{m3} + V_{m4}) \le R_S \cdot I_S + V_{Iref} < -V_{m3}$
	Region I	Region II	Region III	Region IV

Table 2. Control key equations for four operation regions.



Figure 5. OCC level-shifted PWM control circuit of the five-level OCC MV Regen-Load.

The input current of the five-level DCMC input rectifier of the OCC MV Regen-Load accurately tracks the current reference signal and to realize the specified impedance load. For the proposed OCC MV Regen-Load, the control of the input rectifier is the key point. For the five-level DCMC output inverter of the OCC MV Regen-Load, the control goal is to make the output current  $I_O$  of the OCC MV Regen-Load synchronous with the grid voltage  $V_O$  and contribute to the unit power factor injection of the recycled testing energy with the highest efficiency. In this condition, the control requirement is to realize unit power factor operation and stabilize the dc-link voltage. A multilevel converter similar to the input rectifier can be used to implement the inverter. Due to the similarity of the topology

and for the purpose of simplicity but without loss of the generality, the discussion of the multilevel inverter is kept brief.

# 4. DC-Link Capacitor Voltage Balance Analysis

For the DCMCs, a major challenge is to keep all dc-link capacitor voltages balanced, which was usually achieved with an extra voltage-balancing circuitry or a specific voltage-balancing control previously.

In this section, the dc-link capacitor voltage balance issue for the five-level OCC MV Regen-Load is analyzed based on the proposed level-shifted OCC control. Figure 6 shows the dc-link currents of the five-level OCC MV Regen-Load in region I and II when the control reference ( $R_S \cdot I_S + V_{Iref}$ ) is positive during the half-cycle of the input line frequency. In region I and II, the two upper switches ( $S_{A1}$ ,  $S_{A2}$ ) are modulated, respectively, and the two upper dc-link capacitors ( $C_1$ ,  $C_2$ ) are also charged or discharged, respectively, depending on the load emulation and each dc-link capacitor voltage. When the control reference is negative in region III and IV, the other upper two switches ( $S_{A3}$ ,  $S_{A4}$ ) are switched, respectively, with the two lower dc-link capacitors ( $C_3$ ,  $C_4$ ), and the related PWM control and the dc-link voltage-balancing method in region III and IV are the same as those in region I and II. For proper operation of the five-level OCC MV Regen-Load, the amplitudes and dc-level shifts of the four carrier signals (Vcr1-Vcr4) must be properly controlled to achieve dc-link voltage balancing.



Figure 6. DC-link currents of the five-level OCC MV Regen-Load in region I and II.

Figure 7 shows the simplified equivalent circuit models of the five-level OCC MV Regen-Load in region I and II, respectively. From Figure 7a, the two dc-link capacitor currents ( $i_{C1}$ ,  $i_{C2}$ ) in region I can be described by the following expressions:

$$i_{C1} = C_1 \frac{dV_{DC1}}{dt} = i_{REC1} - i_{INV1} = d_{SA1}(i_S + I_{Sref}) - i_{INV1}$$
$$i_{C2} = C_2 \frac{dV_{DC2}}{dt} = i_{C1} + i_{REC2} - i_{INV2} = (i_S + I_{Sref}) - (i_{INV1} + i_{INV2})$$
(4)



Figure 7. Simplified equivalent circuits of the five-level OCC MV Regen-Load. (a) In region I; (b) In region II.

Similarly, the two dc-link capacitor currents in region II, which are shown in Figure 7b can be expressed as: 117

$$i_{C1} = C_1 \frac{dV_{DC1}}{dt} = -i_{INV1}$$
$$i_{C2} = C_2 \frac{dV_{DC2}}{dt} = i_{C1} + i_{REC2} - i_{INV2} = d_{SA2}(i_S + I_{Sref}) - (i_{INV1} + i_{INV2})$$
(5)

Assuming that the four dc-link capacitors  $(C_1-C_4)$  have the same capacitance, when a disturbance causes imbalance in the two upper dc-link capacitor voltages (e.g.,  $V_{DC1} > V_{DC2}^* > V_{DC2}$ ), a state variable  $\Delta V$  is defined as half the difference between the two upper dc-link capacitor voltages ( $V_{DC1}$ ,  $V_{DC2}$ ), which should converge to zero with the proposed level-shifted OCC control. In the unbalanced condition, each dc-link capacitor voltage can be defined as a function of the voltage difference  $\Delta V$  by:

$$V_{DC1} = V_C + \Delta V$$

$$V_{DC2} = V_C - \Delta V$$

$$V_C = \frac{V_{DC1} + V_{DC2}}{2}$$
(6)

where

$$V_C = \frac{V_{DC1} + V_C}{2}$$

$$\Delta V = \frac{V_{DC1} - V_{DC2}}{2} \tag{7}$$

In order to maintain the dc-link capacitor voltage balance, the proposed control of the five-level OCC MV Regen-Load in region I and II is shown in Figure 8. From Figure 8a, the duty ratios of the  $S_{A1}$  switch under an unbalanced dc-link condition can be described as follows:

$$d_{SA1(n)} = \frac{T_{dSA1(n)}}{T_S} = \frac{R_S \cdot i_S + V_{Iref} - V_{m2}}{V_{m1}}$$
$$d_{SA1(n+1)} = \frac{T_{dSA1(n+1)}}{T_S} = \frac{R_S \cdot i_S + V_{Iref} - (V_{m2} - \Delta V_{m2})}{V_{m1} + \Delta V_{m1}}$$
(8)

where  $d_{SA1(n)}$  and  $d_{SA1(n+1)}$  are the duty ratios of the  $S_{A1}$  switch at the (*n*)th and (*n* + 1)th switching cycles, and:

$$V_{m1} = \frac{V_{DC1} \cdot R_S}{R_E}$$
$$\Delta V_{m1} = \frac{R_S}{R_E} \cdot \Delta V_{DC1} = \frac{R_S}{R_E} \cdot \Delta V \tag{9}$$

From (8) and (9), the duty ratio variation of the  $S_{A1}$  switch ( $\Delta d_{SA1}$ ) to compensate the unbalanced dc-link capacitor voltages can be obtained by:

$$\Delta d_{SA1} = d_{SA1(n+1)} - d_{SA1(n)} = \frac{-\Delta V_{DC1(n)}[R_E(i_S + I_{Sref}) + V_{DC2(n)}] + \Delta V_{DC2(n)} \cdot V_{DC1(n)} - V_{DC1(n)}(V_{DC1(n)} + V_{DC2(n)})}{V_{DC1(n)}(V_{DC1(n)} + \Delta V_{DC1(n)})}$$
(10)

Assuming  $V_{DC1(n)} >> \Delta V_{DC1(n)}$ , the above equation can be simplified as:

$$\Delta d_{SA1} = -\frac{\Delta V_{DC1(n)}}{V_{DC1(n)}^2} [R_E(i_S + I_{Sref}) + V_{DC2(n)}] + \frac{\Delta V_{DC2(n)}}{V_{DC1(n)}} - \frac{(V_{DC1(n)} + V_{DC2(n)})}{V_{DC1(n)}}$$
(11)

From (4) and (11), it is possible to define the relationship between the duty ratio variation of the *Vcr*1 carrier signal and the compensation for the dc-link capacitor voltage unbalance. The voltage variations of the two upper dc-link capacitors ( $C_1$ ,  $C_2$ ) in region I are given by:

$$\Delta V_{DC1(n+1)} = -\frac{T_{s}}{C_{1} \cdot V_{DC1(n)}^{2}} [R_{E}(i_{s} + I_{Sref}) + V_{DC2(n)}](i_{s} + I_{Sref}) \cdot \Delta V_{DC1(n)} + \frac{T_{s}}{C_{1} \cdot V_{DC1(n)}}(i_{s} + I_{Sref}) \cdot \Delta V_{DC2(n)} + \frac{T_{s}}{C_{1} \cdot V_{DC1(n)}}(V_{DC1(n)} + V_{DC2(n)})(i_{s} + I_{Sref}) - \frac{T_{s}}{C_{1}} \cdot \Delta I_{INV1} = A_{1} \cdot \Delta V_{DC1(n)} + A_{2} \cdot \Delta V_{DC2(n)} + A_{C1} + A_{C2}$$

$$\Delta V_{DC2(n+1)} = \frac{T_S}{C_2} (-\Delta I_{INV1} - \Delta I_{INV2}) = B_{C1} + B_{C2}$$
(12)

When  $V_{DC1} > V_{DC}^* > V_{DC2}$ ,  $\Delta d_{SA1}$  is negative and  $\Delta I_{INV1}$  is positive in region I. Therefore, the over-charged  $C_1$  capacitor voltage ( $V_{DC1}$ ) will decrease and the undercharged or over-discharged  $C_2$  capacitor voltage ( $V_{DC2}$ ) will increase to reduce the dc-link capacitor voltage deviation, depending on the difference between  $\Delta I_{INV1}$  and  $\Delta I_{INV2}$ .

Since  $\Delta V_{DC1(n)} - \Delta V_{DC1(n+1)} = (1 - A_1) \cdot \Delta V_{DC1(n)} - A_2 \cdot \Delta V_{DC2(n)} - A_{C1} - A_{C2} > 0$ , the following compensation control is obtained:

$$\frac{\Delta V_{DC1(n+1)}}{\Delta V_{DC1(n)}} < 1 \tag{13}$$

In this unbalanced condition,  $\Delta V_{DC1}$  is decreasing during each switching cycle to reach the nominal dc-link capacitor voltage. From Figure 8b, similarly, the duty ratios of the  $S_{A2}$  switch under an unbalanced dc-link condition can be described as follows:

$$d_{SA2(n)} = \frac{T_{dSA2(n)}}{T_S} = \frac{R_S \cdot i_S + V_{Iref}}{V_{m2}}$$

$$d_{SA2(n+1)} = \frac{T_{dSA2(n+1)}}{T_S} = \frac{R_S \cdot i_S + V_{Iref}}{V_{m2} - \Delta V_{m2}}$$
(14)

where  $d_{SA2(n)}$  and  $d_{SA2(n+1)}$  are the duty ratios of the  $S_{A2}$  switch at the (*n*)th and (*n* + 1)th switching cycles, and:

$$V_{m2} = \frac{V_{DC2} \cdot R_S}{R_E}$$
$$\Delta V_{m2} = \frac{R_S}{R_E} \cdot \Delta V_{DC2} = \frac{R_S}{R_E} \cdot \Delta V \tag{15}$$



**Figure 8.** Proposed four-carrier level-shifted OCC PWM control of the proposed five-level OCC MV Regen-Load in region I and II. (a) *Vcr*1 carrier signal modulation when  $V_{DC1} > V_{DC}^*$ ; (b) *Vcr*2 carrier signal modulation when  $V_{DC2} < V_{DC}^*$ .

From (14) and (15), the duty ratio variation of the  $S_{A2}$  switch ( $\Delta d_{SA2}$ ) to adjust the unbalanced dc-link capacitor voltages can be obtained by:

$$\Delta d_{SA2} = d_{SA2(n+1)} - d_{SA2(n)} = \frac{\Delta V_{DC2(n)} \cdot R_E(i_S + I_{Sref})}{V_{DC2(n)}(V_{DC2(n)} - \Delta V_{DC2(n)})}$$
(16)

Assuming  $V_{DC2(n)} >> \Delta V_{DC2(n)}$ , the duty ratio variation of the  $S_{A2}$  switch can be simplified as:

$$\Delta d_{SA2} = d_{SA2(n+1)} - d_{SA2(n)} = \frac{\Delta V_{DC2(n)}}{V_{DC2(n)}^2} R_E(i_S + I_{Sref})$$
(17)

From (5) and (17), the voltage variations of the two upper dc-link capacitors ( $C_1$ ,  $C_2$ ) in region II are given by:

$$\Delta V_{DC1(n+1)} = \frac{T_S}{C_1} (-\Delta I_{INV1}) = A_{C2}$$
  
$$\Delta V_{DC2(n+1)} = \frac{T_S}{C_2 \cdot V_{DC2(n)}^2} R_E (i_S + I_{Sref})^2 \cdot \Delta V_{DC2(n)} - \frac{T_S}{C_2} (\Delta I_{INV1} + \Delta I_{INV2}) = B_2 \cdot \Delta V_{DC2(n)} + B_{C1} + B_{C2}$$
(18)

When  $V_{DC1} > V^*_{DC} > V_{DC2}$ ,  $\Delta d_{SA2}$  is positive and  $\Delta I_{INV1}$  is also positive in region II, the over-charged  $C_1$  capacitor voltage ( $V_{DC1}$ ) will decrease and the under-charged  $C_2$  capacitor voltage ( $V_{DC2}$ ) will increase to eliminate the dc-link capacitor voltage deviation.

Finally, the voltage variations of the four dc-link capacitors  $(C_1-C_4)$  can be described as follows:

$$\begin{bmatrix} \Delta V_{DC1(n+1)} \\ \Delta V_{DC2(n+1)} \\ \Delta V_{DC4(n+1)} \end{bmatrix} = \begin{bmatrix} -\frac{T_s}{C_1 \cdot V_{DC1(n)}^2} \left[ R_E(i_s + I_{Sref}) + V_{DC2(n)} \right] (i_s + I_{Sref})}{0} & \frac{T_s}{C_2 \cdot V_{DC2(n)}^2} R_E(i_s + I_{Sref})^2 & 0 & 0 \\ 0 & \frac{T_s}{C_2 \cdot V_{DC2(n)}^2} R_E(i_s + I_{Sref})^2 & 0 & 0 \\ 0 & 0 & \frac{T_s}{C_4 \cdot V_{DC4(n)}^2} R_E(i_s + I_{Sref})^2 & 0 & 0 \\ 0 & 0 & \frac{T_s}{C_4 \cdot V_{DC4(n)}} \left[ R_E(i_s + I_{Sref}) + V_{DC3(n)} \right] (i_s + I_{Sref}) \end{bmatrix} + \begin{bmatrix} \Delta V_{DC1(n)} \\ \Delta V_{DC3(n)} \\ \Delta V_{DC4(n)} \end{bmatrix} \\ + \begin{bmatrix} -\frac{T_s}{C_1 \cdot V_{DC1(n)}} \left( V_{DC1(n)} + V_{DC2(n)} \right) (i_s + I_{Sref}) - \frac{T_s}{C_1} \cdot \Delta I_{INV1} \\ -\frac{T_s}{C_2} \cdot \Delta I_{INV2} - \frac{T_s}{C_2} \cdot \Delta I_{INV2} \\ -\frac{T_s}{C_2} \cdot \Delta I_{INV3} - \frac{T_s}{C_2} \cdot \Delta I_{INV4} \\ -\frac{T_s}{C_4 \cdot V_{DC4(n)}} \left( V_{DC3(n)} + V_{DC3(n)} \right) (i_s + I_{Sref}) - \frac{T_s}{C_4} \cdot \Delta I_{INV4} \end{bmatrix} \\ = \begin{bmatrix} A_1 \quad A_2 \quad 0 & 0 \\ 0 \quad B_2 \quad 0 & 0 \\ 0 \quad 0 \quad B_3 \quad D_4 \end{bmatrix} \cdot \begin{bmatrix} \Delta V_{DC1(n)} \\ \Delta V_{DC3(n)} \\ \Delta V_{DC3(n)} \\ \Delta V_{DC4(n)} \end{bmatrix} + \begin{bmatrix} A_{C1} + A_{C2} \\ B_{C1} + B_{C2} \\ C_{C1} + C_{C2} \\ D_{C1} + D_{C2} \end{bmatrix} = \begin{bmatrix} A_1 \quad A_2 \quad 0 & 0 \\ 0 \quad B_2 \quad 0 & 0 \\ 0 \quad 0 \quad B_3 \quad D_4 \end{bmatrix} \cdot \begin{bmatrix} \Delta V_{DC1(n)} \\ \Delta V_{DC3(n)} \\ \Delta V_{DC3(n)} \\ \Delta V_{DC4(n)} \end{bmatrix} + \begin{bmatrix} A_{C1} + A_{C2} \\ B_{C1} + B_{C2} \\ C_{C1} + C_{C2} \\ D_{C1} + D_{C2} \end{bmatrix} = \begin{bmatrix} A_1 \quad A_2 \quad 0 & 0 \\ 0 \quad B_2 \quad 0 & 0 \\ 0 \quad 0 \quad B_3 \quad D_4 \end{bmatrix} \cdot \begin{bmatrix} \Delta V_{DC1(n)} \\ \Delta V_{DC3(n)} \\ \Delta V_{DC3(n)} \\ \Delta V_{DC4(n)} \end{bmatrix} + \begin{bmatrix} A_{C1} + A_{C2} \\ B_{C1} + B_{C2} \\ B_{C1} + B_{C2} \\ D_{C1} + D_{C2} \end{bmatrix} = \begin{bmatrix} A_1 \quad A_2 \quad 0 & 0 \\ B_2 \quad 0 & 0 \\ 0 \quad 0 \quad B_3 \quad D_4 \end{bmatrix} \cdot \begin{bmatrix} \Delta V_{DC1(n)} \\ \Delta V_{DC3(n)} \\ \Delta V_{DC3(n)} \\ \Delta V_{DC4(n)} \end{bmatrix} + \begin{bmatrix} A_{C1} + A_{C2} \\ B_{C1} + B_{C2} \\ B_{C1} + B_{C2$$

Using (19), the voltage variation vector  $\Delta V_{DC}(n)$  can be written by a 4 × 4 matrix *A* and the initial voltage variation vector  $\Delta V_{DC}(0)$ :

$$\Delta V_{DC}(n) = \begin{bmatrix} \Delta V_{DC1(n)} \\ \Delta V_{DC2(n)} \\ \Delta V_{DC3(n)} \\ \Delta V_{DC4(n)} \end{bmatrix} = A \begin{bmatrix} \Delta V_{DC1(n-1)} \\ \Delta V_{DC2(n-1)} \\ \Delta V_{DC3(n-1)} \\ \Delta V_{DC4(n-1)} \end{bmatrix} + B = A^n \begin{bmatrix} \Delta V_{DC1(0)} \\ \Delta V_{DC2(0)} \\ \Delta V_{DC3(0)} \\ \Delta V_{DC4(0)} \end{bmatrix} + C = A^n \cdot \Delta V_{DC}(0) + C \quad (20)$$

where:

$$A^{n} = \begin{bmatrix} A_{1}^{n} & (A_{1}^{n-1} + A_{1}^{n-2}B_{2} + \dots + A_{1}B_{2}^{n-2} + B_{2}^{n-1})A_{2} & 0 & 0 \\ 0 & B_{2}^{n} & 0 & 0 \\ 0 & 0 & C_{3}^{n} & 0 \\ 0 & 0 & (C_{3}^{n-1} + C_{3}^{n-2}D_{4} + \dots + C_{3}D_{4}^{n-2} + D_{4}^{n-1})D_{3} & D_{4}^{n} \end{bmatrix}$$
(21)  
and  $C = [A^{n} + A^{n-1} + \dots + A + I] \cdot B$ 

From (19)–(21), it is clear that the voltage variations of the four dc-link capacitors become zero in steady state, even though there are some voltage variations of the dc-link capacitors in the beginning or induced by some perturbation. Based on the proposed level-shifted OCC control, dc-link capacitor voltage balance can be achieved for any load emulation condition. It is also clear that the stabilizing time required to eliminate the dc-link voltage unbalance is proportional to the dc-link capacitance and inversely proportional to the amplitude of the input current.

# 5. Simulation and Experimental Results

#### 5.1. Simulation Results

A single-phase five-level OCC MV Regen-Load has been simulated using PSIM to verify the steady and dynamic performance. In the simulation, the input line voltage ( $V_S$ ) is 4.16 kVac and the input inductor ( $L_S$ ) is 2.8 mH. The input line frequency is 60 Hz and the carrier frequency is 5 kHz. In addition, the main switches  $S_{A1}-S_{A'4}$  have 2.5 V saturation voltage and 2.5 V reverse diode voltage drop. The diode voltage drop of the clamping diodes is also 2.5 V. All the parameters of the simulation system are shown in Table 3.

In this simulation, the nominal dc-link capacitor voltage  $(V_{DC}^*)$  is 2.25 kVdc.

Figure 9 shows the two upper dc-link capacitor voltages ( $V_{DC1}$ ,  $V_{DC2}$ ) and the related upper carrier signals (Vcr1, Vcr2) to compensate the initial dc-link capacitor voltage unbalance ( $V_{DC1} > V_{DC2}$ ). In the simulation, the initial  $V_{DC1}$  is 2.6 kVdc and the initial  $V_{DC2}$ 

is 1.6 kVdc. In region I and II, the amplitudes of the *Vcr*1 and *Vcr*2 carrier signals can be decided by the deviation levels from the reference voltage  $(V_{DC}^*)$ , respectively. For the *Vcr*1 carrier signal, its carrier amplitude is smaller than the *Vcr*2 carrier signal since the initial  $C_1$  capacitor voltage  $(V_{DC1})$  has less deviation level than the  $C_2$  capacitor voltage  $(V_{DC2})$ . Depending on the operation condition, the minimum carrier amplitude should be properly designed to control the compensation time for the dc-link capacitor voltage unbalance.

Table 3. Parameters of the simulation system.

Parameter	Value
Grid phase voltage ( $V_S$ )	4.16 kV
DC bus voltage $(V_{DC})$	9/16 kV
DC-link capacitor voltage ( $V_{DC1}-V_{DC4}$ )	2.25/4 kV
Input line inductor ( $L_S$ )	2.8 mH
DC-link capacitors $(C_1 - C_4)$	2000 µF
Carrier frequency	5 kHz
Grid line frequency	60 Hz



**Figure 9.** Simulation waveforms of the proposed four-carrier level-shifted OCC PWM control of the five-level OCC MV Regen-Load in region I and II. (a)  $V_{DC1}$  and  $V_{DC2}$  dc-link capacitor voltages when  $V_{DC1} > V^*_{DC} > V_{DC2}$ ; (b) *Vcr*1 and *Vcr*2 carrier signals.

Figure 10 shows the dc-link capacitor voltages ( $V_{DC1}-V_{DC4}$ ) and the input line waveforms ( $V_S$ ,  $I_S$ ) for the five-level OCC MV Regen-Load when the initial dc-link capacitor voltages are unbalanced ( $V_{DC1} > V_{DC}^* > V_{DC3} = V_{DC4} > V_{DC2}$ ). In Figure 10a, the two upper dc-link capacitor voltages ( $V_{DC1}$ ,  $V_{DC2}$ ) have different initial values. In this case, the initial  $V_{DC1}$  is 2.6 kVdc and the initial  $V_{DC2}$  is 1.6 kVdc. On the other hand, the two lower dc-link capacitors ( $C_3$ ,  $C_4$ ) have the same initial values ( $V_{DC3} = V_{DC4} = 2$  kVdc). From Figure 10a, it is clear that the dc-link voltage balancing can be achieved within the single cycle of the input line voltage under the unbalanced initial condition. Figure 10b shows the input line voltage and input line current waveforms for an inductive load emulation. The input line current ( $I_S$ ) has about 1 kA peak amplitude and +30° phase lag with the input line voltage, working as a 30° RL load. As shown in Figure 10, the five-level OCC MV Regen-Load has the capability to emulate any high voltage and high current load condition with full control of the dc-link voltage balancing over all the operating conditions.



**Figure 10.** Simulation waveforms of the five-level OCC MV Regen-Load with unbalanced dc-link capacitor voltages. (**a**) Four dc-link capacitor voltages; (**b**) Input line voltage and input line current.

From this simulation, each dc-link capacitor voltage  $V_{DC1}-V_{DC4}$  is 4 kVdc to compare the normal operation of the proposed five-level OCC MV Regen-Load under different dc bus voltage condition.

Figure 11 shows the simulation waveforms of the proposed five-level OCC MV Regen-Load for a resistive load emulation. The input line voltage vs. and the input current  $I_S$  with about 400 A peak amplitude are in phase to represent the resistor load condition–17  $\Omega$  in this case. As expected, the input rectifier has five voltage levels (*Vrec*) from + $V_{DC}/2$  to  $-V_{DC}/2$  and is also in phase with the input line current  $I_S$ .

Figure 12 shows the proposed five-level OCC MV Regen-Load waveforms for an inductive load emulation when the current reference signal  $V_{Iref}$  has 2 V amplitude and  $-60^{\circ}$  phase angle. In Figure 12a, the input line current  $I_S$  has about 200 A peak amplitude with  $+60^{\circ}$  phase delay, compared to the input line voltage  $V_S$ . Similarly, the five-level rectifier voltage has  $60^{\circ}$  phase shift with the input line current, working as a  $60^{\circ}$  RL load. From the fast fourier transform (FFT) of the PSIM, the total harmonic distortion (THD) of the five-level rectifier voltage without filters is about 24%. The generated harmonic distortion can be reduced by employing proper passive or active filters.

Figure 13 shows the voltage and current waveforms for a diode rectifier load emulation when the proposed five-level OCC MV Regen-Load emulates a nonlinear rectified load with a diode bridge rectifier, a 0.5 mH dc link inductor, a 10 mF dc-link capacitor and a 100  $\Omega$  resistor load. In this test condition, the THD of the input current is about 41.5% from the diode rectifier load.

#### 5.2. Experimental Results

To verify the performance of the proposed five-level OCC MV Regen-Load, a smallscale prototype of 1 kVA 120 Vac five-level OCC MV Regen-Load was built in Figure 14, using IGBTs (IRGP4072DPbF), diodes (MUR1540G) and 2.5 A IGBT driver (VO3120) with optical isolation. A magneto-resistive current sensor (NT-5) is used to read the input line current  $I_S$  and a hall-effect voltage sensor (LV25-P) is applied to read the input line voltage  $V_S$ . For dc-link voltage measurement, four isolation amplifiers (AD202KN) are used to read each dc-link capacitor voltage ( $V_{DC1}-V_{DC4}$ ). The input line voltage vs. and the output grid voltage  $V_O$  have the same amplitude, 120 Vac with variable transformers. The dc-link voltage  $V_{DC}$  is 400 Vdc and each dc-link capacitor ( $C_1-C_4$ ) is 1800 µF. In the input rectifier, the input inductor  $L_S$  is 2.8 mH and the carrier frequency is 5 kHz. All the parameters of the experimental system are shown in Table 4.



**Figure 11.** Simulation results for the five-level OCC MV Regen-Load waveforms with R load. (a) Input voltage and input current; (b) Rectifier voltage and input current.



**Figure 12.** Simulation results for the five-level OCC MV Regen-Load waveforms with RL load. (a) Input voltage and input current; (b) Rectifier voltage and input current.



**Figure 13.** Simulation results for the five-level OCC MV Regen-Load waveforms with diode rectifier load. (a) Input voltage and input current; (b) Rectifier voltage and input current.

Figure 15 shows the experimental result for the dc-link voltage balancing of the proposed five-level OCC MV Regen-Load. In Figure 15a, when the five-level OCC MV Regen-Load emulates the diode rectifier load with about 4 A peak amplitude, the two upper dc-link capacitor voltages ( $V_{DC1}$ ,  $V_{DC2}$ ) are regulated under the dc-link balancing condition. Since a variable transformer is used between the power grid and the five-level OCC MV Regen-Load for safety, the input voltage shows somewhat saturated waveform around its peak values but is acceptable by the Standard. As shown in Figure 15b, the four dc-link capacitor voltages ( $V_{DC1}$ - $V_{DC4}$ ) are also balanced by the proposed level-shifted OCC PWM control with variable carrier amplitudes.

Figure 16 shows the experimental result for regenerative operation of the proposed five-level OCC MV Regen-Load. The input rectifier with about 4 A peak input current emulates a RC load and the output inverter feeds back the absorbed testing energy to the power grid as seen in Figure 16. The THD is less than 5% at 60 Hz output frequency and the efficiency is about 88%.

Parameter	Value
Grid phase voltage ( $V_S$ )	120 V
DC bus voltage ( $V_{DC}$ )	400 V
DC-link capacitor voltage ( $V_{DC1}-V_{DC4}$ )	100 V
Input line inductor $(L_S)$	2.8 mH
DC-link capacitor ( $C_1$ – $C_4$ )	1800 μF
Carrier frequency	5 kHz
Grid line frequency	60 Hz

Table 4. Parameters of the experimental system.



Figure 14. 1kVA five-level OCC MV Regen-Load prototype.



**Figure 15.** Experimental result for input voltage, input current and dc-link capacitor voltage waveforms with diode rectifier load. (a) Input voltage, input current and two upper dc-link capacitor voltages; (b) four dc-link capacitor voltages.



Figure 16. Experimental result for input and output waveforms with regenerative operation.

### 6. Conclusions

In this paper, OCC control method is extended for multilevel DCMCs that features a simple control circuit and automatic dc-link voltage balancing. Based on the OCC control, the five-level OCC MV Regen-Load is proposed to emulate linear or nonlinear load and in the meantime recycle the testing energy back to the power grid. The proposed OCC MV Regen-Load is based on back-to-back five-level DCMCs and four-carrier level-shifted OCC PWM control for the single-phase or three-phase configuration. With the proposed level-shifted OCC control, the voltage balancing of the dc-link capacitors for the back-to-back five-level DCMCs is automatically achieved without the need of additional balancing circuitry. The proposed five-level OCC MV Regen-Load can emulate any RLC, diode rectifier load and their combinations for MV applications.

The proposed OCC voltage-balancing technique of the dc-link capacitors is capable of keeping the dc-link capacitor voltages balanced even when the four dc-link capacitors have different capacitance or initial voltage condition. Simulation and experimental results have verified the dc-link voltage balance performance of the proposed five-level OCC MV Regen-Load based on back-to-back configuration. The experimental results based on the 1 kVA 120 Vac small-scale prototype also show that the proposed five-level OCC MV Regen-Load returns about 88% of the testing energy back to the power grid thereby providing significant electrical savings, where the design target is greater than 90%. The proposed five-level OCC MV Regen-Load is very suitable for performance validation, burn-in, life-time test, etc. of MV electrical machines, wind turbine generators and other AC power equipment with convenient dial-in of the impedance type and value.

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#### Abbreviations

The following abbreviations are used in this manuscript:

MV	Medium voltage
DCMC	Diode-clamped multilevel converter
SVPWM	Space vector pulse width modulation
DSP	Digital signal processor
IGBT	Insulated gate bipolar transistor
MV Regen-Load	MV regenerative AC electronic load
OCC	One-cycle control
PFC	Power factor correction
APF	Active power filter
GUI	Graphical user interface
EUT	Equipment under test
PD	Phase disposition
POD	Phase opposition disposition
APOD	Alternative phase opposition disposition
CLK	Clock signal
FFT	Fast fourier transform
THD	Total harmonic distortion

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