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Finite Control Set—Model Predictive Control with Non-Spread Spectrum and Reduced Switching Frequency Applied to Multi-Cell Rectifiers [†]

Eduardo Espinosa ^{1,*}, José Espinoza ², Pedro Melín ³, Jaime Rohten ³, Carlos Baier ⁴ and Marcelo Reyes ^{3,‡}

¹ Department of Electrical Engineering, Faculty of Engineering, Universidad Católica de la Santísima Concepción, Concepción 4090541, Chile

² Department of Electrical Engineering, Universidad de Concepción, Concepción 4070386, Chile; jose.espinoza@udec.cl

³ Department of Electrical and Electronic Engineering, Universidad del Bío-Bío, Concepción 4051381, Chile; pemelin@ubiobio.cl (P.M.); jaimerohten@ubiobio.cl (J.R.); mereyes@ubiobio.cl (M.R.)

⁴ Department of Electrical Engineering, Universidad de Talca, Curicó 3340000, Chile; cbaier@utalca.cl

* Correspondence: eespinosa@ucsc.cl

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[‡] PhD Student, Doctoral Program in Engineering at the MacroFacultad de Ingeniería UFRO-UBB-UTAL, Chile.



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Abstract: Multi-cell converters are widely used in medium-voltage AC drives. This equipment is based on power cells that operate with low-voltage-rating semiconductors and require an input multipulse transformer. This transformer cancels the low-frequency current harmonics generated by the three-phase diode-based rectifier. Unfortunately, this transformer is bulky, heavy, expensive, and does not extend the existing power cell (three-phase rectifier—Direct Current (DC) voltage-link—single-phase inverter) to the transformer. In this study, a harmonic cancelation method based on finite control set-model predictive control (FCS-MPC), extending the power cell's modularity to the input transformer. On the other hand, it considers treating the two disadvantages of the FCS-MPC: High switching frequency and spread spectrum. The details were developed in theory and practice to obtain satisfactory experimental results.

Keywords: predictive control; AFE rectifiers; total harmonic distortion minimization

1. Introduction

Multicell converters are widely used in medium-voltage applications, such as AC drives, active filters, electric vehicles, and PV farms [1]. This type of converter generates high voltage in the inverter stage through the series connection of power cells that use low-voltage semiconductors. Another characteristic of this type of converter is the use of an input multipulse transformer [2], which allows the harmonic cancelation of low-frequency current harmonics generated by the three-phase diode rectifier, obtaining an input current with low THD and a near unitary displacement factor.

In general, this type of converter has the following characteristics: (i) Low harmonic distortion in the AC output voltage, (ii) low switching frequency, and (iii) low common voltage. Thus, these converters can be classified into the following topologies: Neutral Point Clamped (NPC) [3], Cascaded H-Bridge (CHB) [4], and capacitor clamped [5].

This work is focused on a multicell converter based on CHB, which is widely used in the industry, where the power cells are fed by an input multipulse transformer. [6]. Each cell comprises a three-phase diode-based rectifier, a DC link based on a capacitor, and a single-phase voltage source inverter (VSI). For this power cell, using an input transformer is essential because it allows the generation of isolated DC sources.

The three-phase diode rectifier's cancellation of the input current harmonics in multicell converters uses an input multipulse transformer [6–8]. Although from the point of view of energy efficiency, for non-linear load power applications, the transformer must not operate at its nominal power [9], the preceding is due to a possible bad design, where it was not considered the current flowing through the transformer has harmonic content. This has a strong economic impact, especially in the industry [10], where a correct transformer design based on the load it will supply (K-Factor) can have a return rate of 25%. Another improvement in multicell converters is the use of modular transformers that improve both the harmonic cancellation of the input currents and a 15% increase in power density [11].

Modifications have been made in the topology shown [4]. It consists of changes in the multipulse transformer input with a phase shift in the secondary, for a transformer with identical secondaries and AFE rectifiers allowing bidirectional management of the flow of power [12]. Another modification presented in [13] unbalances the input voltages, and the load does not affect the input and output currents of the converter, obtaining satisfactory results. The third modification to this topology is seen in [14], where it is proposed to cancel the low-frequency harmonics by generating a switching pattern and transformer phase shift, achieving an input current with 23rd and 25th harmonics. Finally, a modification made in the rectifier stage is the use of AFE rectifiers; the novelty is using a PIR controller to manipulate the input currents of these rectifiers [15]; despite this, the multipulse transformer is still needed. From the point of view of high-power rectifiers [16], a multicell rectifier with low switching frequency is presented, which seeks to be friendly to the electrical network. For this, an optimal modulation is shown, which is compared to SHE. The result of this technique is slightly better than SHE, but both have the disadvantage of using tables to obtain the shooting angles.

Model predictive control (MPC) is a widely used control strategy in power converters [17,18]. A significant feature of MPC is the possibility of including nonlinearities and restrictions on the operation of the converter in a simple manner, in addition to the natural use of the discrete nature of power converters, and achieving a rapid response to changes in references [19].

This work evaluated the control scheme proposed in [20] based on FCS–MPC [21]. In this scheme, the use of a simple design input transformer (wye–wye) is proposed, where the input current control scheme minimizes the harmonics in each power cell. Thus, it is possible to replace the multipulse input transformer, as shown in Figure 1a. In addition, this control scheme achieves a low THD in the input current and unitary displacement factor. In addition, this control strategy covers two problems that affect the FCS–MPC: Spread spectrum and high switching frequency.

An input current reference is used in each AFE rectifier to the first drawback, which allows concentrating the harmonic spectrum around the harmonics, $6 \cdot n_c \pm 1$, where n_c is the number of cells. The second drawback is solved with a functional cost function FCS–MPC, which reduces the number of commutations in the semiconductor, achieving minimum losses due to switching. Finally, the above is demonstrated using the simulation and experimental results.

2. Topology and Harmonic Cancellation

Figure 1a shows the topology used, which is based on three power cells, $n_c = 3$; (however, the analysis can be extended to arbitrary n_c), where each power cell is composed of an input transformer (wye–wye) and a voltage source AFE rectifier, where the load is resistive for simplicity.

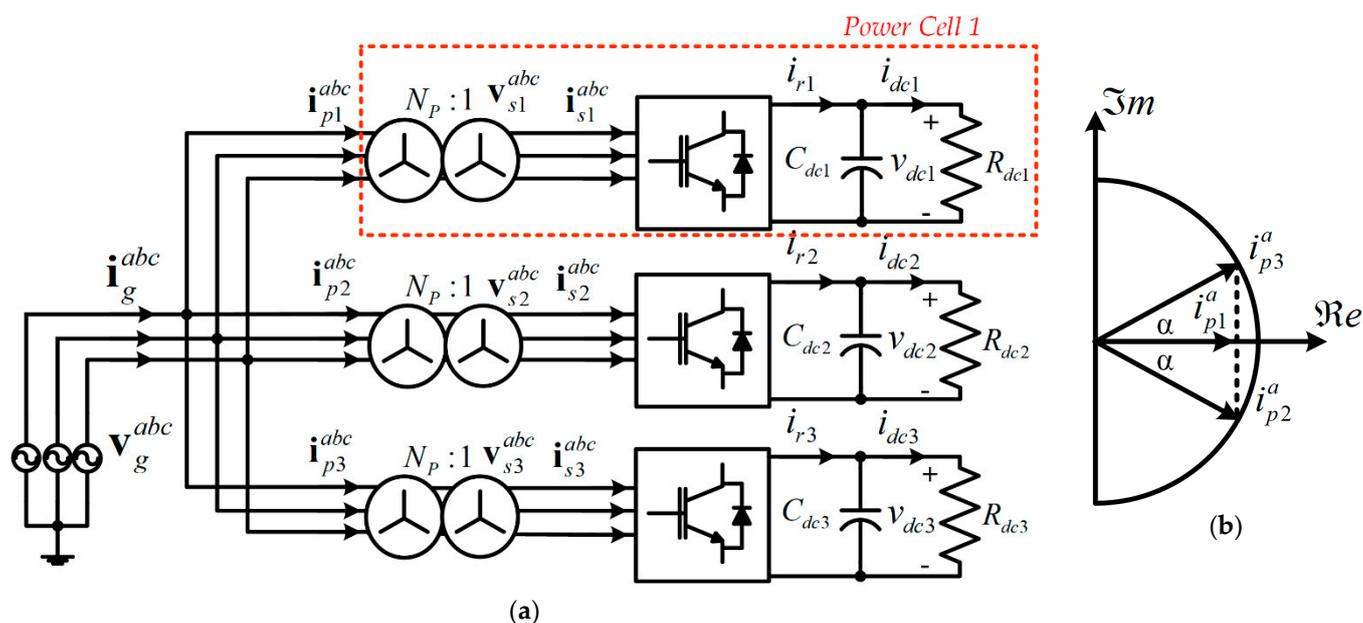


Figure 1. Topology and vector diagram input current power cells. (a) Multicell AFE rectifier, (b) phasor diagram of input currents of power cells.

In each AFE rectifier, the input current reference i_{si}^{abc} has 18 pulses, which is similar to the input current in an 18-pulse diode-based rectifier. Therefore, the dominant harmonics were chosen as the 17th and 19th harmonics, $6 \cdot n_c \pm 1$. The reasons for this are explained later in this section.

On the other hand, these harmonics (17th and 19th) are unwanted in the input current of the multicell AFE rectifier i_g^{abc} ; therefore, the input fundamental current reference in each AFE rectifier i_{si}^{abc} has a phase shift angle α , as shown in Figure 1b. This angle is computed offline to obtain the minimum THD in the total input current of the multicell AFE rectifier i_g^{abc} . Therefore, such harmonics present in the input of the current power cells do not appear in the current multicell AFE rectifier i_p^{abc} .

To minimize the THD of the input current multicell AFE rectifier, the fundamental components of the input currents in each power cell [20] are shown in Figure 1b, where the phase shift angle α is responsible for minimizing the harmonics 17th and 19th in this case. Despite this, the magnitude i_{p1}^a is slightly different i_{p2}^a ; however i_{p3}^a , the AFE rectifiers work with equal active power. This imbalance in the magnitude of the input current in each AFE rectifier is negligible, as discussed later.

To compute the phase shift angle α , a mathematical characterization is necessary for the transformer’s secondary currents; thus, references of the input current waveforms of the AFE rectifiers will be obtained [15]. The characterization is performed only for phase a ; however, it is valid for phases b and c .

Thus, the overall input current in phase a i_g^a , is given by,

$$i_g^a(t) = \frac{I}{N_p} \left[3 \cos(\alpha) \sin(\omega t) - \frac{\sin(17 \cdot \omega t) [\cos(\alpha) + 2 \cos(17 \cdot \alpha)]}{17} - \dots \right] \quad (1)$$

The current i_g^a defined in (1) has a unitary displacement factor desired for the input voltage v_g^a .

$$THD(I) = \frac{\sqrt{\sum_{k=2}^{n=51} I_k^2}}{I_1} \times 100, \quad (2)$$

Using (1) and (2), the THD function to minimize the input current multicell AFE rectifier for phase a is given by

$$THD(i_g^a) = \frac{\sqrt{\left(\frac{\cos(\alpha)+2\cdot\cos(17\cdot\alpha)}{17}\right)^2 + \left(\frac{\cos(\alpha)+2\cdot\cos(19\cdot\alpha)}{19}\right)^2}}{3 \cdot \cos(\alpha)} \times 100\%, \quad (3)$$

Thus, using (3), minimizing the THD of the input current multicell AFE rectifier is possible. This minimizes the 17th and 19th harmonics by obtaining an optimum value of α . The constraint for α is given by,

$$0 < \alpha \leq \frac{\pi}{2}. \quad (4)$$

The THD minimization `fmincon` command was used (Matlab[®]), which minimizes no linear expressions considering the constraints. The minimization result was $\alpha = 6.671^\circ$, which provided a 0.561% THD in the input current multicell AFE rectifier i_g^a .

The waveforms shown in Figure 2 were generated from THD minimization and mathematical characterization. The waveforms shown in Figure 2a–c are used as input current references in the input current loop that will be managed by FCS–MPC. The amplitude of these waveforms depends on the output of the V_{DC} PI controller in each power cell.

The input current references contain the 17th and 19th harmonics, as shown in Figure 2a–c, in which: (i) the harmonic content in the input current in each AFE rectifier is fixed, improving a drawback that has the FCS–MPC spread spectrum, obtaining a fixed spectrum; (ii) the equipment is modular and allows the generation of input current i_g^{abc} with low THD (0.561%), from currents i_{pi}^{abc} of inferior quality; (iii) there is an extension of the conventional power cell of the multicell converter to the input transformer, because harmonic minimization is performed through the control scheme; and (iv) the proposed input transformer (wye–wye with K–Factor = 3.00) has a simpler design than multipulse transformers (K–Factor = 9.00) [22].

Figure 2d shows that i_g^a it does not contain the 17th and 19th harmonics (actual amplitudes lower than 1%), because α is computed to minimize the harmonics present in the input current of the AFE rectifiers i_{si}^a .

Figure 1b shows an apparent power imbalance in each AFE rectifier, and owing to the use of the phase shift angle α , the current i_{p1}^a differs between i_{p2}^a and i_{p3}^a , but the value of $\alpha = 6.671^\circ$ is near zero; therefore, the apparent power imbalance can be neglected.

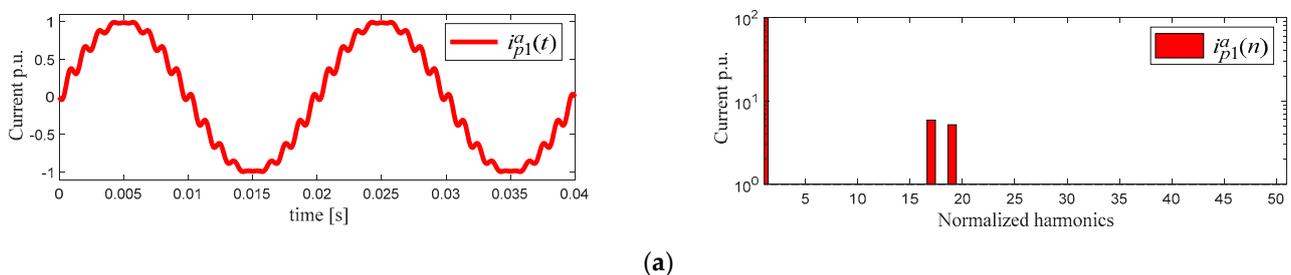


Figure 2. Cont.

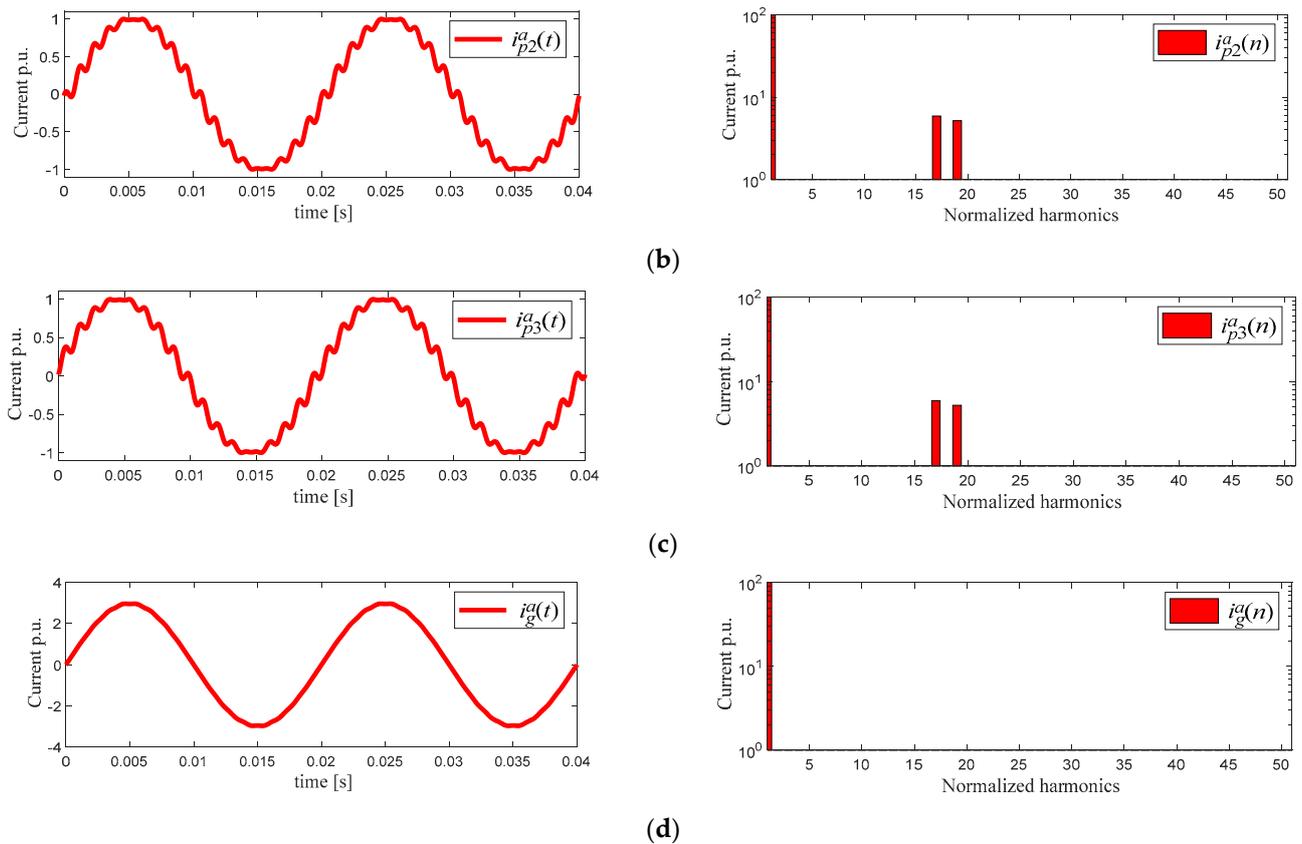


Figure 2. Input current references and harmonic content AFE rectifier for phase *a*. (a) AFE rectifier 1, (b) AFE rectifier 2, (c) AFE rectifier 3, (d) multicell AFE rectifier input current.

3. AFE Rectifier Model

In each power cell, input current control is performed through FCS–MPC [21]. This type of control requires knowledge of the system model, which is necessary to obtain.

The system model is shown in Figure 3. As shown in Figure 3a, the power cell uses a wye-wye transformer, so it is preferable to obtain the input current model for each AFE rectifier, referred to as the primary winding of the input transformer. Moreover, the magnetic branch is neglected in the model.

Thus, applying the KVL in Figure 3b, it is obtained that,

$$\mathbf{v}_g^{abc} = R_p \mathbf{i}_{pi}^{abc} + L_p \frac{d\mathbf{i}_{pi}^{abc}}{dt} + N_p^2 R_s \mathbf{i}_{pi}^{abc} + N_p^2 L_s \frac{d\mathbf{i}_{pi}^{abc}}{dt} + N_p \mathbf{v}_{si}^{abc}, \quad (5)$$

where \mathbf{v}_{si}^{abc} is,

$$\mathbf{v}_{si}^{abc} = \mathbf{M} \mathbf{s}_i^{abc} V_{DCi} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \mathbf{s}_i^{abc} V_{DCi}, \quad (6)$$

Then, using (6) in (5) it follows that,

$$\frac{d\mathbf{i}_{pi}^{abc}}{dt} = \frac{1}{(L_p + N_p^2 L_s)} \left[\mathbf{v}_g^{abc} - (R_p + N_p^2 R_s) \mathbf{i}_{pi}^{abc} - N_p \mathbf{M} \mathbf{s}_i^{abc} V_{DCi} \right]. \quad (7)$$

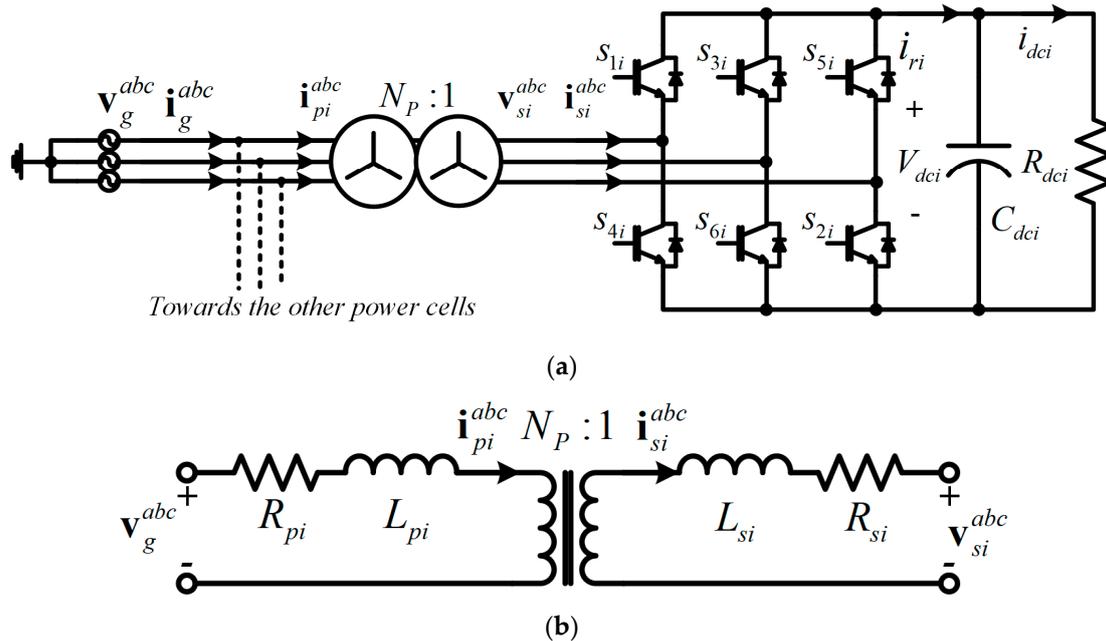


Figure 3. Power cell in multicell AFE rectifier. (a) Power cell. (b) Wye–wye transformer model.

The input current model in each AFE rectifier, referred to as the primary winding of the transformer, is shown in (7). This model is valid for balanced AC voltage sources.

The result in (7) is valid for continuous time, and it is necessary to discretize it for use in the FCS–MPC, where a forward Euler approximation is used. The above is valid because of the low sampling time (50 [μs]), which is given by

$$\frac{dx(t)}{dt} \approx \frac{x(k+1) - x(k)}{T_s}, \tag{8}$$

where T_s is the sampling time. Thus, employing (7) and (8) is obtained by referring to the primary winding of the discrete model of the input current AFE rectifier,

$$\mathbf{i}_{pi}^{abc}(k+1) = \left[1 - \frac{(R_p + N_p^2 R_s)}{(L_p + N_p^2 L_s)} T_s \right] \mathbf{i}_{pi}^{abc}(k) + \left[\mathbf{v}_g^{abc}(k) - N_p \mathbf{M}_i^{abc} V_{DCi}(k) \right] \frac{T_s}{(L_p + N_p^2 L_s)}, \tag{9}$$

Equation (9) shows that it is possible to predict the future behavior of the input current of each power cell through the semiconductor’s previous state, system inputs, and state variables.

4. Control Scheme

The master–slave loop conforms to the control scheme. The master loop (outer) controls the V_{DC} and the slave loop (inner) controls the input current of each power cell.

4.1. DC Voltage Link

A PI controller is used to manage the DC link voltage control in each power cell, as shown in Figure 4. By employing the transfer function defined in (10), it is possible to relate the input current and the DC link voltage in each power cell. Thus,

$$\frac{V_{dci}(s)}{I_{si}(s)} = \frac{3L_{si}I_{si}}{2C_{dci}V_{dci}} \left(\frac{s - \left(\frac{V_{pi} \cos(\phi)}{L_{si}I_{si}} - \frac{2R_{si}}{L_{si}} \right)}{\left(s + \frac{2}{R_{dci}C_{dci}} \right)} \right) \tag{10}$$

The PI controller output provides the reference amplitude value $I(k)$ for the input current for the AFE rectifier because the current waveform is preset, as shown in Figure 2a–c. In addition, it contains the phase shift angle α , previously computed by THD minimization (3).

4.2. Input Current with a Reduced Switching Frequency

Once the current reference is generated, it is compared with the estimated value of the FCS–MPC.

$$\mathbf{i}_{pi}^{abc}(k+2) = \left[1 - \frac{(R_p + N_p^2 R_s)}{(L_p + N_p^2 L_s)} T_s \right] \mathbf{i}_{pi}^{abc}(k+1) + \left[\mathbf{v}_g^{abc}(k+1) - N_p \mathbf{M} s_i^{abc} V_{DCi}(k+1) \right] \frac{T_s}{(L_p + N_p^2 L_s)}, \quad (11)$$

The control scheme in Figure 4 considers delay compensation for calculation. For this reason, (9) can be rewritten for instant $k+2$ (11).

Some approximations are performed in (11), and these are: $\mathbf{v}_g^{abc}(k+1) \approx \mathbf{v}_g^{abc}(k)$ and $V_{DCi}(k+1) \approx V_{DC}(k)$. This is possible because of the low sampling time used compared to the dynamics of these variables.

Using (11) and FCS–MPC, it is possible to test all the valid states of the AFE rectifier (Table 1) by choosing the state that minimizes the cost function defined below:

$$g_1(k+1) = \sum_{j=a}^c \left| i_p^{j*}(k) - i_p^j(k+1) \right|^2. \quad (12)$$

Table 1. Switching states AFE rectifier.

State	0	1	2	3	4	5	6	7
s^a	0	1	1	0	0	0	1	1
s^b	0	0	1	1	1	0	0	1
s^c	0	0	0	0	1	1	1	1

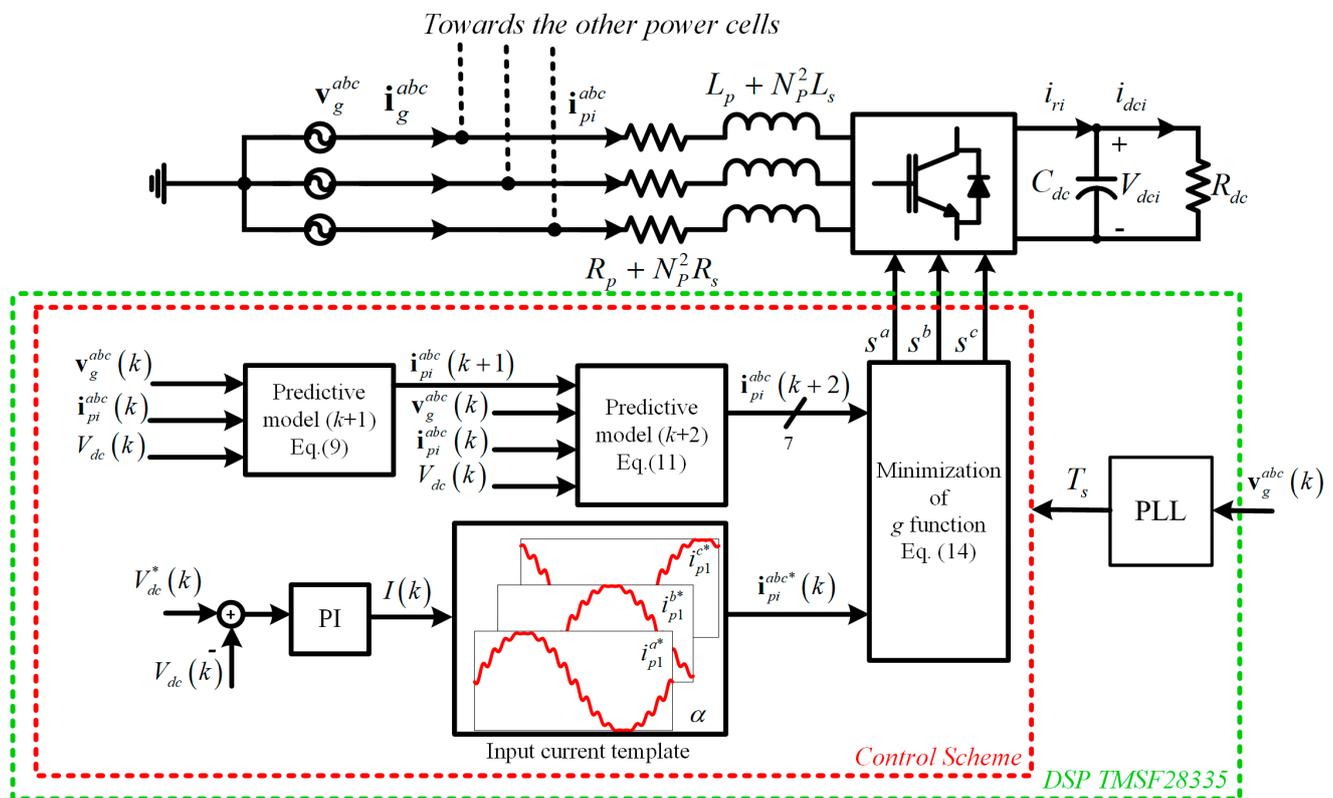


Figure 4. Control scheme in each power cell.

The cost function defined in (12) corresponds to the control of the input current in each AFE rectifier.

The high switching frequency is another disadvantage of the FCS-MPC; consequently, the switching losses are high. To overcome this disadvantage, a cost function is added to penalize the state change in semiconductors [23]. Assuming the switch states in each AFE rectifier (Table 1), it is possible to determine the number of switches that switch to perform the transition from one state to another within the eight possible states of switching of each AFE rectifier, as shown in Table 2.

Table 2. The number of switches between two states.

s^{abc}	0	1	2	3	4	5	6	7
0	0	1	2	1	2	1	2	3
1	1	0	1	2	3	2	1	2
2	2	1	0	1	2	3	2	1
3	1	2	1	0	1	2	3	2
4	2	3	2	1	0	1	2	1
5	1	2	3	2	1	0	1	2
6	2	1	2	3	2	1	0	1
7	3	2	1	2	1	2	1	0

Then, the cost function that considers the penalization of the state changes is,

$$g_2(k+1) = k_{sw} C_{sw} \left(s^{abc}(k), s^{abc}(k+1) \right), \quad (13)$$

C_{sw} depends on the state changes shown in Table 2, and k_{sw} is a weighting factor associated with switching each AFE rectifier.

Finally, the overall cost function to control the input current in each power cell is:

$$g(k+1) = \sum_{j=a}^c \left| i_p^*(k) - i_p^j(k+1) \right|^2 + k_{sw} C_{sw} \left(s^{abc}(k), s^{abc}(k+1) \right). \quad (14)$$

5. Semiconductors Losses

Semiconductor losses are associated with the switching and conduction processes, which depend on the semiconductor used. An analysis of the above processes is detailed below.

5.1. Switching Losses

Considering the non-ideal nature of the commutation process, the switching losses were analyzed [24], as shown in Figure 5.

IGBT switches are used in an AFE rectifier, and the losses in one switching period depend on the following factors: (i) Diode characteristics (reverse recovery time and current peak), (ii) IGBT characteristics (rise and fall time, tail time, and tail current), and (iii) stray inductance [25]. Fast recovery diodes are used in modern IGBTs; thus, the diode turn-on losses are less than 1% compared to the diode turn-off losses [26]; therefore, they are neglected in this analysis. Then, the estimated losses consider the IGBT turn-on shown in Figure 5a, IGBT turn-off in Figure 5b, and diode turn-off in Figure 5c, as in [22].

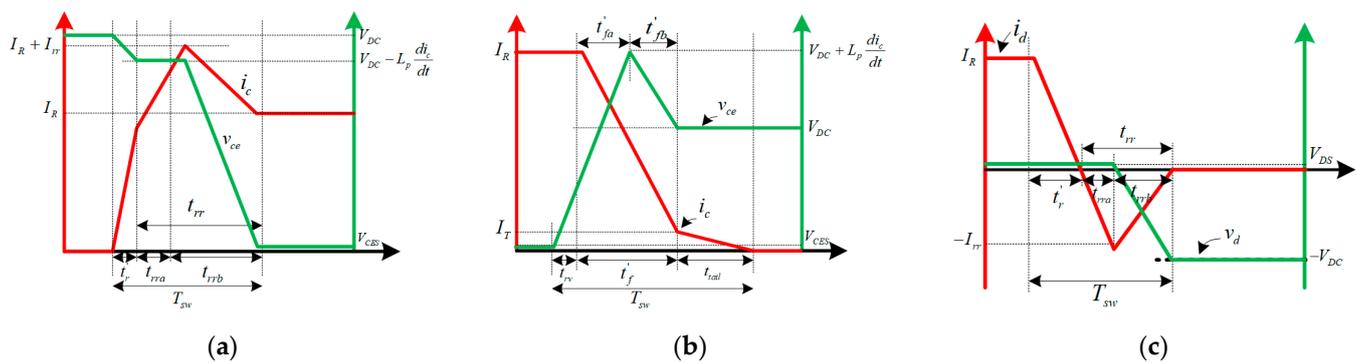


Figure 5. Linear piecewise approximation of the switch behavior. (a) IGBT turn on, (b) IGBT turn off, (c) diode turn off.

5.2. Conduction Losses

The conduction losses are dependent on the saturation voltage v_{sat} and instantaneous current $i(t)$ passing through [27]. The device saturation voltage can be modeled using a first-order linear approximation comprising a threshold voltage V_T and a series resistance R_T .

$$v_{sat}(t) = V_T + R_T \cdot i(t). \quad (15)$$

Thus, the average power dissipated due to conduction losses at the fundamental frequency is given by:

$$P_{COND} = V_T \cdot I_{AVG} + R_T \cdot I_{RMS}^2. \quad (16)$$

I_{AVG} is the average current flowing through the semiconductor, and I_{RMS} is the RMS current flowing through the semiconductor. Finally, the dissipated energy during a period is:

$$E_{COND} = P_{COND} \cdot T_{COND}. \quad (17)$$

where T_{COND} is the semiconductor conduction time, and (17) is used to calculate the conduction losses.

6. Experimental Results

To verify the theoretical results, a low-power experimental prototype was built, as shown in Figure 6, which is based on the circuit shown in Figure 1a. The control scheme described in Figure 4 was tested in transient and steady-state conditions using the parameters shown in Table 3.

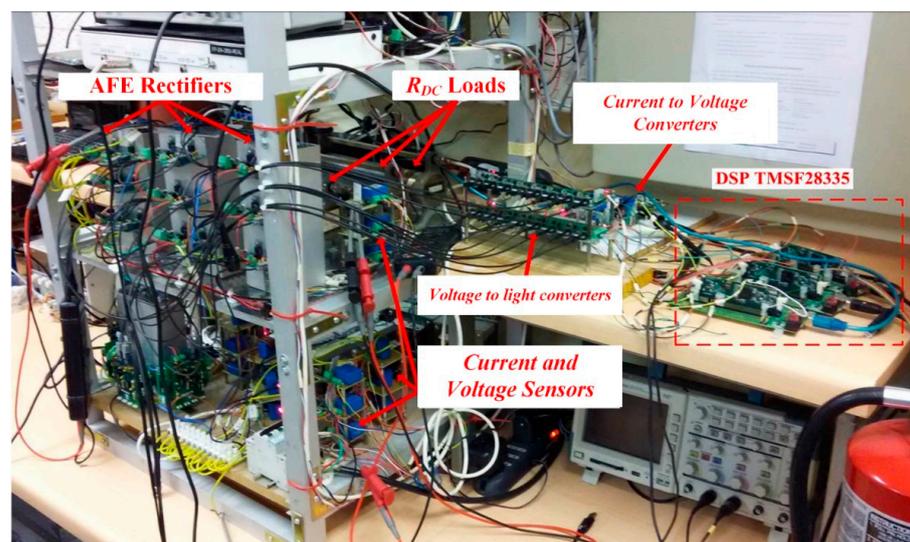


Figure 6. Experimental setup.

Table 3. Experimental Results.

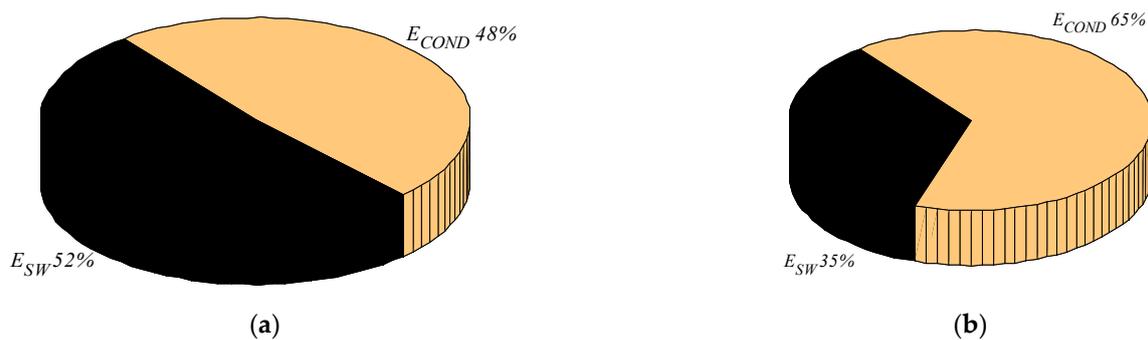
Symbol	Variable	Value
v_g	Phase voltage	31.1 [V]
f	Network frequency	50 [Hz]
R_p, R_s	Transformer primary and secondary resistances	0.5 [Ω]
L_p, L_s	Transformer primary and secondary inductances	6 [mH]
N_p	Turns ratio	1
R_{dc}	DC load resistance	89 [Ω]
C_{dc}	DC link capacitor	4.7 [mF]
V_{dc}	DC link voltage	55 [V]
k_p	Proportional gain	0.8
T_i	Integral time	0.02
T_s	Sampling time	50 [μ s]

This prototype was tested under two conditions for the input current loop in each power cell. The first condition is for $k_{sw} = 0.00$ (FCS–MPC without a reduced switching frequency), and the second is for $k_{sw} = 0.12$; both values are used in (14) to evaluate the switching losses. The semiconductor used in the experimental setup was an IGBT IRG4BC20UDPBF.

For this analysis, the current and voltage at the semiconductor were the same. In Figure 7a, the case for $k_{sw} = 0.00$, where the loss distribution is almost symmetric between conduction and switching, achieves an efficiency of 91.00% with $f_{sw} = 6$ kHz (average value). Then, in Figure 7b, for $k_{sw} = 0.12$, the efficiency is 93.25%, with $f_{sw} = 3$ kHz (average value) in the AFE rectifier. Because of the value of k_{sw} , the switching losses are reduced, and the efficiency in each power cell increases.

The weight factor tuning, k_{sw} , is made empirically, considering the input current THD in the power cells and DC link voltage response time to reference changes [28].

Figure 8a,b shows that the input currents of each power cell follow the reference imposed for both values of k_{sw} using FCS–MPC. These currents contain the 17th and 19th harmonics, concentrating the harmonic content on a fixed frequency, avoiding the AC network resonance problems, as shown in Figure 8a,b.

**Figure 7.** Distribution Semicondutor Losses. (a) FCS–MPC with $k_{sw} = 0.00$, (b) FCS–MPC with $k_{sw} = 0.12$.

Then, these harmonics are canceled out through the phase shift angle α , which allows for obtaining an almost sinusoidal current i_g^a , 1.87% THD for $k_{sw} = 0.00$, and 2.03% for $k_{sw} = 0.12$. The presence of unwanted harmonics in the input currents is due to a reduction in the switching frequency and the number of points by period ($N = 400$), obtaining a resolution of 0.9° by point.

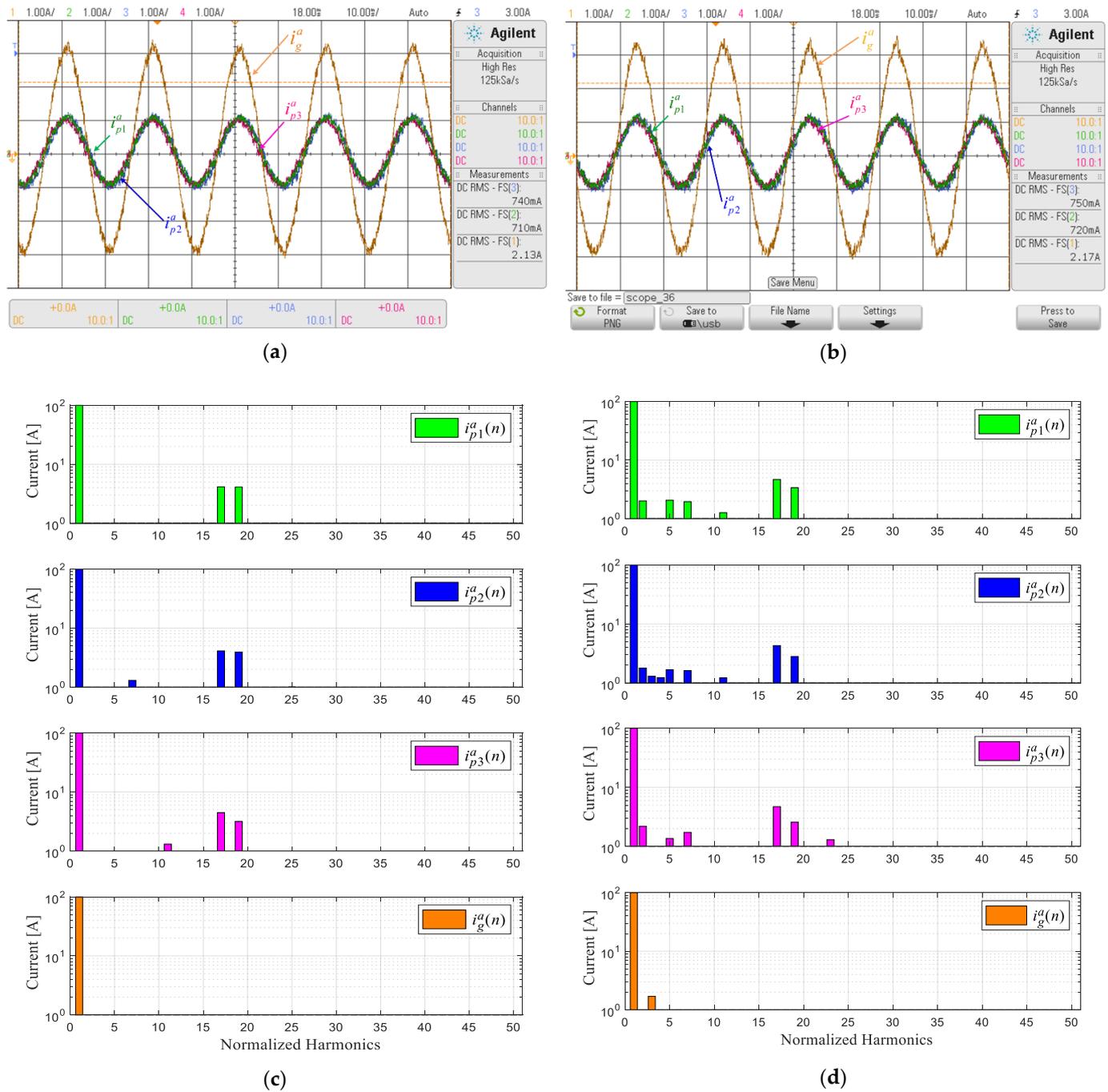


Figure 8. Experimental results input current loop. (a) Input current phase a in each AFE rectifier and input current multicell AFE rectifier for $k_{sw} = 0.00$, (b) input current phase a in each AFE rectifier and input current multicell AFE rectifier for $k_{sw} = 0.12$, (c) harmonic spectrum input current phase a in each AFE rectifier and input current multicell AFE rectifier for $k_{sw} = 0.00$, (d) harmonic spectrum input current phase a in each AFE rectifier and input current multicell AFE rectifier for $k_{sw} = 0.12$.

Despite this, THD minimization is performed correctly, and with i_g^a the THD is low. In the same way i_g^a , it has a unitary displacement for both values of k_{sw} , as shown in Figure 9a,b.

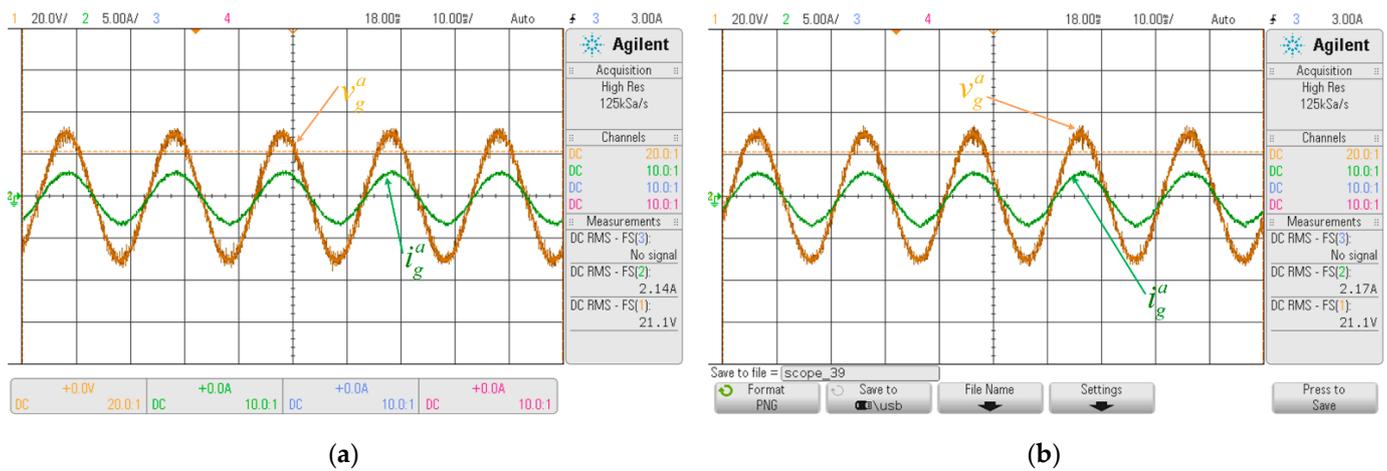


Figure 9. Input voltage and input current multicell AFE rectifier phase *a*. (a) for $k_{sw} = 0.00$, (b) for $k_{sw} = 0.12$.

Figure 10 depicts the behavior of the DC voltage loop (master loop). In Figure 10a,b, the transient response of the DC voltage for each AFE rectifier is presented for $k_{sw} = 0.00$ and $k_{sw} = 0.12$, respectively. The V_{DC} change reference is 55 (V) to 65 (V) and shows that the settling time is 400 ms with an overshoot of 5% in both cases, which is expected due to these PI tuning parameters. Using a reduced switching frequency in the inner loop, the input current does not show differences in the transient responses in the outer-loop voltage DC.

Owing to the control scheme used, the master–slave loop, any change in the reference voltages DC, 55 (V) to 65 (V), affects the input currents of the AFE rectifiers, as shown in Figure 10c,d.

Finally, the steady-state performance of the DC voltage loop for both k_{sw} values is identical, with a ripple below 2% (Figure 10e–f). This DC voltage ripple is at a fundamental frequency because it tracks the input current reference, generating a small second harmonic in the input current in each power cell, thus i_{ri} has a small fundamental component.

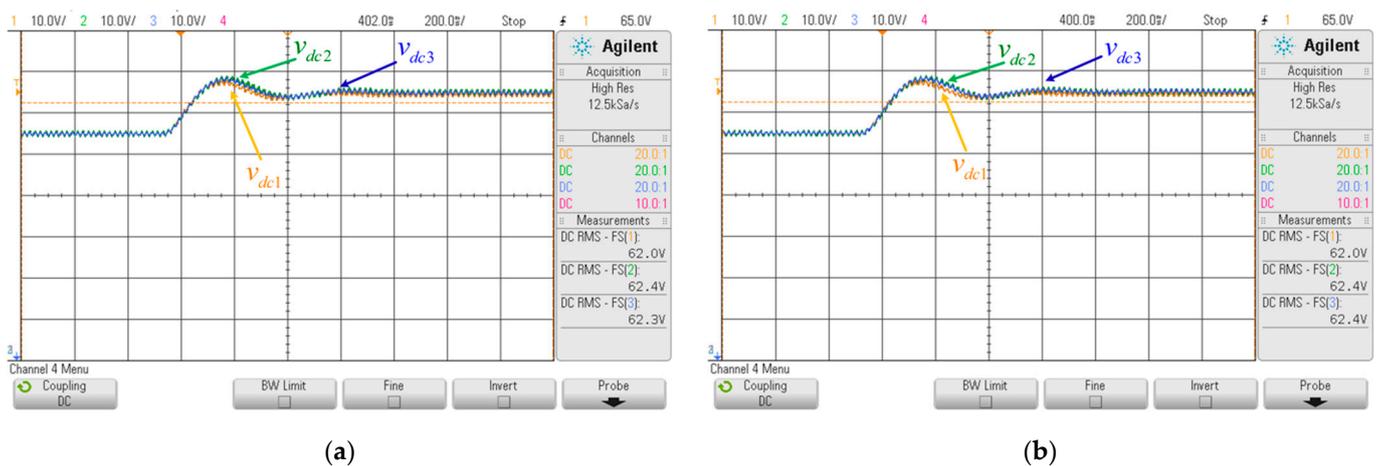


Figure 10. Cont.

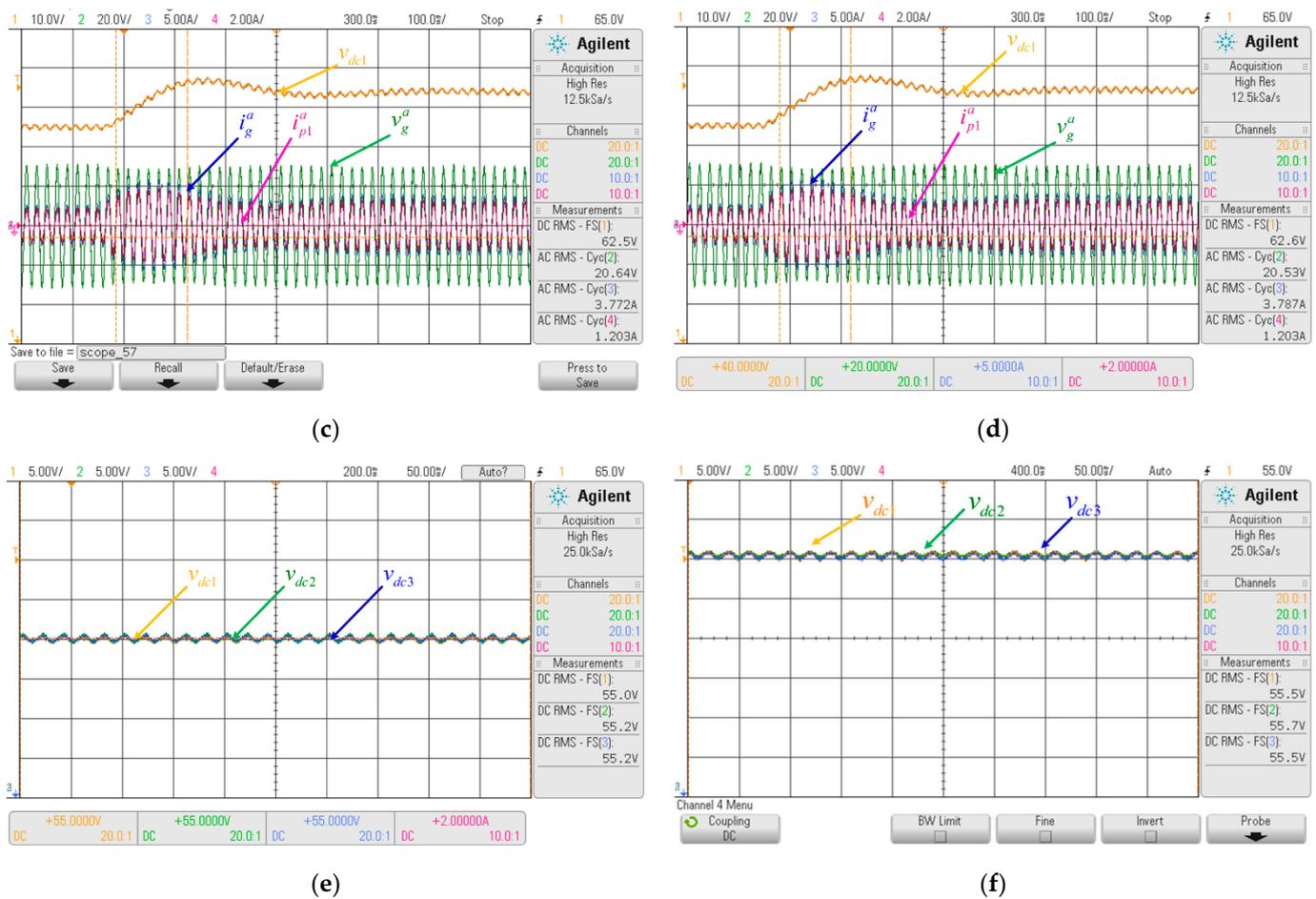


Figure 10. Experimental results V_{DC} voltage loop. (a) Transient response to step change with $k_{sw} = 0.00$. (b) Transient response to step change with $k_{sw} = 0.12$. (c) Input current change by step change in V_{DC} voltages with $k_{sw} = 0.00$. (d) Input current change by step change in V_{DC} voltages with $k_{sw} = 0.12$. (e) Steady-state V_{DC} voltages with $k_{sw} = 0.00$. (f) Steady-state DC voltages with $k_{sw} = 0.12$.

7. Conclusions

A harmonic minimization strategy for a multicell AFE rectifier based on FCS-MPC with a non-spread spectrum and reduced switching frequency is presented. The topology is tested considering a cost function that reduces the state changes in the semiconductors and input current reference preset, overcoming two drawbacks of the FCS-MPC: Spread spectrum and high switching frequency. The utilization of an input current reference preset for each AFE rectifier allows the concentration of current harmonics at a fixed value, avoiding a spread spectrum and achieving 2.03% THD in the input current multicell AFE rectifier by offline calculation of the phase shift angle α through THD minimization. Furthermore, the use of a function that considers the state changes in the semiconductors allows a reduction in the switching frequency in the input current loop managed with FCS-MPC, improving the efficiency of the multicell AFE rectifier, from 91.00% ($k_{sw} = 0.00$) to 93.25% ($k_{sw} = 0.12$). Finally, implementing a reduced switching strategy in a master-slave loop allows proper control of the DC link voltage in each AFE rectifier. Satisfactory experimental results prove the theoretical results.

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