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A Novel Buck Converter with Constant Frequency Controlled Technique

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Abstract: This paper presents a buck converter with a novel constant frequency controlled technique, which employs the proposed frequency detector and adaptive on-time control (AOT) logic to lock the switching frequency. The control scheme, design concept, and circuit realization are presented. In contrast to a complex phase lock loop (PLL), the proposed scheme is easy to implement. With this novel technique, a buck converter is designed to produce an output voltage of 1.0–2.5 V at the input voltage of 3.0–3.6 V and the maximum load current of 500 mA. The proposed scheme was verified using SIMPLIS and MathCAD. The simulation results show that the switching frequency variation is less than 1% at an output voltage of 1.0–2.5 V. Furthermore, the recovery time is less than 2 μs for a step-up and step-down load transient. The circuit will be fabricated using UMC 0.18 μm 1P6M CMOS processes. The control scheme, design concept and circuit realization are presented in this paper.

Keywords: adaptive on time (AOT); constant on time (COT); constant off time (CFT); voltage mode control (VMC); current mode control (CMC); peak current mode (PCM); valley current mode (VCM); average current mode (ACM); electromagnetic interference (EMI); phase lock loop (PLL)

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1. Introduction

Power converter brings convenience to human life [1–3] and plays an indispensable role in various portable devices. Their applications include smartphones, tablet computers, the internet of things (IoT) and other electronic products. The power source of these products is the battery. In order to extend the battery life, the products will enter a standby mode when they are not operating. Therefore, high power efficiency is a critical issue in a wide load range.

For switching converters, the main modulation methods can be divided into two categories: pulse width modulation (PWM) and pulse frequency modulation (PFM) [4,5]. PWM can obtain high power efficiency at heavy load conditions; however, a high switching frequency at light load conditions will induce more considerable switching loss and reduce the power efficiency. Therefore, in contrast to PWM, PFM control has a lower switching frequency at light loads, to reduce the switching loss and improve the power efficiency.

Recently, the control methods of DC-DC converter have mainly been divided into two types: voltage mode control (VMC) [6] and current mode control (CMC) [1–3,7]. Figure 1 shows the methods of the CMC and the VMC. From Figure 1, it is obvious that CMC has one more feedback path of inductor current than VMC; consequently, the CMC has a faster transient response and better voltage regulation than VMC. Therefore, the CMC technique is widely used in today's power management ICs.

Nowadays, there are different modulation schemes for CMC, including peak current mode (PCM) control, valley current mode (VCM) control, average current mode (ACM) control, constant on time (COT) control, adaptive on-time (AOT) control, constant off time (CFT) control and hysteretic control, which are summarized in [2,8–19].

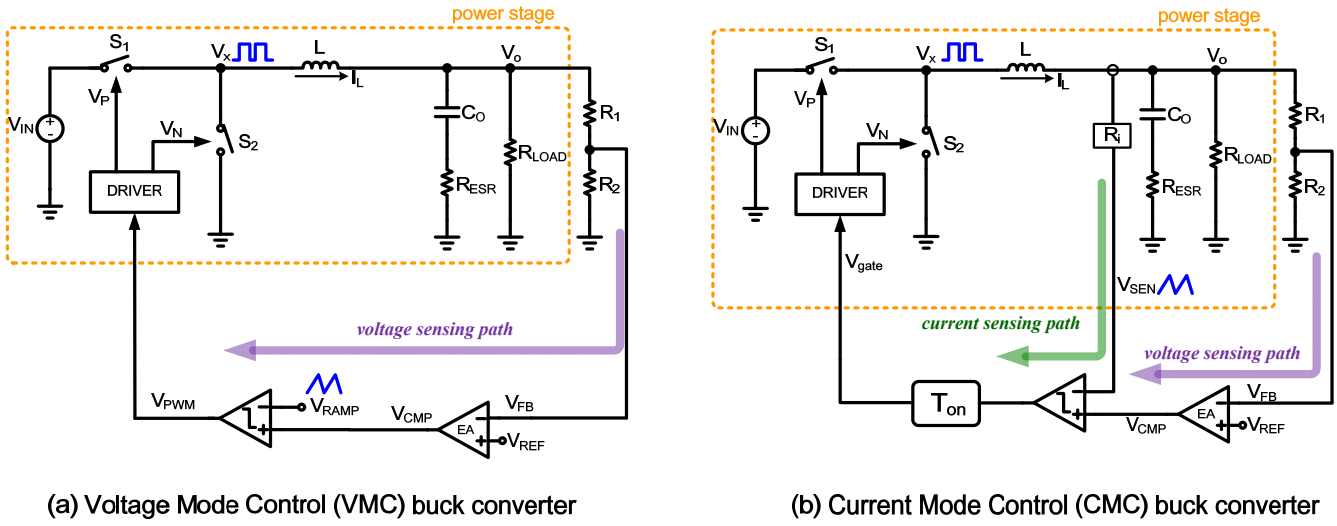


Figure 1. VMC/CMC buck converter.

The constant on-time current-mode (COTCM) control scheme has the inherent advantage of light load efficiency [20,21]. However, the variable switching frequency may cause electromagnetic interference (EMI) problems, which will impact the performance of the other integrated circuits. Moreover, the transient response of the step-load would be poor. This issue is due to the on-time remaining constant in the step-load transient, regardless of input/output conditions. For example, when the load suddenly drops after the switch is turned on, this might induce an overshot output voltage by the constant on-time.

In order to improve the issues of variable frequency and poor load transient in COTCM, a phase lock loop (PLL) based AOT control scheme is proposed [2]. The control scheme is shown in Figure 2. Similarly, the PLL technique can also be used in hysteretic control schemes [7,22,23]. However, these topologies have a high circuit complexity.

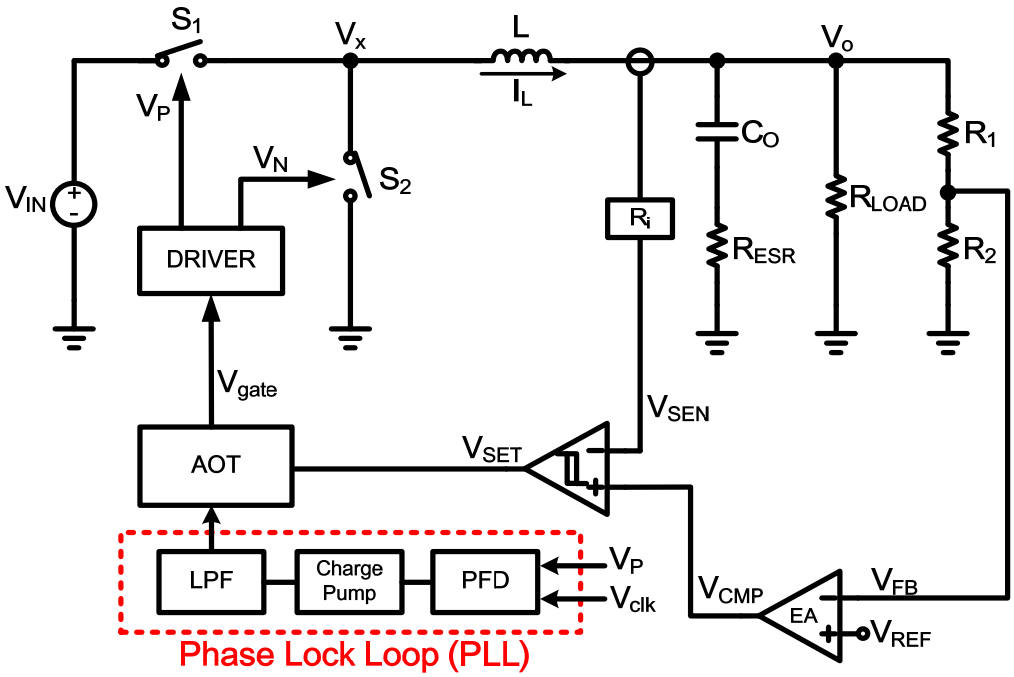


Figure 2. AOT control scheme with PLL.

Based on the above reasons, this paper proposes a novel constant frequency control scheme to maintain the switching frequency constant, instead of PLL. The proposed tech-

nique detailed in this paper is not necessarily superior to a PLL architecture in frequency constancy, but is better for realizing switching frequency constancy in the simplest way, which is suitable for commercialization and compatible with existing architectures.

The paper is organized as follows. Section 2 describes conventional COT/AOT control schemes. Section 3 presents the proposed control scheme and frequency detector. Section 4 introduces the design procedure and modeling analysis with MathCAD. Section 5 gives the SIMPLIS simulation results. Finally, the conclusion is given in Section 6.

2. Conventional Control Schemes Descriptions

2.1. Conventional COT/AOT Control Scheme

The conventional COT/AOT control scheme is as shown in Figure 3. For a COT scheme, the on-time is constant and fixed by the constant voltage V_{R_COT}. For an AOT scheme, the on-time is variable and controlled by V_{R_AOT}. As the scheme can easily get a fast transient response, the AOT scheme is becoming more and more popular.

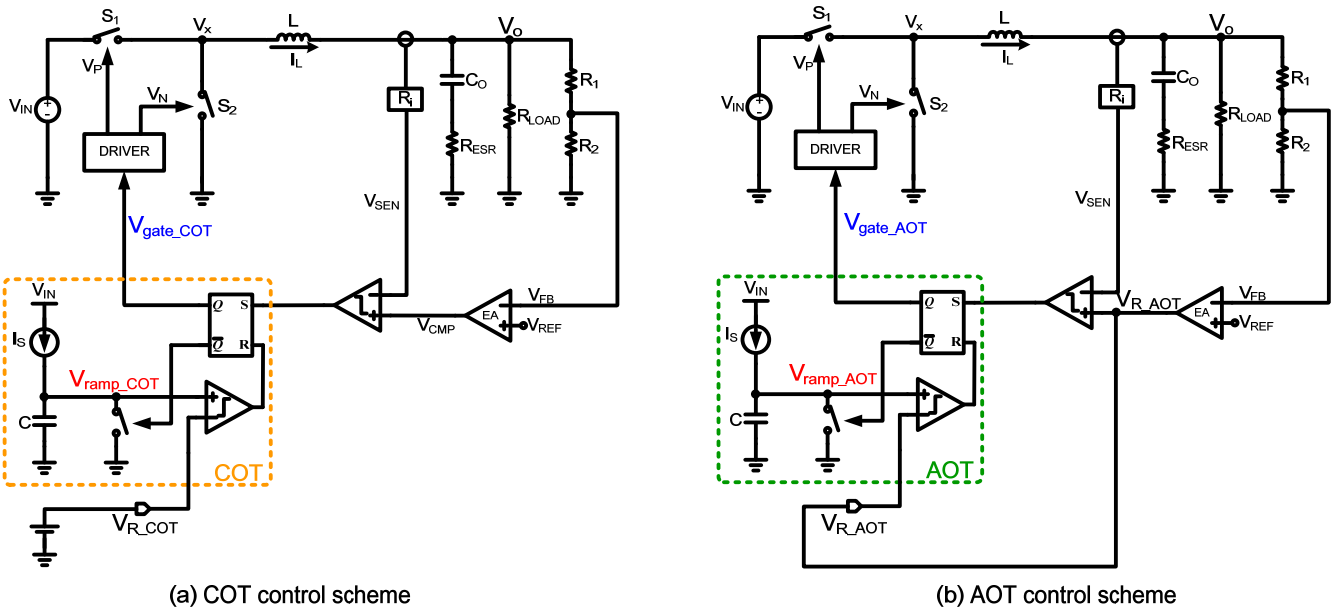


Figure 3. Conventional control schemes.

To illustrate why the AOT can easily get a fast transient response, we can use the conventional COT/AOT schemes in Figure 3. The key waveforms for the AOT/COT scheme are shown in Figure 4. The AOT transient response is better than the COT scheme when the load current is step-up due to the adaptive on-time.

2.2. Conventional AOT Scheme with PLL

Various control schemes based on AOT have been proposed to remedy the drawbacks. The most obvious example is the AOT scheme with PLL, which controls the on time, as shown in Figure 5.

Under a verified AOT control scheme, this paper proposes a novel and simple circuit to replace PLL.

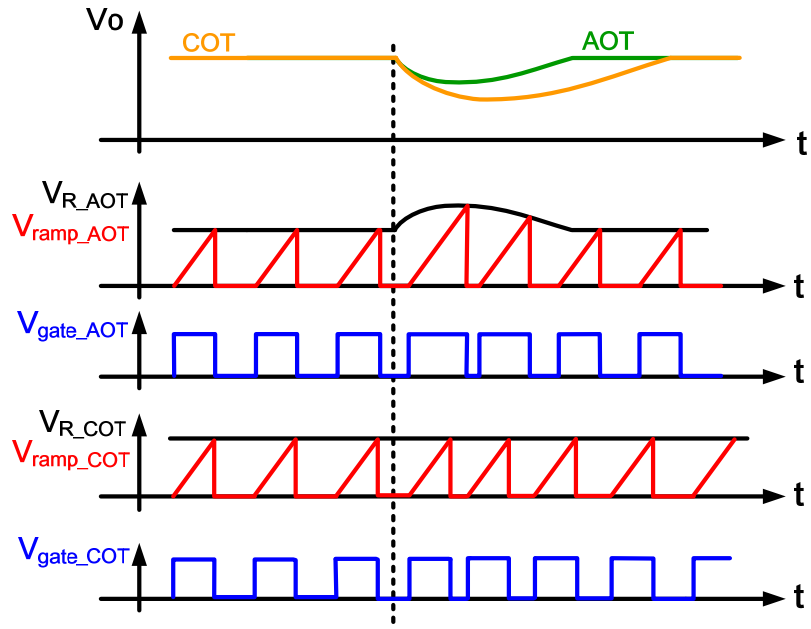


Figure 4. Key waveforms of the conventional control schemes.

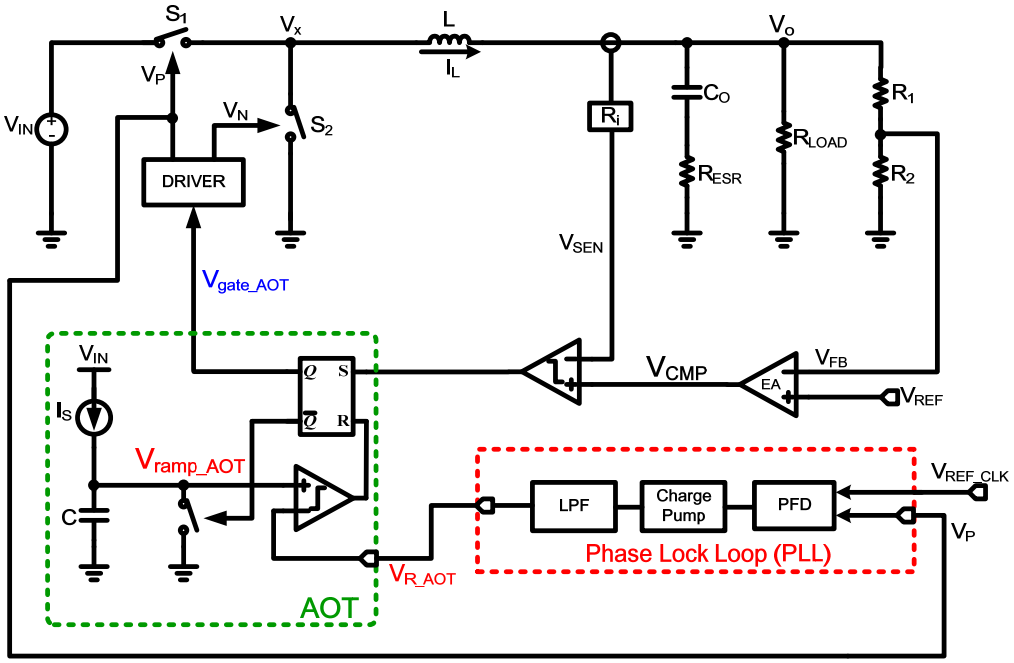


Figure 5. PLL based control scheme (display the AOT implementation).

3. Proposed Control Scheme and Frequency Detector

3.1. Proposed Control Scheme and Operating Principle

Figure 6 shows the proposed constant frequency AOT control scheme. In Figure 6, the proposed frequency detector produces a control voltage proportional to the switching frequency. The proposed AOT module generates an appropriate on-time to control the switches, S_1, S_2. The on-time labeled T_{on} is defined as the turn-on time of switch S_1. The state of S_1 and S_2 in Figure 6 are complementary and non-overlapping. The S_1 operates as follows: S_1 turns off at the end of the on-time, until V_{SEN} drops to V_{CMP}, and then turns on S_1 again. The R_i block in Figure 6 is the current sensor, which senses the inductor current I_L and converts the voltage V_{SEN}. The current sensor is another research topic. Relevant studies are fully introduced in [24]. The g_m in Figure 6 is the trans-conductance of the V-I

converter. The path through R_i to AOT is called the current sensing path, which is fast to improve the transient response. In addition, the path through the error amplifier (EA) to AOT is called the voltage sensing path. This is a slow path, mainly to regulate the output to the defined value. In addition, the EA includes a compensation network, not only an error amplifier.

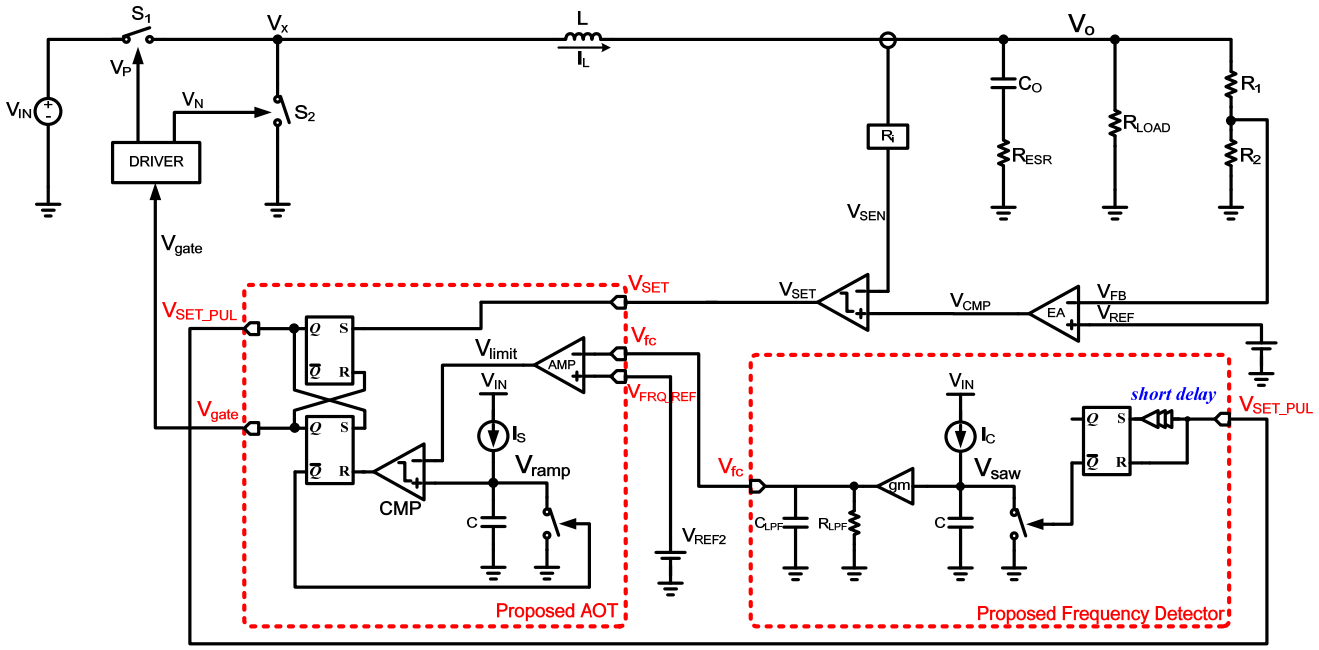


Figure 6. Proposed constant frequency AOT control scheme.

In this paper, the proposed control scheme is based on a AOT scheme, which has been verified and fabricated by 0.18 um/0.35 um CMOS processes in many literatures [17,25,26]. The proposed frequency detector only replaces PLL, and does not change the control topology. In other words, the purpose of this paper is not to propose a new control architecture. Instead, a frequency detector is added under the verified control architecture to replace the PLL. This technique can easily be realized with only D Flip-Flop, SR Flip-Flop, passive RC components, and about 60 dB of an operational amplifier.

3.2. Proposed Frequency Detector

Figure 7 shows the proposed frequency detector. This block mainly converts the switching frequency information into an analog voltage. The operation of the frequency detector can be understood from the key waveforms in Figure 8. The V_{SET_PUL}, V_{saw}, V_{fc}, and V_{gate} are all defined in Figure 6 or Figure 7. The shape converter converts the V_{SET_PUL} into a sawtooth wave. The frequency information is hidden in the sawtooth wave. Therefore, it can be extracted by following a low-pass filter (LPF). Figure 7b shows the implantation of the frequency detector. In contrast to the realization of PLL in Figure 5, the proposed method is simple and easy.

Overall, the proposed frequency detector's design concept involves how to find out the frequency information in the switching signal. Based on this purpose, this frequency detector can basically be divided into two parts: (a) a shape converter and (b) a low pass filter. The shape converter generates the sawtooth wave with switching period information. The low pass filter converts the sawtooth wave into a steady voltage and feeds it to the following stage. The switching frequency can keep constant, as long as the error amplifier locks the V_{fc} through the feedback path. Therefore, the proposed detector does not need special foundry processes to support the circuit implementation and layout issue.

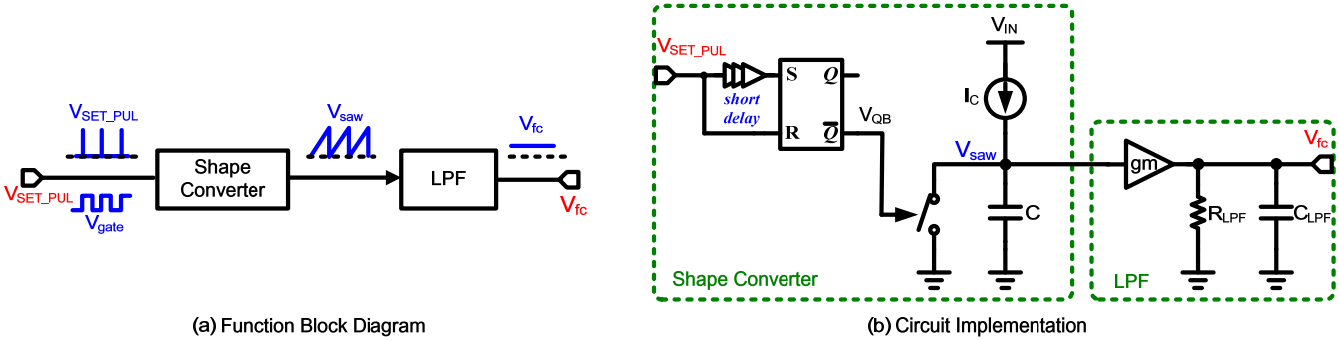


Figure 7. Proposed frequency detector.

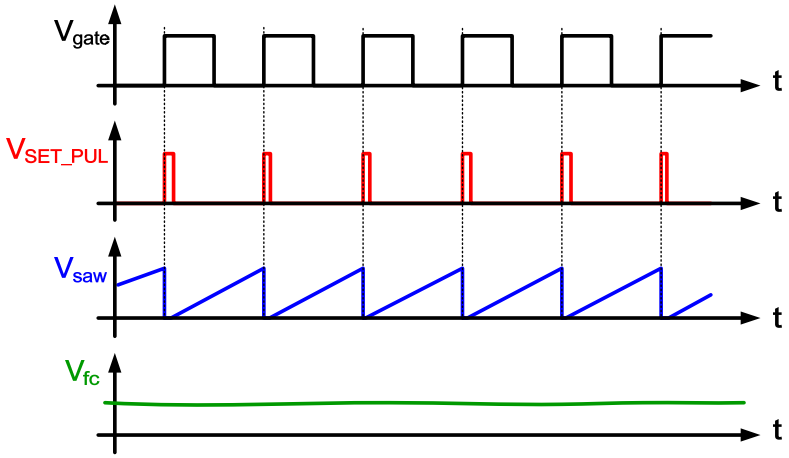


Figure 8. Key waveforms of frequency detector.

Moreover, the switching frequency accuracy depends on the dc gain of the amplifier. In this paper, the dc gain of the amplifier is 60 dB, which means that the accuracy can reach 0.1%.

3.3. Proposed AOT

The proposed AOT is shown in Figure 9. Differently from a conventional AOT, the on-time of the AOT is decided to regulate the switching frequency. In other words, the proposed control scheme contains two regulation loops: a voltage regulation loop and a frequency regulation loop. The voltage regulation loop keeps the output voltage constant, and the frequency regulation loop maintains the switching frequency constant. Figure 10 shows the key waveforms and allows the reader to easily and quickly to understand the operation.

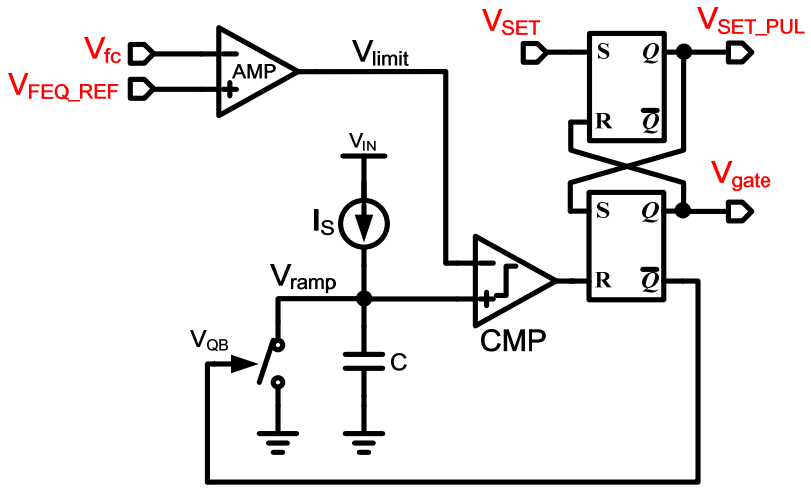


Figure 9. Proposed AOT circuit.

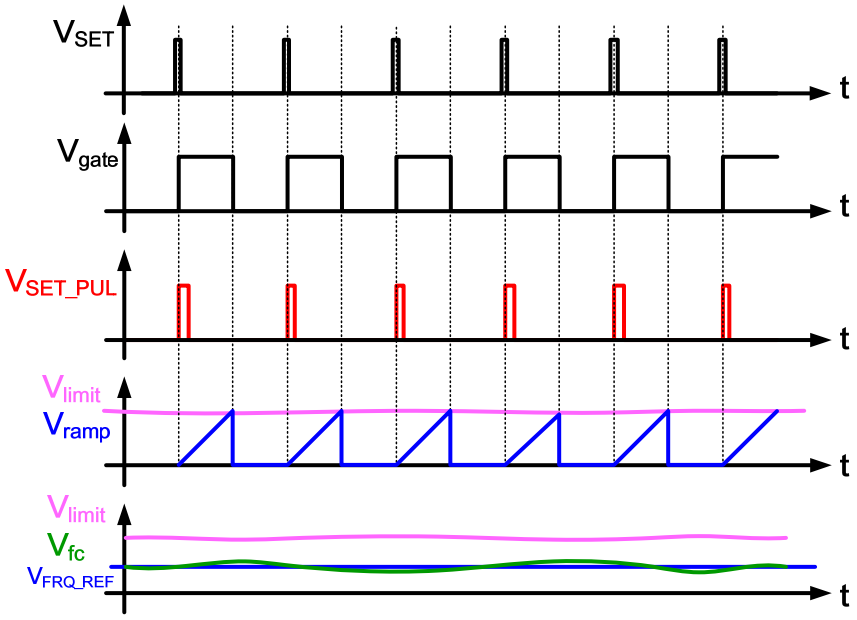


Figure 10. Key waveforms of the proposed AOT.

4. Design Procedure

4.1. Mathematical Modeling for Main Body Converter

Before entering the circuit design phase, we needed to derive the closed-loop transfer function of the control scheme, establish the mathematical model, and determine the pole/zero positions of the system. However, it can be seen from Figure 6 that the whole system includes a comparator, switch, amplifier, and compensation network. Therefore, it is not easy to establish an accurate mathematical model for the CMC scheme. Relevant modeling studies are presented in [10,27–30]. Among these prior works, the small-signal model proposed in [30] is most commonly used. Furthermore, Jian Li et al. [10] also proposed a more effective and intuitive current mode control circuit model for system analysis. In this section, we use MathCAD to obtain relevant design parameters and draw a Bode plot for stability analysis.

In order to derive the system transfer function, we divided Figure 6 into three parts: (a) a main body converter $G_p(s)$, (b) divider, and (c) error amplifier including compensation network A(s), as shown in Figure 11. In [30], we can express $G_p(s)$ as Equation (1).

$$G_P(s) = \frac{v_o(s)}{v_{CMP}(s)} \approx \frac{1}{R_i} \cdot \frac{1}{1 + \frac{s}{Q \cdot \omega} + \frac{s^2}{\omega^2}} \cdot \frac{R_{LOAD}(R_{ESR}C_o s + 1)}{(R_{LOAD} + R_{ESR})C_o s + 1} \quad (1)$$

where R_i is the gain for the current sensor, $\omega = \frac{\pi}{T_{on}}$ and $Q = \frac{2}{\pi}$.

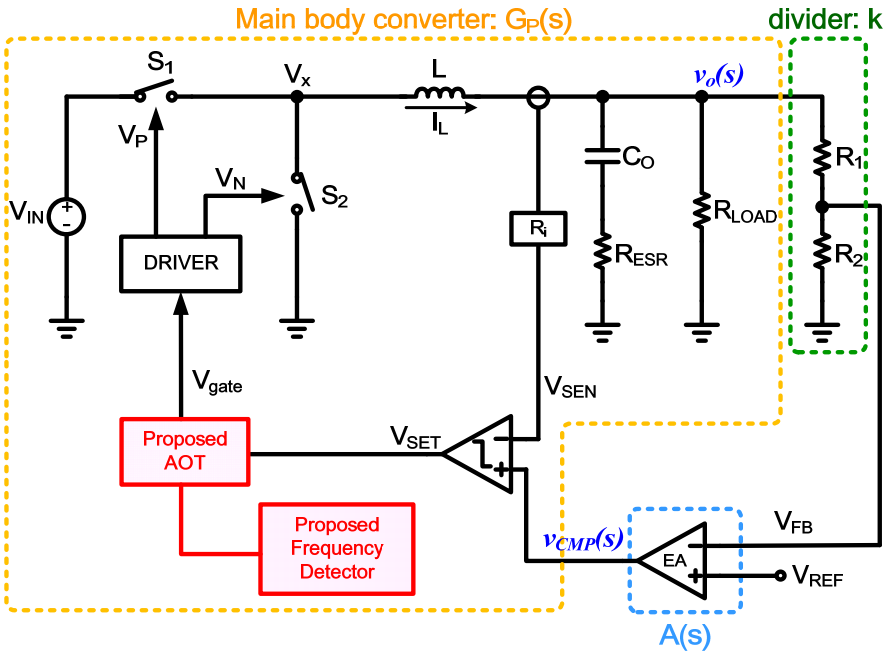


Figure 11. Proposed AOT partition.

Equation (1) is an approximate result. There is a dominant pole at the output, i.e., $w_{pout} \approx \frac{1}{R_{LOAD} \cdot C_o}$. In addition, the ESR of the capacitor will form a zero. Generally, this zero frequency is very high. For example, if C_o=10 µF and R_{ESR} = 5 mΩ, the zero frequency is about 20 MHz.

4.2. Compensation Network Design for A(s)

For the buck converter system, the A(s) design is critical and directly affects the crossover frequency, DC gain, and gain/phase margin of the closed-loop. As shown in Figure 12, the A(s) consists of an error amplifier and compensation network. The compensation network is composed of a resistor R_1 and capacitor C_1. This is a type II compensator. It is an off-chip compensation. The resistor R_o in Figure 12 signifies the output resistance of the error amplifier. The g_m is the trans-conductance of the error amplifier. Thus, the A(s) can be expressed by Equation (2). There is one pole and one zero in A(s). The static error is less than 0.1%, due to the error amplifier gain of 60 dB. From Figure 12, the converter loop gain T(s) can be expressed by Equation (3). In this paper, we set the zero w_z of A(s) at the output pole of the buck converter, as shown in Equation (4). The pole w_p of A(s) is extrapolated to make the feedback system stable.

$$\mathrm{A(s)} = \frac{v_{CMP}}{v_{FB}} = g_m \cdot R_o \cdot \frac{\left(1 + \frac{s}{w_z}\right)}{\left(1 + \frac{s}{w_p}\right)} \quad (2)$$

where $w_z = \frac{1}{R_1 \cdot C_1}$, $w_p = \frac{1}{R_o \cdot C_1}$

$$\mathrm{T(s)} = G_P(s) \cdot A(s) \cdot k \tag{3}$$

$$w_z = \frac{1}{(R_{LOAD} + R_{ESR})C_o} \approx \frac{1}{R_{LOAD} \cdot C_{out}}, f_z = \frac{w_z}{2\pi} \tag{4}$$

where R_{LOAD}, C_{out} is the output resistor and output capacitor in Figure 6, respectively.

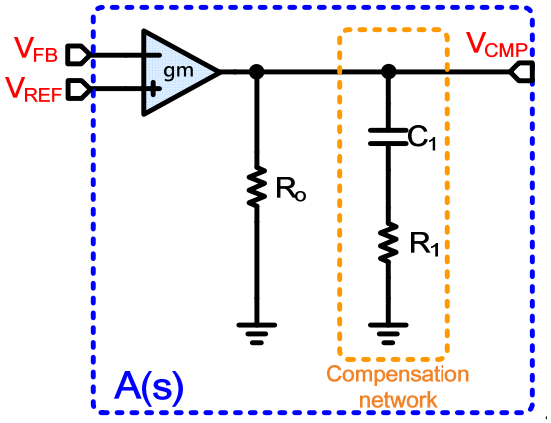


Figure 12. Error amplifier and compensation network.

4.3. Stability Analysis of Mathematical Model

Step 1 Substitute the Table 1 value into Equation (1), and set R_i = 490 m, then calculate the poles and zeros with MathCAD, and draw a Bode plot of the $G_p(s)$. The workspace of the MathCAD is shown in Figure 13. The Bode plot of the $G_p(s)$ is shown in Figure 14, where $w_{pout} \approx \frac{1}{R_{LOAD} \cdot C_o}$ i.e., $f_{pout} \approx 4.4$ kHz.

Step 2 As expressed in (4), the zero $f_z = f_{pout} = 4.4$ kHz. Using Equation (2), suppose $C_1 = 100$ pF, *then* $R_1 = 250$ kΩ can be obtained. In order to obtain a better output regulation, the A(s) gain is set to at least 60 dB. Thus, $R_o = 10$ MΩ, then g_m = 100 μA/V, and f_p ≈160 Hz. Finally, the values of g_m, R_o, C_1, and R_1 are substituted into Equation (2).

Step 3 We substitute Equation (2) into Equation (3) and draw the Bode diagram of T(s) with MathCAD. Here, in Equation (3), the k is substituted by 0.5. The Bode diagrams of T(s), G_p(s), and A(s) are drawn in Figure 15. As can be seen from Figure 15, the T(s) phase margin is about 40 degrees, DC gain is about 71 dB, and the crossover frequency f_c is about 400 kHz.

Table 1. Parameter Condition.

Component	Value	Unit
R_{LOAD}	3.6	Ω
C_o	10	μF
L	4.7	μH
R_{ESR}	5	mΩ

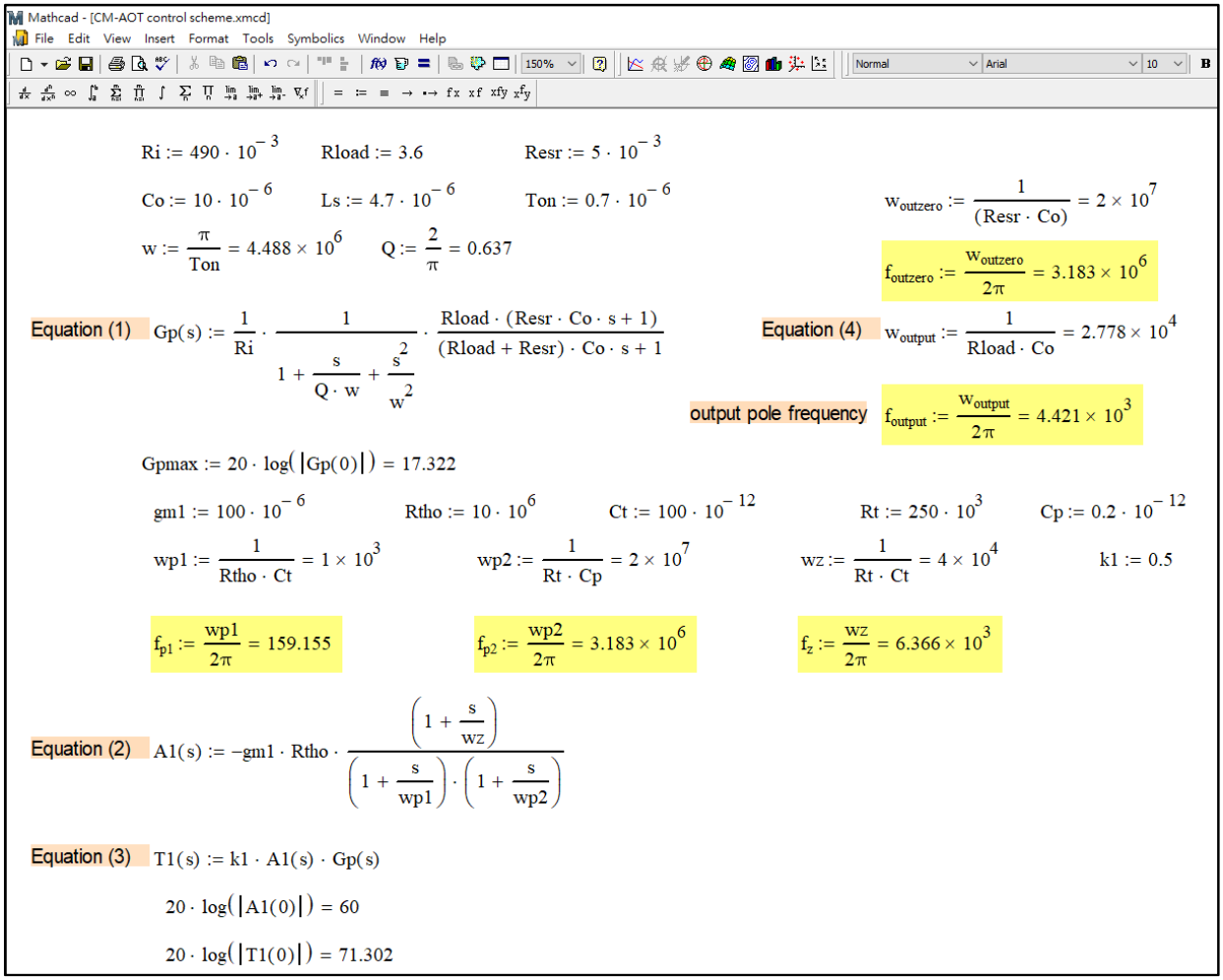


Figure 13. MathCAD workspace.

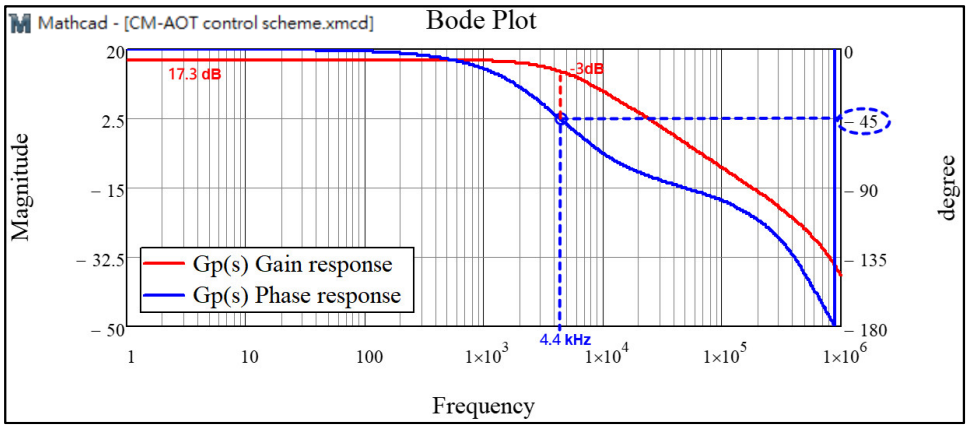
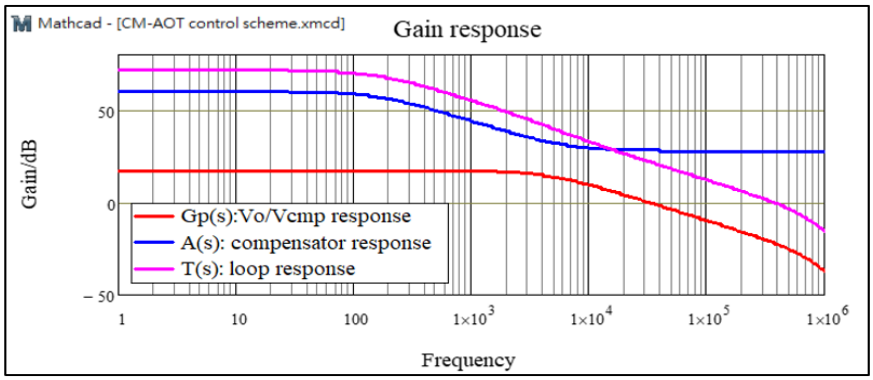
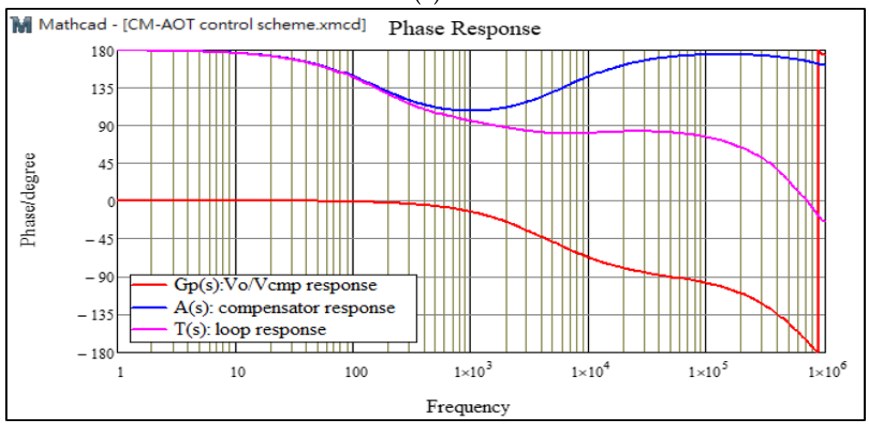


Figure 14. Bode Plot of main body converter $G_p(s)$.



(**a**)



(**b**)

Figure 15. (**a**). Gain response of T(s), G_P(s), and A(s). (**b**). Phase response of T(s), G_p(s), and A(s).

5. Simulation Results

5.1. SIMPLIS Schematic Building

In this section, the proposed control scheme is simulated by SIMPLIS. The schematic is presented in Figure 16.

5.2. Stability Analisis with SIMPLIS

For investigating stability issues, the proposed scheme was verified by SIMPLIS, and Bode diagrams are shown in Figure 17. The legend label names in Figure 17 follow the previous section definitions. As shown in Figure 17, the crossover frequency of the loop response is about 371 kHz, the phase margin is about 41 degrees, and DC gain is about 69 dB.

In Section 4.3, we used MathCAD to show the Bode diagrams of the T(s) by numerical approach. However, in this section, we build a circuit level schematic and confirm the stability by SIMPLIS. In order to compare the differences between MathCAD and SIMPLIS, we put the waveforms of Figures 14 and 17 into Figure 18. From Figure 18, we can see that the numerical approach and the circuit level have some differences. There is a possible reason for this difference: Equation (1) is an approximated result, and Equation (1) does not consider the parasitic effect of the inductor series resistance. Nevertheless, Equation (1) is very close to the real behavior of the system.

Therefore, the difficulty of switching converter design is to build an accurate model to meet the actual circuit behavior. Unfortunately, we could not find a mathematical model to completely represent the circuit behavior from the prior research literature. However, this does not mean that the mathematical model is useless for the design, because the relevant design parameters can be quickly obtained through MathCAD, such as the loop gain, capacitance, and resistance of the compensator.

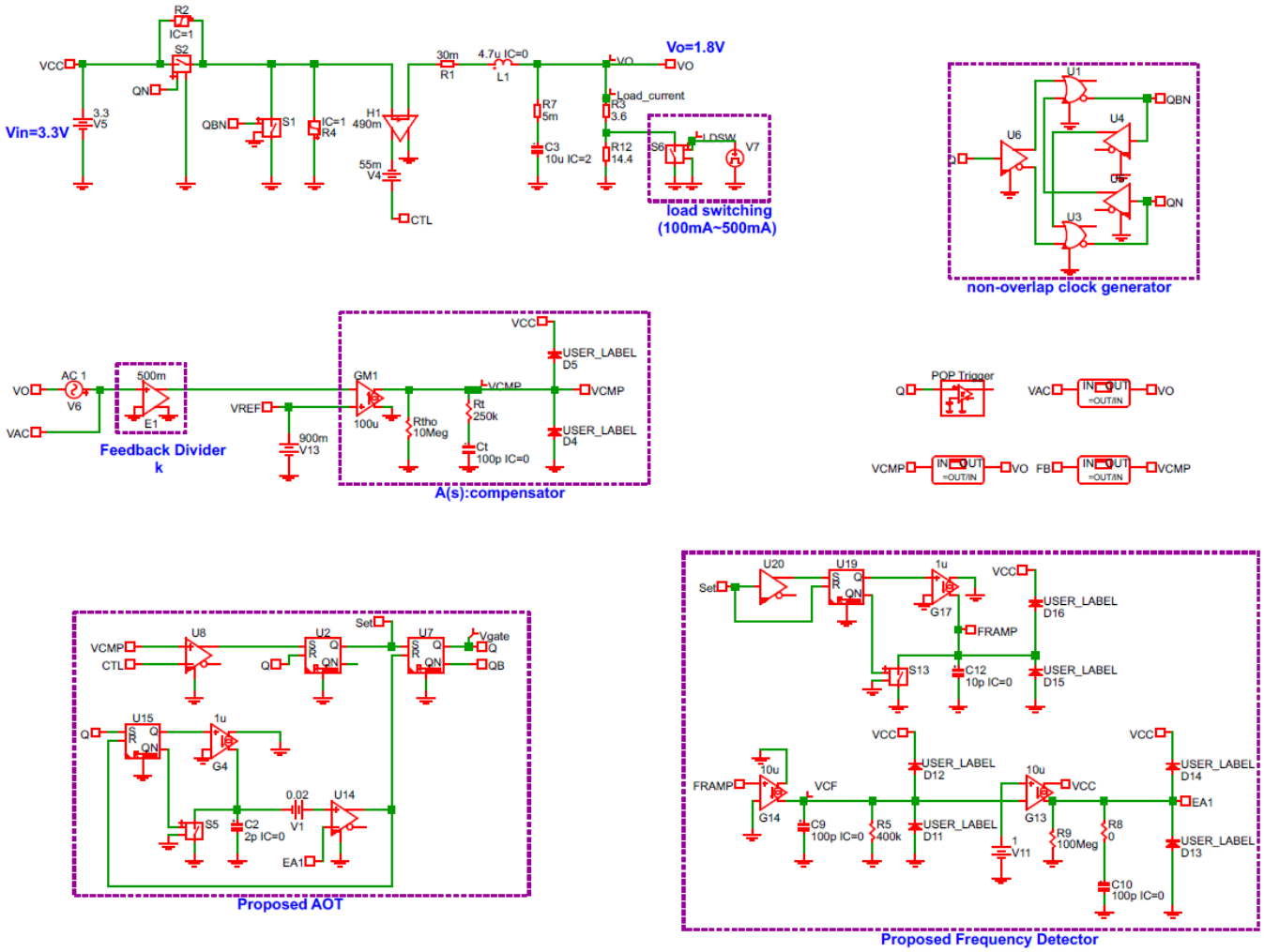


Figure 16. Schematic of proposed control scheme.

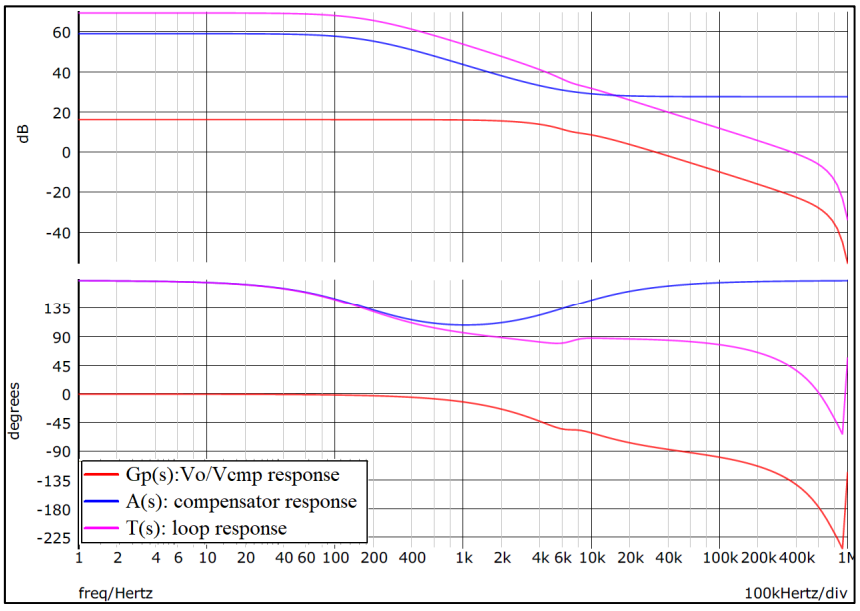


Figure 17. Bode diagrams with SIMPLIS.

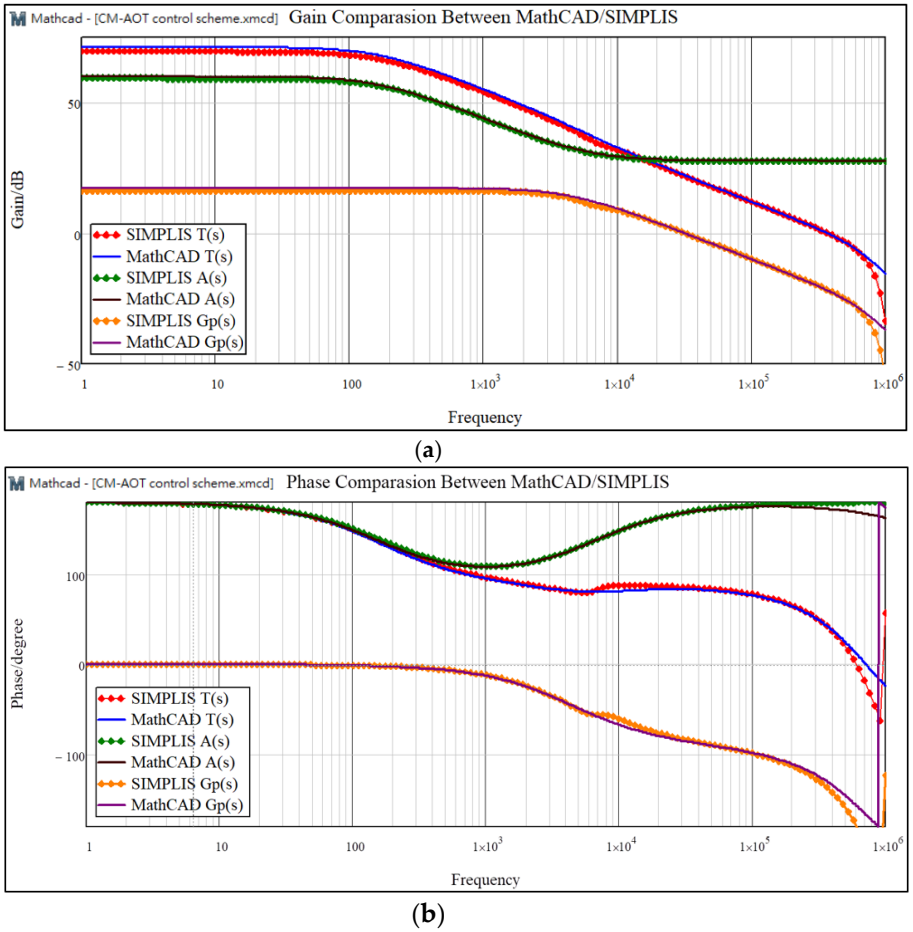


Figure 18. (**a**) MathCAD/SIMPLIS gain response comparison. (**b**) MathCAD/SIMPLIS phase response comparison.

MathCAD helps us quickly obtain system parameters through mathematical models, and SIMPLIS verifies these design parameters in circuits. By comparing the two results, we confirm again that although MathCAD can help us obtain the design parameters quickly, it is challenging to represent the actual circuit behavior. As mentioned earlier, an accurate mathematical model is difficult to obtain. Therefore, we suggest verifying the circuit behavior with SIMPLIS first. Then, to modify the designed parameters appropriately, to approach the actual circuit behavior. Finally, the circuits can deliver to transistor-level simulation efficiently.

It is unwise to bypass SIMPLIS verification and directly deliver the design parameters to Cadence Virtuoso SPICE simulation. Since the switching converter is a circuit with both analog and digital parts, if the circuit is simulated directly with SPICE, the simulation time will be very long, which is inefficient. We can say that the advantage of SIMPLIS is to quickly determine the stability of the system. SPICE is the final step in the design phase before delivering the layout. Therefore, MathCAD and SIMPLIS must design and verify the circuit with each other.

The design of a power converter is a tedious and time-consuming process. Especially when considering the circuit stability, we should pay attention to AC analysis and transient response. Besides MathCAD and SIMPLIS, many computer-aided design (CAD) software platforms can also help designers design the compensator for stability issues, such as LTspice and LTpowerCAD.

5.3. Transient Performance

The load transient response is shown in Figure 19. In this paper, the step transition of load current is between 0.1 A and 0.5 A. The test condition is described as below: under 3.3 V input voltage, the output voltage is 1.8 V. The recovery time is defined as the output voltage recovered to within 1% of the expected voltage of 1.8 V during load transition.

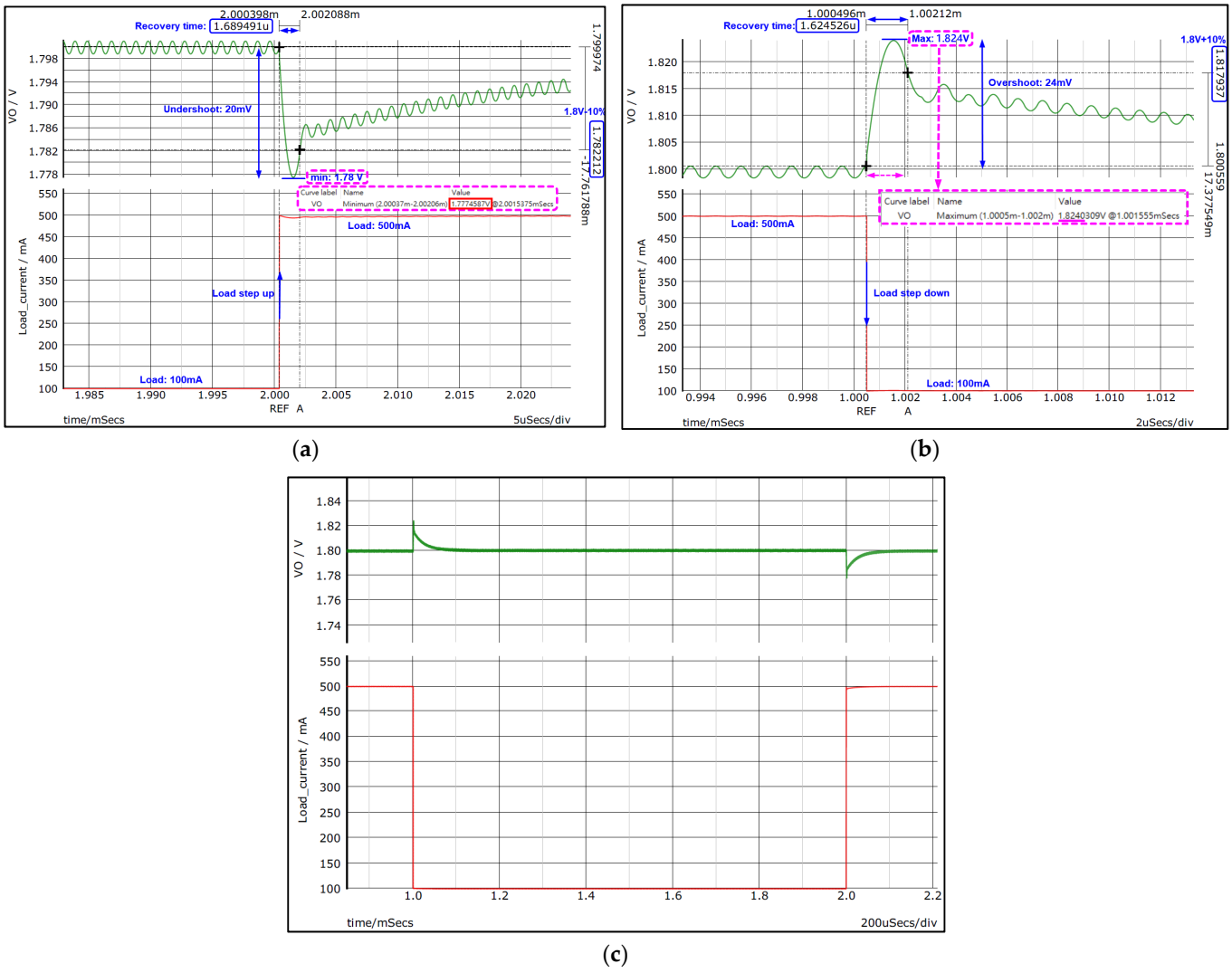


Figure 19. (**a**) Load current step-up. (**b**) Load current step-down. (**c**) Load current transition between 100 mA–500 mA.

From the simulation results in Figure 19, the step-up and step-down load transition recovery times are 1.69 µs and 1.62 µs, respectively. In other words, the recovery time is less than 2 µs for the proposed converter. Moreover, the overshoot and undershoot voltages are measured as 24 mV and 20 mV, respectively; all within 25 mV.

At a 3.0–3.6 V input voltage, 500 mA load current, and 1.0–2.5 V output voltage, the electrical performance of the proposed converter is shown in Figure 20. The maximum ripple voltage can be measured as 2.24 mV at a 3.6 V input voltage and 2.5 V output voltage.

5.4. Load Regulation/Line Regulation

Load/Line regulation is an important specification for a power converter system. The load regulation is defined in Equation (5). In general, the load regulation should be as small as possible. In order to measure the load regulation, the test conditions of the load regulation are as follows: 3.3 V input voltage, 1.8 V output voltage, and a load current from

0.1 A to 0.5 A. As shown in Figure 21, the load regulation can be calculated as −0.03% by Equation (5).

$$\text{Load Regulation} = \frac{V_{o\_\text{min}\_load} - V_{o\_\text{max}\_load}}{V_{o\_\text{normal}\_\text{load}}} \cdot 100\% \quad (5)$$

where $V_{o\_\text{max}\_load}$ is the voltage at maximum load and $V_{o\_\text{min}\_load}$ is the voltage at minimum load. $V_{o\_\text{normal}\_\text{load}}$ is the voltage at the typical load.

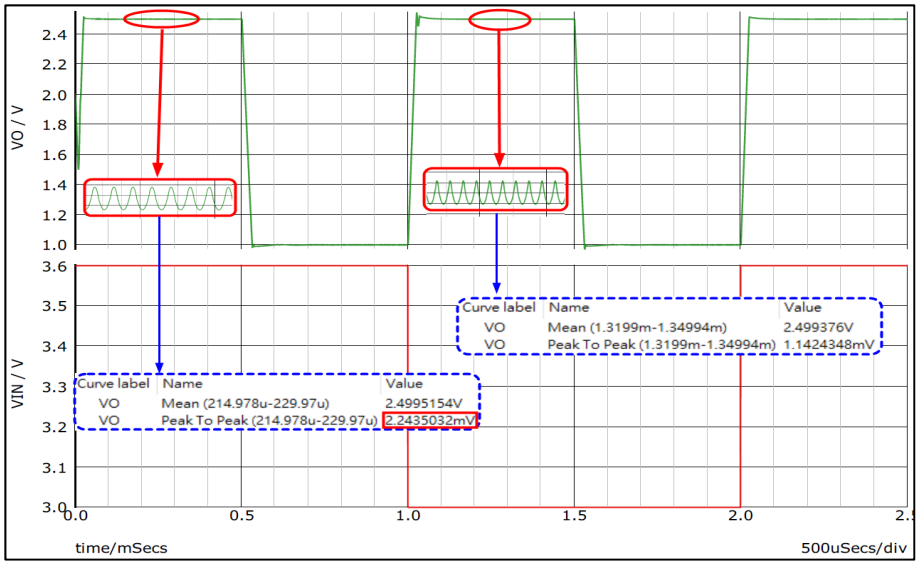


Figure 20. Electrical performance of the proposed converter.

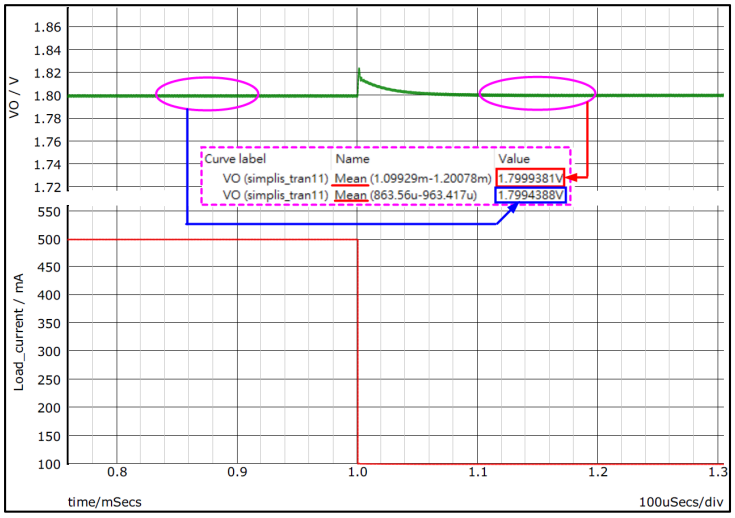


Figure 21. Electrical performance of the proposed converter.

The line regulation is defined as Equation (6). Similarly to the load regulation, the line regulation should be as small as possible. Unfortunately, the line regulation cannot be presented in this system-level simulation. The calculation result is close to 0.

$$\text{Line Regulation} = \frac{\Delta V_o}{\Delta V_{in}} \cdot 100\% \quad (6)$$

where ΔV_{in} is the change of the input voltage, ΔV_o is the change of the output voltage.

5.5. Switching Frquency Regulation

By using the proposed constant frequency technique, the converter has good switching frequency regulation. For example, with a 3.3 V input voltage and 500 mA load current, Figure 22 shows the switching frequency variation for the deferent outputs. As been seen from the results in Figure 22, the frequency variation is smaller than 1%.

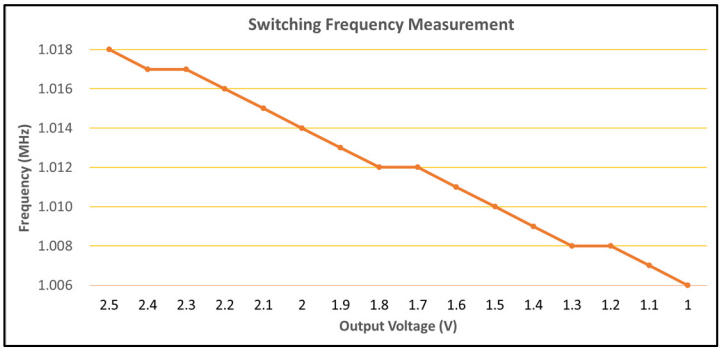


Figure 22. Switching frequency variation for deferent outputs.

Therefore, the switching frequency can keep almost constant for the different outputs. The constant frequency technique can be applied to the buck converters and effectively control the switching frequency. A comparison between the constant frequency technique and non-constant frequency technique is shown in Figure 23. The constant switching frequency can resolve the EMI issue in applications.

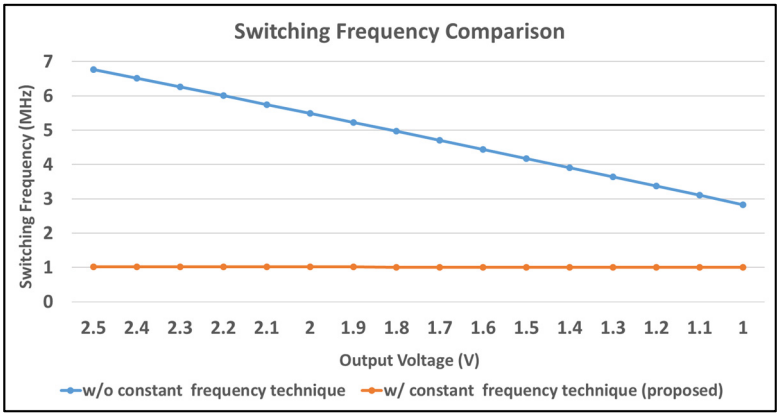


Figure 23. Switching frequency comparison.

5.6. Performance List

The performance of the proposed converter is summarized in Table 2. For a 3.0–3.6 V input voltage and 1.8 V output voltage, the recovery time is smaller than 2 µs for a 100 mA~500 mA load current transition. Moreover, by using the proposed constant frequency technique, the switching frequency is well controlled. Finally, performance comparisons with reported converters are listed in Table 3. From Table 3, there is no significant difference in switching frequency constancy between PLL architectures and the proposed architecture.

Table 2. Performance Summary.

Parameter	Conditions	Min.	Typ.	Max.	Unit
Input voltage		3.0		3.6	V
Output voltage		1.0		2.5	V
Output ripple	Vin = 3.6 V, Vo = 2.5 V			2.24	mV
Load current		100		500	mA
Inductor	DCR *: 30 mΩ		4.7		μH
Output capacitor	ESR: 5 mΩ		10		μF
Switching frequency	Vin = 3.0~3.6 V Vo = 1.0~2.5 V		1		MHz
Recovery time (step-up)	Vo = 1.8 V Load: 100 mA to 500 mA		1.69		μs
Recovery time (step-down)	Vo = 1.8 V Load: 500 mA to 100 mA		1.62		μs
Overshoot voltage	Vo = 1.8 V		24		mV
Undershoot voltage	Vo = 1.8 V		20		mV

* DCR: the DC resistance of the inductor.

Table 3. Performance Comparisons with Reported Converters.

References	2015 [22]	2020 [31]	2021 [7]	This Work
Results	measurement	simulation	measurement	simulation
Control scheme	Hysteretic Window (PLL based)	AOT	Hysteretic PLL	AOT
Process (μm)	0.35	0.18	0.35	0.18 **
Input voltage (V)	2.7–4.2	3.3–5.0	3.3–3.6	3.0–3.6
Output voltage (V)	1.2	1.8	0.9–2.5	1.0–2.5
Inductor (μH)	2.2	1.5	4.7	4.7
Output Capacitor (μF)	10	20	10	10
Switching Frequency(MHz)	1	1	1	1
Max. Load current(mA)	700	2000	600	500
Load current step(mA)	300	800	400	400
Undershoot/Overshoot(mV)	48/30	13/14	30/60	20/24
Recovery time(μs) (step up /step down)	3/5	6/2	2.6/2.2	1.69/1.62
Switching Frequency Variation	<1%	NA	<1%	<1%

** This work is system level simulation with SIMPLIS.

6. Conclusions

This paper presents a novel constant frequency technique and illustrates the concept and implementation of the proposed control scheme in detail. Modeling was derived and verified by MathCAD and SIMPLIS. The proposed frequency detector is designed to detect and lock the switching frequency, rather than using PLL. Compared with a control scheme based on PLL, the proposed method is easy to implement and compatible with the existing schemes. The simulation results show that the switching frequency variation is less than 1% for a 1.0–2.5 V output. The recovery times for the step-up and step-down load transition are 1.69 μs and 1.62 μs, respectively. This novel constant frequency technique can resolve the EMI issue for various applications in converters.

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References

1. Chen, J.-J.; Lu, M.-X.; Wu, T.-H.; Hwang, Y.-S. Sub-1-V Fast-Response Hysteresis-Controlled CMOS Buck Converter Using Adaptive Ramp Techniques. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2013**, *21*, 1608–1618. [CrossRef]
2. Chen, J.-J.; Hwang, Y.-S.; Chen, J.-H.; Ku, Y.-T.; Yu, C.-C. A New Fast-Response Current-Mode Buck Converter with Improved I^2-Controlled Techniques. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2018**, *26*, 903–911. [CrossRef]
3. Hwang, Y.S.; Chen, J.J.; Ku, Y.T.; Yang, J.Y. An Improved Optimum-Damping Current-Mode Buck Converter with Fast-Transient Response and Small-Transient Voltage using New Current Sensing Circuits. *IEEE Trans. Ind. Electron.* **2020**, *68*, 9505–9514. [CrossRef]
4. Kim, M.; Kim, J. A PWM/PFM Dual-Mode DC-DC Buck Converter with Load-Dependent Efficiency-Controllable Scheme for Multi-Purpose IoT Applications. *Energies* **2021**, *14*, 960. [CrossRef]
5. Nguyen, M.-K. Power Converters in Power Electronics: Current Research Trends. *Electronics* **2020**, *9*, 654. [CrossRef]
6. Huang, Q.; Zhan, C.; Burm, J. A 30-MHz Voltage-Mode Buck Converter Using Delay-Line-Based PWM Control. *IEEE Trans. Circuits Syst. II Express Briefs* **2017**, *65*, 1659–1663. [CrossRef]
7. Chen, J.-J.; Hwang, Y.-S.; Ku, Y.-T.; Li, Y.-H.; Chen, J.-A. A Current-Mode-Hysteretic Buck Converter with Constant-Frequency-Controlled and New Active-Current-Sensing Techniques. *IEEE Trans. Power Electron.* **2021**, *36*, 3126–3134. [CrossRef]
8. Yan, Y.; Lee, F.C.; Mattavelli, P.; Liu, P.-H. I^2 Average Current Mode Control for Switching Converters. *IEEE Trans. Power Electron.* **2014**, *29*, 2027–2036. [CrossRef]
9. Redl, R.; Sokal, N.O. Current-mode control, five different types, used with the three basic classes of power converters: Small-signal AC and large-signal DC characterization, stability requirements, and implementation of practical circuits. In Proceedings of the 1985 IEEE Power Electronics Specialists Conference, Toulouse, France, 24–28 June 1985; pp. 771–785.
10. Li, J. Current-Mode Control: Modeling and its Digital Application. Ph.D. Dissertation, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, 2009.
11. Zhong, S.; Shen, Z. A Hybrid Constant On-Time Mode for Buck Circuits. *Electronics* **2021**, *10*, 930. [CrossRef]
12. Lin, Y.-C.; Chen, C.-J.; Chen, D.; Wang, B. A Ripple-Based Constant On-Time Control With Virtual Inductor Current and Offset Cancellation for DC Power Converters. *IEEE Trans. Power Electron.* **2012**, *27*, 4301–4310. [CrossRef]
13. Nien, C.-F.; Chen, D.; Hsiao, S.-F.; Kong, L.; Chen, C.-J.; Chan, W.-H.; Lin, Y.-L. A Novel Adaptive Quasi-Constant On-Time Current-Mode Buck Converter. *IEEE Trans. Power Electron.* **2017**, *32*, 8124–8133. [CrossRef]
14. Lin, H.-C.; Fung, B.-C.; Chang, T.-Y. A current mode adaptive on-time control scheme for fast transient DC-DC converters. In Proceedings of the 2008 IEEE International Symposium on Circuits and Systems, Seattle, WA, USA, 18–21 May 2008; pp. 2602–2605.
15. Zhen, S.; Zhou, S.; Zeng, L.; Yang, M.; Ming, X.; Luo, P.; Zhang, B. Variable on time controlled buck converter for DVS applications. In Proceedings of the IECON 2017—43rd Annual Conference of the IEEE Industrial Electronics Society, Beijing, China, 29 October–1 November 2017; pp. 1642–1648.
16. Bari, S.; Li, Q.; Lee, F.C. Fast adaptive on time control for transient performance improvement. In Proceedings of the 2015 IEEE Applied Power Electronics Conference and Exposition (APEC, Charlotte, NC, USA, 15–19 March 2015; pp. 397–403.
17. Liu, P.-J.; Kuo, M.-H. Adaptive On-Time Buck Converter with Wave Tracking Reference Control for Output Regulation Accuracy. *Energies* **2021**, *14*, 3809. [CrossRef]
18. Bari, S.; Li, Q.; Lee, F.C. A New Fast Adaptive On-Time Control for Transient Response Improvement in Constant On-Time Control. *IEEE Trans. Power Electron.* **2017**, *33*, 2680–2689. [CrossRef]
19. Wong, L.; Man, T. Adaptive On-Time Converters. *IEEE Ind. Electron. Mag.* **2010**, *4*, 28–35. [CrossRef]
20. Sun, J. Characterization and performance comparison of ripple-based control for voltage regulator modules. *IEEE Trans. Power Electron.* **2006**, *21*, 346–353. [CrossRef]
21. Zhou, X.; Donati, M.; Amoroso, L.; Lee, F. Improved light-load efficiency for synchronous rectifier voltage regulator module. *IEEE Trans. Power Electron.* **2000**, *15*, 826–834. [CrossRef]
22. Hu, K.-Y.; Lin, S.-M.; Tsai, C.-H. A Fixed-Frequency Quasi-V^2 Hysteretic Buck Converter with PLL-Based Two-Stage Adaptive Window Control. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2015**, *62*, 2565–2573. [CrossRef]
23. Chen, J.-J. An active current-sensing constant-frequency HCC buck converter using phase-frequency-locked techniques. *IEEE Trans. Ultrason. Ferroelectr. Freq. Control.* **2008**, *55*, 761–769. [CrossRef]
24. Chou, H.-H.; Chen, H.-L.; Fan, Y.-H.; Wang, S.-F. Adaptive On-Time Control Buck Converter with a Novel Virtual Inductor Current Circuit. *Electronics* **2021**, *10*, 2143. [CrossRef]
25. Tsai, C.-H.; Chen, B.-M.; Li, H.-L. Switching Frequency Stabilization Techniques for Adaptive On-Time Controlled Buck Converter With Adaptive Voltage Positioning Mechanism. *IEEE Trans. Power Electron.* **2016**, *31*, 443–451. [CrossRef]
26. Tsai, C.-H.; Lin, S.-M.; Huang, C.-S. A fast-transient quasi-V^2 switching buck regulator using AOT control with a load current correction (LCC) technique. *IEEE Trans. Power Electron.* **2012**, *28*, 3949–3957. [CrossRef]

27. Li, J.; Lee, F.C. New modeling approach and equivalent circuit representation for current-mode control. *IEEE Trans. Power Electron.* **2010**, *25*, 1218–1230.
28. Enrique, J.M.; Barragán, A.J.; Durán, E.; Andújar, J.M.; Gómez, J.M.E.; Piña, A.J.B.; Aranda, E.D.; Márquez, J.M.A. Theoretical Assessment of DC/DC Power Converters' Basic Topologies. A Common Static Model. *Appl. Sci.* **2017**, *8*, 19. [CrossRef]
29. Suntio, T. Dynamic Modeling and Analysis of PCM-Controlled DCM-Operating Buck Converters—A Reexamination. *Energies* **2018**, *11*, 1267. [CrossRef]
30. Ridley, R.B. An Accurate and Practical Small-Signal Model for Current-Mode Control. Available online: www.ridleyengineering.com (accessed on 24 July 2021).
31. Jiang, C.; Chai, C.; Han, C.; Yang, Y. A high performance adaptive on-time controlled valley-current-mode DC–DC buck converter. *J. Semicond.* **2020**, in press. [CrossRef]