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Fault-Ride-Through Approach for Grid-Tied Smart Transformers without Local Energy Storage

Justino Rodrigues [1,*], Carlos Moreira [1,2] and João Peças Lopes [2]

[1] CPES—INESC TEC, FEUP Campus, Rua Dr. Roberto Frias, 4200-465 Porto, Portugal; carlos.moreira@inesctec.pt
[2] DEEC—Faculty of Engineering of the University of Porto, Rua Dr. Roberto Frias, 4200-465 Porto, Portugal; jpl@fe.up.pt
* Correspondence: justino.m.rodrigues@inesctec.pt

Abstract: The Smart Transformer (ST) is being envisioned as the possible backbone of future distribution grids given the enhanced controllability it provides. Moreover, the ST offers DC-link connectivity, making it an attractive solution for the deployment of hybrid AC/DC distribution grids which offer important advantages for the deployment of Renewable Energy Sources, Energy Storage Systems (ESSs) and Electric Vehicles. However, compared to traditional low-frequency magnetic transformers, the ST is inherently more vulnerable to fault disturbances which may force the ST to disconnect in order to protect its power electronic converters, posing important challenges to the hybrid AC/DC grid connected to it. This paper proposes a Fault-Ride-Through (FRT) strategy suited for grid-tied ST with no locally available ESS, which exploits a dump-load and the sensitivity of the hybrid AC/DC distribution grid's power to voltage and frequency to provide enhanced control to the ST in order to handle AC-side voltage sags. The proposed FRT strategy can exploit all the hybrid AC/DC distribution grid (including the MV DC sub-network) and existing controllable DER resources, providing FRT against balanced and unbalanced faults in the upstream AC grid. The proposed strategy is demonstrated in this paper through computational simulation.

Keywords: balanced faults; fault ride through; hybrid AC/DC network; smart transformer; unbalanced faults

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1. Introduction

The expected increase of Distributed Energy Resources (DER) in distribution grids, such as Renewable Energy Sources (RES), Electric Vehicles (EV) and distributed Energy Storage Systems (ESS), is highlighting new challenges regarding operation and control of electric power systems [1–5]. In order to face this new paradigm, advanced concepts aimed to improve controllability and observability of distribution grids have been proposed, such as the microgrid, being regarded as the building block of the broader smart-grids concept [6–11].

AC microgrids have constituted the initial approaches to tackle those challenges [7,8,12], but advancements in power electronics have motivated an increasing interest in DC distribution microgrids, presenting advantages for the integration of resources which are DC by nature such as PV generation, ESS and EV charging [13,14]. The possibility of employing both AC and DC grids for DER integration has attracted attention for the Smart-Transformer (ST) concept as a possible technical solution to improve the controllability of future distribution grids [15–17]. The ST is a three-stage Solid-State Transformer (SST) adapted for advanced monitoring and control of distribution grids [16,17].

However, comparatively to traditional low-frequency magnetic transformers, the ST inherently presents stringent challenges regarding particular operation conditions involving overcurrents—namely overloads and short-circuits—since it is based on power

electronic converters. Fault-Ride-Through (FRT) capabilities in ST are of upmost importance not only for the physical integrity of the ST itself but also for the continuity of supply of the hybrid AC/DC distribution grid derived from the ST itself. The development of FRT capabilities for electronic power converters, especially for distributed generation, has been extensively addressed in the literature [18–22]. The incorporation of FRT capabilities in Medium-Voltage (MV) inverters is also an important research topic [22–25]. Nevertheless, the inclusion of FRT capabilities in ST remains scarcely addressed in the literature, there being a single work on the subject to date, to the best of the authors' knowledge [26].

In [26], FRT strategies are proposed for grid-forming ST and for grid-tied ST without local energy storage integrated in the ST' DC stage. Regarding grid-tied ST, the FRT strategy proposed in [26] aims to mitigate the adverse impacts in the hybrid AC/DC grid derived from the ST, by exploiting the active power-voltage sensitivity of LV DC and LV AC sub-networks in order to support net load and net generation balancing in the hybrid AC/DC distribution grid during voltage sags in the upstream MV AC grid. The ST's MV inverter will increase its injected/absorbed current in order to preserve the power balance in the hybrid AC/DC distribution grid. However, when ST's MV inverter reaches its current limits, the FRT strategy is activated in order to preserve the power balance, by reducing/increasing the load/generation in the ST's hybrid AC/DC distribution grid when it is importing active power, or by increasing/reducing the load/generation in the ST's hybrid AC/DC distribution grid when it is exporting active power.

Simultaneously, the FRT strategy proposed in [26] aims to minimize its impact on the voltage levels in the hybrid AC/DC grid (when current levels in the MV AC inverter saturate during a voltage sag in the MV AC grid) to the strictly necessary to ensure the aimed power balancing in the hybrid AC/DC grid. Thus, besides ensuring power balance in the hybrid AC/DC grid, the FRT strategy proposed in [26] simultaneously improves the voltage levels in the hybrid AC/DC network, circumventing as much as possible the absence of local energy storage capacity associated to the grid-tied ST. However, the methodology proposed in [26] has the following limitations:

- It cannot exploit the active power-voltage sensitivity of an MV DC sub-network constituting the hybrid AC/DC distribution grid. The proposed FRT strategy may be less effective if most of the load/generation is located in a MV DC sub-network.
- It cannot exploit power-frequency sensitive DER located in the LV AC sub-network constituting the hybrid AC/DC distribution grid [27]. This feature would enable the regulation of the net active power in the LV AC sub-network with minimal impact on non-controllable resources.
- It is not capable of exploiting complementary solutions (dump loads, controllable PV generation or ESS available in the hybrid AC/DC grid to further support the power balancing phenomena and voltage control mechanisms in the hybrid distribution grid in the moments subsequent to the fault.
- It is evaluated only for balanced three-phase voltage sags in the upstream MV AC grid.

This paper proposes an improved FRT control strategy for grid-tied ST with no local energy storage capacity suitable to bridge the aforementioned limitations. Following a MV AC grid voltage sag, to foster net load balance downstream from the ST, the proposed FRT control strategy relies on the exploitation of active power-frequency sensitivity in the LV AC sub-network, on the exploitation of active power-voltage sensitivity in LV DC and AC sub-networks by adjusting the transformation ratio of the ST's isolated DC-DC converter, and on the exploitation of active power-voltage sensitivity in MV DC sub-network by adjusting an electronic resistor added in series with the MV DC sub-network specifically for this purpose. The main purpose of the electronic resistor proposed to be integrated in the MV DC sub-network is to provide an additional degree of freedom regarding voltage control in the hybrid AC/DC grid during grid faults in the ST's upstream AC grid. In order to support net generation balance downstream from the ST following an AC MV grid fault, the proposed FRT control strategy relies on a dump-load incorporated in the ST specifically for this purpose. Under the proposed FRT strategy, controllable PV generation

and ESS available in the ST's hybrid AC/DC distribution grid and sensitive to grid voltage and/or frequency can also be exploited to minimize the excess net load/generation in the ST's hybrid AC/DC distribution grid.

The FRT approach proposed in this paper is evaluated for voltage sags resulting from balanced three-phase faults and unbalanced phase–phase and phase-ground faults in the upstream AC grid. An electronically controlled supercapacitor bank is connected to the ST's LV DC bus, aiming to mitigate power oscillations in the ST's DC buses that may result from the unbalanced voltage sags in the upstream AC grid. The effectiveness of the proposed FRT strategy, in enabling the ST to ride through voltage sags in the upstream AC grid while mitigating adverse impacts affecting the ST's hybrid distribution grid, is demonstrated in this paper through computational simulation.

2. Computational Models

The effectiveness of the approaches suggested in this paper is studied and demonstrated using a test network modeled in a computational simulation environment. An overview of the test network is depicted in Figure 1, comprising a hybrid AC/DC distribution grid connected to an upstream MV AC grid through a grid-tied ST. A MV cable models the equivalent impedance in the MV AC grid between the ST and the HV AC grid. The MV AC grid is connected to a High-Voltage (HV) grid, modeled using a Thevenin equivalent comprising an ideal three-phase voltage source in series with an equivalent impedance. This simplification is adopted because frequency variations that may result from grid faults in the power system are not relevant for the subjects under study in this paper. A DYn core type HV/MV transformer was considered to interface HV and MV AC grids, where a neutral earthing through an impedance was considered for the MV AC grid.

The models for the ST are presented and described in Section 2.1. The models for the ST's hybrid AC/DC distribution grid are presented and described in Section 2.2 (LV AC network) and Section 2.3 (MV and LV DC networks). The modeling of the controllable DER incorporated in the hybrid distribution network is described in Section 2.4.

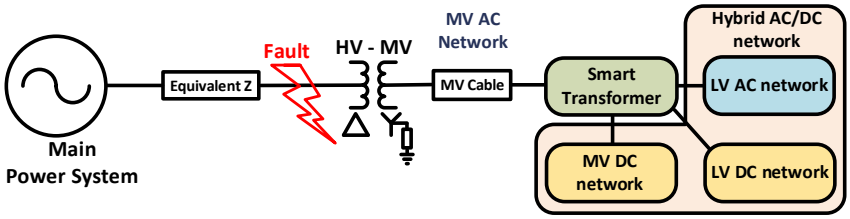

Figure 1. Overall structure of the complete computational model for the test network.

The simulation models were developed in MATLAB® /Simulink® environment. A switching frequency of 20 kHz is chosen for the ST's power converters since it is a realistic value for high power converters [16,28,29]. However, given the considerable computational burden implicit to a detailed computational model simulating power converters operating at such frequency, the Dynamic Average Modeling (DAM) technique proposed in [30] was adopted. The DAM technique uses the moving average operator at the switching frequency to eliminate the need of modeling detailed switching elements [30]. Thus, the detailed power converters can be represented by controllable voltage and current sources without compromising their main dynamic behavior, and the respective control signals can be discretized at the switching frequency by choosing a simulation time step of 50 µs. As a result, the switching effects from the computational model are neglected while obtaining a better compromise between computational burden and model accuracy.

2.1. Smart Transformer

This section aims to summarize the main modeling approach for the ST components. The proposed control options and mitigation solutions regarding the specific case of FRT following MV AC grid voltage sags are described in Section 3. The main modules considered in the modeled three-stage ST are depicted in Figure 2 and described in the following subsections.

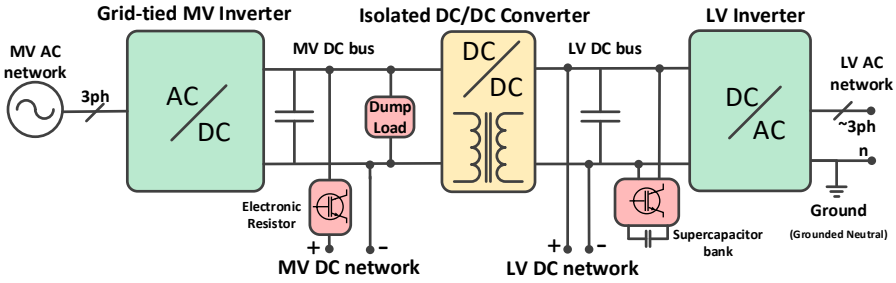

Figure 2. Overall structure of the computational model developed for the Smart Transformer.

2.1.1. Medium Voltage Inverter

The model of ST's MV inverter is illustrated in Figure 3. The power stage of the MV inverter (AC/DC Inverter) and the coupling LC filter are modeled following the assumptions adopted in [27] for the grid-tied ST, where the DAM technique is also adopted. No neutral connection was considered for the MV inverter.

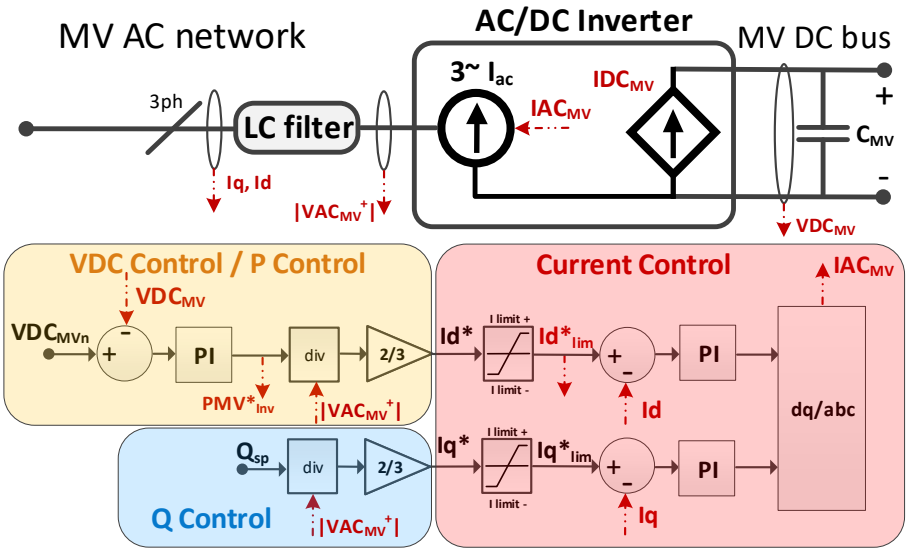

Figure 3. ST's Medium Voltage Inverter and respective control structure.

The active power flow in the MV inverter is modeled according to Equation (1), which determines the power transfer between the coupling LC filter and the MV DC bus. IDC_{MV} is the DC current injected in the MV DC bus, PMV_{Inv} and VDC_{MV} are the active power and the DC voltage in the connection with the MV DC bus, $v_{ab_{MV}}$, $v_{bc_{MV}}$ and $v_{ca_{MV}}$ are the phase–phase MV AC voltages (between phases *a*, *b* and *c*) in the MV inverter, and $i_{a_{MV}}$, $i_{b_{MV}}$ and $i_{c_{MV}}$ are the AC currents in the MV inverter's phases *a*, *b* and *c* (IAC_{MV}). VDC_{MV} is determined according to Equation (2), where C_{MV} is the capacitance of the MV DC bus, and $IDAB_{MV}$, IDC_{MVg} and I_{DL} are the currents exchanged between the MV DC bus and the isolated DC/DC converter, the MV DC grid and the dump-load, respectively.

$$IDC_{MV} = \frac{PMV_{Inv}}{VDC_{MV}} = \frac{1}{VDC_{MV}}[v_{ab_{MV}} - v_{ca_{MV}}, v_{bc_{MV}} - v_{ab_{MV}}, v_{ca_{MV}} - v_{bc_{MV}}] \cdot \begin{bmatrix} i_{a_{MV}} \\ i_{b_{MV}} \\ i_{c_{MV}} \end{bmatrix} \quad (1)$$

$$VDC_{MV} = \frac{1}{C_{MV}} \int (IDC_{MV} + IDAB_{MV} + IDC_{MV_g} + I_{DL})dt \quad (2)$$

Regarding the control structure of the MV inverter, VDC Control / P Control regulates VDC_{MV} by generating the reference for the active current (Id^*) to be followed by the Current Control, which then establishes the active current in the MV inverter. The reference for the reactive current generated by Q Control is set to zero ($Q_{sp} = 0$) given that voltage/VAr support is not addressed in this paper. Only the the positive-sequence component of the current is considered for the controller of the MV inverter. As it will be later discussed in Section 3, the control of the negative-sequence component of the current by the MV inverter, in comparison to the use of a supercapacitor bank, does not represent the most advantageous approach to mitigate power oscillations that may arise in the ST's DC buses as a result of unbalanced voltage sags in the MV AC grid. The zero sequence component of the current does not occur since no neutral connection exists in the MV inverter.

2.1.2. Isolated DC/DC Converter

The isolated DC/DC converter was modeled according to the approach presented in [31], following the considerations described in [26]. The resulting model is depicted in Figure 4 and expressed in Equations (3) and (4), where VDC_{MV} and VDC_{LV} are the voltages in the HFT, VDC_{MVn} and VDC_{LVn} are the nominal voltages for the ST's MV and LV DC buses respectively, $IDAB_{MV}$ and $IDAB_{LV}$ are the currents in the HFT's primary and secondary stages respectively, and d_{FRT} is the duty-cycle adjustment signal.

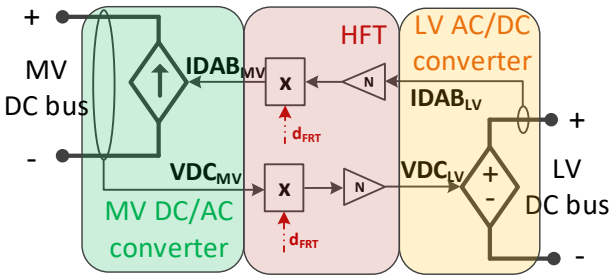

Figure 4. DC-DC converter stage model.

$$VDC_{MV}IDAB_{MV} = VDC_{LV}IDAB_{LV} \iff \frac{VDC_{LV}}{d_{FRT}N}IDAB_{MV} = VDC_{LV}\frac{IDAB_{MV}}{d_{FRT}N} \quad (3)$$

$$N = \frac{VDC_{LVn}}{VDC_{MVn}} \quad (4)$$

2.1.3. Electronic Resistor

The contribution of the MV DC grid for the provision of FRT is important since it may concentrate a large share of the total load of the hybrid distribution network. While it is possible to modulate the voltage levels in the ST's LV DC bus in order to directly exploit the power-voltage sensitivity in the LV DC grid [26], the same approach is not suitable for the ST's MV DC bus in practical terms. Since the MV AC voltage in the ST's MV inverter is imposed by the upstream MV AC grid, allowing the FRT control to reduce the MV DC bus voltage can in practice originate passive rectification in the ST's MV inverter. Passive rectification is an uncontrolled operation mode of the ST MV inverter which can occur when the voltage in the MV DC bus is not enough to block the intrinsic diodes existing in the electronic switches, originating uncontrolled currents capable to damage the ST's MV inverter.

The purpose of the electronic resistor proposed in this work is to provide an additional degree of freedom to control the MC DC grid voltage aiming to support the provision of FRT during AC grid voltage sags without reducing the MV DC bus voltage. By enabling the introduction of a series voltage drop between the MV DC bus and the MV DC grid, the electronic resistor enables the effective reduction of MV DC grid voltage, and thus, the exploitation of its power-voltage sensitivity. A non-isolated bidirectional MV DC/DC converter could be used, but in practice it would represent a more expensive, complex and less energy efficient (in steady-state operation) solution. Instead, the proposed electronic resistor consists of a simpler device inserted in series with the + MV DC line, as depicted in Figure 2. To the best of the authors knowledge, no electronic resistor specified for this purpose was found in the literature. Nevertheless, taking advantage of the main principles adopted in the design of solid-state Fault Current Limiters (FCL) [32] and in the design of HVDC breakers [33], the electronic resistor was conceived and proposed to be integrated in this specific application. The resulting device is depicted in Figure 5.

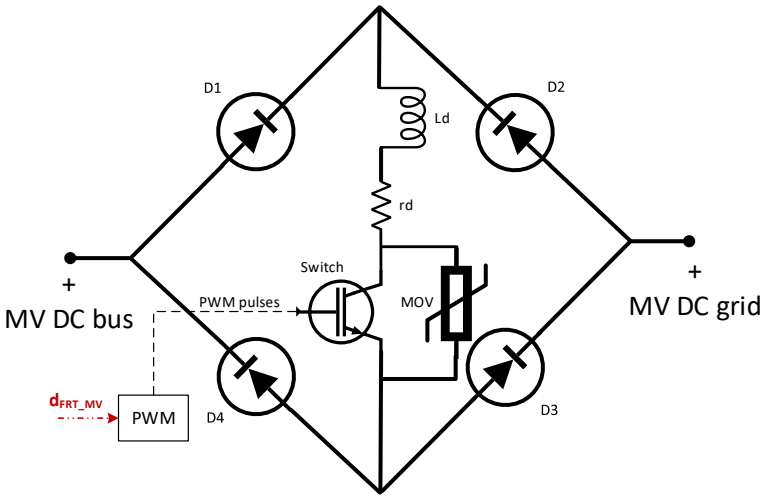

Figure 5. Detailed diagram of the electronic resistor.

The FCL proposed in [32] provides a simple structure based on a four-diode bridge, a single electronic switching device, an inductor (L_d and r_d model the inductance and resistance of the inductor) and a resistor (used for current limiting). The following changes were made to the FCL device described in [32] in order to obtain an electronic resistor device suited to the purpose intended in this paper. Instead of being operated in on/off operation (no fault/fault conditions), the electronic switch is operated in switching mode at the given switching frequency (f_s), commanded by a PWM controlled by the duty-cycle signal d_{FRT_MV} generated by the FRT control described in Section 3. To control the MV DC grid voltage from near zero to VDC_{MVn}, the current limiting resistor is replaced by a Metal-oxide varistor (MOV), whose impedance is much higher than the equivalent impedance of the MV DC grid for a MOV voltage below its clamping voltage, but much lower that the equivalent impedance of the MV DC grid for a MOV voltage above its clamping voltage. The inductance is dimensioned considering f_s in order to reduce the current ripple to acceptable magnitudes. The MOV ensures a path for the inductor's current during electronic switch's off-state (t_{off}), protecting the switching device from voltage surges originated by the inductor. The effectiveness of a MOV in this role is shown in [33].

In comparison with the high voltage values of the MV DC bus, the forward voltage drop in the four-diode bridge and in the electronic switch during its on-state (t_{on}) are much smaller, to the point of being negligible. Thus, the voltage drop in the electronic resistor can be approximated by Equation (5), where V_{EZ} is the voltage drop in the electronic resistor, V_L the voltage drop in the inductor, V_{MOV} the voltage drop in the MOV, t_{on} is the on-state period of the electronic switch, and t_{off} is the off-state period of the electronic switch. t_{on}

and t_{off} are related to the switching period T_s and switching frequency f_s according to Equation (6).

$$\begin{cases} V_{EZ} = V_L; \quad t_{on} \\ V_{EZ} = -V_L + V_{MOV}; \quad t_{off} \end{cases} \tag{5}$$

$$t_{on} + t_{off} = T_s = \frac{1}{f_s} \tag{6}$$

A clamping voltage equal to VDC_{MVn} was considered for the MOV. Considering an inductor dimensioned to not allow a ripple current above 5% of the ST's nominal current, a relatively constant current will flow through the MOV during the off-state of the electronic switch, thus originating a voltage at the MOV's terminals approximately equal to VDC_{MVn}. A relatively constant current in the inductor also means a relatively constant voltage in the MV DC grid (VDC_{MVg}) during the switching interval T_s, assuming the impedance in the MV DC grid does not change significantly in that period. Given this, and considering that the voltage in the MV DC bus (VDC_{MV}) is kept close to VDC_{MVn}, the relationship between VDC_{MVg} and VDC_{MV} can be expressed by Equation (7), which originate Equations (8) and (9), where Z_{MVg} is the equivalent impedance of the MV DC grid (which depends on the connected loads and resources).

$$\begin{cases} V_{EZ} = V_L \Leftrightarrow V_L = VDC_{MV} - VDC_{MVg}; \quad t_{on} \\ V_{EZ} = -V_L + VDC_{MV} \Leftrightarrow V_L = VDC_{MVg}; \quad t_{off} \end{cases} \tag{7}$$

$$d_{FRT\_MV}(VDC_{MV} - VDC_{MVg}) = (1 - d_{FRT\_MV})VDC_{MVg}; \quad d_{FRT\_MV} = \tfrac{t_{on}}{T_s}; \tag{8}$$

$$VDC_{MVg} = d_{FRT\_MV} VDC_{MV}; \quad IDC_{MVg} = \frac{VDC_{MVg}}{Z_{MVg}} \tag{9}$$

Employing the DAM approach to the model depicted in Figure 5, the modulation mechanisms can be neglected without relevant impacts in the dynamics of the electronic resistor [30] since average voltage and current values are determined for each switching period. As a result, given Equation (9) and that input and output currents of the electronic resistor are equal to IDC_{MVg}, the electronic resistor can be modeled using controlled voltage and current sources as illustrated in Figure 6.

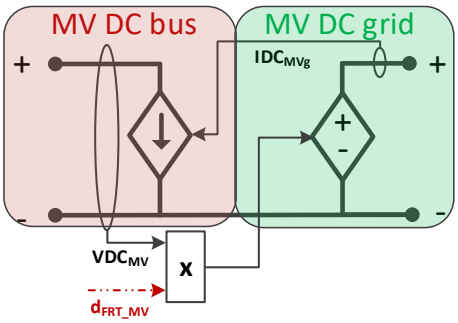

Figure 6. Computational model for the MV DC electronic resistor.

2.1.4. Dump Load

The purpose of the dump-load is to dissipate excessive net generation originated from the hybrid AC/DC network that cannot be delivered to the main power system through the ST's MV inverter. This may happen when the ST's MV inverter reaches its technical current limits, namely during fault disturbances in the upstream power system. The dump-load is connected to the ST's MV DC link and is controlled by the FRT Control described in detail in Section 3. The dump-load is modeled as illustrated in Figure 7. Given the DAM technique was adopted, the electronic converter controlling the power flow in the dump-load's resistor was modeled using a controlled current source.

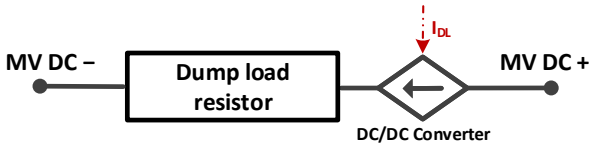

Figure 7. Computational model for the dump-load.

2.1.5. Supercapacitor Bank

The supercapacitor bank aims to mitigate power oscillations (and thus DC voltage oscillations) in the ST's DC buses which may result from the occurrence of unbalanced voltage sags in the MV AC grid. The justification for a supercapacitor bank for this purpose is explained in Section 3. The computational model developed for the supercapacitor bank is depicted in Figure 8. The modeling of the supercapacitor bank itself is neglected, based on two considerations. First, it is assumed that its internal dynamics is much faster than the dynamics of the power converter interfacing it with the LV DC bus. Second, as shown in Section 4.1, the energy storage and output power capacities required to address the aforementioned power oscillations can be met by a relatively small supercapacitor bank with a margin sufficiently high to neglect the modeling of any energy and power constraints affecting the supercapacitor bank. Given this, and based on the adopted DAM technique, the supercapacitor bank is modeled as a controlled current source, which represents its interface power converter.

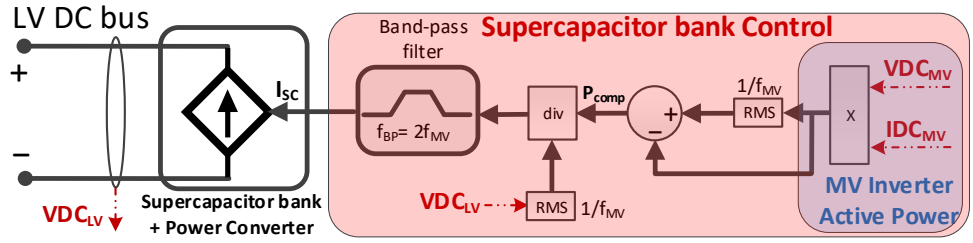

Figure 8. Computational model for the Supercapacitor bank.

The active power compensation delivered to the LV DC bus occurs through the current I_{SC}, obtained from Equation (10) in the Laplace s-domain. In Equation (10), a second-order band-pass filter captures the power oscillations resulting from the negative-sequence component present in the MV AC grid, using the error between the instantaneous active power in the ST's MV inverter (PMV) and the active power related to the positive-sequence component in the MV AC grid (PMV^{+}) given by the RMS of PMV over the time period of the fundamental frequency in the MV AC grid (f_{MV}).

$$I_{SC} = \frac{PMV^{+} - PMV}{VDC_{LV}} \frac{\sqrt{2}\omega_n s}{s^2 + \sqrt{2}\omega_n s + \omega_n^2}; \quad \omega_n = 4\pi f_{MV}; \quad PMV = VDC_{MV} IDC_{MV} \tag{10}$$

2.1.6. Low Voltage Inverter

The model of the ST's LV inverter, responsible to generate the LV AC network (grid-forming operation), is represented in Figure 9. The power stage of the MV inverter AC/DC Inverter) and the LC filter are modeled following the assumptions adopted in [27]. A grounded neutral regime is adopted for the LV AC network.

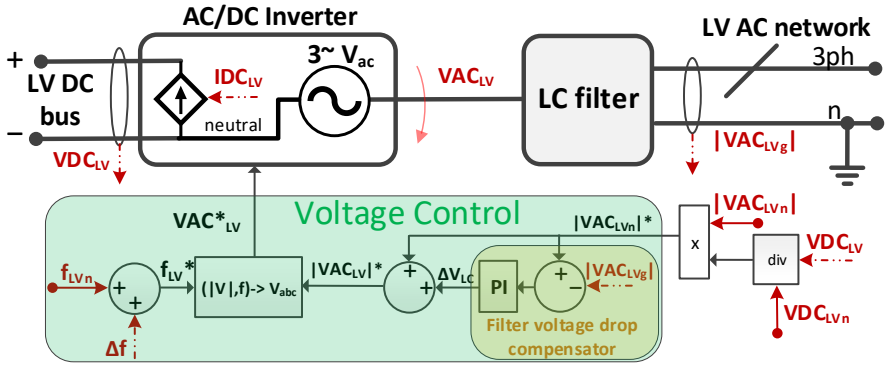

Figure 9. Block diagram of the ST's Low Voltage inverter.

The active power in the LV inverter is defined by Equation (11), where IDC_{LV} is the DC current exchanged with the LV DC bus, PLV_{Inv} is the active power in the LV inverter, VDC_{LV} is the LV DC bus voltage, $v_{an_{LV}}$, $v_{bn_{LV}}$ and $v_{cn_{LV}}$ are the phase-neutral LV AC voltages (in phases a, b and c) in the LV inverter (VAC_{LV}), and $i_{a_{LV}}$, $i_{b_{LV}}$ and $i_{c_{LV}}$ are the AC currents in the LV inverter's phases a, b and c (IAC_{LV}). VDC_{LV} is defined by Equation (12), where C_{LV} is the capacitance of the LV DC bus, and $IDAB_{LV}$, IDC_{LV_g} and I_{SC} are the DC currents exchanged between the LV DC bus and the isolated DC/DC converter, LV DC network and the supercapacitor bank, respectively.

$$IDC_{LV} = \frac{PLV_{Inv}}{VDC_{LV}} = \frac{1}{VDC_{LV}}[v_{an_{LV}}, v_{bn_{LV}}, v_{cn_{LV}}] \cdot \begin{bmatrix} I_{a_{LV}} \\ I_{b_{LV}} \\ I_{c_{LV}} \end{bmatrix} \tag{11}$$

$$VDC_{LV} = \frac{1}{C_{LV}} \int (IDAB_{LV} + IDC_{LV} + IDC_{LV_g} + I_{SC})dt \tag{12}$$

The LV DC bus voltage is regulated according to Equations (13)–(15), obtained combining Equations (2), (3), (9) and (12). During normal operation conditions (no FRT activation), VDC_{LV} is regulated only through IDC_{MV}, given that $d_{FRT} = d_{FRT\_MV} = 1$ and $I_{DL} = 0$ (as explained in Section 3), and the remaining currents varying according to the load/generation profile in the hybrid distribution grid. When FRT is activated, IDC_{MV} becomes saturated, being VDC_{LV} regulated through d_{FRT}, d_{FRT_MV} and I_{DL} (as explained in Section 3).

$$VDC_{LV} = \frac{d_{FRT}N}{C_{MV} - (d_{FRT}N)^2 C_{LV}} \int (IMV - d_{FRT}N(IDC_{LV} + IDC_{LV_g} + I_{SC}))dt \tag{13}$$

$$IMV = IDC_{MV} + IDC_{MV_g} + I_{DL} \tag{14}$$

$$IDC_{MV_g} = \frac{VDC_{MV_g}}{Z_{MV_g}} = \frac{d_{FRT\_MV} VDC_{MV}}{Z_{MV_g}} \tag{15}$$

Regarding the control structure of the ST's LV inverter, a three-phase AC voltage (VAC_{LV}) is generated using the references for the nominal frequency (f_{LVn}) and voltage magnitude ($|VAC_{LV}|^*$), plus a frequency adjustment Δf generated by FRT Control, as expressed by Equation (16). $|VAC_{LV}|$ is given by the sum of the voltage magnitude set-point ($|VAC_{LVn}|^*$) defined by Equation (17), and the component ΔV_{LC} generated by the Filter voltage drop compensator.

$$VAC_{LV} = \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = |VAC_{LV}|^* \cdot \begin{bmatrix} sin\left(2\pi \int (f_{LVn} + \Delta f)\mathrm{d}t\right) \\ sin\left(\frac{-2\pi}{3} + 2\pi \int (f_{LVn} + \Delta f)\mathrm{d}t\right) \\ sin\left(\frac{2\pi}{3} + 2\pi \int (f_{LVn} + \Delta f)\mathrm{d}t\right) \end{bmatrix} \quad (16)$$

$$|VAC_{LVn}|^* = |VAC_{LVn}| \frac{VDC_{LV}}{VDC_{LVn}} \quad (17)$$

2.2. LV AC Network

The LV AC network integrating the hybrid AC/DC distribution grid adopts the topology described in [27], represented in Figure 10. Nevertheless, different power levels for the various elements and load voltage sensitivities were considered. The operation of the PV generation with deloading reserve in normal operation conditions is also adopted.

The exploitation of load-voltage and load-frequency sensitivities in AC networks is already addressed in the literature [34,35], as well as their estimation in AC networks using the ST itself [36,37]. According to [38], exponential load models have been the most frequently used static load models by TSOs worldwide. For that reason, Equations (18) and (19) are used to model the aggregated active (P) and reactive (Q) non-controllable load in the LV AC network, where P_0 and Q_0 are respectively the active and reactive loads at the nominal voltage (VAC_{LVn}) and frequency (f_{LVn}), f_{LV} is the LV AC network frequency, k_{pv} and k_{qv} are respectively the active and reactive power exponents determining the power-voltage load sensitivity, and k_{qf} and k_{pf} are respectively the active and reactive power exponents determining the power-frequency load sensitivity.

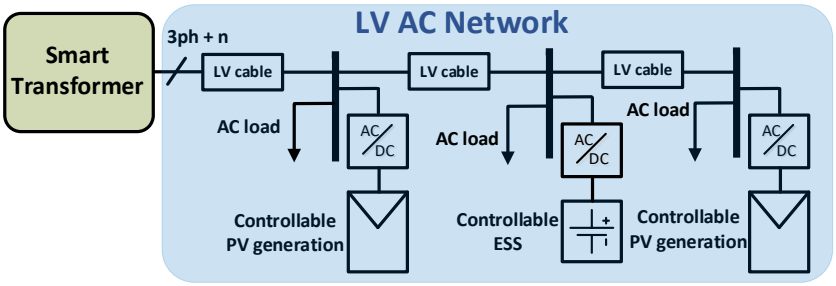

Figure 10. Computational model for the LV AC network.

$$P = P_0 \left(\frac{VAC_{LV}}{VAC_{LVn}}\right)^{k_{pv}} \left(1 - k_{pf} \frac{f_{LV} - f_{LVn}}{f_{LVn}}\right) \quad (18)$$

$$Q = Q_0 \left(\frac{VAC_{LV}}{VAC_{LVn}}\right)^{k_{qv}} \left(1 - k_{qf} \frac{f_{LV} - f_{LVn}}{f_{LVn}}\right) \quad (19)$$

The parametrization of k_{pv} and k_{qv} follows the average value estimations for the entire world presented in [38]. Regarding k_{qf} and k_{pf}, a range of values for residential load in North America is provided in [38], considered realistic to be used here. The resulting load models are described by Equations (20) and (21). The controllable ESS and PV generation were modeled as constant power and constant current devices according to Equation (22), where $|I|$ is the module of the output RMS current and In is the nominal RMS current.

$$P = P_0 \left(\frac{VAC_{LV}}{VAC_{LVn}}\right)^{0.67} \left(1 + 0.84 \frac{f_{LV} - f_{LVn}}{f_{LVn}}\right) \quad (20)$$

$$Q = Q_0 \left(\frac{VAC_{LV}}{VAC_{LVn}} \right)^{1.35} \left(1 + 1.94 \frac{f_{LV} - f_{LVn}}{f_{LVn}} \right) \quad (21)$$

$$\begin{cases} P = P_0; & |I| < In \\ P = P_0 \frac{VAC_{LV}}{VAC_{LVn}}; & |I| = In \end{cases} \quad (22)$$

2.3. MV and LV DC Networks

The MV DC and LV DC grids were modeled according to the topologies described also in [27] and represented in Figure 11, with the same modifications mentioned in Section 2.2. Contrary to LV AC grids, the estimation of load voltage sensitivity in DC grids remains largely unexplored in the literature, although several works suggest that a large portion the load in DC grids may consist of constant power loads since it is based on power electronic converters [39,40]. Given the lack of data, a scenario with a significant ratio of constant power loads presented in [37] is adopted. In this paper, this adopted scenario is intended to represent the non-controllable DC loads only, modeled according to Equation (23) where P_0 is the load power for the nominal voltage (VDC_{LVn}). The controllable EV chargers and PV generation were modeled as constant power and constant current devices according to Equation (24), where $|I|$ is the output current and In is the nominal current.

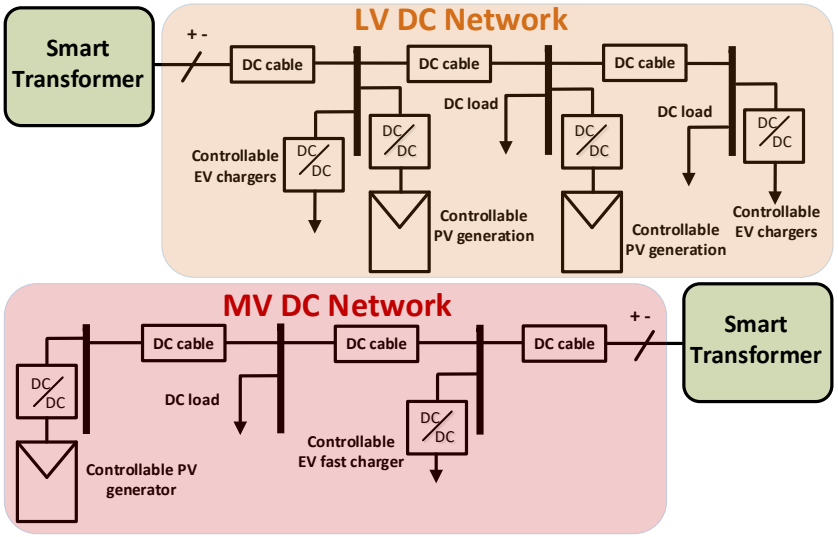

Figure 11. Computational models for the MV and LV DC networks.

$$P = P_0 \left(\frac{VDC_{LV}}{VDC_{LVn}} \right)^{0.45} \quad (23)$$

$$\begin{cases} P = P_0; & |I| < In \\ P = P_0 \frac{VDC_{LV}}{VDC_{LVn}}; & |I| = In \end{cases} \quad (24)$$

2.4. Distributed Energy Resources

The controllable DER considered in the hybrid AC/DC grid were also modeled following the considerations assumed in [27], and are illustrated in the block diagrams presented in Figure 12: The AC/DC Converter for interfacing the PV generator (Figure 12A) and ESS unit (Figure 12B) with the LV AC network, and the DC/DC Converter for interfacing the EV chargers (Figure 12C) and PV generators (Figure 12D) with the DC networks.

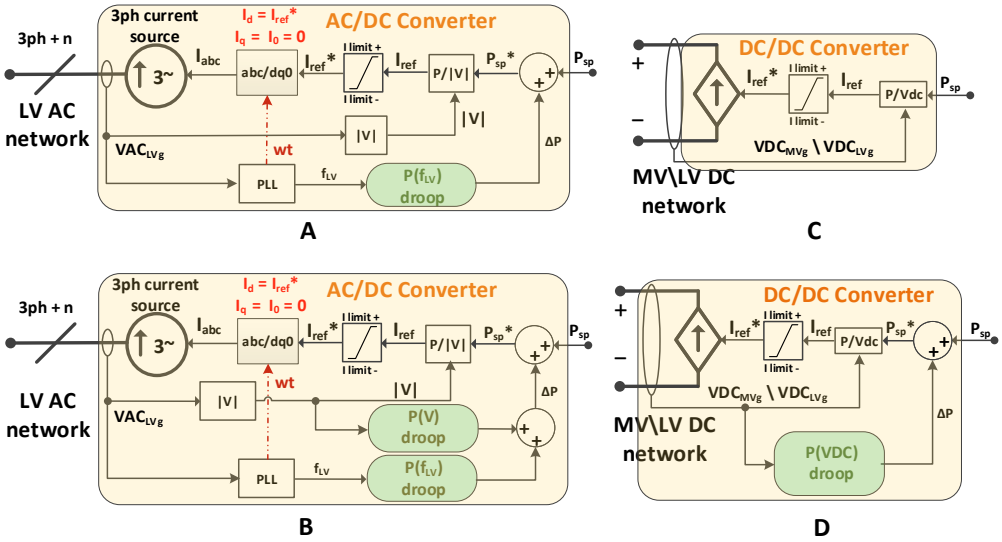

Figure 12. Block diagram of the developed computational models for the controllable DER units: AC (**A**) and DC (**D**) PV generation, ESS (**B**), and EV chargers (**C**).

Not being object of study in this paper, reactive power is not considered in the DER units available in the LV AC distribution grid. Thus, the generated reference current (I^*_{ref}) represents only the direct current component. PV generation and the ESS in the AC network incorporate an active power–frequency droop ($P(f_{LV})$) in order to respond to the frequency deviations induced by the FRT Control described in Section 3. The ESS in the AC network also incorporates an active power–voltage droop ($P(V)$) in order to respond to voltage modulations originated by the FRT Control. PV generation in DC networks incorporates an active power–voltage droop (*P(VDC)*) in order to respond to the voltage deviations induced by the same FRT Control. PV generation operates with 10% of deloading reserve, which is activated in case of under-voltage (DC networks) or under-frequency (LV AC network).

3. Fault-Ride-Through Control

Suited for grid-tied ST with no local energy storage capacity, the underlying rationale of the proposed FRT strategy consists in diverting and/or eliminating excessive net active power (load or generation) from the ST's hybrid AC/DC network that cannot be balanced by the ST's MV inverter without violating its current limits. Different operation modes are used for net load scenarios and net generation scenarios in the hybrid AC/DC grid.

For net load scenarios in the hybrid AC/DC grid, the cascading reaction of the proposed FRT strategy is illustrated in Figure 13. A voltage sag in the MV AC grid causes the FRT control to modulate the voltage and frequency levels in the hybrid AC/DC grid, if the ST's MV inverter is not capable to balance the power in the hybrid AC/DC grid without violating its current limits. The modulation of the voltage and frequency levels in the hybrid AC/DC grid is aimed to exploit the voltage-power and frequency-power sensitivities of the hybrid AC/DC grid (including voltage-power and frequency-power sensitive modes of DER connected downstream from the ST) in order to reduce the net active power consumption in the hybrid AC/DC network. As a result, the active power in the hybrid AC/DC network that cannot be balanced by the ST's MV inverter is eliminated. The participation of the MV DC sub-network in this process is made possible by the electronic resistor incorporated in series between the ST's MV DC bus and the MV DC sub-network. The modeling of the electronic resistor proposed for this purpose is presented in Section 2.1.3.

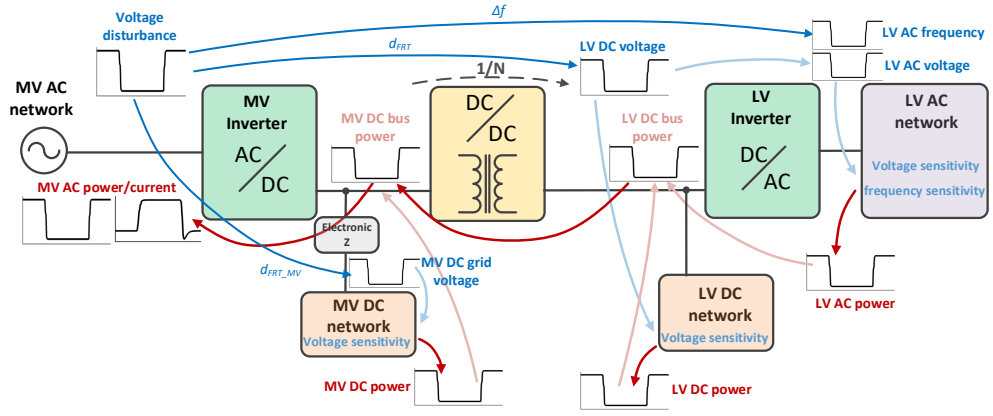

Figure 13. Overview of the cascading effects resulting from the proposed FRT control strategy during a net load scenario in the ST's hybrid AC/DC grid, following a voltage sag in the MV AC network.

The cascading actuation of the proposed FRT strategy during net generation scenarios in the hybrid AC/DC grid is illustrated in Figure 14. If the ST's MV inverter is not capable to balance all the net active power in the hybrid AC/DC grid during the occurrence of a voltage sag in the MV AC grid, the FRT control will modulate the frequency in the LV AC sub-network (using a proportional gain, as shown in Figure 15 and expressed in Equation (27)) and also command the dump-load to dissipate net active power in excess. The modulation of the frequency in the LV AC sub-network aims to exploit the frequency-power sensitivity of the LV AC sub-network and of power-frequency sensitive DER located in the LV AC sub-network in order to decrease power generation and increase power consumption in the LV AC sub-network. As a result, the active power in the hybrid AC/DC network that the ST's MV inverter cannot balance is eliminated. The modeling of the dump-load for the aforementioned purpose is presented in Section 2.1.4.

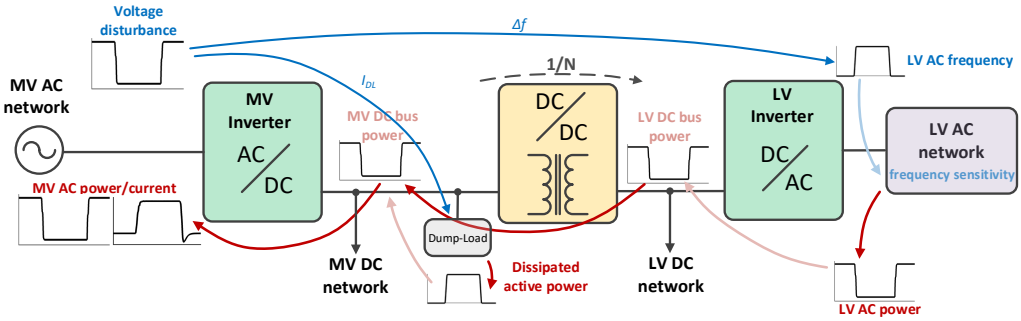

Figure 14. Overview of the cascading effects resulting from the proposed FRT control strategy during a net generation scenario in the ST's hybrid AC/DC grid, following a voltage sag in the MV AC network.

As shown in Figures 13 and 14, the operation of the proposed FRT strategy relies on d_{FRT}, d_{FRT_MV}, I_{DL} and Δf signals. These signals are generated by the FRT control whose structure is depicted in the block diagram presented in Figure 15. d_{FRT}, d_{FRT_MV}, I_{DL} and Δf signals depend on the reference signal for the MV inverter overload current I_{FRT}, which is calculated according to Equation (25), where VDC_{MV} is the voltage in the MV DC bus, PMV_{Inv} is the maximum instant active power in the MV inverter, PMV^{*}_{Inv} is the unrestricted reference for the active power (generated by the *VDC Control / P Control* illustrated in Figure 3), $|VAC^{+}_{MV}|$ is the magnitude of the positive sequence component of the MV AC voltage measured at the ST's MV inverter (Figure 3)) and Id^{*}_{lim} is the limited reference for the direct current component (generated by the Current Control illustrated in Figure 3).

The FRT mechanism is activated when the overload current (I_{FRT}) is non-zero. While the proposed FRT control strategy relies solely in proportional gains to calibrate the response of each four control signals, it is capable to eliminate the steady-state error due to the dependence of I_{FRT} on the PI controller responsible to generate PMV^*_{Inv} (see VDC Control / P Control in Figure 3).

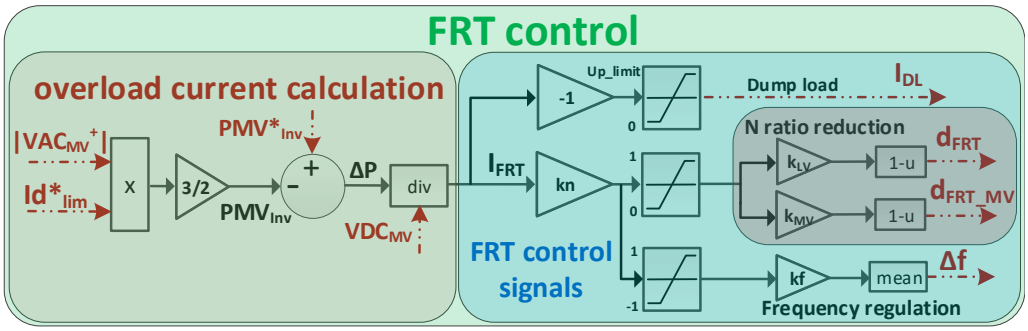

Figure 15. Block diagram of the proposed Fault-Ride-Through control strategy.

$$I_{FRT} = \frac{1}{VDC_{MV}}(PMV^*_{Inv} - PMV_{Inv}) = \frac{1}{VDC_{MV}}(PMV^*_{Inv} - \frac{3}{2}|VAC^+_{MV}|Id^*_{lim}) \quad (25)$$

The occurrence of unbalanced voltage sags in the MV AC grid may induce an oscillatory active power component in the MV inverter, here denominated by P^-, which is a result of a negative-sequence component in the MV AC grid voltage. P^- propagates to the MV DC bus, introducing voltage oscillations in the hybrid AC/DC grid, whose compensation effort by VDC Control / P Control will originate an oscillatory component in PMV^*_{Inv}.

Using the ST's MV inverter to compensate P^- (by injecting a negative-sequence component current) may imply severe reductions in the transferable active power (positive-sequence component) through the ST's MV inverter during severe unbalanced voltage sags in the MV AC grid. As a result, this approach could result in adverse impacts on the hybrid AC/DC grid as the proposed FRT mechanism promotes the power balance within the hybrid AC/DC grid.

P^- could also be mitigated by increasing the capacitance in the ST's DC buses, but unrealistic bulky capacitors would be required in order to achieve an acceptable maximum limit for the DC voltage ripple. Additionally, this solution would significantly degrade the dynamics of the ST itself.

To avoid the drawbacks of the aforementioned solutions, an electronically controlled supercapacitor bank, described in Section 2.1.5, was incorporated as part of the proposed FRT strategy. Besides preserving the transferable power in the ST's MV inverter, it also preserves the dynamics of the ST because it only actuates against power oscillations associated to the negative-sequence component, as explained in Section 2.1.5. Based on [41], the maximum voltage ripple ($\Delta V_{C_{pp}}$) for the ST's MV DC bus voltage can be expressed by Equation (26), where M is the modulation index of the ST's MV inverter, $|P^-|$ is the maximum amplitude of the active power oscillation associated to the negative-sequence component of the MV AC grid voltage, f_{MV} is the MV AC grid frequency, $|VAC^-_{MV}|$ is the maximum amplitude of the negative-sequence component of the MV AC grid voltage, C_{MV} and C_{LV} are the capacitances of the ST's MV and LV DC buses respectively, C_{SC} is the capacitance of the supercapacitor bank, and V_{SC} is the supercapacitor bank voltage.

$$\Delta V_{C_{pp}} = \frac{\sqrt{3}M|P^-|}{8\pi f_{MV}|VAC^-_{MV}|(C_{MV} + (d_{FRT}N)^2(C_{MV} + (\frac{V_{SC}}{VDC_{LV}})^2 C_{SC}))} \quad (26)$$

Still, it is also necessary to prevent the amplification of the aforementioned power and voltage oscillations in the hybrid AC/DC grid by the FRT control during unbalanced voltage sags in the MV AC grid. For that reason, $|VAC^+_{MV}|$ is used to calculate PMV_{Inv}

in order to obtain an active power limit for the ST's MV inverter based on the positive-sequence component of the MV AC grid voltage.

3.1. Elimination of Excessive Net Generation

The elimination of excessive net generation in the hybrid AC/DC grid is mainly performed by the dump-load, controlled by the I_{DL} signal. I_{DL} is set to zero in normal conditions ($I_{FRT} = 0$) or during excessive net load in the hybrid AC/DC grid ($I_{FRT} > 0$). If $I_{FRT} < 0$, an excess of net generation in the hybrid AC/DC network exists, and a non-zero I_{DL} signal ($= -I_{FRT}$) is generated, forcing the dump-load (described in Section 2.1.4) to dissipate the active power in excess.

Additionally, if $I_{FRT} \neq 0$, a nonzero Δf is also generated, which enables any controllable power-frequency sensitive DER located in the LV AC network to actively contribute to the active power balancing problem by modulating the power output as a function of the LV AC grid frequency in order to reduce the amount of net generation. Δf is added to the nominal frequency of the LV AC grid (f_{LVn}), as depicted in Figure 9, and is given by Equation (27), where kn is a gain to regulate the sensitivity of the FRT control to I_{FRT}, and k_f is a droop gain to adjust Δf in order to best exploit the existing frequency-controllable DER available in the LV AC sub-network (see Figure 15). Δf is set to 0 in normal conditions ($I_{FRT} = 0$).

$$\begin{cases} f^*_{LV} = f_{LVn} - k_f; & \text{if } k_n I_{FRT} <= -1 \\ f^*_{LV} = f_{LVn} + k_f k_n I_{FRT}; & \text{if } -1 < k_n I_{FRT} < 1 \\ f^*_{LV} = f_{LVn} + k_f; & \text{if } k_n I_{FRT} >= 1 \end{cases} \quad (27)$$

3.2. Elimination of the Excessive Net Load

The elimination of the excessive net load in the hybrid AC/DC grid is performed by the combined actuation of d_{FRT}, d_{FRT_MV} and Δf signals. The d_{FRT} and d_{FRT_MV} signals are set to 1 in normal conditions ($I_{FRT} = 0$) or during excessive net generation in the hybrid AC/DC grid ($I_{FRT} < 0$). As a result, the transformation ratio in the isolated DC/DC converter remains in its default value (VDC_{LVn}/VDC_{MVn}), and the electronic resistor (described in Section 2.1.3) is not actuating (the voltage in the MV DC grid (VDC_{MV_g}) follows the voltage in the MV DC bus (VDC_{MV})). When $I_{FRT} > 0$, d_{FRT} reduces the transformation ratio in the isolated DC/DC converter and d_{FRT_MV} controls the electronic resistor to insert a series resistance in the connection point of the MV DC grid with the ST's MV DC bus. As a result the voltages in the LV DC grid (VDC_{LV}) and MV DC grid (VDC_{MV_g}) are reduced, according to Equations (28) and (29) respectively.

$$\begin{cases} VDC_{LV} = VDC_{MV} N; \quad k_{LV} \in [0,1]; & \text{if } k_{LV} k_n I_{FRT} <= 0 \\ VDC_{LV} = VDC_{MV} N(1 - k_{LV} k_n I_{FRT}); \quad k_{LV} \in [0,1]; & \text{if } 0 < k_{LV} k_n I_{FRT} < 1 \\ VDC_{LV} = 0; \quad k_{LV} \in [0,1]; & \text{if } k_{LV} k_n I_{FRT} >= 1 \end{cases} \quad (28)$$

$$\begin{cases} VDC_{MV_g} = VDC_{MV}; \quad k_{MV} \in [0,1]; & \text{if } k_{MV} k_n I_{FRT} <= 0 \\ VDC_{MV_g} = VDC_{MV}(1 - k_{MV} k_n I_{FRT}); \quad k_{MV} \in [0,1]; & \text{if } 0 < k_{MV} k_n I_{FRT} < 1 \\ VDC_{MV_g} = 0; \quad k_{MV} \in [0,1]; & \text{if } k_{MV} k_n I_{FRT} >= 1 \end{cases} \quad (29)$$

The sensitivity of d_{FRT} and d_{FRT_MV} to I_{FRT} can be adjusted using the gain kn (see Figure 15). The relative contribution of d_{FRT_MV} and d_{FRT} can be adjusted using the gains k_{MV} and k_{LV} respectively, with real values between 0 and 1 (see Figure 15). Equal values for k_{MV} and k_{LV} means that d_{FRT_MV} and d_{FRT} will originate similar per unit voltage reductions in their respective sub-networks. d_{FRT} also affects the magnitude of the LV AC grid voltage given its dependence on VDC_{LV} as depicted in Figure 9. Thus, by reducing VDC_{LV} and $|VAC_{LV}|$, the FRT mechanism aims to reduce the active power load in the LV DC and LV AC grids by exploiting their power-voltage sensitivity.

Regarding the Δf signal, its actuation mechanism is as already described in Section 3.1.

4. Results and Discussion

Using the computational models described in Sections 2 and 3, the effectiveness of the proposed FRT control strategy is demonstrated. The location of the simulated faults is also illustrated in Figure 1. The proposed FRT strategy was evaluated for the 30 operational scenarios encompassing all combinations for the scenarios enumerated in Table 1. The main parameters used in the modeled test system are presented in Section 4.1. The obtained results are discussed in Section 4.2.

Table 1. Operational scenarios.

Fault Type		Net Power in ST's Hybrid Network		Fault Resistance
three phase phase–phase phase-ground	X	net load net generation	X	0.01 Ω 0.05 Ω 0.2 Ω 0.8 Ω 2.4 Ω

4.1. Model Parameters

The relevant data of the ST is presented in Table 2. The main parameters of the equivalent main power system are presented in Table 3. The steady-state operation of the hybrid AC/DC network for the scenarios listed in Table 1 was parameterized according to the data presented in Table 4. A total active load of 1.1 MW in the hybrid AC/DC grid for net load and generation scenarios was considered. Total active generations in the hybrid AC/DC grid of 300 kW for net load scenarios and of 2.0 MW for net generation scenarios were considered. The droop controllers of PV generators and ESS unit were parameterized according to Table 5 for all scenarios. The settings of the FRT control are presented in Table 6.

Table 2. Smart Transformer: Main parameters.

Nominal Power	1 MVA
Nominal MV AC Voltage (ph-ph)	15 kV (RMS)
Nominal MV DC link Voltage	27 kV
Nominal LV DC link Voltage	720 V
Nominal LV AC Voltage (ph-n)	230 V (RMS)
MV DC bus capacitance	1.008×10^{-5} F
LV DC bus capacitance	1.42×10^{-2} F

The presented nominal values correspond to the base values for apparent power and voltages in the respective AC and DC networks, used to calculate the *per unit* voltages and currents presented in Section 4.2.

Table 3. Main power system: Main parameters.

High-Voltage	60 kV
Medium-Voltage	15 kV
Generation Capacity	infinite
Equivalent Z	0.4 + j0.6283 Ω
MV cable impedance	0.4 + j0.6283 Ω
Earthing impedance (HV/MV transformer)	8.661 Ω (for 1000 A)

Table 4. Steady-state conditions and operation limits (nominal voltage and frequency).

Net Load Scenario				
Z Cables *	**Load**	**PV Generation ****	**EV Charging ****	**ESS ****
		LV AC network		
0.05 + j0.03 Ω	200 kW/100 kvar	−50 kW (−495–0 kW)	-	0 kW (±100 kW)
		LV DC network		
0.1 Ω	250 kW/-	−50 kW (−605–0 kW)	50 kW	-
		MV DC network		
0.6 Ω	150 kW/-	−200 kW (−1100–0 kW)	450 kW	-
		Smart Transformer		
-	700 kW/0 kvar ***	-	-	
Net Generation Scenario				
Z Cables *	**Load**	**PV Generation ****	**EV Charging ****	**ESS ****
		LV AC network		
0.05 + j0.03 Ω	200 kW/450 kvar	−300 kW (−495–0 kW)	-	0 kW (±100 kW)
		LV DC network		
0.1 Ω	250 kW/-	−550 kW (−605–0 kW)	50 kW	-
		MV DC network		
0.6 Ω	150 kW/-	−1000 kW (−1100–0 kW)	450 kW	-
		Smart Transformer		
-	−750 kW / 0 kvar ***	-	-	

* All cable sections in each sub-network have the same impedance; ** the allowable range is represented between brackets; *** net load in the ST MV inverter (sum of active load and generation in the hybrid network.

An illustrative example of a supercapacitor bank suited to mitigating power oscillations in the ST's DC buses due to unbalanced voltage sags in the MV AC grid is presented in Table 7. Using a commercially available solution [42] as reference (see Table 7), the required capacitance was determined according to Equation (26) for the following assumptions: A maximum DC voltage ripple of 0.5% in the ST's MV DC bus due to unbalanced voltage sags in the MV AC grid, and a maximum 90% drop in the LV DC bus voltage during a voltage sag in the MV AC grid.

Table 5. Droop Controllers: Main characteristics.

Droop	**Slope**	**Limits**
P(f)-ESS	20 Pn/fn *	±Pn kW
P(V)-ESS	2.5 Pn/Vn *	±Pn kW
P(f)-PV	10 Psp/fn **	0/−Pn%
P(V)-PV	2 Psp/Vn **	0/−Pn%

Note: Vn—nominal voltage; fn—nominal frequency; Pn—nominal active power; Psp—active power set-point; */** function of Pn / Psp.

Table 6. FRT control settings.

kn	0.05
k_{LV}	1
k_{MV}	1
kf	−0.2

Table 7. Hypothetical Supercapacitor Bank (not modeled).

Pack: Assembling	63 (parallel) × 4 (series)		
Pack: Nominal voltage	10.8 V	Unit: Nominal voltage	2.7 V
Pack: Capacitance	7.88 kF	Unit: Capacitance	500 F
Pack: Peak power	1.8 MW	Unit: Peak current	400 A

4.2. Simulation Results

4.2.1. Balanced Three-Phase Voltage Sags

The effectiveness of the proposed FRT control strategy for balanced three-phase voltage sags is demonstrated in the results presented in Figures 16–18. Figure 16 shows the voltage sags at the ST's MV inverter resulting from the simulated faults, and the voltage and frequency modulation originated by the FRT control in the sub-networks of the hybrid AC/DC grid.

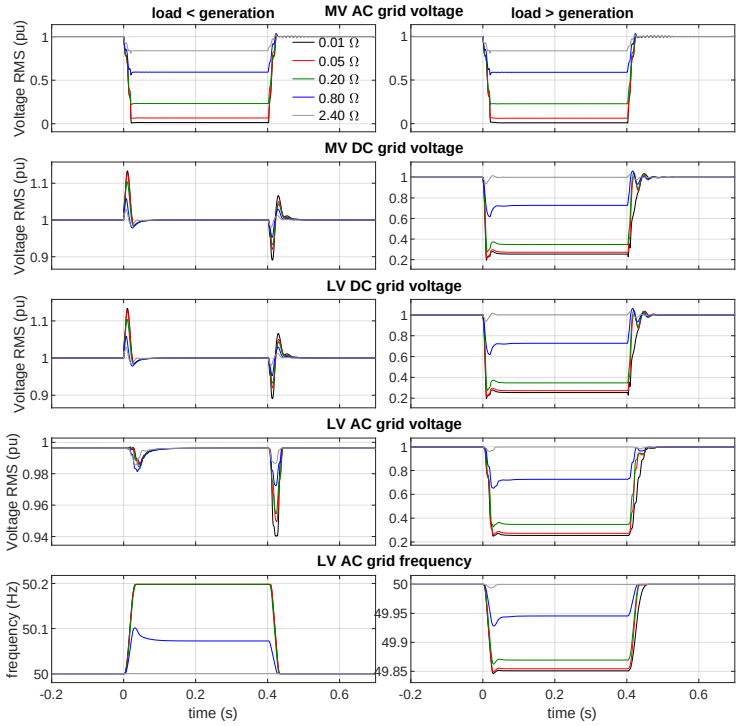

Figure 16. Voltage and frequency in the hybrid AC/DC network following balanced three-phase faults in the HV AC grid for the considered fault resistances.

Figure 17 shows the ST's MV inverter current (MV inverter current) and active power (MV inverter active power), and net active power in the sub-networks of the hybrid AC/DC grid due to the actuation of the FRT control. Figure 18 shows the contribution of each load/generation type located in the hybrid AC/DC grid for the FRT provision. Positive values for the active power represent consumed power.

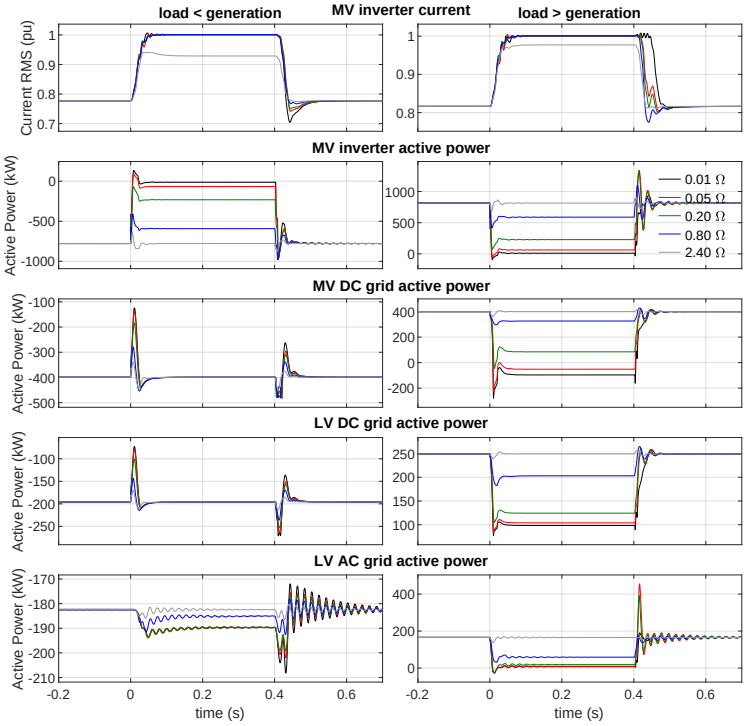

Figure 17. Current and active power in the ST's MV inverter and active power in the hybrid AC/DC grid following balanced three-phase faults in the HV AC grid for the considered fault resistances.

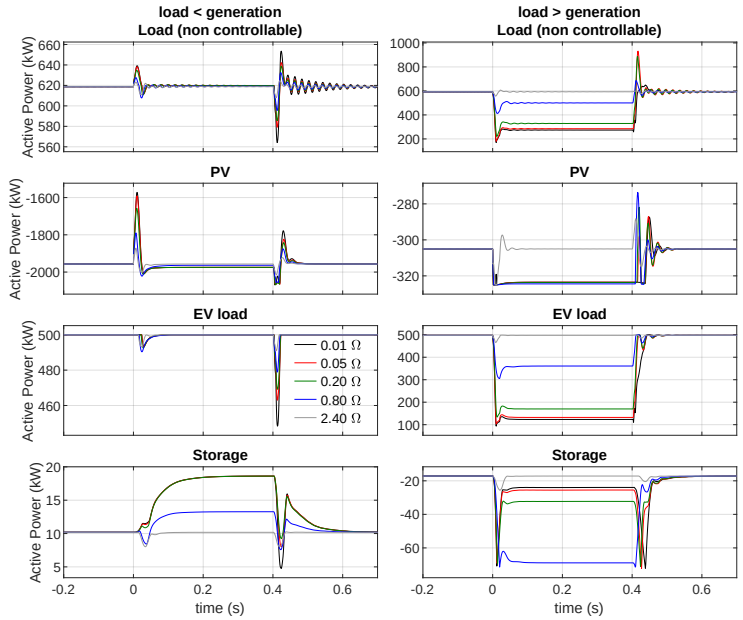

Figure 18. Active power per type of resources following balanced three-phase faults in the HV AC grid for the considered fault resistances.

The presented results show that the proposed FRT strategy mitigates the impact of the grid fault in the ST's hybrid AC/DC grid. Voltage levels in the hybrid AC/DC grid are significantly affected only during net load scenarios (load > generation) when the current levels in the ST's MV inverter reach the saturation level of 1 p.u. For the remaining cases, the voltages in the hybrid AC/DC grid remains practically immune to the grid faults in the upstream AC grid. It is also possible to observe from Figure 18 that energy storage capacity in the LV AC sub-network and PV generation with deloading reserve can be exploited to

mitigate the excessive net load in the hybrid AC/DC grid, as their injected power increase with the severity of the fault.

During net generation scenarios (load < generation), the generation in excess is dissipated in the dump-load. The voltages in the hybrid AC/DC grid are kept around their nominal values (excepting the brief transitory variations in the start and end of the voltage sags) and the active power in the ST's MV inverter gets reduced (Figure 17—MV inverter active power) for the fault scenarios where it is necessary to keep the current in the ST's MV inverter within the acceptable limits of 1 p.u. (Figure 17—MV inverter current). Only power-frequency sensitivity is exploited in the LV AC sub-network during net generation scenarios when the current levels in the ST's MV inverter reach the saturation level of 1 p.u., leading the existing controllable ESS to increase/reduce their active power charging/discharging and thus positively contributing to the power balancing in the hybrid system in the moments subsequent to the fault (Figure 18—Storage).

The presented results also show that the severity of the load reduction in the hybrid AC/DC network increases as the impedance of the simulated fault decreases. This is expected given that lower fault impedances result in more severe voltage sags, and thus, in a tighter active power margin in the ST's MV inverter. The power oscillation observed in the LV AC grid after the fault clearance are due to a decaying exponential DC current component originated by the reactive load in the LV AC grid, in response to the fast voltage changes shown in Figure 16.

4.2.2. Unbalanced Phase–Phase Voltage Sags

Regarding unbalanced phase–phase voltage sags, the effectiveness of the proposed FRT control strategy is demonstrated in the results shown in Figures 19–23. The voltage sags at the ST's MV inverter resulting from the simulated faults are presented in Figure 19.

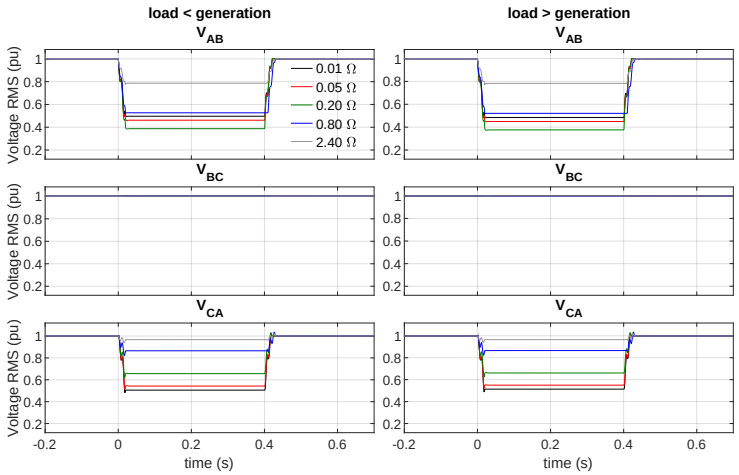

Figure 19. Phase–phase voltages at ST's MV Inverter (AC side) following unbalanced phase–phase faults in the HV AC grid for the considered fault resistances.

The current levels in the ST's MV inverter are presented in Figure 20. Figure 21 shows the voltage and frequency modulation originated by the FRT control in the various sub-networks of the hybrid AC/DC grid. Figure 22 depicts the net active power in the ST's MV inverter and in the various sub-networks of the hybrid AC/DC grid due to the actuation of the FRT control. Finally, Figure 23 shows the contribution of each load/generation type located in the hybrid AC/DC grid for the FRT provision. Positive values for the active power represent consumed power.

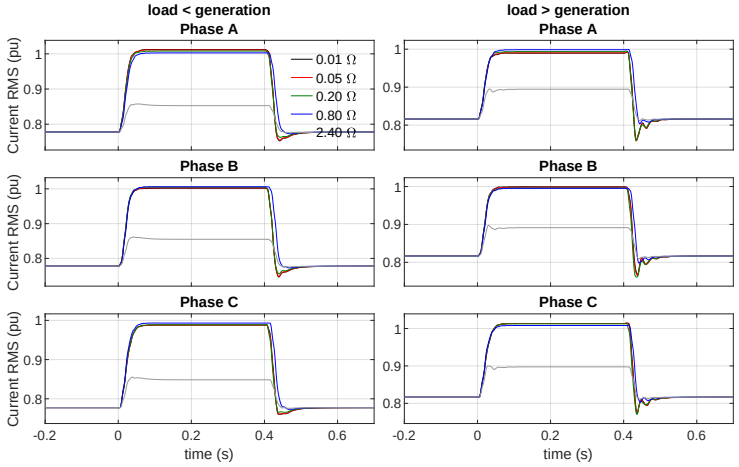

Figure 20. Phase currents at ST's MV Inverter (AC side) following unbalanced phase–phase faults in the HV AC grid for the considered fault resistances.

While simulated phase–phase faults affected AB and CA voltages (as shown in Figure 19), no difference exists between the RMS currents in the different phases (Figure 20), as the implemented current controller was designed to generate positive-sequence currents only. The presented results also show that the severity of the load reduction in the hybrid AC/DC network increases as the impedance of the simulated fault decreases. This is expected given that lower fault impedances result in more severe voltage sags, and thus, in a tighter active power margin in the ST's MV inverter.

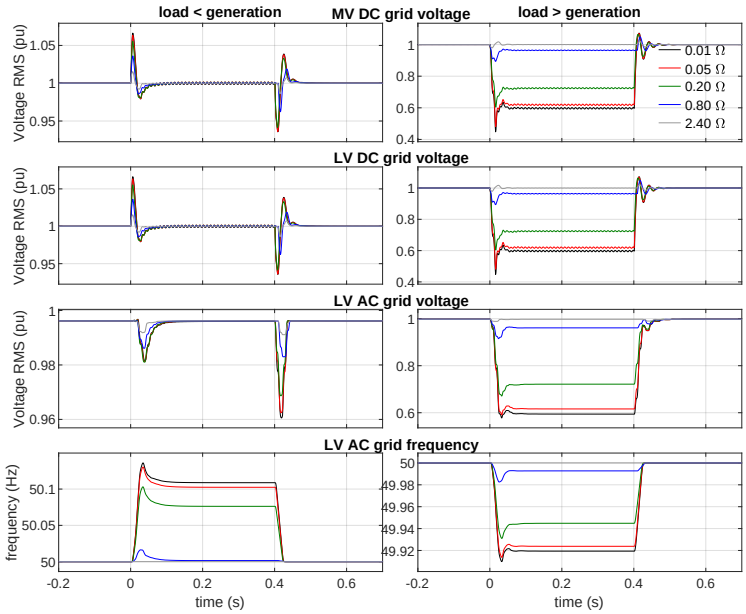

Figure 21. Voltage and frequency levels in the hybrid AC/DC network following unbalanced phase–phase faults in the HV AC grid for the considered fault resistances.

It is possible to observe that the proposed FRT strategy mitigates the impact of the grid fault in the ST's hybrid AC/DC grid. Figure 22 shows the impact of the supercapacitor bank to smooth power oscillations in the MV inverter resulting from unbalanced voltage sags in the MV AC grid, by comparing the "MV inverter active power" and "active power: MV inverter + Supercapacitor bank" plots. As a result, the FRT control does not originate significant voltage and frequency oscillations in the hybrid AC/DC grid during the grid disturbance in spite of responding to unbalanced faults. In Figure 21 it is possible to observe the protective effect of the proposed FRT strategy over the voltage profiles in

hybrid AC/DC grid, as the voltage levels in the hybrid AC/DC grid are significantly affected only during net load scenarios (load > generation) when the current levels in the ST's MV inverter reach the saturation level of 1 p.u. However, it is worth to mention that the voltage in all LV AC sub-network phases are impacted, despite an unbalanced phase–phase fault took place in the ST's upstream AC grid. Figure 23 also shows that energy storage capacity in the LV AC sub-network and PV generation with deloading reserve can be exploited to mitigate the excessive net load in the hybrid AC/DC grid, as their injected power increase with the severity of the fault.

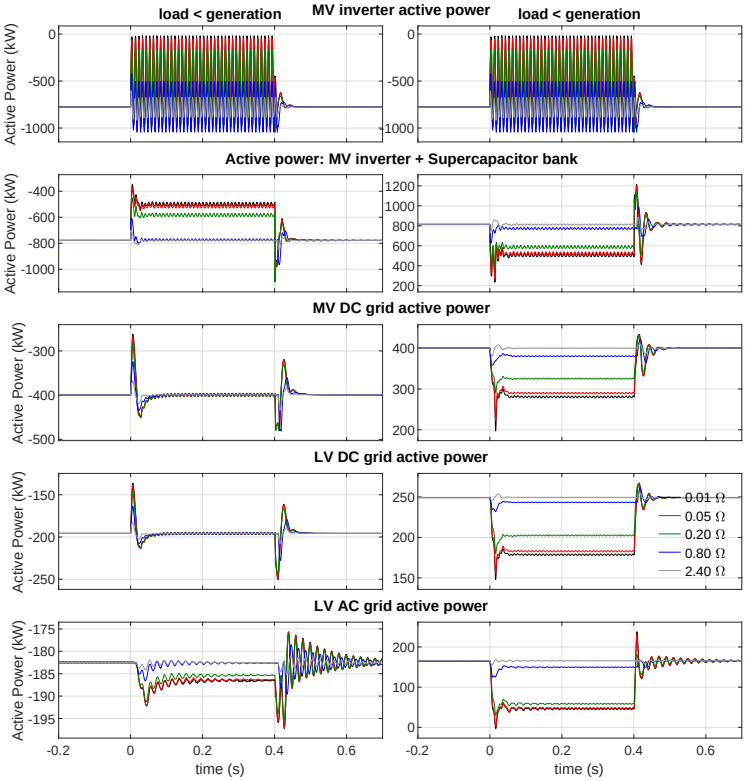

Figure 22. Active power in the ST's MV inverter and hybrid AC/DC sub-networks following unbalanced phase–phase faults in the HV AC grid for the considered fault resistances.

For the remaining cases, the hybrid AC/DC grid remains practically immune to the adverse impacts of the grid faults in the upstream MV AC grid. During net generation scenarios (load < generation), the generation in excess is dissipated in the dump-load, not existing necessity for the FRT control to modulate the voltages in the hybrid AC/DC grid, which are kept around their nominal values (excepting the brief transitory variations in the start and end of the voltage sags). As shown in Figure 22—MV inverter active power, the active power in the ST's MV inverter gets reduced during net generation scenarios where the current in the ST's MV inverter reaches its limits of 1 p.u. Only power-frequency sensitivity is exploited in the LV AC sub-network during net generation scenarios when the current levels in the ST's MV inverter reach the saturation level of 1 p.u., so the existing controllable ESS increases/reduces its active power charging/discharging to save some of the net generation surplus (Figure 23—Storage).

The power oscillation observed in the LV AC grid after the fault clearance are due to the same reasons already explained in Section 4.2.1.

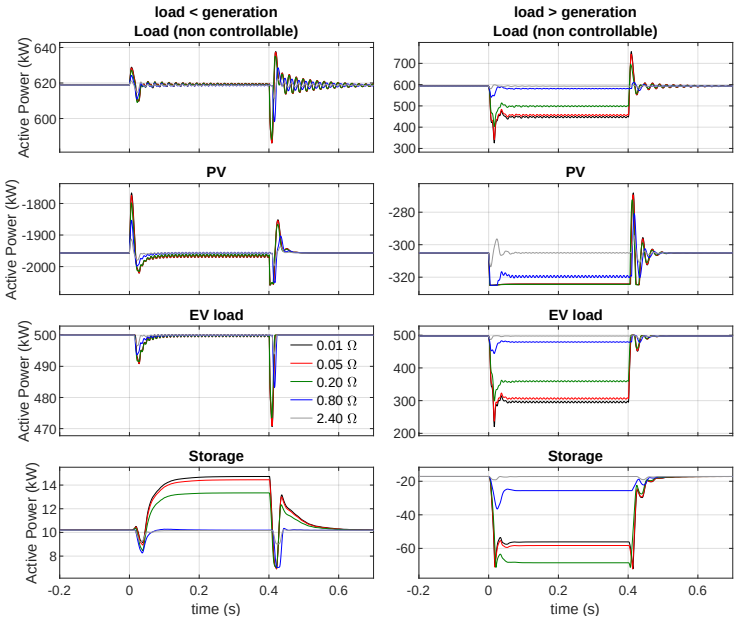

Figure 23. Active power per type of resources connected to the ST's hybrid AC/DC network following unbalanced phase–phase faults in the HV AC grid for the considered fault resistances.

4.2.3. Unbalanced Phase-Ground Voltage Sags

The effectiveness of the proposed FRT control strategy for unbalanced phase-ground voltage sags is shown in Figures 24–28. The voltage sags at the ST's MV inverter resulting from the simulated faults are presented in Figure 24. The current levels in the ST's MV inverter are presented in Figure 25. Figure 26 shows the voltage and frequency modulation originated by the FRT control in the various sub-networks of the hybrid AC/DC grid. Figure 27 depicts the net active power in the ST's MV inverter and in the various sub-networks of the hybrid AC/DC grid due to the actuation of the FRT control. Figure 28 shows the contribution of each load/generation type located in the hybrid AC/DC grid for the FRT provision. Positive values for the active power represent consumed power.

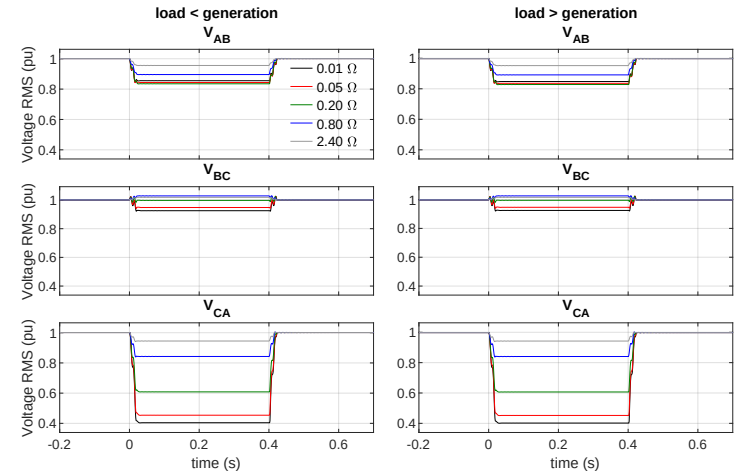

Figure 24. Phase–phase voltages at ST's MV Inverter (AC side) following unbalanced phase-ground faults in the HV AC grid for the considered fault resistances.

From the obtained results, conclusions similar to those presented in Section 4.2.2 are observed, although the simulated phase-ground fault affected mostly CA voltage (as it is explicit in Figure 24). No difference exists between the RMS currents in the different phases (Figure 25) for the same reason pointed in Section 4.2.2. It is also observed that the severity of the load reduction in the hybrid AC/DC network increases as the impedance of the

simulated fault decreases. This is expected given that lower fault impedances result in more severe voltage sags, and thus, in a tighter active power margin in the ST's MV inverter.

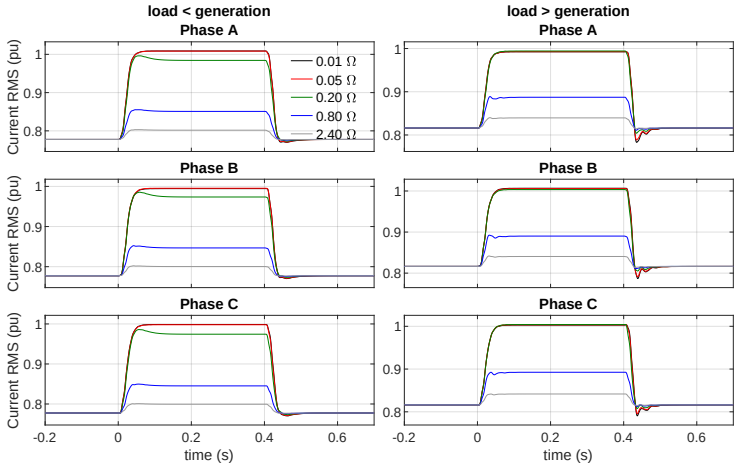

Figure 25. Phase currents at ST's MV Inverter (AC side) following unbalanced phase-ground faults in the HV AC grid for the considered fault resistances.

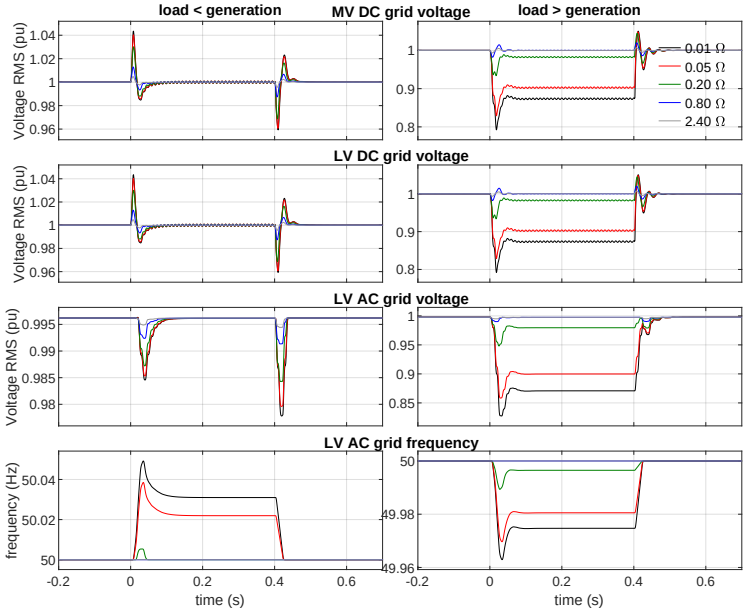

Figure 26. Voltage and frequency levels in the hybrid AC/DC network following unbalanced phase-ground faults in the HV AC grid for the considered fault resistances.

As in Sections 4.2.1 and 4.2.2, the proposed FRT strategy mitigates the impact of the grid fault in the ST's hybrid AC/DC grid. In Figure 27 it is possible to observe the impact of the supercapacitor bank to smooth power oscillations in the MV inverter resulting from unbalanced voltage sags in the MV AC grid voltage, by comparing the "MV inverter active power" and "active power: MV inverter + Supercapacitor bank" plots. As a result, the FRT control does not originate significant voltage and frequency oscillations in the hybrid AC/DC grid during the grid disturbance in spite of responding to unbalanced faults. The mitigating effect of the proposed FRT strategy over the voltage profiles in hybrid AC/DC grid is depicted in Figure 26, as the voltage levels in the hybrid AC/DC grid are significantly affected only during net load scenarios (load > generation) when the current levels in the ST's MV inverter reach the saturation level of 1 p.u. Worth to mention that the voltage in all LV AC sub-network phases are impacted, in spite that an unbalanced phase-ground fault took place in the ST's upstream AC grid. Figure 23 also

shows that energy storage capacity in the LV AC sub-network and PV generation with deloading reserve can be exploited to contribute to mitigate the excessive net load in the hybrid AC/DC grid, as their injected power increase with the severity of the fault.

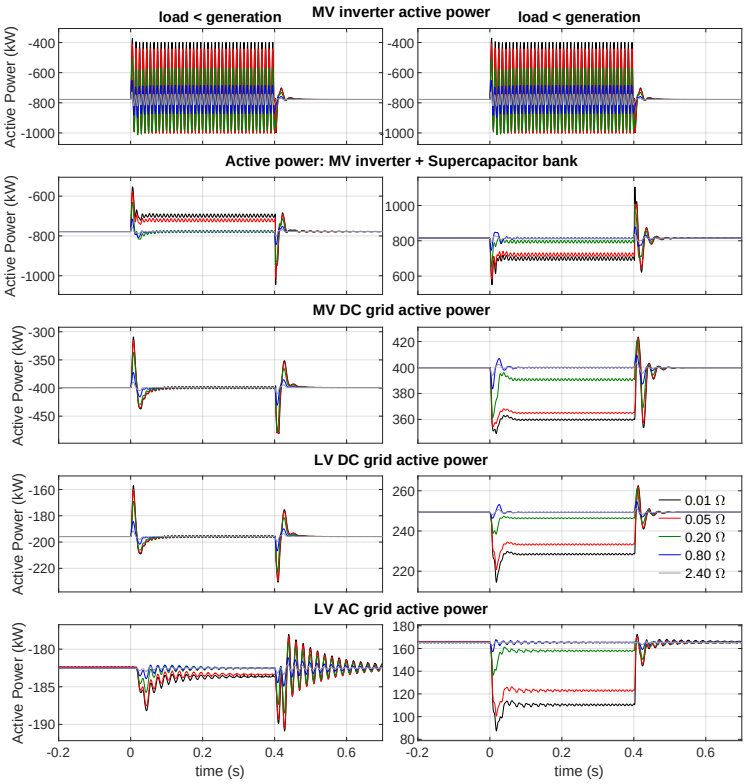

Figure 27. Active power in the ST's MV inverter and hybrid AC/DC sub-networks following unbalanced phase-ground faults in the HV AC grid for the considered fault resistances.

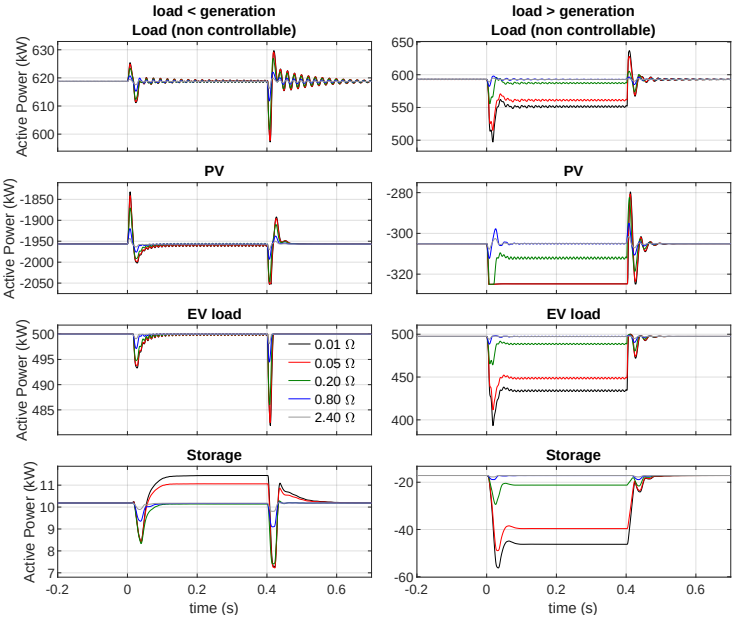

Figure 28. Active power per type of resources connected to the ST's hybrid AC/DC network following unbalanced phase-ground faults in the HV AC grid for the considered fault resistances.

For the remaining cases, the hybrid AC/DC grid remains practically immune to the adverse impacts of the grid faults in the upstream AC grid. During net generation scenarios (load < generation), the generation in excess is dissipated in the dump-load, not existing necessity for the FRT control to modulate the voltages in the hybrid AC/DC grid, which are kept around their nominal values (excepting the brief transitory variations in the start and end of the voltage sags). As shown in Figure 27—MV inverter active power, the active power in the ST's MV inverter gets reduced during net generation scenarios where the current in the ST's MV inverter reaches its limits of 1 p.u. Only power-frequency sensitivity is exploited in the LV AC sub-network during net generation scenarios when the current levels in the ST's MV inverter reach the saturation level of 1 p.u., so the existing controllable ESS increases/reduces its active power charging/discharging to save some of the net generation surplus (Figure 28—Storage).

The power oscillation observed in the LV AC grid after the fault clearance are due to the same reasons already explained in Section 4.2.1.

5. Conclusions

The work presented in this paper addresses the presentation and discussion of a novel FRT control strategy suited for ST with no local energy storage capacity. Four important improvements comparatively to previously proposed FRT control strategies are exposed in this paper: The participation of the MV DC sub-network of the hybrid AC/DC grid, the use of frequency modulation to control the active power output in DER located in the LV AC sub-network of the hybrid AC/DC grid, the dissipation of excessive net generation in the hybrid AC/DC grid to a dump-load, and the use of a electronically controlled supercapacitor bank to compensate active power oscillations in the ST's DC buses resulting from unbalanced faults in the upstream AC power grid.

The effectiveness of the proposed strategy is demonstrated for balanced three-phase voltage sags and unbalanced phase–phase and phase-ground voltage sags, while considering also net load and net generation scenarios in the ST's hybrid AC/DC distribution grid. During net generation scenarios, the proposed FRT control strategy relied successfully on a dump-load do dissipate the excessive net generation in the hybrid AC/DC network, but also exploited the energy storage capacity available in the hybrid AC/DC grid to absorb part of the generation in excess. Regarding net load scenarios, the proposed FRT control strategy modulated the electrical quantities in the hybrid AC/DC grid (voltages in DC and LV AC grids and frequency in LV AC grid), thus exploiting its power-voltage and power-frequency sensitivities in order to eliminate its excessive net load. It also took advantage of PV generation with deloading reserve to reduce the net load in excess, and of energy storage capacity available in the hybrid AC/DC grid which also actively participated in the process by reducing their charging power or by injecting more power to the hybrid AC/DC grid. It is also demonstrated that active power oscillations in the ST's DC buses resulting from unbalanced faults in the upstream AC power grid can be successfully mitigated.

The proposed FRT approach addresses a research gap with great relevance in future scenarios where hybrid AC/DC distribution grids based on ST may play a central role in a context of massive integration of DER in distribution grids. The proposed FRT control strategies aim at exploiting all the available resources connected downstream from the ST together with complementary solutions at the ST level. However, the parametrization of the FRT controller as a function of the existing resources in the hybrid AC/DC distribution network is not addressed. Moreover, computational models for real-time simulation can also be developed using the DAM approach according to [30], but this subject was not addressed in the scope of this work. These topics remain to be addressed in future works.

Author Contributions: J.R. carried out the main research task and wrote the full manuscript. C.M. proposed the original idea and contributed to the revision of the obtained results and of the whole manuscript. J.P.L. contributed with a valuable evaluation of the scenarios to be considered and contributed to the revision of the whole manuscript. All authors have read and agreed to the published version of the manuscript.

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Nomenclature

ΔV_{LC}	Compensation component for the Voltage drop in the LC filter
C_{LV}	Capacitance of the ST's LV DC bus
C_{MV}	Capacitance of the ST's MV DC bus
d_{FRT_MV}	duty-cycle adjustment (from *FRT Control*) for the electronic resistor
d_{FRT}	duty-cycle adjustment (from *FRT Control*) for the isolated DC/DC inverter
f_{LVn}	Nominal frequency of the LV AC grid
f^*_{LV}	Reference frequency for the ST's LV inverter
f_{LV}	Frequency in the LV AC grid
I_{DL}	Current exchanged between the MV DC bus and the dump-load
IAC_{LV_mp}	Maximum AC current peak value of the ST's LV inverter
IAC_{LV}	Three-phase AC current in the ST's LV inverter
IAC_{MV}	Three-phase AC current in the ST's MV inverter
Id^*, Id^*_{lim}	References for the active current in the ST's MV inverter
$IDAB_{LV}$	DC current in the secondary stage of the isolated DC/DC converter
$IDAB_{MV}$	DC current in the primary stage of the isolated DC/DC converter
IDC_{LVg}	Current exchanged between C_{LV} and the ST's LV DC network
IDC_{LV}	Current exchanged between the ST's LV inverter and the ST's LV DC bus
IDC_{MVg}	Current exchanged between C_{MV} and the ST's MV DC network
IDC_{MV}	Current exchanged between the ST's MV inverter and the ST's MV DC bus
Id	Measured active current in the ST's MV inverter
Iq^*, Iq^*_{lim}	References for the reactive current in the ST's MV inverter
Iq	Measured reactive current in the ST's MV inverter
N	Transformation ratio of the isolated DC-DC converter
PI	Proportional-Integral controller
PLV_{Inv}	Active power in the ST's LV inverter
PMV^*_{Inv}	Reference active power for the ST's MV inverter
PMV_{Inv}	Active power in the ST's MV inverter
VAC_{LVg}	AC voltage in the LV AC grid
VAC_{LVg}	Three-phase AC voltage in the ST's LV coupling LC filter
VAC_{LVn}	Nominal value for the AC voltage in the ST's LV inverter
VAC^*_{LV}	Reference for the three-phase AC voltage in the ST's LV inverter
VAC_{LV}	Three-phase AC voltage in the ST's LV inverter
VAC^+_{MV}	Positive sequence component of three-phase AC voltage in the ST's MV inverter
VAC_{MV}	Three-Phase AC voltage in the ST's MV inverter
VDC_{LVg}	DC voltage in the LV DC grid
VDC_{LVn}	Nominal value for the DC voltage in the ST's LV DC bus
VDC_{LV}	DC voltage in the ST's LV DC bus
VDC_{MVg}	DC voltage in the MV DC grid
VDC_{MVn}	Nominal DC voltage for the ST's MV DC bus
VDC_{MV}	DC voltage in the ST's MV DC bus
X_L	Primary-referred leakage reactance of the isolated DC/DC converter
Z_{MVg}	Equivalent impedance of the MV DC grid
ϕ	Phase-shift between the square waveforms applied to the HFT

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